FAIRCHILD SEMICONDUCTOR

DATA BOOK TWO

ADVANCED LOGIC

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ADVANCED LOGIC

CONTENTS

9S/54S,74S SERIES

SUPER HIGH SPEED TTL/SSI INTEGRATED CIRCUITS

SCHOTTKY DIODE CLAMPED TTL

9S/54S, 74S SERIES
SUPER HIGH SPEED TTL/SSI INTEGRATED CIRCUITS
SCHOTTKY DIODE CLAMPED TTL

GENERAL DESCRIPTION – The Fairchild Super High Speed 9S/54S, 74S series of TTL circuits is designed to be used in any digital system to achieve ultra high speeds. These circuits, featuring Schottky-barrier diode clamping, are completely compatible with the Fairchild 9N, 9H and 9300 MSI/TTL families.

Schottky diode clamping prevents transistors from achieving saturation, thereby effectively eliminating the excess stored charge effect on turn off delays. The result is an overall improvement in propagation delay and greatly reduced sensitivity of delay time to temperature variation.

These high speed TTL devices are generally recommended for improving the performances of existing TTL systems or for speeding up critical delay paths. For the design of highest performance digital systems using similar interconnection rules to this 9S/54S, 74S series of devices, see the Fairchild 9500 series temperature compensated ECL Family.

Pinning is compatible with Fairchild saturated TTL circuits allowing for direct replacement to achieve improved performance of existing systems.

FEATURES

SUPER HIGH SPEED WITHOUT ADDED POWER

- 3 ns TYPICAL GATE PROPAGATION DELAYS
- 22 mW-PER-GATE POWER DISSIPATION AT 50% DUTY CYCLE
- 125 MHz TYPICAL INPUT CLOCK FREQUENCY FOR J-K FLIP-FLOPS
- STANDARD 14 AND 16 LEAD CERAMIC DUAL IN-LINE PACKAGES

SYSTEM DESIGN CONSIDERATIONS

- GATE AND FLIP-FLOP PINNING IS IDENTICAL TO 9N/74 EQUIVALENT TO ALLOW FOR "PLUG-IN" CONVERSION OF EXISTING SYSTEM DESIGNS FOR HIGHER SPEED
- FULLY COMPATIBLE WITH ALL FAIRCHILD TTL PRODUCTS
- SCHOTTKY CLAMPED INPUTS HELP SIMPLIFY SYSTEM DESIGN BY LIMITING HIGH SPEED TERMINATION EFFECTS
- LOW OUTPUT IMPEDANCE TO DRIVE HIGH CAPACITIVE LOADS, AND PROVIDE EXCELLENT IMMUNITY TO CROSS TALK
- TERMINATED, CONTROLLED IMPEDANCE LINES NOT NORMALLY REQUIRED FOR INTERCONNECTION
- EXTRA HIGH LEVEL FANOUT TO PROVIDE FOR UNUSED INPUT CONNECTIONS

CIRCUIT PERFORMANCE

- HIGH DC NOISE MARGIN – TYPICALLY 1 VOLT IN LOW STATE, 2.1 VOLTS IN HIGH STATE
- HIGH FAN OUT: 12.5 TTL LOADS, 10 SCHOTTKY TTL LOADS

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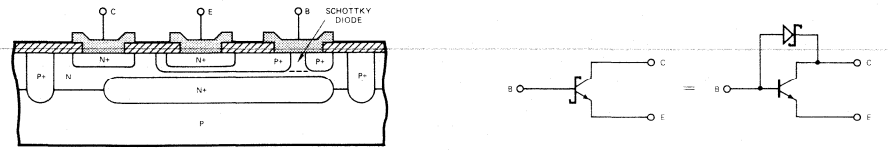
SCHOTTKY NPN TRANSISTOR



FAIRCHILD
SEMICONDUCTOR

ABSOLUTE MAXIMUM RATINGS (Above Which the Useful Life May be Impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground	−0.5V to +7.0V
Input Voltage (dc) (See Note)	−1.2V to +5.5V
Input Current (See Note)	−30 mA to 1.0 mA
Output Voltage, Output Normally HIGH	0V to +V_{CC} value
D.C. Current into Output Terminal, Output LOW (except 9S40/9S140)	50 mA
D.C. Current into Output Terminal, Output LOW (9S40/9S140)	100 mA

NOTE:
Because of the input clamp diodes, excess current can be drawn out of the inputs if the dc input voltage is more negative than −1.2V. The diode is designed to clamp off large negative ac swings associated with fast fall times and long lines. This maximum rating is intended only to limit a steady state input voltage and current condition.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SERIES 9S/54S CIRCUITS			SERIES 9S/74S CIRCUITS			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating free-air temperature range, T_A	−55	25	125	0	25	75	°C

UNUSED INPUTS

To minimize noise sensitivity and optimize switching times, unused inputs of all circuits in the family should be held between 2.7V and the absolute maximum 5.5V. This eliminates the effect of the distributed capacitance associated with the floating input emitter, bond wire, and package lead, and ensures that no degradation will occur in the propagation delay times.

Possible ways of handling unused inputs are:

1. Connect unused inputs to V_{CC} through a 1kΩ resistor. If a transient exceeding the 5.5V maximum rating should occur, the impedance will be high enough to protect the input. One to 25 unused inputs may be connected to each 1kΩ resistor. fan-out for all circuits has been specified at double the LOW level fan-out specifically to provide for this method of treating unused inputs.
2. Connect unused inputs to V_{CC} through a 1kΩ resistor so that if a transient which exceeds the 5.5V maximum rating should occur, the impedance will be high enough to protect the input. One to 25 unused inputs may be connected to each 1kΩ resistor.
3. Tie the inputs to the output of an unused gate in the system. The gate must provide a constant HIGH level output.
4. Connect unused inputs to an independent supply voltage in the range of 2.7V to 3.5V.

LOADING AND FANOUT CHARACTERISTICS

The basic load and fanout factors for the Schottky TTL family of circuits are:

INPUT LOAD REQUIREMENTS

LOGIC LEVEL	SYMBOL	LOAD CURRENT	CONDITIONS
LOW	I_{IL}	−2.0mA	V_{CC} = Max, V_{IN} = 0.4V
HIGH	I_{IH}	50 μA	V_{CC} = Max, V_{IN} = 2.7V

These loading factors are guaranteed over the temperature range, with supply voltage at its maximum value and with the other inputs conditioned to give the absolute worst case load current that the device will ever present to a driver.

The LOW level input current is specified at an input voltage of 0.4V to provide a specification directly compatible when interfacing with other logic families such as TTL and MSI.

FANOUT CHARACTERISTICS

LOGIC LEVEL	SYMBOL	DRIVE CURRENT	CONDITIONS
LOW	I_{OL}	20mA	V_{CC} = Min, V_{OL} = 0.5V
HIGH	I_{OH}	−1.0mA	V_{CC} = Min, V_{OH} = 2.7V (59X)
			2.5V (51X)

These fanout specifications are also guaranteed over the temperature range and with supply voltage and other inputs at conditions that result in the absolute worst case condition for a device as a driver.

Dividing worst case drive current capability by load current requirements gives a basic fanout capability of 10 loads in the LOW logic level and 20 loads in the HIGH logic level. The excess HIGH level capability is provided to allow for tieing unused inputs HIGH (see Unused Inputs).

The loading and/or drive factors of some elements differ from the basic factors listed above. For example the 9S40 can drive 60 mA in the LOW state and 3 mA in the HIGH state. It also has different input load currents. Consistent worst case conditions have been used, however, so that loading and drive factors are easily related to other elements in the family in addition to other circuit families such as TTL and MSI.

BREADBOARDING CONSIDERATIONS

With any high speed TTL circuit, the designer must always be aware of the problems caused by very high switching speeds. Good high-frequency layout techniques should be used for PC boards. Special care should be taken to insure adequate distribution of power and ground systems. To reduce supply transients, bypass capacitors should be supplied at intervals throughout the board.

SCHOTTKY PROCESSING TECHNOLOGY

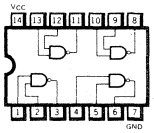
The Schottky barrier diode (SBD) clamped transistor is produced by using standard TTL diffusion techniques. The base contact window is enlarged to include the base diffusion and the collector region (See illustration on page 1). Metal deposited over both the base and collector areas serves as the transistor base contact and the SBD anode contact. The N-type collector and the metal then form the metal-silicon Schottky diode.

Gold doping to decrease excess minority carrier lifetime is not required since all transistors are clamped out of saturation. This and shallow diffusions enable the production of higher gain and f_T transistors which further enhances circuit switching performance.

QUAD 2-INPUT NAND GATE

LOGIC AND CONNECTION DIAGRAM

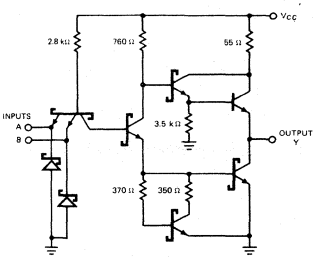
DIP (TOP VIEW)



Positive logic: $Y = \overline{AB}$

SCHEMATIC DIAGRAM

(EACH GATE)



Component values shown are nominal.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9S0051X/54S00			9S0059X/74S00			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	75	°C
Normalized Fan-Out From Each Output			10*			10*	N.L.

*10 Normalized Loads (N.L.) is the LOW drive factor, and 20 N.L. is the HIGH drive factor.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER		LIMITS MIN.	LIMITS TYP. (Note 2)	LIMITS MAX.	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			Volts	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage				0.8	Volts	Guaranteed Input LOW Voltage
V_I	Input Clamp Voltage			–0.65	–1.2	Volts	V_{CC} = MIN., I_{IN} = -18mA
V_{OH}	Output HIGH Voltage	51X	2.5	3.4		Volts	V_{CC} = MIN., I_{OH} = -1.0mA, V_{IN} = 0.8V
		59X	2.7	3.4			
V_{OL}	Output LOW Voltage			0.35	0.5	Volts	V_{CC} = MIN., I_{OL} = 20mA, V_{IN} = 2.0V
I_{IH}	Input HIGH Current			1.0	50	µA	V_{CC} = MAX., V_{IN} = 2.7V, Each Input
					1.0	mA	V_{CC} = MAX., V_{IN} = 5.5V
I_{IL}	Input LOW Current			–1.4	–2.0	mA	V_{CC} = MAX., V_{IN} = 0.4V, Each Input
I_{OS}	Output Short Circuit Current (Note 3)		–40	–65	–100	mA	V_{CC} = MAX., V_{OUT} = 0V
I_{CCH}	Supply Current (HIGH)			10.8	16.0	mA	V_{CC} = MAX., V_{IN} = 0V
I_{CCL}	Supply Current (LOW)			25.2	36.0	mA	V_{CC} = MAX., Inputs Open

SWITCHING CHARACTERISTICS (T_A = 25°C)

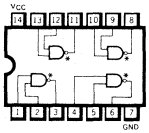
SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS	TEST FIGURES
t_{PLH}	Turn Off Delay Input to Output	2.0	3.0	4.5	ns	V_{CC} = 5.0V	11–15,
t_{PHL}	Turn On Delay Input to Output	2.0	3.0	5.0	ns	C_L = 15pF	16

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0V, 25°C.
(3) Not more than one output should be shorted at a time.

QUAD 2-INPUT NAND GATE
(WITH OPEN-COLLECTOR OUTPUT)

LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)

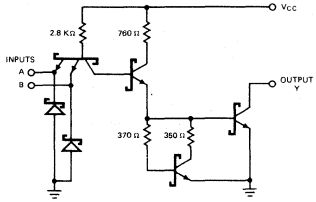


* OPEN COLLECTOR

Positive logic: $Y = \overline{AB}$

SCHEMATIC DIAGRAM

(EACH GATE)



Component values shown are nominal.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9S0351X/54S03			9S0359X/74S03			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	75	°C
Normalized Fan-Out From Each Output			10*			10*	N.L.

*10 Normalized Load (N.L.) is the LOW drive factor.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)
		MIN.	TYP. (Note 2)	MAX.		
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage
V_I	Input Clamp Voltage		–0.65	–1.2	Volts	V_{CC} = MIN., I_{IN} = -18mA
I_{OH}	Output HIGH Current		0.1	250	μA	V_{CC} = MIN., V_{OH} = 5.5V, V_{IN} = 0.8V
V_{OL}	Output LOW Voltage		0.35	0.5	Volts	V_{CC} = MIN., I_{OL} = 20mA, V_{IN} = 2.0V
I_{IH}	Input HIGH Current		1.0	50	μA	V_{CC} = MAX., V_{IN} = 2.7V — Each Input
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5V
I_{IL}	Input LOW Current		–1.4	–2.0	mA	V_{CC} = MAX., V_{IN} = 0.4V — Each Input
I_{CCH}	Supply Current (HIGH)		6.0	13.2	mA	V_{CC} = MAX., V_{IN} = 0V
I_{CCL}	Supply Current (LOW)		25.2	36.0	mA	V_{CC} = MAX., Inputs Open

SWITCHING CHARACTERISTICS (T_A = 25°C)

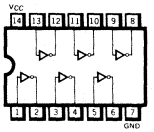
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURES
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output	2.0	5.0	7.5	ns	V_{CC} = 5.0V	11–15,
t_{PHL}	Turn On Delay Input to Output	2.0	4.5	7.0	ns	C_L = 15pF	17

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0V, 25°C.

HEX INVERTER

LOGIC AND CONNECTION DIAGRAM

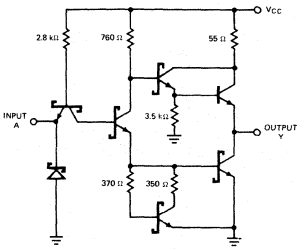
DIP (TOP VIEW)



Positive logic: $Y = \overline{A}$

SCHEMATIC DIAGRAM

(EACH INVERTER)



Component values shown are nominal.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9S0451X/54S04			9S0459X/74S04			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	75	°C
Normalized Fan-Out From Each Output			10*			10*	N.L.

*10 Normalized Loads (N.L.) is the LOW drive factor, and 20 N.L. is the HIGH drive factor.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER		LIMITS MIN.	LIMITS TYP. (Note 2)	LIMITS MAX.	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			Volts	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage				0.8	Volts	Guaranteed Input LOW Voltage
V_I	Input Clamp Voltage			–0.65	–1.2	Volts	V_{CC} = MIN., I_{IN} = -18mA
V_{OH}	Output HIGH Voltage	51X	2.5	3.4		Volts	V_{CC} = MIN., I_{OH} = -1.0mA, V_{IN} = 0.8V
		59X	2.7	3.4			
V_{OL}	Output LOW Voltage			0.35	0.5	Volts	V_{CC} = MIN., I_{OL} = 20mA, V_{IN} = 2.0V
I_{IH}	Input HIGH Current			1.0	50	µA	V_{CC} = MAX., V_{IN} = 2.7V
					1.0	mA	V_{CC} = MAX., V_{IN} = 5.5V
I_{IL}	Input LOW Current			–1.4	–2.0	mA	V_{CC} = MAX., V_{IN} = 0.4V
I_{OS}	Output Short Circuit Current (Note 3)		–40	–65	–100	mA	V_{CC} = MAX., V_{OUT} = 0V
I_{CCH}	Supply Current (HIGH)			16.2	24.0	mA	V_{CC} = MAX., V_{IN} = 0V
I_{CCL}	Supply Current (LOW)			37.8	54.0	mA	V_{CC} = MAX., Inputs Open

SWITCHING CHARACTERISTICS (T_A = 25°C)

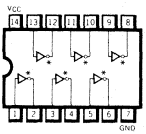
SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS	TEST FIGURES
t_{PLH}	Turn Off Delay Input to Output	2.0	3.0	4.5	ns	V_{CC} = 5.0V	11–15,
t_{PHL}	Turn On Delay Input to Output	2.0	3.0	5.0	ns	C_L = 15pF	16

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0V, 25°C.
(3) Not more than one output should be shorted at a time.

HEX INVERTER
(WITH OPEN-COLLECTOR OUTPUT)

LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)

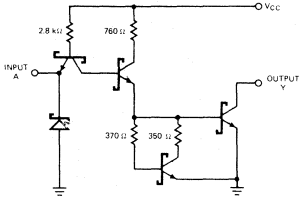


* OPEN COLLECTOR

Positive logic: $Y = \overline{A}$

SCHEMATIC DIAGRAM

(EACH INVERTER)



Component values shown are nominal.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9S0551X/54S05			9S0559X/74S05			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	−55	25	125	0	25	75	°C
Normalized Fan-Out From Each Output			10*			10*	N.L.

*10 Normalized Load (N.L.) is the LOW drive factor.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)
		MIN.	TYP. (Note 2)	MAX.		
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed input LOW Voltage
V_I	Input Clamp Voltage		−0.65	−1.2	Volts	V_{CC} = MIN., I_{IN} = -18mA
I_{OH}	Output HIGH Current		0.1	250	μA	V_{CC} = MIN., V_{OH} = 5.5V, V_{IN} = 0.8V
V_{OL}	Output LOW Voltage		0.35	0.5	Volts	V_{CC} = MIN., I_{OL} = 20mA, V_{IN} = 2.0V
I_{IH}	Input HIGH Current		1.0	50	μA	V_{CC} = MAX., V_{IN} = 2.7V
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5V
I_{IL}	Input LOW Current		−1.4	−2.0	mA	V_{CC} = MAX., V_{IN} = 0.4V
I_{CCH}	Supply Current (HIGH)		9.0	19.8	mA	V_{CC} = MAX., V_{IN} = 0V
I_{CCL}	Supply Current (LOW)		37.8	54.0	mA	V_{CC} = MAX., Inputs Open

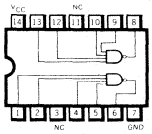
SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURES
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output	2.0	5.0	7.5	ns	V_{CC} = 5.0V	11–15,
t_{PHL}	Turn On Delay Input to Output	2.0	4.5	7.0	ns	C_L = 15pF	17

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0V, 25°C.

DUAL 4 – INPUT NAND GATE

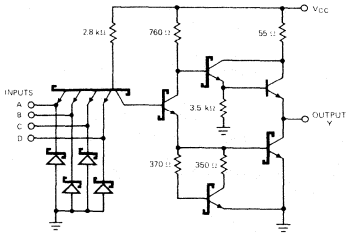
LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



Positive logic: $Y = \overline{ABCD}$

NC–No internal connection.

SCHEMATIC DIAGRAM
(EACH GATE)



Component values shown are nominal.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9S2051X/54S20			9S2059X/74S20			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	75	°C
Normalized Fan-Out From Each Output			10*			10*	N.L.

*10 Normalized Loads (N.L.) is the LOW drive factor, and 20 N.L. is the HIGH drive factor.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER		LIMITS MIN.	LIMITS TYP. (Note 2)	LIMITS MAX.	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			Volts	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage				0.8	Volts	Guaranteed Input LOW Voltage
V_I	Input Clamp Voltage			–0.65	–1.2	Volts	V_{CC} = MIN., I_{IN} = -18mA
V_{OH}	Output HIGH Voltage	51X	2.5	3.4		Volts	V_{CC} = MIN., I_{OH} = -1.0mA, V_{IN} = 0.8V
		59X	2.7	3.4			
V_{OL}	Output LOW Voltage			0.35	0.5	Volts	V_{CC} = MIN., I_{OL} = 20mA, V_{IN} = 2.0V
I_{IH}	Input HIGH Current			1.0	50	µA	V_{CC} = MAX., V_{IN} = 2.7V — Each Input
					1.0	mA	V_{CC} = MAX., V_{IN} = 5.5V — Each Input
I_{IL}	Input LOW Current			–1.4	–2.0	mA	V_{CC} = MAX., V_{IN} = 0.4V
I_{OS}	Output Short Circuit Current (Note 3)		–40	–65	–100	mA	V_{CC} = MAX., V_{OUT} = 0V
I_{CCH}	Supply Current (HIGH)			5.4	8.0	mA	V_{CC} = MAX., V_{IN} = 0V
I_{CCL}	Supply Current (LOW)			12.6	18.0	mA	V_{CC} = MAX., Inputs Open

SWITCHING CHARACTERISTICS (T_A = 25°C)

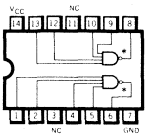
SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS	TEST FIGURES
t_{PLH}	Turn Off Delay Input to Output	2.0	3.0	4.5	ns	V_{CC} = 5.0V	11–15,
t_{PHL}	Turn On Delay Input to Output	2.0	3.0	5.0	ns	C_L = 15pF	16

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0V, 25°C.
(3) Not more than one output should be shorted at a time.

DUAL 4 – INPUT NAND GATE
(WITH OPEN-COLLECTOR OUTPUT)

LOGIC AND CONNECTION DIAGRAM

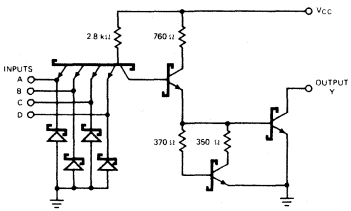
DIP (TOP VIEW)



* OPEN COLLECTOR
NC—No internal connection.
Positive logic: $Y = \overline{ABCD}$

SCHEMATIC DIAGRAM

(EACH GATE)



Component values shown are nominal.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9S2251X/54S22			9S2259X/74S22			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	75	°C
Normalized Fan-Out From Each Output			10*			10*	N.L.

*10 Normalized Load (N.L.) is the LOW drive factor.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)	
		MIN.	TYP. (Note 2)	MAX.			
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage	
V_I	Input Clamp Voltage		–0.65	–1.2	Volts	V_{CC} = MIN., I_{IN} = –18mA	
I_{OH}	Output HIGH Current		0.1	250	μA	V_{CC} = MIN., V_{OH} = 5.5V, V_{IN} = 0.8V	
V_{OL}	Output LOW Voltage		0.35	0.5	Volts	V_{CC} = MIN., I_{OL} = 20mA, V_{IN} = 2.0V	
I_{IH}	Input HIGH Current		1.0	50	μA	V_{CC} = MAX., V_{IN} = 2.7V	Each Input
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5V	
I_{IL}	Input LOW Current		–1.4	–2.0	mA	V_{CC} = MAX., V_{IN} = 0.4V	Each Input
I_{CCH}	Supply Current (HIGH)		3.0	6.6	mA	V_{CC} = MAX., V_{IN} = 0V	
I_{CCL}	Supply Current (LOW)		12.6	18.0	mA	V_{CC} = MAX., Inputs Open	

SWITCHING CHARACTERISTICS (T_A = 25°C)

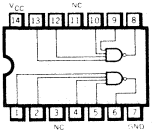
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURES
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output	2.0	5.0	7.5	ns	V_{CC} = 5.0V	11–15,
t_{PHL}	Turn On Delay Input to Output	2.0	4.5	7.0	ns	C_L = 15pF	17

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0V, 25°C.

DUAL 4 – INPUT NAND BUFFER

LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)

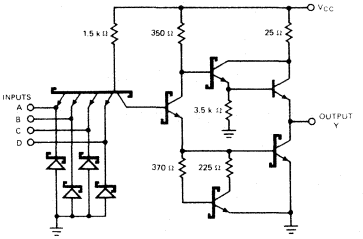


NC—No internal connection.

Positive logic: $Y = \overline{ABCD}$

SCHEMATIC DIAGRAM

(EACH GATE)



Component values shown are nominal.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9S4051X/54S40			9S4059X/74S40			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	75	°C
Normalized Fan-Out From Each Output			30*			30*	N.L.

*30 Normalized Loads (N.L.) is the LOW drive factor and 60 N.L. is the HIGH drive factor.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER		LIMITS MIN.	LIMITS TYP. (Note 2)	LIMITS MAX.	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			Volts	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage				0.8	Volts	Guaranteed Input LOW Voltage
V_I	Input Clamp Voltage			–0.65	–1.2	Volts	V_{CC} = MIN., I_{IN} = –18mA
V_{OH}	Output HIGH Voltage	51X	2.5	3.4		Volts	V_{CC} = MIN., I_{OH} = –3.0mA, V_{IN} = 0.8V
		59X	2.7	3.4			
V_{OL}	Output LOW Voltage			0.4	0.5	Volts	V_{CC} = MIN., I_{OL} = 60mA, V_{IN} = 2.0V
I_{IH}	Input HIGH Current			1.0	100	μA	V_{CC} = MAX., V_{IN} = 2.7V; Each Input
					1.0	mA	V_{CC} = MAX., V_{IN} = 5.5V
I_{IL}	Input LOW Current			–2.5	–4.0	mA	V_{CC} = MAX., V_{IN} = 0.4V Each Input
I_{OS}	Output Short Circuit Current (Note 3)		–50	–150	–225	mA	V_{CC} = MAX., V_{OUT} = 0V
I_{CCH}	Supply Current (HIGH)			8.2	18.0	mA	V_{CC} = MAX., V_{IN} = 0V
I_{CCL}	Supply Current (LOW)			27.2	44.0	mA	V_{CC} = MAX., Inputs Open

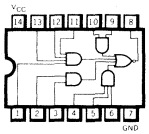
SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS	TEST FIGURES
t_{PLH}	Turn Off Delay Input to Output	2.0	4.0	6.5	ns	V_{CC} = 5.0V	11–15,
t_{PHL}	Turn On Delay Input to Output	2.0	4.0	6.5	ns	C_L = 50pF	16

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0V, 25°C.
(3) Not more than one output should be shorted at a time.

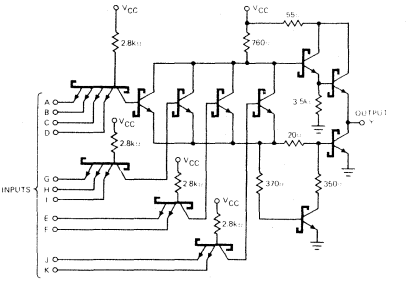
4-2-3-2-INPUT AND-OR-INVERT GATE

LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



Positive logic: $\overline{ABCD + EF + GHE + JK}$

SCHEMATIC DIAGRAM



Component values shown are nominal

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9S6451X/54S64			9S6459X/74S64			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	75	°C
Normalized Fan-Out from Each Output			10*			10*	N.L.

*10 Normalized Loads (N.L.) is the LOW drive factor, and 20 N.L. is the HIGH drive factor.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER		LIMITS MIN.	LIMITS TYP. (Note 2)	LIMITS MAX.	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			Volts	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage				0.8	Volts	Guaranteed Input LOW Voltage
V_I	Input Clamp Voltage			–0.65	–1.2	Volts	V_{CC} = MIN., I_{IN} = –18 mA
V_{OH}	Output HIGH Voltage	51X	2.5	3.4		Volts	V_{CC} = MIN., I_{OH} = –1.0 mA, V_{IN} = 0.8 V
		59X	2.7	3.4			
V_{OL}	Output LOW Voltage			0.35	0.5	Volts	V_{CC} = MIN., I_{OL} = 20 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	50	μA	V_{CC} = MAX., V_{IN} = 2.7 V
					1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{IL}	Input LOW Current			–1.4	–2.0	mA	V_{CC} = MAX., V_{IN} = 0.4V
I_{OS}	Output Short Circuit Current (Note 3)		–40	–65	–100	mA	V_{CC} = MAX., V_{OUT} = 0V
I_{CCH}	Supply Current (HIGH)			7.0	12.5	mA	V_{CC} = MAX., V_{IN} = 0 V
I_{CCL}	Supply Current (LOW)			8.5	16	mA	V_{CC} = MAX., Note 4

SWITCHING CHARACTERISTICS (T_A = 25°C)

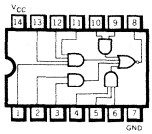
SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS	TEST FIGURES
t_{PLH}	Turn Off Delay Input to Output	2.0	3.5	5.5	ns	V_{CC} = 5.0 V	11-15,
t_{PHL}	Turn On Delay Input to Output	2.0	3.5	5.5	ns	C_L = 15 pF	18

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.
(4) I_{CCL} is measured with all inputs of one gate open, and remaining inputs grounded.

*To be announced first quarter 1972.

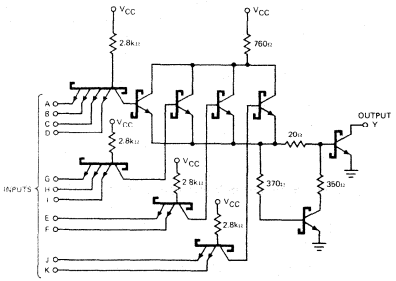
4-2-3-2-INPUT AND-OR-INVERT GATE (WITH OPEN COLLECTOR)

LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



Positive logic: $\overline{ABCD + EF + GHI + JK}$

SCHEMATIC DIAGRAM



Component values shown are nominal

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9S6551X/54S65			9S6559X/74S65			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	−55	25	125	0	25	75	°C
Normalized Fan-Out from Each Output			10*			10*	N.L.

*10 Normalized Load (N.L.) is the LOW drive factor.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)
		MIN.	TYP. (Note 2)	MAX.		
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage
V_I	Input Clamp Voltage			−1.2	Volts	V_{CC} = MIN., I_{IN} = −18 mA
I_{OH}	Output HIGH Current		0.1	250	μA	V_{CC} = MIN., V_{OH} = 5.5 V, V_{IN} = 0.8 V
V_{OL}	Output LOW Voltage		0.35	0.5	Volts	V_{CC} = MIN., I_{OL} = 20 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current		1.0	50	μA	V_{CC} = MAX., V_{IN} = 2.7 V
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{IL}	Input LOW Current		−1.4	−2.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V
I_{CCH}	Supply Current (HIGH)		6.0	11.0	mA	V_{CC} = MAX., V_{IN} = 0 V
I_{CCL}	Supply Current (LOW)		8.5	16	mA	V_{CC} = MAX., Note 4

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURES
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output	2.0	5.0	7.5	ns	V_{CC} = 5.0 V	11-15,
t_{PHL}	Turn On Delay Input to Output	2.0	5.5	8.5	ns	C_L = 15 pF	18

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.
(4) I_{CCL} is measured with all inputs of one gate open, and remaining inputs grounded.

*To be announced first quarter 1972.

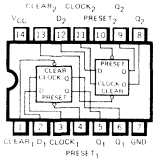
DUAL D-TYPE EDGE TRIGGERED FLIP-FLOP

DESCRIPTION – The 9S74/54S74, 74S74 dual edge-triggered flip-flops utilize Schottky TTL circuitry to produce very high speed D-type flip-flops. Each flip-flop has individual clear and preset inputs, and also complementary Q and $\overline{Q}$ outputs.

Information at input D is transferred to the Q output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the HIGH or LOW level the D-input signal has no effect.

These circuits are fully compatible for use with most TTL or DTL circuits. Maximum clock frequency is 75 mHz, with a typical power dissipation of 75 mW per flip-flop.

LOGIC AND CONNECTION DIAGRAM DIP (TOP VIEW)



Positive logic: LOW input to preset sets Q to HIGH level
LOW input to clear resets Q to LOW level
Preset and clear are independent of clock

SYNCHRONOUS TRUTH TABLE (EACH FLIP-FLOP)

t_n	t_{n+1}
INPUT	OUTPUT
D	Q $\overline{Q}$
L	L H
H	H L

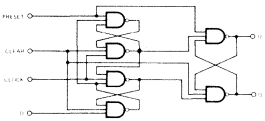
H = HIGH level
L = LOW level
D = Data

NOTES:
A. t_n = bit time before clock pulse
B. t_{n+1} = bit time after clock pulse

ASYNCHRONOUS TRUTH TABLE (EACH FLIP-FLOP)

INPUT		OUTPUT	
Preset	Clear	Q	$\overline{Q}$
L	L	H	H
L	H	H	L
H	L	L	H
H	H	No Change	

LOGIC DIAGRAM (EACH FLIP-FLOP)



RECOMMENDED OPERATING CONDITIONS

PARAMETER	9S7451X/54S74			9S7459X/74S74			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	75	°C
Normalized Fan-Out from Each Output			10*			10*	N.L.

*10 Normalized Loads (N.L.) is the LOW drive factor, and 20 N.L. is the HIGH drive factor.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

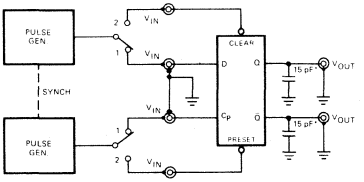
SYMBOL	PARAMETER		LIMITS MIN.	LIMITS TYP. (Note 2)	LIMITS MAX.	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			Volts	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage				0.8	Volts	Guaranteed Input LOW Voltage
V_I	Input Clamp Voltage			–0.65	–1.2	Volts	V_{CC} = MIN., I_{IN} = –18 mA
V_{OH}	Output HIGH Voltage	51X	2.5	3.4		Volts	V_{CC} = MIN., I_{OH} = –1.0 mA
		59X	2.7	3.4			
V_{OL}	Output LOW Voltage			0.35	0.5	Volts	V_{CC} = MIN., I_{OL} = 20 mA
I_{IH}	Input HIGH Current at	D		1.0	50	µA	V_{CC} = MAX., V_{IN} = 2.7 V
		Preset or Clock		2.0	100		
		Clear		3.0	150		
I_{IL}	Input LOW Current at	D		–1.4	–2.0	mA	V_{CC} = MAX., V_{IN} = 0.4V
		Preset or Clock		–2.8	–4.0		
		Clear		–4.2	–6.0		
I_{OS}	Output Short Circuit Current (Note 3)		–40	–65	–100	mA	V_{CC} = MAX., V_{OUT} = 0V
I_{CC}	Supply Current			26.4	40	mA	V_{CC} = MAX. Note 4

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.
(4) I_{CC} is measured with clock and data inputs grounded and either preset or clear inputs grounded.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
f_{max}	Maximum Clock Frequency		100		MHz	V_{CC} = 5.0 V C_L = 15 pF	1
t_{PLH}	Turn Off Delay Clear or Preset to Output		4.0		ns		
t_{PHL}	Turn On Delay Clear or Preset to Output		7.0		ns		
t_{PLH}	Turn Off Delay Clock to Output		7.0		ns		
t_{PHL}	Turn On Delay Clock to Output		7.0		ns		

SWITCHING CHARACTERISTICS



*Includes all probe and jig capacitance.

PULSE GENERATOR SETTINGS

CLOCK

f ≈ 1 MHz
$t_f = t_r$ = 2.5 ns
Amp = 0 to 3 V
Duty cycle= 50%

D

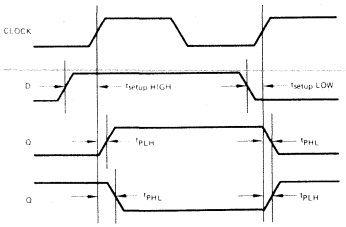
f ≈ 500 kHz
$t_f = t_r$ = 2.5 ns
Amp = 0 to 3 V
t_{setup} (HIGH) = 5 ns
t_{setup} (LOW) = 4 ns
Duty cycle = Adjust pulse width to attain t_{setup} (HIGH) and t_{setup} (LOW) relative to clock as shown in waveforms.

DIRECT SET, CLEAR

f ≈ 1 MHz
$t_f = t_r$ = 2.5 ns
Amp = 0 to 3 V
Duty cycle =Adjust pulse width and synch to attain waveforms shown.

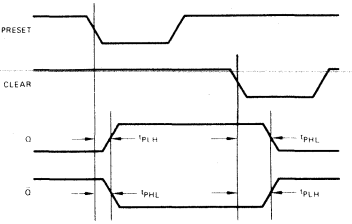
SWITCHING WAVEFORMS

CLOCK TO OUTPUT DELAY†



SWITCH IN POSITION 1

DIRECT SET, AND CLEAR TO OUTPUT DELAY



SWITCH IN POSITION 2

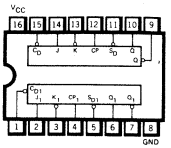
†Direct set and clear inputs connected to V_{CC} thru 2 kΩ resistor during test.

Fig. 1

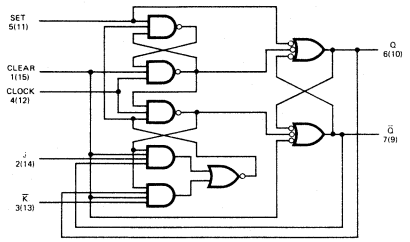
DUAL J-$\overline{K}$ FLIP-FLOP

DESCRIPTION — The 9S109 consists of two high-speed, completely independent transition clocked J$\overline{K}$ flip-flops. The clocking operation is independent of rise and fall times of the clock waveform. The J$\overline{K}$ design allows operation as a D flip-flop by simply connecting the J and $\overline{K}$ pins together. The 9S109 is a pin for pin replacement of the 9024.

LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



LOGIC DIAGRAM



TRUTH TABLES

SYNCHRONOUS ENTRY D MODE OPERATION

INPUTS AT t_n	OUTPUTS AT t_{n+1}	
D	Q	$\overline{Q}$
L	L	H
H	H	L

SYNCHRONOUS ENTRY J-$\overline{K}$ MODE OPERATION

INPUTS AT t_n		OUTPUTS AT t_{n+1}	
J	$\overline{K}$	Q	$\overline{Q}$
L	H	No Change	
L	L	L	H
H	H	H	L
H	L	Toggles	

ASYNCHRONOUS ENTRY INDEPENDENT OF CLOCK & SYNCHRONOUS INPUTS

INPUTS		OUTPUTS	
S_D	C_D	Q	$\overline{Q}$
L	L	H	H
L	H	H	L
H	L	L	H
H	H	No Change	

L = LOW Logic Level
H = HIGH Logic Level

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9S10951X/54S109			9S10959X/74S109			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	75	°C
Normalized Fan-Out from Each Output			10*			10*	N.L.

*10 Normalized Loads (N.L.) is the LOW drive factor, and 20 N.L. is the HIGH drive factor.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER		LIMITS MIN.	LIMITS TYP. (Note 2)	LIMITS MAX.	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			Volts	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage				0.8	Volts	Guaranteed Input LOW Voltage
V_I	Input Clamp Voltage			–0.65	–1.2	Volts	V_{CC} = MIN., I_I = –18 mA
V_{OH}	Output HIGH Voltage	51X	2.5	3.4		Volts	V_{CC} = MIN., I_{OH} = –1.0 mA
		59X	2.7	3.4			
V_{OL}	Output LOW Voltage			0.35	0.5	Volts	V_{CC} = MIN., I_{OL} = 20 mA
I_{IH}	Input HIGH Current at	J$\overline{K}$		1.0	50	µA	V_{CC} = MAX., V_{IN} = 2.7 V
		$\overline{S}_D$		2.0	100		
		$\overline{C}_D$		4.0	200		
I_{IL}	Input LOW Current at	J$\overline{K}$		–1.4	–2.0	mA	V_{CC} = MAX., V_{IN} = 0.5 V
		$\overline{S}_D$		–2.8	–4.0		
		$\overline{C}_D$		–5.6	–8.0		
I_{OS}	Output Short Circuit Current (Note 3)		–40	–65	–100	mA	V_{CC} = MAX., V_{OUT} = 0V
I_{CC}	Supply Current			28	42	mA	V_{CC} = MAX., Note 4

Notes on following page

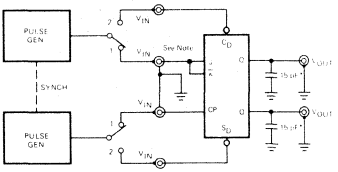
*To be announced first quarter 1972.

SWITCHING CHARACTERISTICS ($T_A = 25^\circ C$)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS	TEST FIGURE
f_{max}	Maximum Clock Frequency		100		MHz	$V_{CC} = 5.0$ V, $C_L = 15$ pF	2
t_{PLH}	Turn Off Delay Clear or Preset to Output		4.0		ns		
t_{PHL}	Turn On Delay Clear or Preset to Output		7.0		ns		
t_{PLH}	Turn Off Delay Clock to Output		7.0		ns		
t_{PHL}	Turn On Delay Clock to Output		7.0		ns		

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at $V_{CC} = 5.0$ V, 25°C.
(3) Not more than one output should be shorted at a time.
(4) I_{CC} is measured Clock, Set and $\overline{K}$ inputs grounded.

SWITCHING CHARACTERISTICS



*Includes all probe and jig capacitance.

NOTE: For testing 9S109, connect J,$\overline{K}$ pins together to form a D input.

PULSE GENERATOR SETTINGS

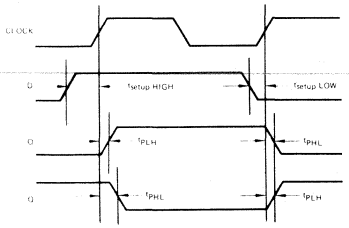
CLOCK
f ≈ 1 MHz
$t_f \approx t_r = 2.5$ ns
Amp = 0 to 3 V
Duty cycle = 50%

J$\overline{K}$
f ≈ 500 kHz
$t_f = t_r = 2.5$ ns
Amp = 0 to 3 V
t_{setup} (HIGH)
t_{setup} (LOW)
Duty cycle = Adjust pulse width to attain t_{setup} (HIGH) and t_{setup} (LOW) relative to clock as shown in waveforms.

DIRECT SET, CLEAR
f ≈ 1 MHz
$t_f = t_r = 2.5$ ns
Amp = 0 to 3 V
Duty cycle = Adjust pulse width and synch to attain waveforms shown.

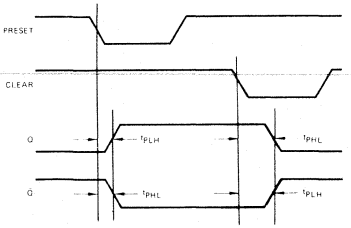
SWITCHING WAVEFORMS

CLOCK TO OUTPUT DELAY†



SWITCH IN POSITION 1

DIRECT SET, AND CLEAR TO OUTPUT DELAY



SWITCH IN POSITION 2

†Direct set and clear inputs connected to V_{CC} thru 2 kΩ resistor during test.

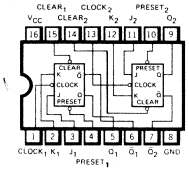
Fig. 2

*To be announced first quarter 1972

DUAL J-K EDGE-TRIGGERED FLIP-FLOP

DESCRIPTION — The 9S112/54S112, 74S112 dual J-K flip-flops feature individual J, K, clock, and asynchronous preset and clear inputs to each flip-flop. When the clock goes HIGH, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is HIGH and the bistable will perform according to the truth table as long as minimum setup and hold time are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



Positive logic: LOW input to preset sets Q to HIGH level.
LOW input to clear resets Q to LOW level.
Clear and preset are independent of clock.

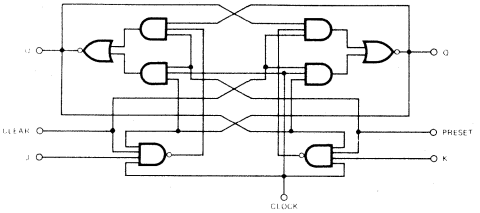
TRUTH TABLES

t_n		t_n+1
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\bar{Q}_n$

Preset	Clear	Q	$\bar{Q}$
L	L	H	H
L	H	L	H
H	L	H	L
H	H	No Change	

NOTES:
A. t_n = Bit time before clock pulse.
B. t_n+1 = Bit time after clock pulse.

LOGIC DIAGRAM
(Each Flip-Flop)



RECOMMENDED OPERATING CONDITIONS

PARAMETER	9S11251X/54S112			9S11259X/74S112			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	−55	25	125	0	25	75	°C
Normalized Fan-Out from Each Output			10*			10*	N.L.

*10 Normalized Loads (N.L.) is the LOW drive factor, and 20 N.L. is the HIGH drive factor.

*To be announced first quarter 1972

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER		LIMITS MIN.	LIMITS TYP. (Note 2)	LIMITS MAX.	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			Volts	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage				0.8	Volts	Guaranteed Input LOW Voltage
V_I	Input Clamp Voltage			−0.65	−1.2	Volts	V_{CC} = MIN., I_I = −18 mA
V_{OH}	Output HIGH Voltage	51X	2.5	3.4		Volts	V_{CC} = MIN., I_{OH} = −1.0 mA
		59X	2.7	3.4			
V_{OL}	Output LOW Voltage			−0.35	0.5	Volts	V_{CC} = MIN., I_{OL} = 20 mA
I_{IH}	Input HIGH Current at	J,K		1.0	50	μA	V_{CC} = MAX., V_{IN} = 2.7 V
		Clock Preset Clear		2.0	100		
I_{IL}	Input LOW Current at	J,K		−0.96	−1.6	mA	V_{CC} = MAX., V_{IN} = 0.4V
		Clock		−2.8	−4.0		
		Preset Clear		−4.9	−7.0		
I_{OS}	Output Short Circuit Current (Note 3)		−40	−65	−100	mA	V_{CC} = MAX., V_{OUT} = 0V
I_{CC}	Supply Current			30	50	mA	V_{CC} = MAX. Note 4

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS	TEST FIGURE
f_{max}	Maximum Clock Frequency	80	125		MHz	V_{CC} = 5.0 V, C_L = 15 pF	Note 5
t_{PLH}	Turn Off Delay.Clear or Preset to Output			7.0	ns		
t_{PHL}	Turn On Delay Clear or Preset to Output			7.0	ns		
t_{PLH}	Turn Off Delay Clock to Output			7.0	ns		
t_{PHL}	Turn On Delay Clock to Output			7.0	ns		

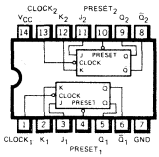
NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.
(4) I_{CC} is measured with outputs open, clock grounded and J,K, preset and clear at 4.5 V.
(5) Switching curves to be available at later date.

*To be announced first quarter 1972.

DUAL J-K EDGE-TRIGGERED FLIP-FLOP

DESCRIPTION – The 9S113/54S113, 74S113 offer individual J, K, preset, and clock inputs. These monolithic dual flip-flops are designed so that when the clock goes HIGH, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is HIGH and the bistable will perform according to the truth table as long as minimum setup times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



Positive logic: LOW input to preset sets Q to HIGH level
Preset is independent of clock

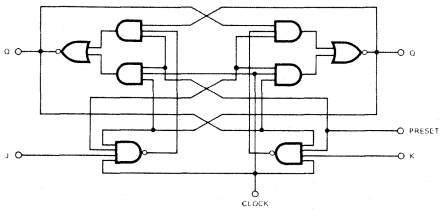
TRUTH TABLES

t_n		t_n+1
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	L	$\bar{Q}_n$

Preset	Q	$\bar{Q}$
L	H	L
H	No Change	

NOTES:
A. t_n = Bit time before clock pulse.
B. t_n+1 = Bit time after clock pulse.

LOGIC DIAGRAM
(Each Flip-Flop)



RECOMMENDED OPERATING CONDITIONS

PARAMETER	9S11351X/54S113			9S11359X/74S113			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	75	°C
Normalized Fan-Out from Each Output			10*			10*	N.L.

*10 Normalized Loads (N.L.) is the LOW drive factor, and 20 N.L. is the HIGH drive factor.

*To be announced first quarter 1972

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER		LIMITS MIN.	LIMITS TYP. (Note 2)	LIMITS MAX.	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			Volts	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage				0.8	Volts	Guaranteed Input LOW Voltage
V_I	Input Clamp Voltage			−0.65	−1.2	Volts	V_{CC} = MIN., I_I = −18 mA
V_{OH}	Output HIGH Voltage	51X	2.5	3.4		Volts	V_{CC} = MIN., I_{OH} = −1.0 mA
		59X	2.7	3.4			
V_{OL}	Output LOW Voltage			0.35	0.5	Volts	V_{CC} = MIN., I_{OL} = 20 mA
I_{IH}	Input HIGH Current at	J,K		1.0	50	μA	V_{CC} = MAX., V_{IN} = 2.7 V
		Clock		2.0	100		
		Preset		2.0	100		
I_{IL}	Input LOW Current at	J,K		−0.96	−1.6	mA	V_{CC} = MAX., V_{IN} = 0.4V
		Clock		−2.8	−4.0		
		Preset		−4.9	−7.0		
I_{OS}	Output Short Circuit Current (Note 3)		−40	−65	−100	mA	V_{CC} = MAX., V_{OUT} = 0V
I_{CC}	Supply Current			30	50	mA	V_{CC} = MAX. Note 4

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS	TEST FIGURE
f_{max}	Maximum Clock Frequency	80	125		MHz	V_{CC} = 5.0 V, C_L = 15 pF	Note 5
t_{PLH}	Turn Off Delay Clear or Preset to Output			7.0	ns		
t_{PHL}	Turn On Delay Clear or Preset to Output			7.0	ns		
t_{PLH}	Turn Off Delay Clock to Output			7.0	ns		
t_{PHL}	Turn On Delay Clock to Output			7.0	ns		

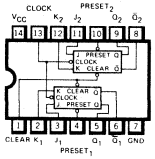
NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.
(4) I_{CC} is measured with outputs open, clock grounded and J,K, preset and clear at 4.5 V.
(5) Switching curves to be available at later date.

*To be announced first quarter 1972.

DUAL J-K EDGE-TRIGGERED FLIP-FLOP

DESCRIPTION – The 9S114/54S114, 74S114 offer common clock and common clear inputs and individual J, K, and preset inputs. These monolithic dual flip-flops are designed so that when the clock goes HIGH, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is HIGH and the bistable will perform according to the truth table as long as minimum setup times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



Positive logic: LOW input to preset sets Q to HIGH level.
LOW input to clear resets Q to LOW level.
Preset and clear are independent of clock.

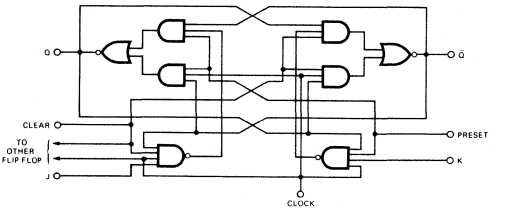
TRUTH TABLES

t_n		t_n+1
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\bar{Q}_n$

Preset	Clear	Q	$\bar{Q}$
L	L	H	H
L	H	H	L
H	L	L	H
H	H	No Charge	

NOTES:
A. t_n = Bit time before clock pulse.
B. t_n+1 = Bit time after clock pulse.

LOGIC DIAGRAM
(Each Flip-Flop)



RECOMMENDED OPERATING CONDITIONS

PARAMETER	9S11451X/54S114			9S11459X/74S114			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	-55	25	125	0	25	75	°C
Normalized Fan-Out from Each Output			10 *			10 *	N.L.

*10 Normalized Loads (N.L.) is the LOW drive factor, and 20 N.L. is the HIGH drive factor.

*To be announced first quarter 1972

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER		LIMITS MIN.	LIMITS TYP. (Note 2)	LIMITS MAX.	UNITS	TEST CONDITIONS (Note 2)
V_{IH}	Input HIGH Voltage		2.0			Volts	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage				0.8	Volts	Guaranteed Input LOW Voltage
V_I	Input Clamp Voltage			–0.65	–1.2	Volts	V_{CC} = MIN., I_I = –18 mA
V_{OH}	Output HIGH Voltage	51X	2.5	3.4		Volts	V_{CC} = MIN., I_{OH} = –1.0 mA
		59X	2.7	3.4			
V_{OL}	Output LOW Voltage			–0.35	0.5	Volts	V_{CC} = MIN., I_{OL} = 20 mA
I_{IH}	Input HIGH Current at	JK		1.0	50	µA	V_{CC} = MAX., V_{IN} = 2.7 V
		Clock		4.0	200		
		Preset		2.0	100		
		Clear		4.0	200		
I_{IL}	Input LOW Current at	JK		–0.96	–1.6	mA	V_{CC} = MAX., V_{IN} = 0.4V
		Clock		–5.6	–8.0		
		Preset		–4.9	–7.0		
		Clear		–9.8	–14		
I_{OS}	Output Short Circuit Current (Note 3)		–40	–65	–100	mA	V_{CC} = MAX., V_{OUT} = 0V
I_{CC}	Supply Current			30	50	mA	V_{CC} = MAX. Note 4

SWITCHING CHARACTERISTICS (T_A = 25° C)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS	TEST FIGURE
f_{max}	Maximum Clock Frequency	80	125		MHz	V_{CC} = 5.0 V, C_L = 15 pF	Note 5
t_{PLH}	Turn Off Delay Clear or Preset to Output			7.0	ns		
t_{PHL}	Turn On Delay Clear or Preset to Output			7.0	ns		
t_{PLH}	Turn Off Delay Clock to Output			7.0	ns		
t_{PHL}	Turn On Delay Clock to Output			7.0	ns		

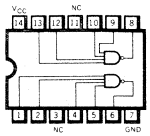
Notes:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.
(4) I_{CC} is measured with outputs open, clock grounded and J, K, preset and clear at 4.5 V.
(5) Switching curves to be available at later date.

*To be announced first quarter 1972.

DUAL 4 – INPUT NAND LINE DRIVER

LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)

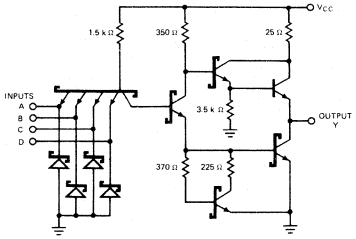


Positive logic: $Y = \overline{ABCD}$

NC—No internal connection.

SCHEMATIC DIAGRAM

(EACH GATE)



Component values shown are nominal.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9S14051X/54S140			9S14059X/74S140			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	75	°C
Normalized Fan-Out From Each Output			30*			30*	N.L.

*30 Normalized Loads (N.L.) is the LOW drive factor, and 60 is the HIGH drive factor.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER		LIMITS MIN.	LIMITS TYP. (Note 2)	LIMITS MAX.	UNITS	TEST CONDITIONS (Note 1)	
V_{IH}	Input HIGH Voltage		2.0			Volts	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	Volts	Guaranteed Input LOW Voltage	
V_I	Input Clamp Voltage			–0.65	–1.2	Volts	V_{CC} = MIN., I_{IN} = -18mA	
V_{OH}	Output HIGH Voltage	51X	2.0	2.8		Volts	V_{CC} = MIN., V_{IN} = 0.5V, R_0 = 50Ω to Gnd	
		59X	2.0	2.8				
V_{OL}	Output LOW Voltage			0.4	0.5	Volts	V_{CC} = MIN., I_{OL} = 60mA, V_{IN} = 2.0V	
I_{IH}	Input HIGH Current			1.0	100	µA	V_{CC} = MAX., V_{IN} = 2.7V	Each Input
					1.0	mA	V_{CC} = MAX., V_{IN} = 5.5V	
I_{IL}	Input LOW Current			–2.5	–4.0	mA	V_{CC} = MAX., V_{IN} = 0.4V	Each Input
I_{OS}	Output Short Circuit Current (Note 3)		–50	–150	–225	mA	V_{CC} = MAX., V_{OUT} = 0V	
I_{CCH}	Supply Current (HIGH)			8.2	18.0	mA	V_{CC} = MAX., V_{IN} = 0V	
I_{CCL}	Supply Current (LOW)			27.2	44.0	mA	V_{CC} = MAX., Inputs Open	

SWITCHING CHARACTERISTICS (T_A = 25°C)

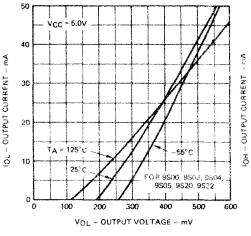
SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS	TEST FIGURES
t_{PLH}	Turn Off Delay Input to Output	2.0	4.0	6.5	ns	V_{CC} = 5.0V, C_L = 50pF	11–16
t_{PHL}	Turn On Delay Input to Output	2.0	4.0	6.5	ns		

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0V, 25°C.
(3) Not more than one output should be shorted at a time.

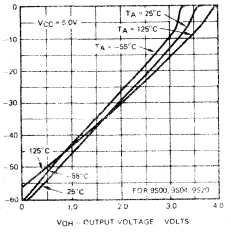
*To be announced first quarter 1972.

TYPICAL INPUT AND OUTPUT CHARACTERISTICS (Figs. 3 Thru 10)

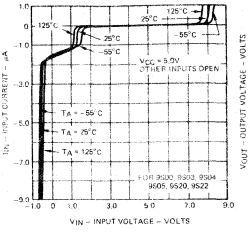
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)



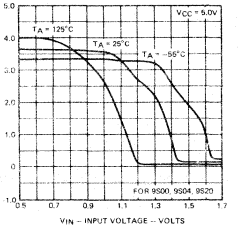
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)



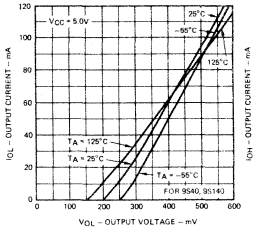
INPUT CURRENT VERSUS INPUT VOLTAGE



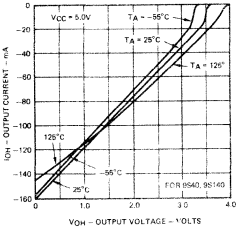
OUTPUT VOLTAGE VERSUS INPUT VOLTAGE



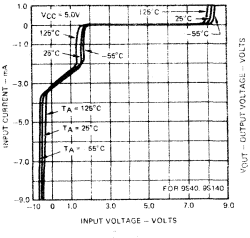
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)



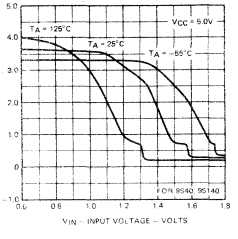
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)



INPUT CURRENT VERSUS INPUT VOLTAGE



OUTPUT VOLTAGE VERSUS INPUT VOLTAGE



TYPICAL PROPAGATION DELAY TIME CHARACTERISTICS FOR 9S GATES, BUFFER, AND INVERTER

Fig. 11 PROPAGATION DELAY TIME, LOW-TO-HIGH-LEVEL OUPUT VERSUS FREE-AIR TEMPERATURE

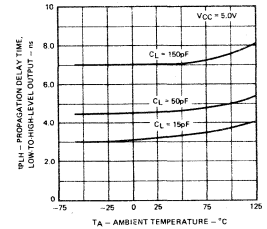


Fig. 12 PROPAGATION DELAY TIME, LOW-TO-HIGH-LEVEL OUTPUT VERSUS SUPPLY VOLTAGE

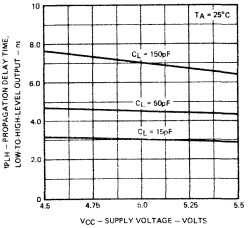


Fig. 13 PROPAGATION DELAY TIME, HIGH-TO-LOW-LEVEL OUTPUT VERSUS FREE-AIR TEMPERATURE

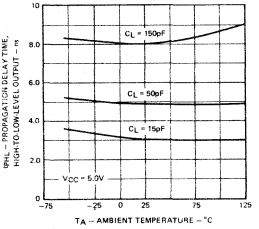


Fig. 14 PROPAGATION DELAY TIME, HIGH-TO-LOW LEVEL OUTPUT VERSUS SUPPLY VOLTAGE

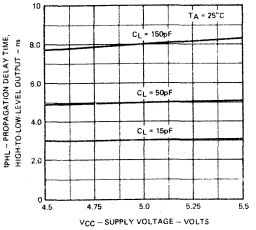
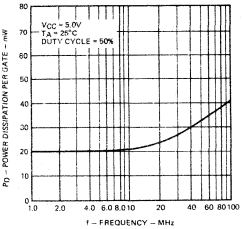


Fig. 15 POWER DISSIPATION PER GATE VERSUS FREQUENCY



SWITCHING CHARACTERISTICS

TEST CIRCUIT AND WAVEFORM FOR 9S00, 9S04, 9S20, 9S40 AND 9S140

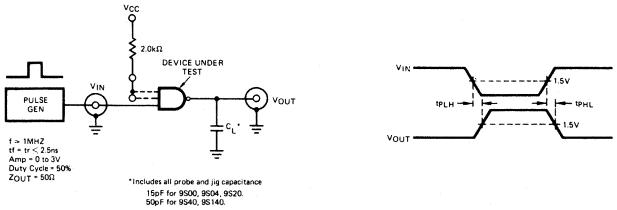


Fig. 16

TEST CIRCUIT AND WAVEFORM FOR 9S03, 9S05 AND 9S22

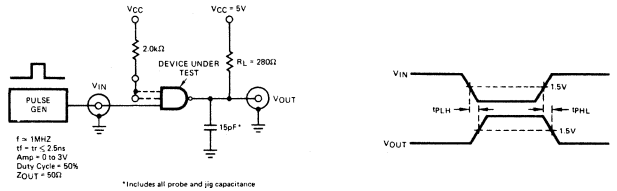


Fig. 17

TEST CIRCUIT AND WAVEFORM FOR 9S64, 9S65

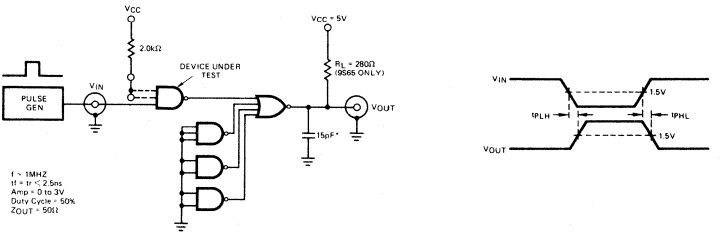
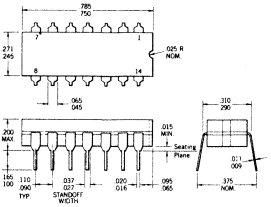


Fig. 18

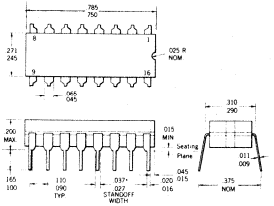
PACKAGE OUTLINES

6A – 14 LEAD DUAL IN-LINE
in accordance with JEDIC (TO-116) outline



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers.
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.0 grams

6B - 16 LEAD DUAL IN-LINE



NOTES:
All dimensions are in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Broad-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.2 grams
*The .037/.027 dimension does not apply to the corner leads.

ORDER INFORMATION

SPECIFY: U6A9SXX51X for 14-Lead Dual In-Line Package, –55°C to +125°C range
U6A9SXX59X for 14-Lead Dual In-Line Package, 0°C to +75°C range
U6B9SXX51X for 16-Lead Dual In-Line Package, –55°C to +125°C range
U6B9SXX59X for 16-Lead Dual In-Line Package, 0°C to +75°C range,
where XX are the Last Two Digits of the Product Number.

NOTES

9500 Series Temperature Compensated ECL

Numerical Index of Devices

FAIRCHILD SEMICONDUCTOR

9500 Series • High Speed Logic

easy ECL

FAIRCHILD 9500 EASY ECL FAMILY

SSI		MSI						Interface	
Gates	Flip Flops	Decoders	Multiplexers	Registers	Latches	Operators	Counters	Memory		
95L22 Dual 95L23 Triple 95L24 Quad										LOW POWER
9502 Dual 9503 Triple 9504 Quad 9505 OR/And 9507 Quad And	9528 Dual D	9538 1 of 8	9578 Quad 2 9580 Trip 2 9581 8 Input		9534 4 Bit	9578 Ex-Or/ Comparator		95410 256 Bit Ram	9582 Receiver/ Amplifier 9598 Converter	STANDARD
95H02 Dual 95H03 Triple 95H04 Quad	95H28 Dual D 95H29 J-K			95H39 Multi-port 95H00 4 Bit		95H55 5-Bit Comparator 95H42 Carry 95H41 4 Bit ALU 95H84 2 Bit Adder	95H10 Decimal 95H16 Binary 95H90 Prescaler	95400 64 Bit Ram 95401 16 Bit Ram		HIGH SPEED

FAIRCHILD 9500 EASY ECL

ECL offers both maximum speed performance and optimum logic flexibility in the design of high speed systems. Circuit features such as Wired-OR, complementary outputs and series gating permit the implementation of many digital functions with lower package count and therefore lower component cost, with similar system power dissipation, than with high speed TTL.

9500 ECL incorporates unique design features, including temperature compensation and on chip terminating resistors to eliminate many of the application problems (low noise margin and instability) associated with earlier forms of ECL. In addition the basic gate characteristics have been chosen to allow the use of more relaxed wiring rules and therefore lower cost interconnection methods than any logic family in the same speed range.

By taking advantage of Fairchild's experience in designing high speed custom circuits the 9500 user will have at his disposal one of the best planned circuit families available. The intermixing of high speed and very high speed ECL technologies, and basic gates with complex MSI functions in a single logic family allows a designer to optimise a system to his particular cost-performance goal.

The 9500 product range has been planned around the requirements of the three basic application areas for high speed circuits.

Computers – Basic Gates in 2.5 ns and 1.5 ns ranges, complex gate functions, dual D flip-flops, latches scratchpad memories, decoders, registers, adders.

Communications – Prescalers, mixers, broad band amplifiers, oscillators, multiplexers, decoders.

Instrumentation – High speed flip-flops for 100 MHz and 250 MHz applications, multiplexers, demultiplexers, line receivers.

This dynamic logic family will continue to expand as technology and applications demand. All additions to the 9500 range will be compatible with the present devices, permitting upgrading of existing designs to take advantage of economic and performance improvements as they become available.

SYSTEMS ADVANTAGES OF ECL

In addition to the maximum possible operating speeds, ECL also offers many advantages over other logic forms for the design of digital systems.

ADVANTAGES	FEATURE
• Transmission line compatible • Can be fully terminated • Minimum line reflections • Low transient noise susceptibility • High fan in/fan out possible across speed range	HIGH INPUT/LOW OUTPUT IMPEDANCE
• No additional inversion delay • Two logic decisions per gate delay • Up to 30% lower system package count	COMPLEMENTARY OUTPUTS/WIRE-OR CAPABILITY
• Low crosstalk • Simpler wiring rules for same system speed	HIGHER NOISE MARGIN RELATIVE TO LOGIC SWING. LOWER EDGE SPEED RELATIVE TO DELAY
• Low internal noise generation • Constant power dissipation across frequency range	CONSTANT SUPPLY CURRENT DRAIN
• Circuitry oriented to design of very high speed, medium power MSI functions	SERIES GATING, EMITTER AND COLLECTOR DOTTING,ETC.

9500 TEMPERATURE COMPENSATED ECL –

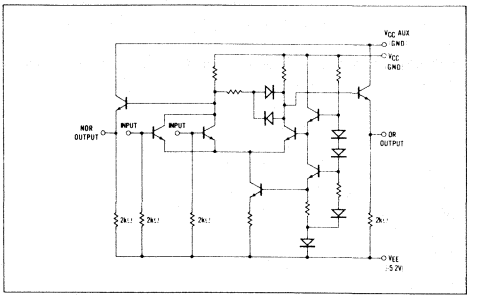
Significant applications characteristics of 9500 are:

- **Temperature Compensation**
  Logic levels remain constant across range 0°C to 75°C. Maintains maximum system noise immunity and eliminates saturation problems.
- **Packaging**
  Hermetic 16 pin Dual In-Line Package
- **Internal Pull Down Resistors**
  Point to point wiring up to 8" on single sided boards permitted by internal 2 k ohm resistors and choice of edge rates. These resistors also eliminate oscillation problems and allow unused inputs to be left open.
- **Low Crosstalk And Noise Generation**
  Insured by provision of split V_{CC} lines and location of supply pins.
- **50 Ohm Line Drive Capability**
  Output transistors designed to drive a 50 ohm terminated line and a fanout of 10 loads simultaneously.
- **Single Power Supply**
  9500 elements are specified for use with a single power supply.
- **MSI Flexibility**
  The 9500 product range has been designed to take maximum advantage of MSI performance in logic flexibility, economy and speed-power optimisation. Basic building blocks are aimed at computing, communications and instrumentation applications.
- **Cost Effectiveness**
  Low cost processing, together with above features insure simple applications rules and lowest cost hardware and components for high speed systems.

9500 ECL FAMILY CHARACTERISTICS

The 9500 circuit uses the same basic configuration as conventional ECL with the addition of temperature compensated internal reference and current source networks. These maintain the logic ZERO state insensitive to temperature variations. Logic ONE is clamped to ZERO by the collector cross-coupling diode network.

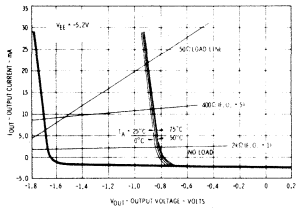
The temperature compensation networks require only minimal additional chip area for the gate functions. On MSI and complex gate elements the additional area is insignificant as compensation is only applied to the output nodes.



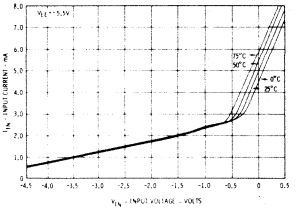
With –5.2 volt V_{EE} logic ONE is typically V_{OH} = –850 mV and logic ZERO V_{OL} = –1700 mV. These levels will interface directly with other ECL families, and with DTL and TTL using simple discrete and monolithic interface circuits. 9500 elements can also be operated from a positive supply if desired. (See Fairchild Application Brief 157).

9500 Input-Output Characteristics

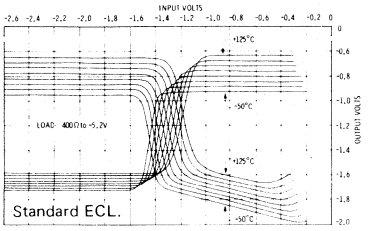
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE

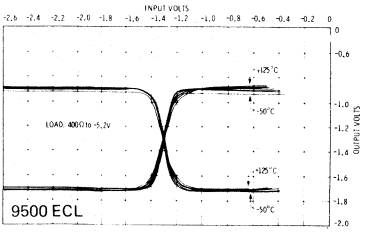


INPUT CURRENT VERSUS INPUT VOLTAGE



Conventional ECL vs. 9500 Transfer Characteristics

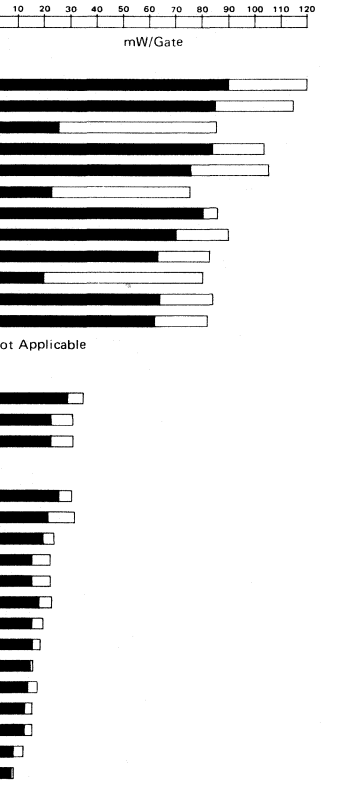




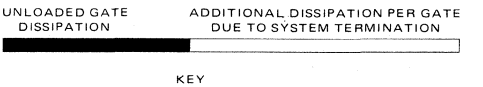
- **50 Ω Line Drive Capability**
  Output transistors designed to drive a 50 Ω terminated line and a fanout of 10 loads simultaneously.
- **Single Power Supply**
  9500 elements are specified for use with a single power supply.
- **MSI Flexibility**
  The 9500 product range has been designed to take maximum advantage of MSI devices to insure highest speed at low power.

ECL – MSI INSURES LOWEST POWER, HIGH PERFORMANCE SYSTEMS

DEVICE	DESCRIPTION	GATES/ FUNCTION (1)
SSI – GATES		
9502	General Purpose Dual OR–NOR (2.4 ns)	2
95H02	High Speed Dual OR–NOR (1.6 ns)	2
95L22	Low Power Dual OR–NOR (2 ns)	2
9503	General Purpose Triple OR–NOR	3
95H03	High Speed Triple OR–NOR	3
95L23	Low Power Triple OR–NOR (2 ns)	3
9582	Triple Line Receiver/Amplifier	3
9504	General Purpose Quad NOR	4
95H04	High Speed Quad NOR (1.6 ns)	4
95L24	Low Power Quad NOR (2 ns)	4
9505	Four Wide OR–AND	5
9507	Quad AND–NAND	5
9595	Dual ECL–TTL Converters	2
SSI – FLIP-FLOPS		
95H29	210 MHz J–K	9
9528	Dual 160 MHz D-Type	12
95H28	Dual 220 MHz D-Type	12
MSI – ELEMENTS		
9538	1 of 8 Decoder	12
9581	8 Input Multiplexer	12
9580	Triple 2 Input Multiplexer	13
9578	Quad EX/OR Comparator	16
9579	Quad 2 Input Multiplexer	16
95H42	Carry Look Ahead Unit	18
9534	Quad Latch	24
95H84	Adder/Subtractor	29
95H90	250 MHz Prescaler	29
95H00	4 Bit Shift Register	38
95H10	Decimal Counter	40
95H16	Binary Counter	40
95H41	4 Bit A.L.U.	75
95H39	8 Bit Multiport Register	76



Note (1). On-chip ECL gates, not discrete TTL equivalents.



The chart above compares the unloaded and system loaded power dissipations of 9500 ECL functions. The increase in power is due to dissipation in the output stage and either 2 kΩ on-chip or 50 Ω external termination resistors. Note that 20 mW SSI gates increase to 80 mW in a 50 Ω shunt termination system.

In an MSI function the additional power is only incurred at the output gate and is amortized over many internal gates. Thus in a system built largely with MSI, the system power per gate remains close to the unloaded power. Lowest power systems are therefore achieved with maximum use of MSI.

PRODUCT SUMMARY

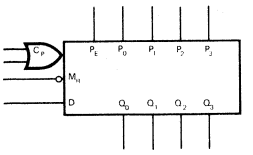
easy ECL

95H00 FOUR BIT UNIVERSAL SHIFT REGISTER

DESCRIPTION The 95H00 is a four bit Parallel/Serial In, Parallel/Serial Out Universal shift register. High speed ECL technology permits storage, shifting, counting and serial code conversion in excess of 150 MHz.

Features include assertion outputs on each state, overriding asynchronous master reset, serial and parallel D type inputs and a gated clock. Availability of all these features on one chip significantly improves the reliability, performance, and power consumption of high speed systems.

- **HIGH SPEED . . . 150 MHz SHIFT FREQUENCY**
- **D TYPE INPUT IN SERIAL AND PARALLEL**
- **GATED CLOCK INPUT**
- **ASYNCHRONOUS MASTER RESET**
- **50 Ω DRIVE ON Q3 OUTPUT**
- **WIRED OR CAPABILITY**
- **SEPARATE CURRENT SWITCH EMITTER FOLLOWER V_{CC} PINS – ELIMINATE NOISE COUPLING**
- **TEMPERATURE COMPENSATION**
- **INTERNAL PULL DOWN**
- **SINGLE –5.2 VOLT POWER SUPPLY**
- **HERMETIC CERAMIC 16 PIN DIP**
- **COMPLEX MULTI-GATE CHIP REDUCES PACKAGE COUNT & POWER**



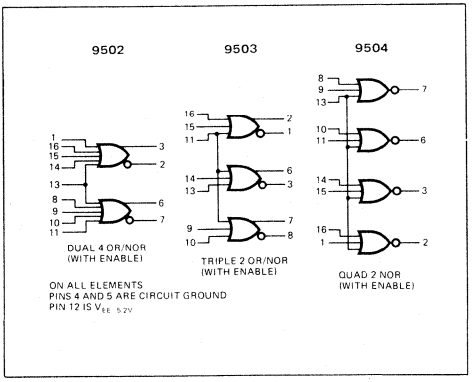
P_N = PARALLEL IN
P_E = PARALLEL ENABLE
Q_N = PARALLEL OUT, 10 LOADS
Q_3 = SERIAL 0 t, 50 Ω + 10 LOADS
C_P = CLOCK IN, SHIFTS ON POS. EDGE
M_R = ASYNCHRONOUS MASTER RESET
D = DATA INPUT, SERIAL

9502·9503·9504 BASIC GATES

DESCRIPTION The 9502, 9503 and 9504 are temperature compensated OR/NOR Gates employing a nonsaturating current switch, emitter follower configuration to achieve high speed. The elements are intended for the design of high speed central processors, terminals, instrumentation and digital communications systems.

Input and output 2K Ω pulldown resistors eliminate the necessity for external termination of lines up to 6-8 inches and unused logic inputs. Package pin locations are chosen to reduce internal noise generation and crosstalk.

- **HIGH SPEED . . . 2.3 ns PER GATE**
- **SEPARATE V_{CC} PINS – ELIMINATE NOISE COUPLING**
- **TEMPERATURE COMPENSATION**
- **INTERNAL PULLDOWN RESISTORS**
- **COMMON ENABLE INPUTS**
- **LOW CROSSTALK AND NOISE GENERATION**
- **WIRE-OR CAPABILITY**
- **50 Ω LINE DRIVING CAPABILITY**
- **COMPLEMENTARY OR/NOR OUTPUTS (9502, 9503)**
- **SINGLE –5.2V POWER SUPPLY**
- **HERMETIC CERAMIC 16 PIN DUAL IN-LINE PACKAGE**

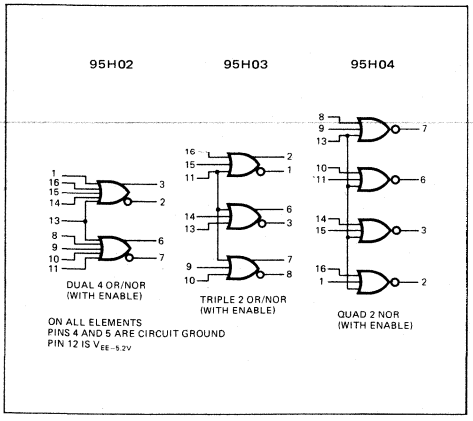


95H02·95H03·95H04 CLOCK DRIVER/ HIGH SPEED GATES

DESCRIPTION The 95H02, H03 and H04 are temperature compensated OR/NOR Gates employing a nonsaturating current switch, emitter follower configuration to achieve a very high speed. The elements are intended for use where higher logic speeds and faster edges than standard 9500 gates are required, as in clock and flip-flop driving.

These gates will improve available speed performance of 9528 flip-flops and 9534 latches in counting and register application.

- **HIGH SPEED . . . 1.6 ns PER GATE**
- **SEPARATE CURRENT SWITCH AND EMITTER FOLLOWER V_{CC} PINS – ELIMINATES NOISE COUPLING**
- **TEMPERATURE COMPENSATION**
- **INTERNAL PULLDOWN RESISTORS**
- **COMMON ENABLE INPUTS**
- **LOW CROSSTALK AND NOISE GENERATION**
- **WIRE-OR CAPABILITY**
- **50 Ω LINE DRIVING CAPABILITY**
- **COMPLEMENTARY OR/NOR OUTPUTS (95H02, H03)**
- **SINGLE –5.2V POWER SUPPLY**
- **HERMETIC CERAMIC 16 PIN DUAL IN-LINE PACKAGE**



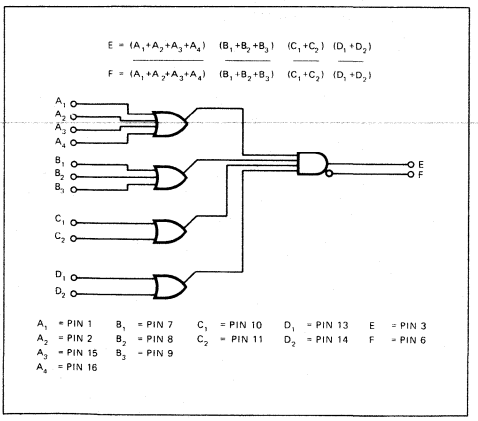
9505 4 WIDE OR-AND GATE

DESCRIPTION The 9505 is a temperature compensated OR-AND gate that achieves in slightly over one basic gate delay the AND of four different OR'ed functions.

The NOR outputs of the four OR gates are OR'ed to derive the OR-NOR function.

This element is useful in the design of Arithmetic Logic Units for construction of adders, subtracters, multipliers etc. Just two 9505's will implement a full carry adder function.

- **HIGH SPEED . . . 2.7 ns OR-AND, 2.5 ns NOR-OR**
- **SEPARATE CURRENT SWITCH & EMITTER FOLLOWER V_{CC} PINS – ELIMINATES NOISE COUPLING**
- **TEMPERATURE COMPENSATED**
- **INTERNAL 2K PULL DOWN RESISTORS**
- **COMPLEX LOGIC FUNCTION REDUCES PACKAGE COUNT**
- **WIRE OR CAPABILITY**
- **50 Ω LINE DRIVING CAPABILITY**
- **SINGLE –5.2V POWER SUPPLY**
- **HERMETIC CERAMIC 16 PIN DUAL IN-LINE PACKAGE**

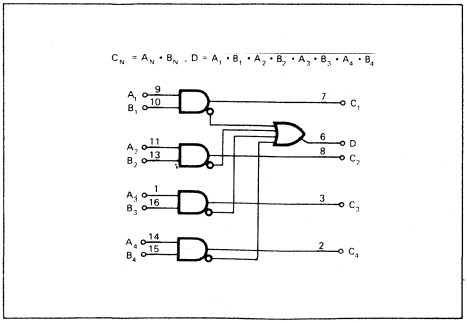


9507
QUAD AND/NAND

DESCRIPTION The 9507 is a Temperature Compensated Quad ECμL AND gate using series gating and collector and emitter dotting to achieve the logical functions within approximately one gate delay.

The uses are for any logical AND or 8 input NAND function with higher speed than similar logic implemented with standard gates. This element is designed to increase speed and reduce package count in high performance processors and controllers.

- HIGH SPEED . . . 2.6 ns PER GATE
- 8 INPUT LOGIC NAND IN ONE GATE DELAY
- SEPARATE NON-STANDARD ECL LOGIC FUNCTIONS —4 DUAL AND GATES
- HIGHER SYSTEM RELIABILITY AND LOWER COST BY ELIMINATING COMPLEX WIRING OF OR/NOR GATES
- SEPARATE CURRENT SWITCH & EMITTER FOLLOWER V_{CC} PINS
- TEMPERATURE COMPENSATION
- INTERNAL PULLDOWN RESISTORS
- LOW CROSSTALK AND NOISE GENERATION
- WIRE OR CAPABILITY
- 50 Ω LINE DRIVING CAPABILITY
- SINGLE —5.2V POWER SUPPLY
- HERMETIC CERAMIC 16 PIN DIP

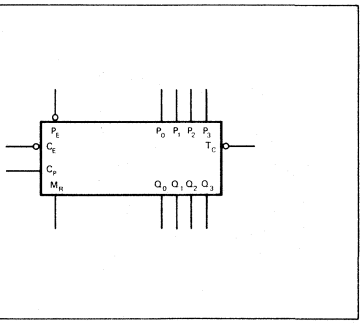


95H10 MSI BCD
DECADE COUNTER

DESCRIPTION The 95H10 is a high speed synchronously presettable 8421 BCD decade counter. It is a synchronously presettable, multifunction MSI building block useful for a large number of counting, digital integration, and conversion applications. Up to 9 decades can be cascaded with no speed degradation using the standard 9500 gates. With 95H00 gates a multidecade synchronous load counter to over 150 MHz can be built. Typical counter frequency is over 180 MHz or easy frequency increase to over 250 MHz with the 95H29 JK Flip Flop.

Features include assertion inputs and outputs on each of the 4 master slave counting flip flop. Terminal count is generated internally in a manner that allows synchronous loading at nearly the speed of the basic counter. When the parallel load feature is not needed, the CE input may be used as a clock gate regardless of clock input level. Availability of all these features on one chip significantly improves the reliability, performance and power consumption of high speed systems.

- HIGH SPEED COUNT . . . 180 MHz TYPICAL COUNT FREQUENCY
- HIGH SPEED SYNCHRONOUSLY LOAD . . . OVER 150 MHz SYNCHRONOUS LOAD FREQUENCY
- INTERNAL COUNT ENABLE
- EXPANDABLE TO OVER 250 MHz WITH THE 95H29
- ASYNCHRONOUS MASTER RESET
- 50 Ω OR FANOUT OF 10 ON EACH OUTPUT
- WIRE OR CAPABILITY
- SEPARATE CURRENT SWITCH EMITTER FOLLOWER V_{CC} PINS — ELIMINATE NOISE COUPLING
- TEMPERATURE COMPENSATION
- INTERNAL PULLDOWN FOR DIRECT LOW COST WIRING
- SINGLE —5.2 VOLT POWER SUPPLY
- HERMETIC CERAMIC 16 PIN DIP
- COMPLEX MULTI-GATE CHIP REDUCES PACKAGE COUNT AND POWER

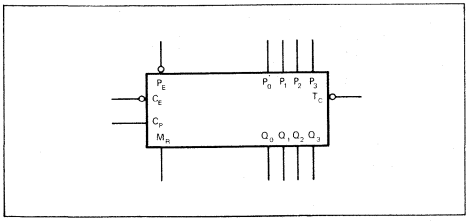


95H16 MSI 4-BIT BINARY COUNTER

DESCRIPTION The 95H16 is a high speed synchronously presettable 4-Bit Binary counter. It is a synchronously presettable, multifunction MSI building block useful for a large number of counting, digital, integration, and conversion applications. Up to 9 devices can be cascaded with no speed degradation using the standard 9500 gates. With 95H00 gates a multidecade synchronous load counter to over 150 MHz can be built. Typical count frequency is over 180 MHz or easy frequency increase to over 250 MHz with the 95H29 JK Flip Flop.

Features include assertion inputs and outputs on each of the 4 master slave counting flip flop. Terminal count is generated internally in a manner that allows synchronous loading at nearly the speed of the basic counter. When the parallel load feature is not needed, the CE input may be used as a clock gate regardless of clock input level. Availability of all these features on one chip significantly improves the reliability, performance and power consumption of high speed systems.

- HIGH SPEED COUNT . . . 180 MHz TYPICAL COUNT FREQUENCY
- HIGH SPEED SYNCHRONOUSLY LOAD . . . OVER 150 MHz SYNCHRONOUS LOAD FREQUENCY
- INTERNAL COUNT ENABLE
- EXPANDABLE TO OVER 250 MHz WITH THE 95H29
- ASYNCHRONOUS MASTER RESET
- 50 Ω OR FANOUT OF 10 ON EACH OUTPUT
- WIRE OR CAPABILITY
- SEPARATE CURRENT SWITCH EMITTER FOLLOWER V_{CC} PINS – ELIMINATE NOISE COUPLING
- TEMPERATURE COMPENSATION
- INTERNAL PULLDOWN FOR DIRECT LOW COST WIRING
- SINGLE –5.2 VOLT POWER SUPPLY
- HERMETIC CERAMIC 16 PIN DIP
- COMPLEX MULTI-GATE CHIP REDUCES PACKAGE COUNT AND POWER

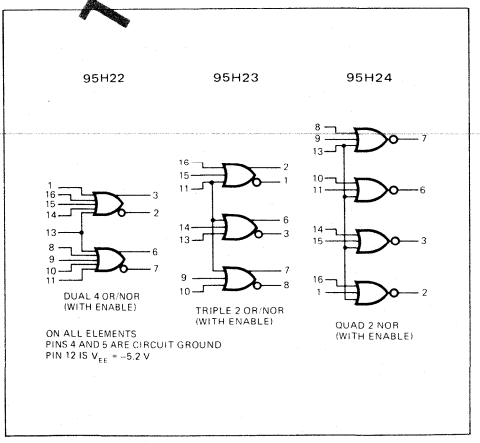


95H22·95H23·95H24 CLOCK DRIVER/ HIGH SPEED GATES

DESCRIPTION The 95H22, H23 and H24 are temperature compensated OR/NOR Gates employing a nonsaturating current switch, emitter follower configuration to achieve a very high speed. The elements are intended for use where higher logic speeds and faster edges than standard 9500 gates are required, as in clock and flip-flop driving.

These gates will improve available speed performance of 9528 flip-flops and 9534 latches in counting and register application.

- HIGH SPEED . . . 1.6 ns PER GATE
- SEPARATE CURRENT SWITCH EMITTER FOLLOWER V_{CC} PINS – ELIMINATES NOISE COUPLING
- TEMPERATURE COMPENSATION
- INTERNAL 50 KΩ RESISTORS FOR GREATER FANOUT
- COMMON ENABLE INPUT
- LOW CROSSTALK AND NOISE GENERATION
- WIRE-OR CAPABILITY
- 50 Ω LINE DRIVING CAPABILITY
- COMPLEMENTARY OR/NOR OUTPUTS (95H22, H23)
- SINGLE –5.2V POWER SUPPLY
- HERMETIC CERAMIC 16 PIN DUAL IN-LINE PACKAGE

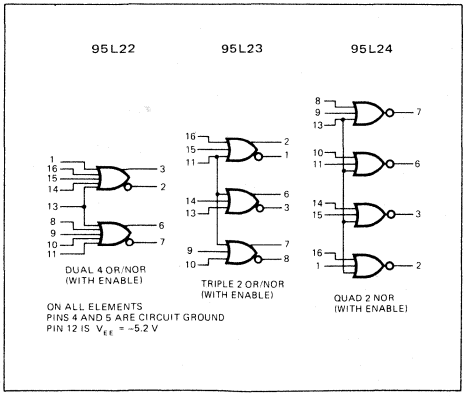


95L22·95L23·95L24
LOW POWER GATES

DESCRIPTION The 95L22, L23, and L24 are temperature compensated ECμL OR/NOR Gates employing a non-saturating current switch, emitter follower configuration to achieve high speed. These elements are intended for use where power is to be minimized. External pull-down resistors are needed for all outputs. For longer lines series termination may be used to further reduce system power.

These gates will improve available power performance of ECL systems where speed degrading due to fanout and loading can be tolerated.

- LOW POWER . . . 20 MW PER GATE
- HIGH SPEED . . . 2.0 ns INTO 50 OHMS
- TEMPERATURE COMPENSATION
- INTERNAL 50 K Ω RESISTORS ON INPUTS
- COMMON ENABLE INPUTS
- 50 Ω LINE DRIVE CAPABILITY
- WIRE-OR CAPABILITY
- PIN COMPATIBLE WITH OTHER 9500 GATES
- SINGLE –5.2 VOLT POWER SUPPLY
- HERMETIC CERAMIC 16 PIN DUAL IN-LINE PACKAGE



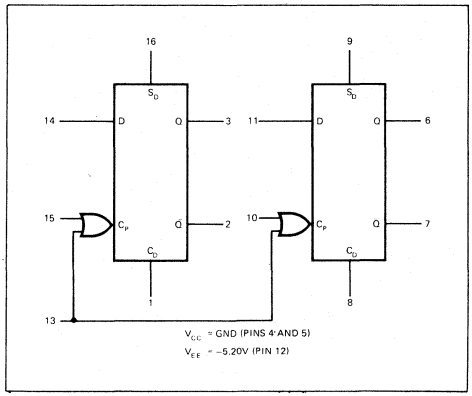
95H26
VERY HIGH SPEED DUAL D FLIP-FLOP

DESCRIPTION The 95H26 is a high speed, temperature compensated ECμL dual D (data) flip-flop compatible with all other members of the 9500 series of ECμL circuits. The device is versatile and permits easy implementation of high speed counters, registers, and control circuits.

FUNCTIONAL DESCRIPTION Each D Flip-Flop consists of both a master and a slave. While the clock is LOW the slave is held steady, but the information on the D input is permitted to enter the master. The next clock transition from LOW to HIGH locks the master in its present state making it insensitive to the D input and connects the slave to the master causing the new information to be reflected on the outputs. Logic races are avoided by offsetting the master and slave thresholds to avoid simultaneous switching when low speed edges are encountered in the system.

The internal clock is the OR of two clock inputs, one common to both flip-flops. The ORed clock permits the use of one input as a clock pulse input and the other as an active low enable.

- 260 MHz OPERATION
- SEPARATE CURRENT SWITCH AND EMITTER FOLLOWER V_{CC} PINS – ELIMINATES NOISE COUPLING
- TEMPERATURE COMPENSATION
- INTERNAL 50 K Ω RESISTORS FOR GREATER FANOUT
- MASTER-SLAVE CONFIGURATION
- SEPARATE DIRECT SET AND CLEAR INPUTS
- BOTH COMMON AND SEPARATE CLOCK INPUTS
- WIRED-OR CAPABILITY ON OUTPUTS
- 50 Ω LINE DRIVE CAPABILITY
- SINGLE –5.2 VOLT POWER SUPPLY
- HERMETIC CERAMIC 16 PIN DUAL IN-LINE PACKAGE



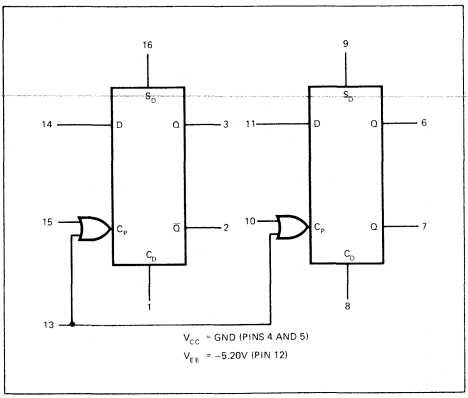
9528 HIGH SPEED DUAL D FLIP-FLOP

DESCRIPTION The 9528 is a high speed, temperature compensated ECμL dual D (data) flip-flop compatible with all other members of the 9500 series of ECμL circuits. The device is versatile and permits easy implementation of high speed counters, registers, and control circuits.

FUNCTIONAL DESCRIPTION Each D Flip-Flop consists of both a master and a slave. While the clock is LOW the slave is held steady, but the information on the D input is permitted to enter the master. The next clock transition from LOW to HIGH locks the master in its present state making it insensitive to the D input and connects the slave to the master causing the new information to be reflected on the outputs. Logic races are avoided by offsetting the master and slave thresholds to avoid simultaneous switching when low speed edges are encountered in the system.

The internal clock is the OR of two clock inputs, one common to both flip-flops. The ORed clock permits the use of one input as a clock pulse input and the other as an active low enable.

- 160 MHz OPERATION
- SEPARATE CURRENT SWITCH AND EMITTER FOLLOWER V_{CC} PINS – ELIMINATES NOISE COUPLING
- TEMPERATURE COMPENSATION
- INTERNAL PULLDOWN RESISTORS
- MASTER-SLAVE CIRCUIT
- SEPARATE DIRECT SET AND CLEAR INPUTS
- BOTH COMMON AND SEPARATE CLOCK INPUTS
- WIRED-OR CAPABILITY ON OUTPUTS
- 50 Ω LINE DRIVING CAPABILITY
- SINGLE –5.2 VOLT POWER SUPPLY
- HERMETIC CERAMIC 16 PIN DUAL IN-LINE PACKAGE



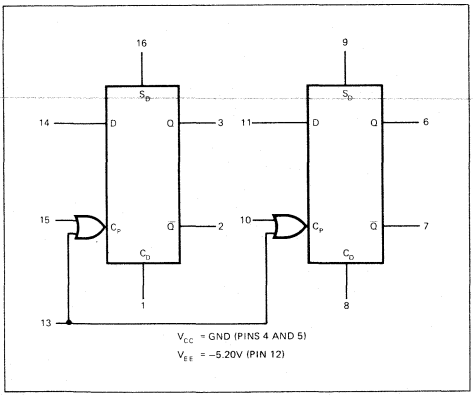
95H28 VERY HIGH SPEED DUAL D FLIP-FLOP

DESCRIPTION The 95H28 is a high speed, temperature compensated ECμL dual D (data) flip-flop compatible with all other members of the 9500 series of ECμL circuits. The device is versatile and permits easy implementation of high speed counters, registers, and control circuits.

FUNCTIONAL DESCRIPTION Each D Flip-Flop consists of both a master and a slave. While the clock is LOW the slave is held steady, but the information on the D input is permitted to enter the master. The next clock transition from LOW to HIGH locks the master in its present state making it insensitive to the D input and connects the slave to the master causing the new information to be reflected on the outputs. Logic races are avoided by offsetting the master and slave thresholds to avoid simultaneous switching when low speed edges are encountered in the system.

The internal clock is the OR of two clock inputs, one common to both flip-flops. The ORed clock permits the use of one input as a clock pulse input and the other as an active low enable.

- 260 MHz OPERATION
- SEPARATE CURRENT SWITCH AND EMITTER FOLLOWER V_{CC} PINS – ELIMINATES NOISE COUPLING
- TEMPERATURE COMPENSATION
- INTERNAL PULLDOWN RESISTORS
- MASTER-SLAVE CIRCUIT
- SEPARATE DIRECT SET AND CLEAR INPUTS
- BOTH COMMON AND SEPARATE CLOCK INPUTS
- WIRED-OR CAPABILITY ON OUTPUTS
- 50 Ω L'NE DRIVING CAPABILITY
- SINGLE –5.2 VOLT POWER SUPPLY
- HERMETIC CERAMIC 16 PIN DUAL IN-LINE PACKAGE

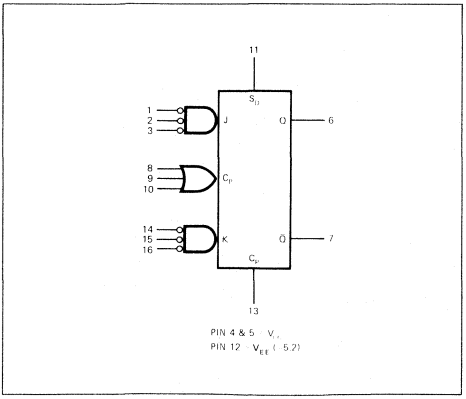


95H29 VERY HIGH SPEED J-K FLIP-FLOP

DESCRIPTION The 95H29 is a Hi-Speed edge-triggered $\overline{J}$ $\overline{K}$ Master-Slave flip-flop with both direct set and clear inputs. The $\overline{J}$, $\overline{K}$ and Clock functions are the active low AND of three inputs. With these inputs this device may be used effectively in counters, registers and other applications where data must be stored or shifted at a high rate.

In addition the full frequency range may be used effectively as a prescaler and controlled divider for frequencies up to 250 MHz.

- 250 MHz OPERATION
- ASYNCHRONOUS DIRECT SET AND CLEAR
- MASTER-SLAVE CIRCUIT
- NON-ONES CATCHING
- SEPARATE CURRENT SWITCH & EMITTER FOLLOWER V_{CC} PINS
- $\overline{J}$ AND $\overline{K}$ INPUTS
- INTERNAL PULLDOWN RESISTORS
- WIRED-OR CAPABILITY ON OUTPUTS
- 50 Ω LINE DRIVING CAPABILITY
- TEMPERATURE COMPENSATION
- SINGLE −5.2 VOLT POWER SUPPLY
- HERMETIC CERAMIC 16 PIN DIP

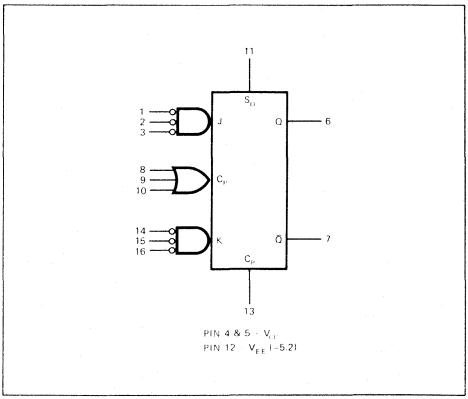


95H30 VERY HIGH SPEED J-K FLIP-FLOP

DESCRIPTION The 95H30 is a Hi-Speed edge-triggered $\overline{J}$ $\overline{K}$ Master-Slave flip-flop with both direct set and clear inputs. The $\overline{J}$, $\overline{K}$ and Clock functions are the active low AND of three inputs. With these inputs this device may be used effectively in counters, registers and other applications where data must be stored or shifted at a high rate.

In addition the full frequency range may be used effectively as a prescaler and controlled divider for frequencies up to 250 MHz.

- 250 MHz OPERATION
- ASYNCHRONOUS DIRECT SET AND CLEAR
- MASTER-SLAVE CIRCUIT
- NON-ONES CATCHING
- SEPARATE CURRENT SWITCH & EMITTER FOLLOWER V_{CC} PINS
- $\overline{J}$ AND $\overline{K}$ INPUTS
- INTERNAL 50K Ω INPUT RESISTORS FOR GREATER FANOUT
- WIRED-OR CAPABILITY ON OUTPUTS
- 50 Ω LINE DRIVING CAPABILITY
- TEMPERATURE COMPENSATION
- SINGLE −5.2 VOLT POWER SUPPLY
- HERMETIC CERAMIC 16 PIN DIP

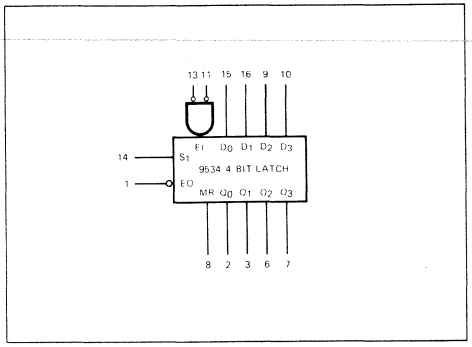


9534 QUAD LATCH WITH INPUT AND OUTPUT ENABLES

DESCRIPTION The 9534 quad D latch will store four bits of information simultaneously. Two Input enable inputs and a common output enable allow maximum logic flexibility. A common Select input selects 'D' type or 'Set' type of operation. A common reset clears the device so that the 1's catching feature may be used when desired.

This element is designed as a storage buffer for high speed registers in arithmetic logic units and parallel-serial conversion in communication systems.

- HIGH SPEED . . . 4.3 ns TYPICAL DATA DELAYS 'S
- COMMON LATCH ENABLE
- COMMON MASTER RESET
- COMMON SELECT FOR 'D' OR 'SET'
- COMPLEX MULTIGATE CHIP REDUCES PACKAGE COUNT
- EASILY EXPANDED TO LARGE HIGH SPEED MEMORY
- WIRED-OR CAPABILITY
- SEPARATE CURRENT SWITCH AND EMITTER FOLLOWER V_{CC} PINS – ELIMINATES NOISE COUPLING
- TEMPERATURE COMPENSATION
- INTERNAL PULLDOWN
- 50 Ω LINE DRIVE CAPABILITY
- SINGLE –5.2 VOLT POWER SUPPLY
- HERMETIC CERAMIC 16 PIN DIP



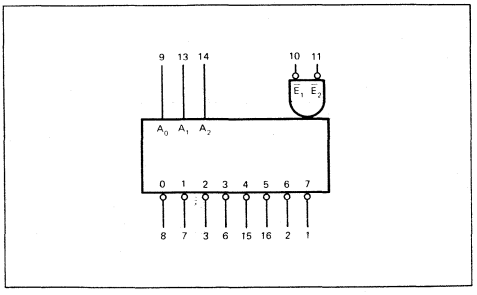
9538 OCTAL DECODE 3 LINE/8 LINE

DESCRIPTION The 9538 decoder accepts three binary address inputs and under control of the enables activate one of the eight active low outputs. Both enables must be low for any output to go low.

The ECL 9538 may be used as a demultiplexer by connecting a data source to one of the enable inputs. The other enable input will function as a data enable line while inputs A_0, A_1, and A_2 select the desired data output line (0 through 7).

The 9538 is particularly useful in memory expansion and register or peripheral selection applications.

- HIGH SPEED . . . 4 ns FROM ADDRESS TO OUTPUT
- USEABLE FOR DEMULTIPLEXING – 2 ENABLE INPUTS
- OUTPUTS ACTIVE LOW FOR ENABLING WITH OTHER MEMBERS OF THE 9500 FAMILY
- NO INVERSION FROM ENABLE TO SELECTED OUTPUT
- WIRED-OR CAPABILITY
- SEPARATE CURRENT SWITCH EMITTER FOLLOWER V_{CC} PINS – ELIMINATE NOISE COUPLING
- TEMPERATURE COMPENSATION
- INTERNAL PULL DOWN
- 50 Ω LINE DRIVE CAPABILITY
- SINGLE –5.2 VOLT POWER SUPPLY
- HERMETIC CERAMIC 16 PIN DIP
- COMPLEX MULTI-CATE CHIP REDUCES PACKAGE COUNT & POWER

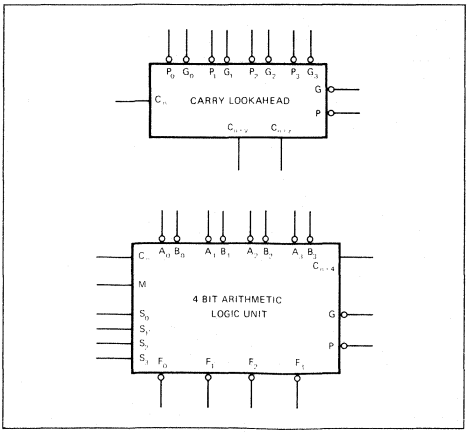


95H41 MSI 4 BIT ALU
95H42 MSI CARRY LOOKAHEAD UNIT

DESCRIPTION The 95H41 is a 4 Bit High Speed Arithmetic Logic Unit (ALU) which can perform all the possible 16 logic operations on two variables and a variety of arithmetic operations; the Add and Subtract modes being the most important. This ALU is ideally suited for mini-computers, data processors, peripheral systems, and instrument systems. The functions found in the successful TTL 9341/54181 have been used to define this ECL/MSI. Although not as fast as the 95H84 2 Bit Adder/Subtractor the multiple functions permit reduced package count for the multiple function applications.

Features include: All 16 operations of two variables – Exclusive OR, Comparator, AND, NAND, OR, NOR, plus ten other logic operations. The experience gained from use of the TTL equivalent can be directly applied to this high speed ECL MSI. The 95H42 is the Carry Lookahead Generator.

- **HIGH SPEED . . . TYPICAL 4 BIT ADD OF 5 ns**
- **COMPLEX MULTIFUNCTION CHIP REDUCES PACKAGE AND POWER REQUIREMENTS**
- **50 Ω OR FANOUT OF 10 ON EACH OUTPUT**
- **WIRE-OR CAPABILITY**
- **SEPARATE CURRENT SWITCH, EMITTER FOLLOWER V_{CC} PINS – ELIMINATE NOISE COUPLING**
- **TEMPERATURE COMPENSATION**
- **INTERNAL PULLDOWN FOR DIRECT LOW COST WIRING**
- **SINGLE –5.2 VOLT SUPPLY**
- **HERMETIC CERAMIC 24 PIN DIP**

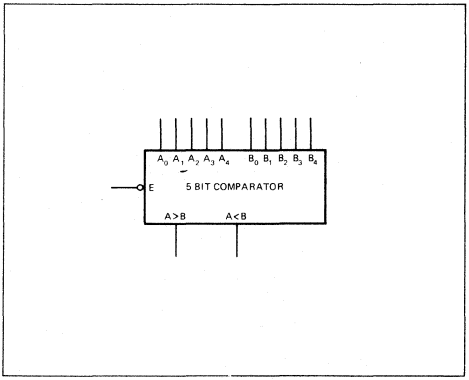


95H55 MSI 5 BIT COMPARATOR WITH ENABLE

DESCRIPTION The 95H55 is a high speed expandable 5 Bit Comparator which provides comparisons between two 5 bit words and gives two outputs, "Less Than" and "Greater Than". "Equal To" can be obtained by ORing the "Less Than" and "Greater Than" outputs. A high level on the Enable function forces both outputs low.

Features include easy expansion to larger word comparisons and very high speed operation. Experience gained in use of the TTL 9324 can be directly applied to the 95H55.

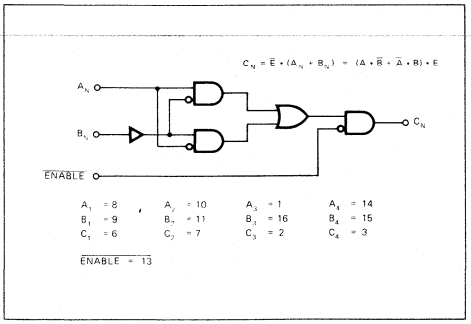
- **HIGH SPEED . . . 1.0 ns INTERNAL GATE DELAYS**
- **"GREATER THAN" AND "LESS THAN" IN ONE DEVICE**
- **OUTPUT ENABLE INPUT IS ACTIVE LOW FOR EASE OF USE WITH OTHER MEMBERS OF THE 9500 FAMILY**
- **WIRE-OR CAPABILITY**
- **50 Ω OR FANOUT OF 10 ON EACH OUTPUT**
- **SEPARATE CURRENT SWITCH EMITTER FOLLOWER V_{CC} PINS – ELIMINATE NOISE COUPLING**
- **TEMPERATURE COMPENSATED**
- **INTERNAL PULLDOWN RESISTORS FOR DIRECT LOW COST WIRING**
- **SINGLE –5.2 VOLT POWER SUPPLY**
- **HERMETIC CERAMIC 16 PIN DIP**



9578 QUAD EXCLUSIVE - OR WITH ENABLE, 4 BIT COMPARATOR

DESCRIPTION The 9578 provides four exclusive OR gates in one package using internal gating to achieve the logic function within approximately one gate delay. An additional enable gate is included so that all outputs may be held low if desired. With four of these devices a 16 bit compare function may be built with one gate delay. This element is useful in many applications such as data comparison, parity generation and checking, frequency mixing, decision and code conversion, etc.

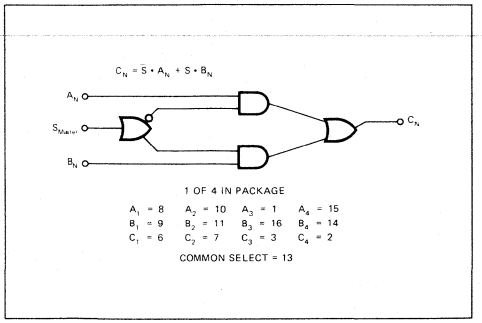
- HIGH SPEED . . . 3.0 ns FOR EX-OR
- COMMON ENABLE
- WIRED OR CAPABILITY
- SEPARATE CURRENT SWITCH EMITTER FOLLOWER V_{CC} PINS – ELIMINATE NOISE COUPLING
- TEMPERATURE COMPENSATION
- INTERNAL PULLDOWN
- 50 Ω LINE DRIVE CAPABILITY
- SINGLE –5.2 VOLT POWER SUPPLY
- HERMETIC CERAMIC 16 PIN DIP
- COMPLEX MULTI-GATE CHIP REDUCES PACKAGE COUNT & POWER



9579 QUAD 2 INPUT MULTIPLEXER WITH COMMON SELECT

DESCRIPTION The 9579 is a Temperature Compensated logic equivalent of a 4 pole – 2 position switch. It will select logically one of two groups of 4 data sources with a common select line. This high speed switch operates within about one 9500 gate delay and provides a significant increase in reliability and power savings by delivering this function in one 16 pin package.

- HI-SPEED . . . 3.0 ns FROM SELECT TO OUTPUT
- COMMON SELECT
- WIRED OR CAPABILITY
- SEPARATE CURRENT SWITCH EMITTER FOLLOWER V_{CC} PINS – ELIMINATE NOISE COUPLING
- TEMPERATURE COMPENSATION
- INTERNAL PULL DOWN .
- 50 Ω LINE DRIVE CAPABILITY
- SINGLE –5.2 VOLT POWER SUPPLY
- HERMETIC CERAMIC 16 PIN DIP
- COMPLEX MULTI-GATE CHIP REDUCES PACKAGE COUNT & POWER



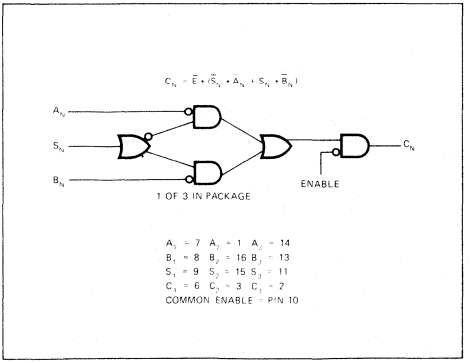
9580 TRIPLE 2 INPUT MULTIPLEXER WITH COMMON ENABLE

DESCRIPTION The 9580 multiplexer is the logic equivalent of 3 single pole, two position switches.

By the use of the separate select lines the 9580 may be interconnected as a 4 input multiplexer.

The output Enable function allows ease of expansion into more complex elements by use of the wired OR feature. For example with the additional use of a standard gate two 9580's will expand into a triple 4 input multiplexer, useful in register and peripheral applications.

- HIGH SPEED . . . 3.0 ns FROM SELECT TO OUTPUT
- SEPARATE SELECTS
- COMMON ENABLE
- INTERCONNECTS TO 4 INPUT MULTIPLEXER
- WIRED OR CAPABILITY
- SEPARATE CURRENT SWITCH EMITTER FOLLOWER V_{CC} PINS – ELIMINATE NOISE COUPLING
- TEMPERATURE COMPENSATION
- INTERNAL PULL DOWN
- 50 Ω LINE DRIVER CAPABILITY
- SINGLE –5.2 VOLT POWER SUPPLY
- HERMETIC CERAMIC 16 PIN DIP
- COMPLEX MULTI-GATE CHIP REDUCES PACKAGE COUNT & POWER



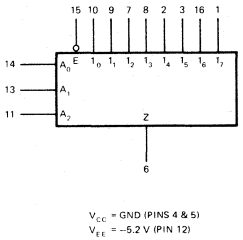
9581 1 OF 8 MULTIPLEXER

DESCRIPTION The 9581 eight input multiplexer is fundamentally a high speed semiconductor implementation of a single-pole eight-position switch. Three address lines select one out of the eight data inputs and feed this input to the output (Z). An active low enable forces the output LOW if held HIGH.

The 9581 provides the ability to select from or sequence eight data sources. It may therefore be used as a parallel to serial converter by sequentially advancing through the input address combinations.

The device may also be used as a universal logic element capable of generating any function of four variables by proper manipulation of the inputs. The wire-ORable outputs and the input enable permit easy expansion of several 9581's to form multiplexers with more than eight inputs.

- HIGH SPEED . . . 3.2 ns DATA
- ACTIVE LOW ENABLE – INTERFACES WITH OTHER MEMBERS OF THE LINE
- PARALLEL TO SERIAL CONVERTER
- WIRED OR CAPABILITY
- SEPARATE CURRENT SWITCH EMITTER FOLLOWER V_{CC} PINS – ELIMINATE NOISE COUPLING
- TEMPERATURE COMPENSATION
- INTERNAL PULL DOWN
- 50 Ω LINE DRIVE CAPABILITY
- SINGLE –5.2 VOLT POWER SUPPLY
- HERMETIC CERAMIC 16 PIN DIP
- COMPLEX MULTI-GATE CHIP REDUCES PACKAGE COUNT & POWER

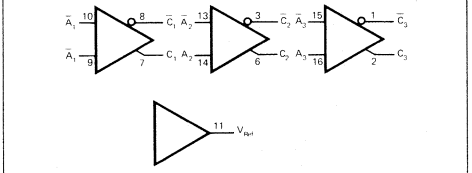


V_{CC} = GND (PINS 4 & 5)
V_{EE} = –5.2 V (PIN 12)

9582 MULTI-FUNCTION LINE RECEIVER/ AMPLIFIER

DESCRIPTION The 9582 is 3 differential input amplifiers. Both the true and complement outputs are temperature compensated to be compatible with other ECL 9500 products. With appropriate connection of the base pins the device will function as a differential line receiver; Schmitt trigger; high speed comparator; broad band video, IF. or R.F. amplifier; or oscillator. V_{ref} is made available to allow use of this device as a high input impedance buffer gate.

- DIFFERENTIAL INPUT
- TRUE AND COMPLEMENT OUTPUT
- HIGH INPUT IMPEDANCE
- HIGH SPEED . . . 3.0 ns
- OUTPUTS PRE-LOADED WITH 2K
- WIRED OR CAPABILITY
- SEPARATE CURRENT SWITCH EMITTER FOLLOWER V_{CC} PINS – ELIMINATE NOISE COUPLING
- TEMPERATURE COMPENSATION
- 50 Ω LINE DRIVER CAPABILITY
- SINGLE –5.2 VOLT POWER SUPPLY
- HERMETIC CERAMIC 16 PIN DIP

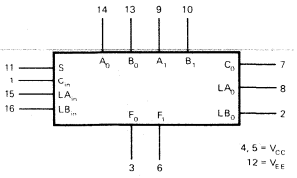


95H84 2 BIT ADDER/SUBTRACTOR

DESCRIPTION Performs addition and subtraction on two bits with full internal carry look ahead expandable between units. No additional carry look ahead unit is required. Can be implemented to add or subtract 2 64 bit words within 20 nsec at a power comparable to a TTL adder with carry look ahead units.

An arithmetic logic unit using 95H84 for adders, 9528 and 34 for registers and a scratchpad memory of 9538 and 95H40 could effectively process 32 bit words at a 40 MHz clock rate using a multiphase clocking scheme.

- HIGH SPEED . . . 1.5 ns INTERNAL GATE DELAYS
- ADDS AND SUBTRACTS WITH ONE DEVICE
- INTERNAL CARRY LOOKAHEAD
- WIRED OR CAPABILITY
- SEPARATE CURRENT SWITCH EMITTER FOLLOWER V_{OC} PINS – ELIMINATE NOISE COUPLING
- TEMPERATURE COMPENSATION
- INTERNAL PULL DOWN
- 50 Ω LINE DRIVE CAPABILITY
- SINGLE –5.2 VOLT POWER SUPPLY
- HERMETIC CERAMIC 16 PIN DIP
- COMPLEX MULTI-GATE CHIP REDUCES PACKAGE COUNT & POWER



ACTIVE HIGH BLOCK DIAGRAM

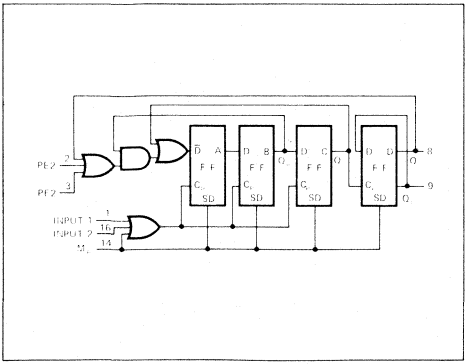
A_0, B_0, A_1, B_1	OPERAND INPUTS
F_0, F_1	FUNCTION OUTPUTS
S	SUBTRACT SELECT LINE
C_n, C_0	CARRY IN AND OUT
LA_n, LB_n	CARRY LOOKAHEAD INPUTS FROM PREVIOUS UNIT
LA_0, LB_0	CARRY LOOKAHEAD OUTPUTS TO FOLLOWING UNIT

95H90 VHF PRESCALER ÷ 10/11

DESCRIPTION *The 95H90 prescaler is a high speed ECL MSI designed* specifically for the communication and instrumentation manufacturer. In its simplest use it will divide any clock frequency up to 250 MHz, by 10. By using the 9590 with other control logic a divide by 10/11 logic control element allows a divide by "N" counter to be constructed with a max frequency over 250 MHz.

By keeping all the high speed logic manipulation "on chip", a dramatic decrease in power and increase in reliability and wire-ability are made available at much lower cost than a comparable SSI function.

- HIGH SPEED . . . 300 MHz
- ÷10/11 ENABLE
- HIGH SPEED RESET
- WIRED OR CAPABILITY
- SEPARATE CURRENT SWITCH EMITTER FOLLOWER V_{CC} PINS ELIMINATE NOISE COUPLING
- TEMPERATURE COMPENSATION
- INTERNAL PULL DOWN
- 50 Ω LINE DRIVE CAPABILITY
- SINGLE –5.2 VOLT POWER SUPPLY
- HERMETIC CERAMIC 16 PIN DIP
- COMPLEX MULTI-GATE CHIP REDUCES PACKAGE COUNT & POWER

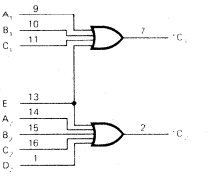


9595 DUAL ECL/TTL CONVERTER

DESCRIPTION *The 9595 is a high speed logic converter for use in* systems using both the high speed of ECL and the many available functions of TTL. The 9595 requires the –5.2 volt V_{EE} supply of ECμL and the +5 volt V_{CC} of TTL. The TTL fanout of 4 may be expanded by adding more pulldown current at the TTL output pin.

By allowing the logic converter to function as a logic gate the normally wasted time of logic conversion may be used in the logic implementation with the through delay generally less than that found in TTL circuits.

- HIGH SPEED . . . 6 ns
- FAN OUT 10
- NO INVERSION THROUGH CONVERTER
- ECL INPUT TEMPERATURE COMPENSATED
- INTERNAL PULL DOWNS
- HERMETIC CERAMIC 16 PIN DIP
- FUNCTIONS AS DUAL 2 INPUT GATE
- MULTIPLE LOGIC GATE CAPABILITY



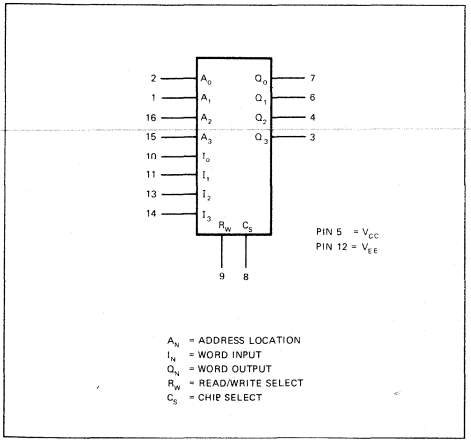
* CCSL, UP TO 4 LOADS, UP TO 10 WITH EXTERNAL R TO V_{EE}

95400 64 BIT MEMORY

DESCRIPTION The 95400 is a very high speed 64 bit memory organized 16 words by 4 bits. Internal decoding is employed with the 16 words selected through four address lines. A chip select input, read/write control line, and OR-tieable outputs are also provided.

The 16x4 organization was chosen as optimum for small high speed scratchpad applications. For word capacities in excess of 16, the 9538 decoder will permit expansion with very little decrease in overall speed.

- **HIGH SPEED . . . 12 ns ACCESS TIME**
- **LARGE CAPACITY – 64 BITS**
- **OPTIMIZED FOR SMALL WORDS – 16 x 4**
- **HIGH SPEED CHIP ENABLE FOR EASE OF EXPANSION**
- **WIRED-OR CAPABILITY**
- **TEMPERATURE COMPENSATION**
- **ALL INPUTS AND OUTPUTS OPEN FOR EASE OF EXPANSION**
- **50 Ω LINE DRIVE CAPABILITY**
- **SINGLE –5.2 VOLT POWER SUPPLY**
- **HERMETIC CERAMIC 16 PIN DIP**
- **COMPLEX MULTI-GATE CHIP REDUCES PACKAGE COUNT & POWER**



95401 16 BIT SCRATCHPAD MEMORY

DESCRIPTION This element is a 16 bit monolithic integrated memory element designed for use in very high speed scratchpad memory applications. The element consists of 16 nonsaturating bistable storage cells arranged in an addressable four-by-four matrix.

The logic diagram below indicates the X and Y address lines, sense zero and sense one, S_0, S_1 and write zero and write one. W_0, W_1, pin locations.

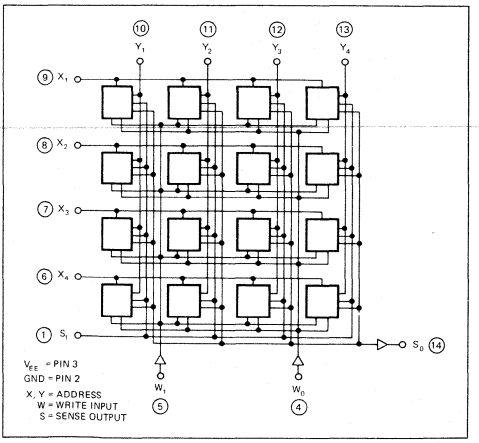
All outputs are normal logic "0" for ease of expansion to larger word sizes.

A desired bit location is selected by raising the coincident X–Y address lines to a logic "1" (typically –0.8 volts) and holding the nonselected address lines at logic "0" (typically –1.6 volts). The data, and its complement stored at the addressed location are read at the sense output terminals. If a "1" is stored, terminal S_1 will be at logical "1", if "0" is stored, terminal S_0 will be at "1".

Writing a logical "1" is accomplished by raising W_1 to "1" and addressing the appropriate location, as for sensing. A logic "0" is stored by applying "1" to terminal W_0.

This element is available in the hermetically sealed, 14 lead ceramic Dual-In-line Package, suitable for operation over the temperature range 0°C to 75°C. This device is second sourced by RCA as the CD2155D.

- **HIGH SPEED – ACCESS TIME <6 ns, READ/WRITE CYCLE TIME <18 ns**
- **OUTPUT WIRE – OR FACILITY FOR WORD EXPANSION**
- **NON-DESTRUCTIVE READ-OUT**
- **TRUE AND COMPLEMENTARY OUTPUTS PROVIDED**
- **50 Ω LINE DRIVE CAPABILITY**
- **ECL COMPATIBLE – LOGIC "1" TYPICALLY –0.8V**
  – LOGIC "0" TYPICALLY –1.6V
- **SINGLE POWER SUPPLY (–5.0V/–5.2V)**
- **POWER DISSIPATION TYPICALLY 300 mW**



DATA SHEETS easy ECL

95H00

HIGH SPEED 4-BIT UNIVERSAL SHIFT REGISTER

FAIRCHILD TEMPERATURE COMPENSATED ECL

GENERAL DESCRIPTION

The 95H00 is a four bit Parallel/Serial In, Parallel/Serial Out Universal shift register. High speed ECL technology permits storage, shifting, counting and serial code conversation in excess of 150 MHz.

Features include assertion outputs on each state, overriding asynchronous master reset, serial and parallel D type inputs and a gated clock. Availability of all these features on one chip significantly improves the reliability, performance, and power consumption of high speed systems.

- HIGH SPEED - 150 MHz SHIFT FREQUENCY
- D TYPE INPUT IN SERIAL AND PARALLEL
- GATED CLOCK INPUT
- ASYNCHRONOUS MASTER RESET
- 50 Ω DRIVE ON Q3 OUTPUT
- WIRED OR CAPABILITY
- SEPARATE CURRENT SWITCH EMITTER FOLLOWER V_{CC} PINS - ELIMINATE NOISE COUPLING
- TEMPERATURE COMPENSATION
- INTERNAL PULL DOWN
- SINGLE -5.2 VOLT POWER SUPPLY
- HERMETIC CERAMIC 16 PIN DIP
- COMPLEX MULTI-GATE CHIP REDUCES PACKAGE COUNT & POWER

PIN NAMES

P_N	PARALLEL IN
P_E	PARALLEL ENABLE - ACTIVE LOW
C_P	CLOCK IN, SHIFTS ON POSITIVE TRANSITION
M_R	ASYNCHRONOUS MASTER RESET
D	DATA INPUT, SERIAL
Q_N	SLAVE OUTPUTS
Q3	SERIAL DATA OUTPUT

ORDER INFORMATION - SPECIFY U6B95H00 XX FOR 16 PIN DUAL IN-LINE PACKAGE WHERE XX IS 9X FOR 0°C TO + 75°C TEMPERATURE RANGE.

FAIRCHILD SEMICONDUCTOR

ELECTRICAL SPECS D.C. 0^{o} - 75^{o} C, V_{EE} = -5.2O

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
V_{CH}	OUTPUT HIGH LEVEL	-92O	-86O	-8OO	mV	F.O. = 1
V_{OH}	OUTPUT HIGH LEVEL	-97O	-91O	-85O	mV	F.O. = 5
V_{OH}	OUTPUT HIGH LEVEL	-1O1O	-95O	-89O	mV	5O Ω to -2.OV + 5 pf to V_{CC}
V_{OL}	OUTPUT LOW LEVEL	-178O	-169O	-16OO	mV	F.O. = 1
V_{OL}	OUTPUT LOW LEVEL	-183O	-174O	-165O	mV	F.O. = 5
V_{OL}	OUTPUT LOW LEVEL	-181O	-172O	-163O	2 mV	5O Ω to -2.OV + 5pf to V_{CC}
V_{ILX}	INPUT THRESHOLD LOW	-	-	-145O	mV	MAX. INPUT VOLTAGE FOR LOW LOGIC
V_{IHX}	INPUT THRESHOLD HIGH	-114O	-	-	mV	MIN. INPUT VOLTAGE FOR HIGH LOGIC
I_{IN}	INPUT CURRENT HIGH		2.25	3.16	mA	V_{IN} = -9OO mV
I_{IN}	INPUT CURRENT LOW		1.75	2.46	mA	V_{IN} = -17OO mV
I_{PS}	POWER SUPPLY CURRENT		1OO		mA	

ELECTRICAL SPECS A.C.

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
Tpd	CLOCK TO OUTPUT (AII)		3.6		nS	
Tpd	M_R TO OUTPUT		5.O		nS	
Tpcd	$\overline{P}_E$ PRIOR TO CLOCK		1.5		nS	
Tpch	$\overline{P}_E$ HOLD AFTER CLOCK		1.O		nS	
Tcpw	CLOCK PULSE WIDTH		2.5		nS	
Trw	RESET PULSE WIDTH		4		nS	
fc	SHIFT FREQUENCY		16O		MHz	
Tr, Tf	RISE FALL TIME	1.5	2.5		nS	
It	TRANSIANT INPUT CURRENT		2.5	3.5	mA	

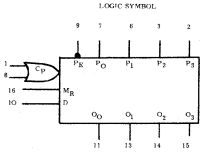


FIG 1

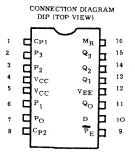


FIG 2

9502 • 9503 • 9504

HIGH SPEED GATES

FAIRCHILD TEMPERATURE COMPENSATED ECL

GENERAL DESCRIPTION — The 9502, 9503 and 9504 are temperature compensated ECμL OR/NOR Gates employing a nonsaturating current switch, emitter follower configuration to achieve high speed. The elements are intended for the design of high speed central processors, terminals, instrumentation and digital communications systems.

All 9500 series elements incorporate a unique temperature compensation network. This insures that significant parameters such as logic levels, noise margin and speed remain relatively constant over a wide temperature range. Input and output 2 kΩ pulldown resistors eliminate the necessity for external termination of lines up to 6-8 inches and unused logic inputs. Package pin locations are chosen to reduce internal noise generation and crosstalk.

The devices are packaged in the hermetic CERAMIC, 16 pin Dual In-Line Package and specified for operation over the temperature range 0°C to 75°C.

- **HIGH SPEED . . . 2.3 ns PER GATE**
- **SEPARATE CURRENT SWITCH AND EMITTER FOLLOWER V_{CC} PINS — ELIMINATES NOISE COUPLING**
- **TEMPERATURE COMPENSATION**
- **INTERNAL PULLDOWN RESISTORS**
- **COMMON ENABLE INPUTS**
- **LOW CROSSTALK AND NOISE GENERATION**
- **WIRE-OR CAPABILITY**
- **50 Ω LINE DRIVING CAPABILITY**
- **COMPLEMENTARY OR/NOR OUTPUTS (9502, 9503)**
- **SINGLE —5.2 V POWER SUPPLY**
- **HERMETIC CERAMIC 16 PIN DUAL IN-LINE PACKAGE**

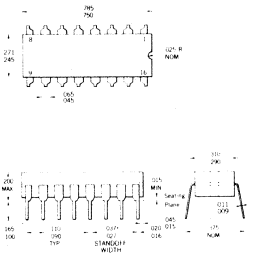
ABSOLUTE MAXIMUM RATINGS (above which useful life may be impaired)

Storage Temperature	−65°C to +150°C
Junction Temperature	+150°C
Supply Voltage V_{EE} (Continuous)	−6 Volts
Supply Voltage V_{EE} (Pulsed)	−8 Volts
Input Voltage	GND to V_{EE} (max)
Output Current	40 mA

ORDER INFORMATION

Specify U6B9502XXX for 16 pin Dual In-Line Package where XXX is 59X for the 0°C to +75°C temperature range for 9502 gate. Substitute 9503 or 9504 for other elements.

PHYSICAL DIMENSIONS
16 LEAD DUAL IN-LINE



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin plated kovar
Package weight is 2.0 grams
The .027/.037 dimensions does not apply to the corner leads

FUNCTIONAL DESCRIPTION

The 9500 Series Temperature Compensated ECμL Gates are based on the current switch-emitter follower (CSEF), or emitter coupled (ECμL), configuration of Figure 1. Additional circuit complexity compared with conventional ECμL is incorporated to improve system operating characteristics. This includes temperature compensation networks to insure that logic levels and thresholds, set by the on chip bias driver, are essentially independent of temperature. On chip output emitter follower and input pulldown 2 k ohm resistors reduce external components normally required for short line termination and unused logic inputs. A current source in the tail of the differential amplifier equalizes ONE and ZERO level noise margins by removing the NOR side saturation knee, and also improves saturation temperature dependency.

Defining logic "ONE" as $V_{OH} = -895$ mV (typ) and logic "ZERO" as $V_{OL} = -1710$ mV (typ), the elements perform the logical NOR and OR functions. The opposite definition specifies NAND/AND operation. All parameters specified in the characteristics are defined by the algebraic maximum and minimum limits.

Gate pin configurations are indicated in Fig. 2. An input enable line common to all gates in each package is provided for additional logical flexibility.

Fig. 1 — CIRCUIT SCHEMATIC

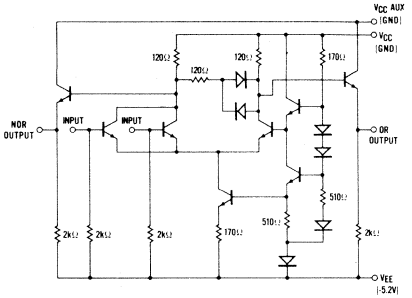
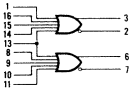


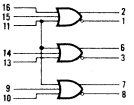
Fig. 2 — LOGIC DIAGRAM AND PIN CONNECTION

9502



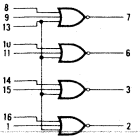
Dual 4 OR/NOR
(with enable)

9503



Triple 2 OR/NOR
(with enable)

9504



Quad 2 NOR
(with enable)

On all elements
Pins 4 and 5
are circuit
ground, V_{CC}
Pin 12 is
V_{EE}, −5.2 V

D.C. ELECTRICAL CHARACTERISTICS (Industrial Temperature Range 0°C to +75°C, V_{CC} = Gnd, V_{EE} = −5.2 V)

SYMBOL	CHARACTERISTIC	LIMITS 0°C MIN.	0°C TYP.	0°C MAX.	+25°C MIN.	+25°C TYP.	+25°C MAX.	+75°C MIN.	+75°C TYP.	+75°C MAX.	UNITS	CONDITIONS
$I_{IN}(1)$	Input Current at V_{IH}											
	Standard Gate		2.30	3.15		2.25	3.10		2.15	3.00	mA	V_{IH} = −900 mV to each input sequentially
	Enable Lines											
	9502		4.60	6.30		4.50	6.20		4.30	6.00	mA	
	9503		6.90	9.45		6.75	9.30		6.45	9.00	mA	
	9504		9.20	12.60		9.00	12.40		8.60	12.00	mA	
$I_{IN}(0)$	Input Current at V_{IL}											
	Standard Gate		1.80	2.40		1.75	2.35		1.65	2.25	mA	V_{IL} = −1700 mV to each input sequentially
	Enable Lines											
	9502		3.60	4.80		3.50	4.70		3.30	4.50	mA	
	9503		5.40	7.20		5.25	7.05		4.95	6.75	mA	
	9504		7.20	9.60		7.00	9.40		6.60	9.00	mA	
I_{PD}	Power Supply Current											
	9502	25	33	43	29	35	44	30	37	48	mA	All inputs
	9503	35	46	59	40	48	60	40	51	65	mA	open
	9504	40	52	67	45	54	68	41	57	74	mA	
ΔI_{IN}	Input Saturation Test									50	μA	See Fig. 4 $\Delta I_{IN} = I_B - I_A$ $I_A = I_{IN}$ @ V_{IN} = 800 mV $I_B = I_{IN}$ @ V_{IN} = 750 mV

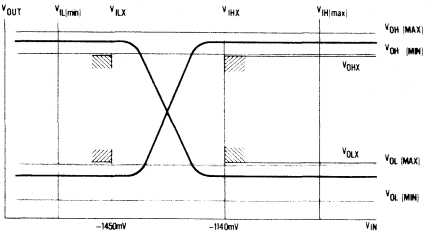
A.C. ELECTRICAL CHARACTERISTICS (Industrial Temperature Range 0°C to +75°C)

SYMBOL	CHARACTERISTIC	LIMITS 0°C MIN.	0°C TYP.	0°C MAX.	+25°C MIN.	+25°C TYP.	+25°C MAX.	+75°C MIN.	+75°C TYP.	+75°C MAX.	UNITS	CONDITIONS
t_{pd}	Propagation Delay											
	t_{pd-}		2.3			2.3	3.5		2.5		ns	See Fig. 5
	t_{pd+}		2.2			2.2	3.5		2.4		ns	R_L = 50 Ω to −2.0 V
	t_{pd-}		2.4			2.4	3.5		2.6		ns	C_L <5.0 pF
	t_{pd+}		2.5			2.5	3.2		2.7		ns	$t_r = t_f$ = 2.5 ns
t_r	Rise Time	1.5		4.5	1.5	3.0	4.5	1.5		4.5	ns	See Fig. 5 R_L = 50 Ω to −2.0 V C_L <5.0 pF
t_f	Fall Time	1.5		4.5	1.5	3.0	4.5	1.5		4.5	ns	See Fig. 5 R_L = 50 Ω to −2.0 V C_L <5.0 pF
I_T	Transient Input Current											
	Standard Gate					2.5	3.5				mA	See Fig. 6 on Page 5
	Enable Lines											
	9502					3.4	4.5				mA	
	9503					4.7	5.7				mA	
	9504					5.0	6.0				mA	
t_{pd}	Propagation Delay											
	t_{pd-}		2.6			2.6	3.5		2.8		ns	See Fig. 5
	t_{pd+}		2.5			2.5	3.5		2.7		ns	R_L = 50 Ω to −2.0 V
	t_{pd-}		2.7			2.7	3.5		2.9		ns	C_L = 15 pF ±5%
	t_{pd+}		2.8			2.8	3.5		3.0		ns	$t_r = t_f$ = 2.5 ns

D.C. ELECTRICAL CHARACTERISTICS (Industrial Temperature Range 0°C to +75°C, V_{CC} = Gnd, V_{EE} = −5.2 V)

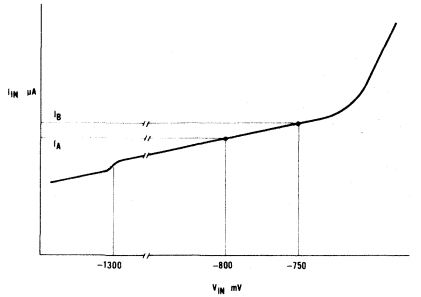
SYMBOL	CHARACTERISTIC	LIMITS									UNITS	CONDITIONS
		0°C			+25°C			+75°C				
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
V_{OH}	Output High Voltage											V_{IL} = −1700 mV for NOR gate; V_{IH} = −900 mV for OR gate
	F.O. = 1 gate	−900	−850	−800	−900	−850	−800	−890	−840	−790	mV	
	F.O. = 5 gates	−940	−890	−840	−940	−890	−840	−940	−890	−840	mV	
	50 Ω to −2.0 V	−975	−925	−875	−975	−925	−875	−975	−925	−875	mV	
V_{OL}	Output Low Voltage											V_{IL} = −1700 mV for OR gate; V_{IH} = −900 mV for NOR gate
	F.O. = 1 gate	−1745	−1670	−1595	−1745	−1670	−1595	−1745	−1670	−1595	mV	
	F.O. = 5 gates	−1785	−1710	−1635	−1785	−1710	−1635	−1785	−1710	−1635	mV	
	50 Ω to −2.0 V	−1775	−1700	−1625	−1775	−1700	−1625	−1775	−1700	−1625	mV	
V_{OHX}	Output High Voltage at V_{IN} (threshold)											See Fig. 3; V_{ILX} = −1450 mV for NOR gate; V_{IHX} = −1140 mV for OR gate (To each input sequentially, other inputs open)
	F.O. = 1 gate	−910			−910			−900			mV	
	F.O. = 5 gates	−950			−950			−950			mV	
	50 Ω to −2.0 V	−985			−985			−985			mV	
V_{OLX}	Output Low Voltage at V_{IN} (threshold)											See Fig. 3; V_{ILX} = −1450 mV for OR gate; V_{IHX} = −1140 mV for NOR gate (To each input sequentially, other inputs open)
	F.O. = 1 gate			−1585			−1585			−1585	mV	
	F.O. = 5 gates			−1625			−1625			−1625	mV	
	50 Ω to −2.0 V			−1615			−1615			−1615	mV	

Fig. 3 — NOISE MARGIN SPECIFICATION POINTS



Corner points indicated on the transfer characteristics represent the worst case points (thresholds) at which the device will start to switch. The values V_{ILX} and V_{IHX} define the maximum width of the transition region.

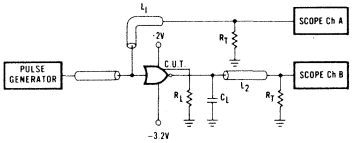
Fig. 4 — INPUT SATURATION TEST

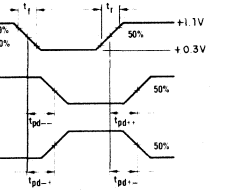


This test insures that the input transistor is not in saturation at $V_{IN} = 750$ mV. This represents a worst case condition with the driving gate at V_{OH} (min) = 750 mV (ie. for $T_A = 75°C$ this is equivalent to driving gate into FO = 1 with its power supply at −5%).

Saturation is defined as no increase in collector current for 20% increase in base drive current I_R. The effect is to increase t_{pd}.

Fig. 5 — SWITCHING TIME TEST CIRCUIT AND WAVEFORM



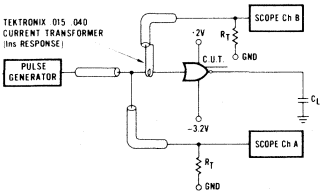


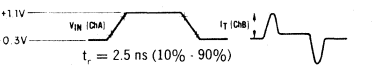
$t_r = t_f = 2.5$ ns (10% · 90%) Jig setup with no circuit under test

$V_{CC} = V_{CC}$ (AUX) = +2.0 V

V_{EE} = −3.2 V

Fig. 6 — TRANSIENT INPUT CURRENT TEST CIRCUIT AND WAVEFORMS





This test provides a measure of the average value of C_{IN}; also current mismatch in the line.

$V_{CC} = V_{CC}$ (AUX) = +2.0 V

V_{EE} = −3.2 V

L_1 and L_2 = equal length 50 Ω impedance lines

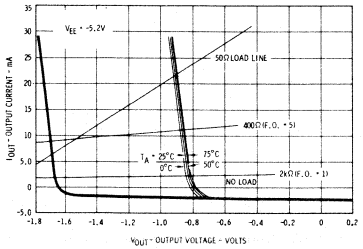
$R_L = R_T = 50\ \Omega$ Termination of Scope

C_L = Jig and Stray Capacitance < 5.0 pF

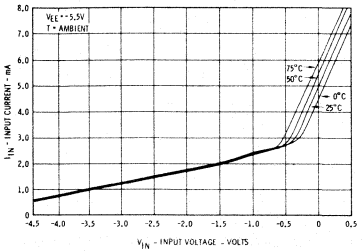
Logic levels for Figs. 5 and 6 are nominal values at 50 Ω fanout determined by indicated power supplies. These values chosen to permit use of scope 50 Ω termination to ground.

Decoupling 0.1 μF from GND to V_{EE}.

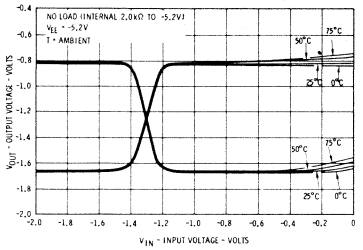
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE



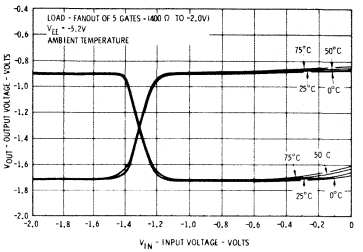
INPUT CURRENT VERSUS INPUT VOLTAGE



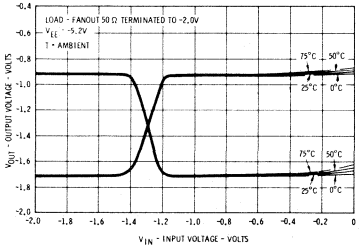
TRANSFER CHARACTERISTICS VERSUS AMBIENT TEMPERATURE



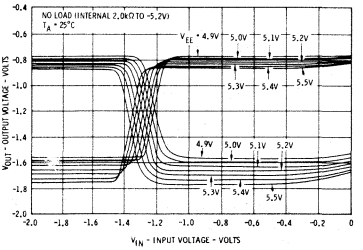
TRANSFER CHARACTERISTICS VERSUS AMBIENT TEMPERATURE



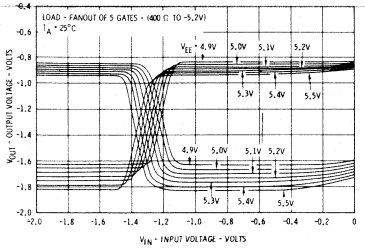
TRANSFER CHARACTERISTICS VERSUS AMBIENT TEMPERATURE



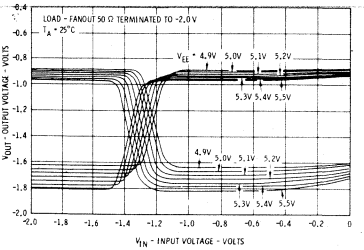
TRANSFER CHARACTERISTICS VERSUS POWER SUPPLY VARIATION



TRANSFER CHARACTERISTICS VERSUS POWER SUPPLY VARIATION

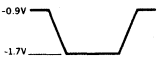


TRANSFER CHARACTERISTICS VERSUS POWER SUPPLY VARIATION

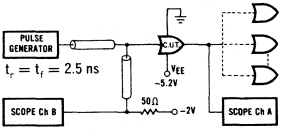


TYPICAL PROPAGATION DELAY VERSUS FAN OUT

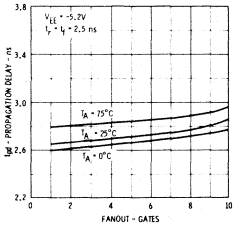
INPUT WAVEFORM



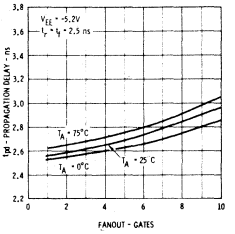
$t_r = t_f = 2.5$ ns (10% - 90%)



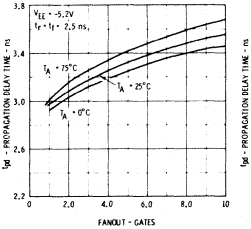
TYPICAL PROPAGATION DELAY VERSUS FANOUT t_{pd++} (OR output)



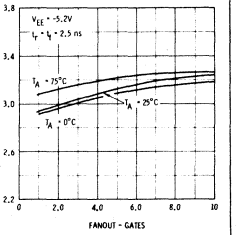
TYPICAL PROPAGATION DELAY VERSUS FANOUT t_{pd--} (OR output)



TYPICAL PROPAGATION DELAY VERSUS FANOUT t_{pd+-} (NOR output)

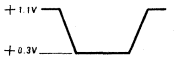


TYPICAL PROPAGATION DELAY VERSUS FANOUT t_{pd-+} (NOR output)



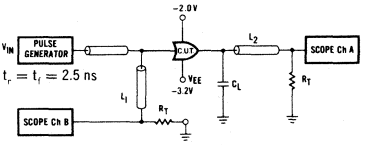
TYPICAL PROPAGATION DELAY VERSUS CAPACITIVE LOAD (in a 50 ohm system)

INPUT WAVEFORM

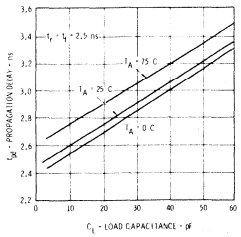


$t_r = t_f = 2.5$ ns (10% - 90%)

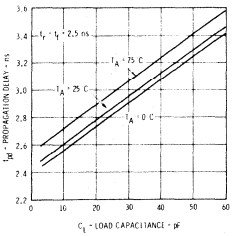
$V_{CC} = V_{CC}(AUX) = +2.0$ V
$V_{EE} = -3.2$ V
$R_T = 50\ \Omega$ Termination of scope
L_1 & L_2 = Equal length 50 Ω impedance lines



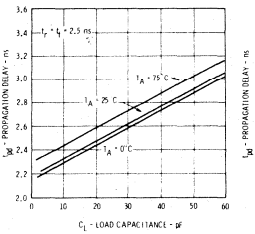
TYPICAL PROPAGATION DELAY VERSUS LOAD CAPACITANCE t_{pd+-} (NOR output)



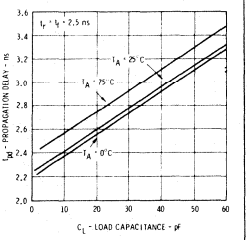
TYPICAL PROPAGATION DELAY VERSUS LOAD CAPACITANCE t_{pd-+} (NOR output)



TYPICAL PROPAGATION DELAY VERSUS LOAD CAPACITANCE t_{pd++} (OR output)

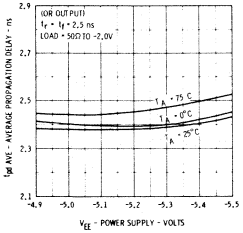


TYPICAL PROPAGATION DELAY VERSUS LOAD CAPACITANCE t_{pd--} (OR output)

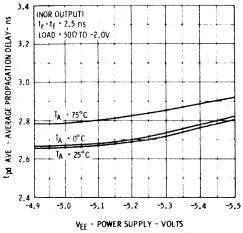


TYPICAL AVERAGE PROPAGATION DELAY VERSUS POWER SUPPLY

TYPICAL AVERAGE PROPAGATION DELAY VERSUS POWER SUPPLY



TYPICAL AVERAGE PROPAGATION DELAY VERSUS POWER SUPPLY



$$t_{pd\ ave} = \frac{t_{pd\ rising} + t_{pd\ falling}}{2}$$

APPLICATIONS NOTES

INTERCONNECTION RECOMMENDATIONS

All high speed ECμL circuits demand that special precautions be taken for optimum system performance. A ground plane must be provided for a good, low impedance, ground current return path and to transform interconnections into microstrip transmission lines. The voltage supply line should be well decoupled with small ceramic capacitors throughout each card between V_{EE} and the ground plane and by including at least one larger tantalum capacitor per card.

Typical microstrip lines have a characteristic impedance between 50 and 150 ohms with the lower being more desirable in ECμL systems. For local interconnects the internal 2 kΩ resistors provide adequate termination but for optimum performance lines longer than 6 or 8 inches in length should be terminated in their characteristic impedance.

Lines up to 12 inches may be left unterminated if a degraded waveform can be tolerated with the resultant decrease in speed and increase in ringing.

Microstrip interconnections may be terminated by a resistor to a −2 volt supply: $R = \frac{Z_O}{1 - NZ_O/2000}$ where Z_O is the characteristic impedance of the line and N is the number of loads. Alternately, a 2 resistor divider network may be used with $R_1 = 1.6\,R$ connected to ground and $R_2 = 2.6\,R$ connected to V_{EE}.

Series terminating resistors decrease noise immunity and slow rise and fall times, but can still be used if these effects are tolerable. In addition, care must be taken to avoid glitches in the threshold region of the waveform occurring at certain combinations of line length and series resistor value.

A single terminated wire running over a ground screen can be used for backpanel interconnections up to 4 or 5 inches in length, but terminated coaxial cables or terminated twisted pairs of wire are required for longer interconnections.

LINE DRIVING CAPABILITY

The 9500 series ECμL circuits are capable of driving fairly long lines if the previous recommendations are followed. 50 ohm coaxial cables 10 feet in length or longer and properly terminated may be driven with almost no degradation in the waveform. The normal delay due to the finite speed of the signal traveling down the cable will be encountered in addition to a slight decrease in signal swing. This decrease caused by the attenuation of the cable (about 40 mV for 10 feet of 50 ohm coax) will lower the noise immunity of the receiving circuit by the same amount. Care must be exercised to ensure the ground potentials at the driving and receiving ends of a line are equal and no differential noise is present.

95H02 • 95H03 • 95H04

VERY HIGH SPEED GATES

FAIRCHILD TEMPERATURE COMPENSATED ECL

GENERAL DESCRIPTION – The 95H02, 95H03 and 95H04 are temperature compensated ECL OR/NOR Gates employing a nonsaturating current switch, emitter follower configuration to achieve high speed. The elements are intended for the design of high speed central processors, terminals, instrumentation and digital communications systems.

All 9500 series elements incorporate a unique temperature compensation network. This insures that significant parameters such as logic levels, noise margin and speed remain relatively constant over a wide temperature range. Input and output 2 kΩ pulldown resistors eliminate the necessity for external termination of lines up to 6-8 inches and unused logic inputs. Package pin locations are chosen to reduce internal noise generation and crosstalk.

The devices are packaged in the hermetic CERAMIC, 16 pin Dual In-Line Package and specified for operation over the temperature range 0°C to 75°C.

- **PIN IDENTICAL TO LOWER SPEED GATES (9502 • 9503 • 9504)**
- **VERY HIGH SPEED . . . 1.7 ns PER GATE**
- **SEPARATE CURRENT SWITCH AND EMITTER FOLLOWER V_{CC} PINS – ELIMINATES NOISE COUPLING**
- **TEMPERATURE COMPENSATION**
- **INTERNAL PULLDOWN RESISTORS**
- **COMMON ENABLE INPUTS**
- **LOW CROSSTALK AND NOISE GENERATION**
- **WIRED–OR CAPABILITY**
- **50 Ω LINE DRIVING CAPABILITY**
- **COMPLEMENTARY OR/NOR OUTPUTS (9502, 9503)**
- **SINGLE –5.2 V POWER SUPPLY**
- **HERMETIC CERAMIC 16 PIN DUAL IN-LINE PACKAGE**

ORDER INFORMATION – Specify U6B95H02XX for 16 pin Dual In-Line Package where XXX is 59X for the 0°C to +75°C temperature range for 95H02 gate. Substitute 95H03 or 95H04 for other elements.

CIRCUIT SCHEMATIC

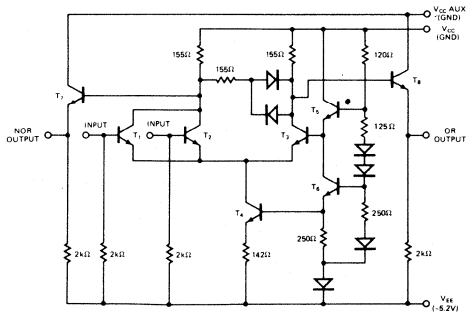
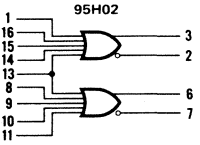


Fig. 1

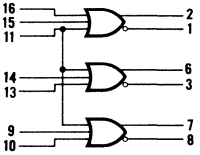
LOGIC DIAGRAM AND PIN CONNECTION

95H02



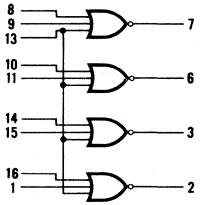
Dual 4 OR/NOR
(with enable)

95H03



Triple 2 OR/NOR
(with enable)

95H04



Quad 2 NOR
(with enable)

On all elements Pins 4 and 5 are circuit ground, V_{CC}. Pin 12 is V_{EE}, –5.2 V

Fig. 2

FUNCTIONAL DESCRIPTION — The 9500 Series Temperature Compensated ECL Gates are based on the current switch-emitter follower (CSEF), or emitter coupled (ECL), configuration of Figure 1. Additional circuit complexity compared with conventional ECL is incorporated to improve system operating characteristics. This includes temperature compensation networks to insure that logic levels and thresholds, set by the on chip bias driver, are essentially independent of temperature. On chip output emitter follower and input pulldown 2 k ohm resistors reduce external components normally required for short line termination and unused logic inputs. A current source in the tail of the differential amplifier equalizes ONE and ZERO level noise margins by removing the NOR side saturation knee, and also improves saturation temperature dependency.

Defining logic "ONE" as V_{OH} = −900 mV (typ) and logic "ZERO" as V_{OL} = −1700 mV (typ), the elements perform the logical NOR and OR functions. The opposite definition specifies NAND/AND operation. All parameters specified in the characteristics are defined by the algebraic maximum and minimum limits.

Gate pin configurations are indicated in Fig. 2. An input enable line common to all gates in each package is provided for additional logical flexibility.

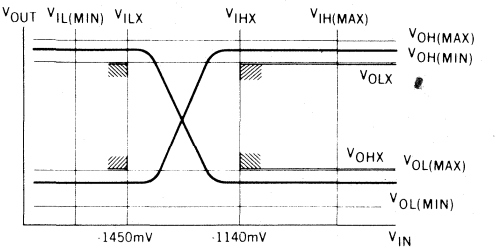
ABSOLUTE MAXIMUM RATINGS (above which useful life may be impaired)

Storage Temperature	−65°C to +150°C
Junction Temperature	+150°C
Supply Voltage V_{EE} (Continuous)	−6 Volts
Supply Voltage V_{EE} (Pulsed)	−8 Volts
Input Voltage	GND to V_{EE} (max)
Output Current	40 mA

D.C. ELECTRICAL CHARACTERISTICS (Operating Temperature Range: T_A = 0°C to 75°C, V_{CC} = GND, V_{EE} = −5.2 V)

SYMBOL	CHARACTERISTIC	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS		CONDITIONS
V_{OH}	Output Voltage High		−860 −910 −950		mV	FO = 1 Gate FO = 5 Gates 50 Ω to −2.0 V	$V_{IN} = V_{IL}$ = −1700 mV for NOR Gate $V_{IN} = V_{IH}$ = −900 mV for OR Gate
V_{OL}	Output Voltage Low		−1690 −1740 −1720		mV	FO = 1 Gate FO = 5 Gates 50 Ω to −2.0 V	$V_{IN} = V_{IH}$ = −900 mV for NOR Gate $V_{IN} = V_{IL}$ = −1700 mV for OR Gate
V_{OHX}	Output Voltage High at $V_{IN} = V_{IX}$ (Threshold)	−930 −970 −1010			mV	FO = 1 Gate FO = 5 Gates 50 Ω to −2.0 V	See Fig. 3 $V_{IN} = V_{ILX}$ = −1450 mV for NOR Gate $V_{IN} = V_{IHX}$ = −1140 mV for OR Gate
V_{OLX}	Output Voltage Low at $V_{IN} = V_{IX}$ (Threshold)			−1605 −1655 −1635	mV	FO = 1 Gate FO = 5 Gates 50 Ω to −2.0 V	See Fig. 3 $V_{IN} = V_{ILX}$ = −1450 mV for OR Gate $V_{IN} = V_{IHX}$ = −1140 mV for NOR Gate
V_{IHX}	Guaranteed Input High Threshold Voltage	−1140			mV		Guaranteed Input High Threshold Voltage
V_{ILX}	Guaranteed Input Low Threshold Voltage			−1450	mV		Guaranteed Input Low Threshold Voltage
$V_{IN(H)}$	Input Current High		2.40	3.58	mA		V_{IN} = −900 mV to Common Enable Input
$V_{IN(H)}$	Input Current High		2.25	3.16	mA		V_{IN} = −900 mV to Other Inputs Sequentially
$V_{IN(L)}$	Input Current Low		1.75	2.46	mA		V_{IN} = −1700 mV to Each Input Sequentially
I_{PS}	Power Supply Current 95H02 95H03 95H04	 26 36 48	 34 49 62	 45 64 80	mA		All Inputs & Outputs Open

NOISE MARGIN SPECIFICATION POINTS



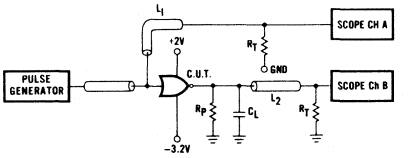
Corner points indicated on the transfer characteristics represent the worst case points (thresholds) at which the device will start to switch. The values V_{ILX} and V_{IHX} define the maximum width of the transition region.

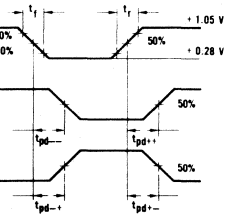
Fig. 3

AC ELECTRICAL CHARACTERISTICS (T_A = 0°C to 75°C)

SYMBOL	CHARACTERISTIC	LIMITS 0°C TYP.	LIMITS MIN.	LIMITS 25°C TYP.	LIMITS MAX.	LIMITS 75°C TYP.	UNITS	CONDITIONS
	Propagation Delay							
t_{pd}	10% – 50%						ns	See Fig. 5
	t_{pd} – –	1.6	–	1.6	2.4	1.8		R_L = 50 Ω to –2 V
	t_{pd} + +	1.7	–	1.7	2.4	1.9		C_L <5 pF
	t_{pd} – +	1.6	–	1.6	2.4	1.8		$t_r = t_f$ = 2.2 ns (10 – 90%)
	t_{pd} + –	1.8	–	1.8	2.4	2.0		
t_f	Fall Time 10% – 90%	2.2	1.4	2.2	3.0	2.2	ns	
t_r	Rise Time 10% – 90%	2.2	1.4	2.2	3.0	2.2		

SWITCHING TIME TEST CIRCUIT AND WAVEFORM





$t_r = t_f$ = 2.4 ns (10% - 90%)

Jig setup with no circuit under test.

$V_{CC} = V_{CC(AUX)}$ = +2.0 V

V_{EE} = –3.2 V

L_1 and L_2 = equal length 50 Ω impedance lines

$R_L = R_T$ = 50 Ω Termination of Scope

C_L = Jig and Stray Capacitance <5.0 pF

Logic levels for Fig. 5 is nominal values at 50 Ω fanout determined by indicated power supplies. These values chosen to permit use of scope 50 Ω termination to ground.

Decoupling 0.1 μF from GND to V_{EE}.

Fig. 4

APPLICATION

INTERCONNECTION RECOMMENDATIONS – All high speed ECL circuits demand that special precautions be taken for optimum system performance. A ground plane must be provided for a good, low impedance, ground current return path and to transform interconnections into microstrip transmission lines. The voltage supply line should be well decoupled with small ceramic capacitors throughout each card between V_{EE} and the ground plane and by including at least one larger tantalum capacitor per card.

Typical microstrip lines have a characteristic impedance between 50 and 150 ohms with the lower being more desirable in ECL systems. For local interconnects the internal 2 kΩ resistors provide adequate termination but for optimum performance lines longer than 6 or 8 inches in length should be terminated in their characteristic impedance.

Lines up to 12 inches may be left unterminated if a degraded waveform can be tolerated with the resultant decrease in speed and increase in ringing.

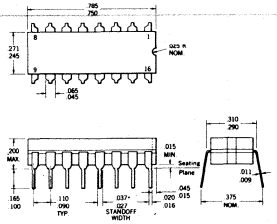
Microstrip interconnections may be terminated by a resistor to a −2 volt supply. Alternately, a 2 resistor divider network may be used with R_1 = 1.6 R connected to ground and R_2 = 2.6 R connected to V_{EE}.

Series terminating resistors decrease noise immunity and slow rise and fall times, but can still be used if these effects are tolerable. In addition, care must be taken to avoid glitches in the threshold region of the waveform occurring at certain combinations of line length and series resistor value.

A single terminated wire running over a ground screen can be used for backpanel interconnections up to 4 or 5 inches in length, but terminated coaxial cables or terminated twisted pairs of wire are required for longer interconnections.

LINE DRIVING CAPABILITY – The 9500 series ECL circuits are capable of driving fairly long lines if the previous recommendations are followed. 50 ohm coaxial cables 10 feet in length or longer and properly terminated may be driven with almost no degradation in the waveform. The normal delay due to the finite speed of the signal traveling down the cable will be encountered in addition to a slight decrease in signal swing. This decrease caused by the attenuation of the cable (about 40 mV for 10 feet of 50 ohm coax) will lower the noise immunity of the receiving circuit by the same amount. Care must be exercised to ensure the ground potentials at the driving and receiving ends of a line are equal and no differential noise is present.

PHYSICAL DIMENSIONS
16 LEAD SSI DUAL IN-LINE



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin plated kovar
Package weight is 2.0 grams
*The .037/.027 dimensions does not apply to the corner leads

9505

FOUR WIDE-OR AND/NAND (NOR-OR) GATE

FAIRCHILD TEMPERATURE COMPENSATED ECL

GENERAL DESCRIPTION – The ECL 9505 is a temperature compensated OR-AND gate that achieves in slightly over one basic gate delay, the AND of four different ORed functions.

The NOR outputs of the four OR gates are ORed to derive the OR-NAND (NOR-OR) function.

This element is useful in the design of Arithmetic Logic Units for construction of adders, multipliers, comparitors, etc. Just two 9505's will implement a full carry adder function.

FEATURES:

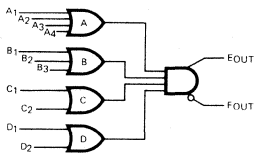
- **HIGH SPEED . . . 2.7 ns OR-AND, 2.5 ns OR-NAND**
- **COMPLEX LOGIC FUNCTION REDUCES PACKAGE COUNT**
- **WIRE OR CAPABILITY**
- **50 Ω LINE DRIVING CAPABILITY**
- **INTERNAL 2 k PULL DOWN RESISTORS**
- **TEMPERATURE COMPENSATED**
- **SEPARATE V_{CC} PINS - ELIMINATE NOISE COUPLING**

PIN NAMES

A_N = 4 Inputs to OR Gate A
B_N = 3 Inputs to OR Gate B
C_N = 2 Inputs to OR Gate C
D_N = 2 Inputs to OR Gate D
E_{OUT} = AND Output of Gates A, B, C and D
F_{OUT} = NAND Output of Gates A, B, C and D

ORDER INFORMATION – Specify U6B9505XXX for 16 pin Dual In-Line Package where XXX is 59X for the 0°C to 75°C temperature range.

LOGIC SYMBOL



CONNECTION DIAGRAM
DIP (TOP VIEW)

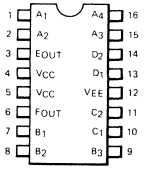
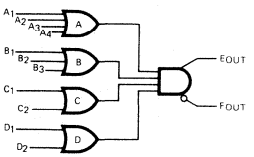


Fig. 2.

LOGIC DIAGRAM



$E = A_N \cdot B_N \cdot C_N \cdot D_N$
$F = A_N \cdot B_N \cdot C_N \cdot D_N$

Where:

$A_N = A_1 + A_2 + A_3 + A_4$,
$B_N = B_1 + B_2 + B_3$
$C_N = C_1 + C_2$
$D_N = D_1 + D_2$

Fig. 3.

FUNCTIONAL DESCRIPTION – The 9505 OR-AND gate combines two of the most often used functions in logic into one package to obtain maximum utilization of power and pin connections with minimum logic delay.

The AND of four OR gates is obtained by connecting the four collectors of the OR gates together with one collector load resistor and one emitter follower output device. High speed and temperature compensated output levels are maintained by a special controlled clamp at the collectors. This prevents saturation and loss of noise immunity as different logic conditions are encountered.

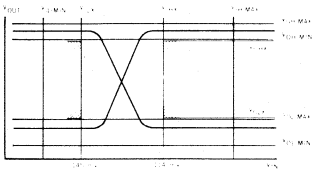
The NAND (NOR-OR) function is obtained by connecting the four NOR output emitter followers together at the output. In this way maximum speed is maintained with optimum use of package pins. This output is temperature compensated by an additional pulldown transistor on each NOR gate collector.

Selection of this input configuration of the four OR-NOR gates gives maximum utilization of available pins and meets almost all of the system requirements for this type of logic block.

DC ELECTRICAL CHARACTERISTICS (Operating Temperature: T_A = 0°C to 75°C, V_{CC} = GND, V_{EE} = −5.2 V

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS	
		MIN.	TYP.	MAX.			
V_{OH}	Output Voltage High	−920	−850	−770	mV	F.O. = 1 Gate	$V_{IN} = V_{IH}$ = −900 mV
		−960	−885	−790	mV	F.O. = 5 Gates	
		−995	−905	−805	mV	R_L = 50 Ω to −2.0 V	
$V_{OL(OR-AND)}$	Output Voltage Low	−2055	−1750	−1595	mV	F.O. = 1 Gate	$V_{IN} = V_{IL}$ = −1700 mV
		−2055	−1760	−1630	mV	F.O. = 5 Gates	
		−2055	−1755	−1625	mV	R_L = 50 Ω to −2.0 V	
$V_{OL(OR-NAND)}$	Output Voltage Low	−1805	−1750	−1595	mV	F.O. = 1 Gate	$V_{IN} = V_{IH}$ = −900 mV
		−1825	−1760	−1630	mV	F.O. = 5 Gates	
		−1815	−1755	−1625	mV	R_L = 50 Ω to −2.0 V	
V_{OHX}	Output Voltage HIgh	−1005			mV	R_L = 50 Ω to −2.0 V	$V_{IN} = V_{IHX}$ = −1140 V for OR-AND $V_{IN} = V_{ILX}$ = −1450 V for OR-NAND
V_{OLX}	Output Voltage Low			−1615	mV	R_L = 50 Ω to −2.0 V	$V_{IN} = V_{ILX}$ = −1450 V for OR-AND $V_{IN} = V_{IHX}$ = −1140 V for OR-NAND
V_{IHX}	Input High Threshold Voltage	−1140			mV	Guaranteed Input High Voltage	
V_{ILX}	Input Low Threshold Voltage			−1450	mV	Guaranteed Input Low Voltage	
$I_{IN(1)}$	Input Current at V_{IH}			3.15	mA	V_{IH} = −900 mV to Each Input Sequentially	
$I_{IN(0)}$	Input Current at V_{IL}			2.40	mA	V_{IL} = −1700 mV to Each Input Sequentially	
I_{PS}	Power Supply Current	43	61	81	mA	All Inputs Open	

Fig. 4. **NOISE MARGIN SPECIFICATION POINTS**

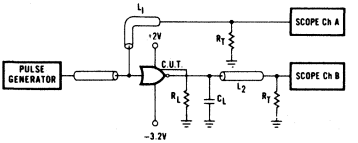


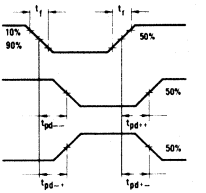
Corner points indicated on the transfer characteristics represent the worst case points (thresholds) at which the device will start to switch. The values V_{ILX} and V_{IHX} define the maximum width of the transition region.

AC ELECTRICAL CHARACTERISTICS (Operating Temperature: T_A = 0°C to 75°C, V_{CC} = GND, V_{EE} = −5.2 V)

SYMBOL	CHARACTERISTIC	LIMITS						UNITS	CONDITIONS
		0°C	25°C			75°C			
		TYP	MIN	TYP	MAX	MIN	TYP	MAX	
	Propagation Delay								
	t_{pd++}	2.8		2.8	3.7		2.8		ns	R_L = 50 Ω to −2.0 V
t_{pd}	t_{pd--}	2.5		2.5	3.3		2.5		ns	C_L = 5.0 pF
	t_{pd+-}	2.4		2.4	3.2		2.4		ns	$t_r = t_f$ = 2.5 ns
	t_{pd-+}	2.4		2.4	3.2		2.4		ns	See Fig. 5
I_T	Transient Input Current			2.0	3.5				mA	See Fig. 6

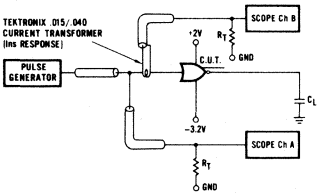
Fig. 5. SWITCHING TIME TEST CIRCUIT AND WAVEFORM

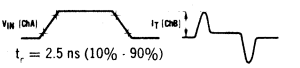




L_1 and L_2 = equal length 50 Ω impedance lines
$R_L = R_T$ = 50 Ω Termination of Scope
C_L = Jig and Stray Capacitance < 5.0 pF
$t_r = t_f$ = 2.5 ns (10% - 90%) Jig setup with no circuit under test
$V_{CC} = V_{CC}$ (AUX) = +2.0 V
V_{EE} = −3.2 V

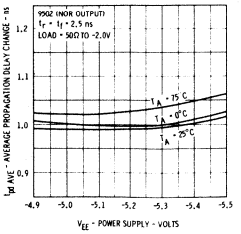
Fig. 6. TRANSIENT INPUT CURRENT TEST CIRCUIT AND WAVEFORMS





This test provides a measure of the average value of C_{IN}; also current mismatch in the line.
$V_{CC} = V_{CC}$ (AUX) = +2.0 V
V_{EE} = −3.2 V

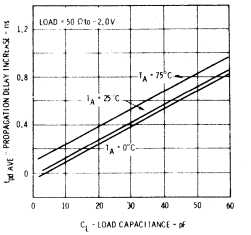
TYPICAL AVERAGE PROPAGATION DELAY CHANGE VERSUS POWER SUPPLY



$$t_{pd\ AVE} = \frac{t_{pd\ rising} + t_{pd\ falling}}{2}$$

Reference:
AC Electrical Characteristic

TYPICAL PROPAGATION DELAY INCREASE VERSUS LOAD CAPACITANCE t_{pd} AVE (OR output)



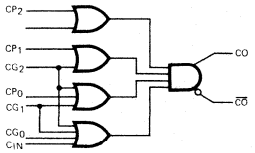


Fig. 7. **LOGIC EQUATIONS** – The 9505 is useful in implementing a large variety of logic equations with minimum propagation delay. As an example the equation for carry lookahead is:

$CO = CG_2+CG_1 \cdot CP_2+CG_0 \cdot CP_1 \cdot CP_2+C_{IN} \cdot CP_0 \cdot CP_1 \cdot CP_2$

An equivalent form of this equation is:

$\overline{CO} = \overline{CP_2}+\overline{CG_2} \cdot \overline{CP_1}+\overline{CG_1} \cdot \overline{CG_2} \cdot \overline{CP_0}+\overline{CG_0} \cdot \overline{CG_1} \cdot \overline{CG_2} \cdot \overline{C_{IN}}$

By DeMorgan's theorem this may be written as:

$CO = CP_2 \cdot (CG_2+CP_1)\,(CG_1+CG_2+CP_0)\,(CG_0+CG_1+CG_2+C_{IN})$

Fig. 8. **ADDER** – Two 9505's may be used to build a fast full adder.

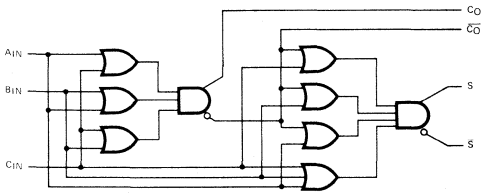


Fig. 9. **COMPARE CIRCUIT** – 9505's may be used to generate a compare circuit capable of handling two bit per 9505.

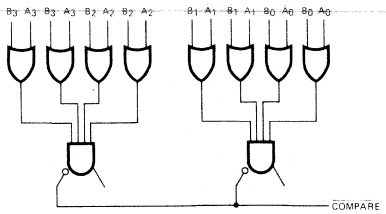
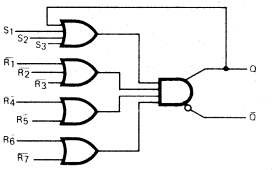
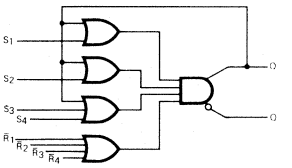


Fig. 10. **LATCHES** – A 9505 may be used to store one bit of information by connecting it as a latch. Many configurations of set and reset inputs are possible.

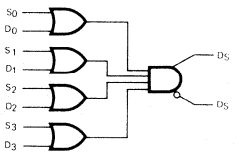


$S = S_1 + S_2 + S_3$ $\quad \bar{R} = (\bar{R}_1 + \bar{R}_2 + \bar{R}_3)(\bar{R}_4 + \bar{R}_5)(\bar{R}_6 + \bar{R}_7)$ $\quad R = R_1 \cdot R_2 \cdot R_3 + R_4 \cdot R_5 + R_6 \cdot R_7$



$S = S_1 \cdot S_2 \cdot (S_3 + S_4)$ $\quad \bar{R} = (\bar{R}_1 + \bar{R}_2 + \bar{R}_3 + \bar{R}_4)$ $\quad R = R_1 \cdot R_2 \cdot R_3 \cdot R_4$

Fig. 11. **MILTIPLEXERS** – A 9505 may be used as a 4 input multiplexer. A logic "0" on the selected S_N will allow D_N to be selected. All other S_N must be a "1".



INTERCONNECTION RECOMMENDATIONS

All high speed ECL circuits demand that special precautions be taken for optimum system performance. A ground plane must be provided for a good, low impedance, ground current return path and to transform interconnections into microstrip transmission lines. The voltage supply line should be well decoupled with small ceramic capacitors throughout each card between V_{EE} and the ground plane and by including at least one larger tantalum capacitor per card.

Typical microstrip lines have a characteristic impedance between 50 and 150 ohms with the lower being more desirable in ECL systems. For local interconnects the internal 2 kΩ resistors provide adequate termination but for optimum performance lines longer than 6 or 8 inches in length should be terminated in their characteristic impedance.

Lines up to 12 inches may be left unterminated if a degraded waveform can be tolerated with the resultant decrease in speed and increase in ringing.

Microstrip interconnections may be terminated by a resistor to a −2 volt supply. Alternately, a 2 resistor divider network may be used with R_1 = 1.6 R connected to ground and R_2 = 2.6 R connected to V_{EE}.

Series terminating resistors decrease noise immunity and slow rise and fall times, but can still be used if these effects are tolerable. In addition, care must be taken to avoid glitches in the threshold region of the waveform occurring at certain combinations of line length and series resistor value.

A single terminated wire running over a ground screen can be used for backpanel interconnections up to 4 or 5 inches in length, but terminated coaxial cables or terminated twisted pairs of wire are required for longer interconnections.

LINE DRIVING CAPABILITY

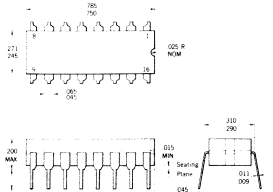
The 9500 series ECL circuits are capable of driving fairly long lines if the previous recommendations are followed. 50 Ω coaxial cables 10 feet in length or longer and properly terminated may be driven with almost no degradation in the waveform. The normal delay due to the finite speed of the signal traveling down the cable will be encountered in addition to a slight decrease in signal swing. This decrease caused by the attenuation of the cable (about 40 mV for 10 feet of 50 Ω coax) will lower the noise immunity of the receiving circuit by the same amount. Care must be exercised to ensure the ground potentials at the driving and receiving ends of a line are equal and no differential noise is present.

ABSOLUTE MAXIMUM RATINGS (above which useful life may be impaired)

Storage Temperature	−65°C to +150°C
Junction Temperature	+150°C
Supply Voltage V_{EE} (Continuous)	−6 Volts
Supply Voltage V_{EE} (Pulsed)	−8 Volts
Input Voltage	GND to V_{EE} (max)
Output Current	40 mA

PACKAGE INFORMATION

6B–16 LEAD SSI DUAL IN-LINE



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin plated kovar
Package weight is 2.0 grams
* The .037/.027 dimensions does not apply to the corner leads

9507
QUAD 2-INPUT AND/8-INPUT NAND
FAIRCHILD TEMPERATURE COMPENSATED ECL

GENERAL DESCRIPTION – The 9507 is a Temperature Compensated ECL gate that combines four 2-input AND gates with one 8-input NAND gate. By use of series gating and collector and emitter dotting these logical functions are achieved within approximately one gate delay.

To prevent excessive loading on the inputs the 8-input NAND function is derived by ORing the complement outputs of the four AND gates. (See logic diagram below.)

The 9507 may be used whenever a 2 to 8-input NAND function is required by connecting the unused inputs to a standard HIGH level. Higher average speed can be achieved by using the A_N inputs wherever possible and connecting a standard HIGH level to the B_N inputs, although this difference is only 0.5 to 0.8 ns.

Generally for a single 2 to 4 input AND/NAND function the 9505 should be considered.

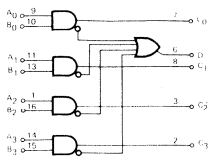
- **HIGH SPEED . . . 3.2 ns DELAY**
- **8 INPUT LOGIC NAND IN ONE GATE DELAY**
- **SEPARATE NON-STANDARD ECL LOGIC FUNCTION – 4 DUAL AND GATES**
- **HIGHER SYSTEM RELIABILITY AND LOWER COST BY ELIMINATING COMPLEX WIRING OF OR/NOR GATES**
- **SEPARATE CURRENT SWITCH & EMITTER FOLLOWER V_{CC} PINS**
- **TEMPERATURE COMPENSATION**
- **INTERNAL PULLDOWN RESISTORS**

PIN NAMES

A_N	Input of 2-Input AND Gate, also Input of 8-Input NAND Gate
B_N	Input of 2-Input AND Gate, also Input of 8-Input NAND Gate
C_N	Output of A_N and B_N
D	Output of 8-Input NAND Gate – 4 Unit Loads

ORDER INFORMATION – Specify U6B950759X for 16 pin Dual In-Line package and 0°C to +75°C temperature range.

LOGIC DIAGRAM



NOTE: Output pin 6 has an output loading factor of 4 loads. Maximum unterminated load is 13 D.C. loads or 7 loads + 50Ω line.

Fig. 3

LOGIC SYMBOL

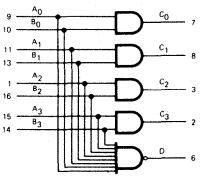
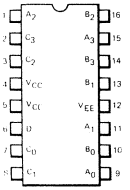


Fig. 1

CONNECTION DIAGRAM
DIP (TOP VIEW)



Pins 4 and 4 = V_{CC} = GND
Pin 12 = V_{EE} = –5.2 V

Fig. 2

FAIRCHILD SEMICONDUCTOR

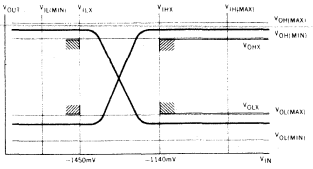
FUNCTIONAL DESCRIPTION – The 9507 AND functions are obtained by the series gating of two ECL current switches, sharing the same current source. This technique minimizes the power but results in slightly different path delays for the two inputs. The A inputs are faster by about 0.6 ns.

The NAND functions are obtained within the delay of the AND by OR dotting of the complement outputs of the AND gates.

D.C. ELECTRICAL CHARACTERISTICS – Over Operating Temperature Range (T_A = 0°C to 75°C, V_{EE} = –5.2 V)

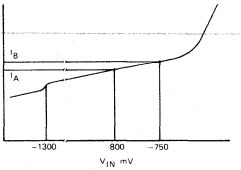
SYMBOL	CHARACTERISTIC	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	CONDITIONS	
V_{OH}	Output HIGH Voltage AND Outputs	–905 –945 –980	–850 –890 –925	–785 –835 –870	mV	FO = 1 Gate FO = 5 Gates 50 Ω to –2 V	V_{IN} = –0.900 V
V_{OH}	Output HIGH Voltage NAND Output	–945 –965 –1000	–855 –875 –900	–765 –785 –800	mV	FO = 1 Gate FO = 5 Gates 50 Ω to –2 V	V_{IN} = –0.900 V
V_{OL}	Output LOW Voltage AND Outputs	–1755 –1795 –1785	–1670 –1710 –1700	–1585 –1625 –1615	mV	FO = 1 Gate FO = 5 Gates 50 Ω to –2 V	V_{IN} = –1.700 V
V_{OL}	Output LOW Voltage NAND Output	–1740 –1750 –1750	–1655 –1665 –1665	–1570 –1580 –1580	mV	FO = 1 Gate FO = 5 Gates 50 Ω to –2 V	V_{IN} = –1.700 V
V_{OHC}	Output HIGH Corner Point AND Outputs (See Fig. 4)	–915 –955 –990			mV	FO = 1 Gate FO = 5 Gates 50 Ω to –2 V	$V_{IN} = V_{IHX}$ $V_{IN} = V_{ILX}$
V_{OHC}	Output HIGH Corner Point NAND Output (See Fig. 4)	–955 –975 –1010			mV	FO = 1 Gate FO = 5 Gates 50 Ω to –2 V	$V_{IN} = V_{IHX}$ $V_{IN} = V_{ILX}$
V_{OLC}	Output LOW Corner Point AND Outputs (See Fig. 4)			–1575 –1615 –1605	mV	FO = 1 Gate FO = 5 Gates 50 Ω to –2 V	$V_{IN} = V_{ILX}$ $V_{IN} = V_{IHX}$
V_{OLC}	Output LOW Corner Point NAND Output (See Fig. 4)			–1560 –1570 –1570	mV	FO = 1 Gate FO = 5 Gates 50 Ω to –2 V	$V_{IN} = V_{ILX}$ $V_{IN} = V_{IHX}$
V_{IHX}	Input HIGH Level	–1140			mV	Guaranteed Input HIGH Threshold Voltage	
V_{ILX}	Input LOW Level			–1450	mV	Guaranteed Input LOW Threshold Voltage	
$I_{IN(H)}$	Input Current at V_{IH}		2.25	3.15	mA	V_{IN} = –900 mV to Each Input Sequentially	
$I_{IN(L)}$	Input Current at V_{IL}		1.75	2.40	mA	V_{IN} = –1700 mV to Each Input Sequentially	
I_{PS}	Power Supply Current		61	84	mA	V_{EE} = –5.2 V, All Inputs Open	
ΔI_N	Input Saturation Current (See Fig. 5)			50	μA	$\Delta I_{IN} = I_B - I_A$, $I_A = I_{IN}$ @ V_{IN} = 800 mV $I_B = I_{IN}$ @ V_{IN} = 750 mV	

Fig. 4 NOISE MARGIN SPECIFICATION POINTS



Corner points indicated on the transfer characteristics represent the worst case points (thresholds) at which the device will start to switch. The values V_{ILX} and V_{IHX} define the maximum width of the transition region.

Fig. 5 INPUT SATURATION TEST



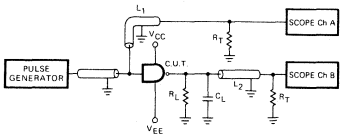
This test insures that the input transistor is not in saturation at V_{IN} = 750 mV. This represents a worst case condition with the driving gate at V_{OH} (min) = 750 mV (ie. for T_A = 75°C this is equivalent to driving gate into FO = 1 with its power supply at –5%).

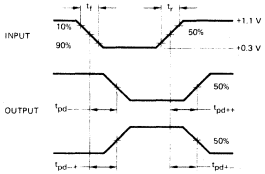
Saturation is defined as no increase in collector current for 20% increase in base drive current I_R. The effect is to increase t_{pd}.

AC ELECTRICAL CHARACTERISTICS (Operating Temperature: T_A = 0°C to 75°C, V_{CC} = GND, V_{EE} = −5.2 V)

SYMBOL	CHARACTERISTIC	LIMITS							UNITS	CONDITIONS
		0°C	25°C			75°C				
		TYP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
t_{pd}	Propagation Delay t_{pd} ± A Inputs	2.6		2.6	3.5		2.7		ns	R_L = 50 Ω to −2.0 V
	t_{pd} ± B Inputs	3.2		3.2	4.3		3.3		ns	C_L <5.0 pF
t_r, t_f	Rise and Fall Time	3.0	1.5	3.0	4.5		3.0		ns	t_r = t_f = 2.5 ns See Fig. 6
I_T	Transient Input Current			2.5	3.5				mA	See Fig. 7

Fig. 6. SWITCHING TIME TEST CIRCUIT AND WAVEFORM

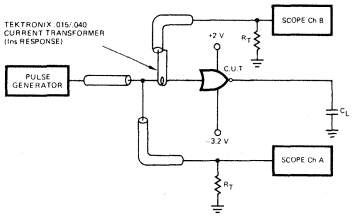


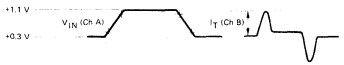


L_1 and L_2 = equal length 50 Ω impedance lines
R_L = R_T = 50 Ω Termination of Scope
C_L = Jig and Stray Capacitance < 5.0 pF
t_r = t_f = 2.5 ns (10% - 90%)

V_{CC} = V_{CC} (AUX) = +2.0 V
V_{EE} = −3.2 V

Fig. 7. TRANSIENT INPUT CURRENT TEST CIRCUIT AND WAVEFORMS

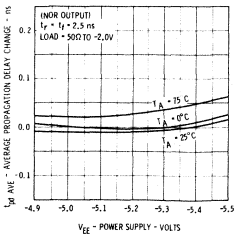




t_r = 2.5 ns (10% - 90%)

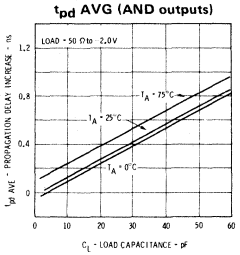
This test provides a measure of the average value of C_{IN}; also current mismatch in the line.
V_{CC} = V_{CC} (AUX) = +2.0 V
V_{EE} = −3.2 V

TYPICAL AVERAGE PROPAGATION DELAY CHANGE VERSUS POWER SUPPLY



$$t_{pd}\ AVG = \frac{t_{pd}\ rising + t_{pd}\ falling}{2}$$

TYPICAL PROPAGATION DELAY INCREASE VERSUS LOAD CAPACITANCE t_{pd} AVG (AND outputs)

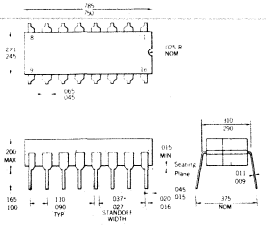


ABSOLUTE MAXIMUM RATINGS (above which useful life may be impaired)

Storage Temperature	−65°C +150°C
Junction Temperature	+150°C
Supply Voltage V_{EE} (Continuous)	−6 Volts
Supply Voltage V_{EE} (Pulsed)	−8 Volts
Input Voltage	GND to V_{EE} (max)
Output Current	40 mA

PACKAGE INFORMATION

6B — 16 Lead SSI Dual In-Line Package



NOTES
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin plated kovar
Package weight is 2.0 grams
The .037/.027 dimensions does not apply to the corner leads.

95H10

BCD SYNCHRONOUS DECADE COUNTER
FAIRCHILD TEMPERATURE COMPENSATED ECL

GENERAL DESCRIPTION

The 95H10 is a high speed synchronously presettable 8421 BCD decade counter. It is a synchronously presettable, multifunction MSI building block useful for a large number of counting, digital integration, and conversion applications. Up to 9 decades can be cascaded with no speed degradation using the standard 95OO gates. With 95HOO gates a multidecade synchronous load counter to over 15O MHz can be built. Typical count frequency is over 18O MHz.

Features include assertion inputs and outputs on each of the 4 master slave counting flip flop. Terminal count is generated internally in a manner that allows synchronous loading at nearly the speed of the basic counter. When the parallel load feature is not needed, the CE input may be used as a clock gate regardless of clock input level. Availability of all these features on one chip significantly improves the reliability, performance and power consumption of high speed systems.

- HIGH SPEED COUNT - 18O MHz TYPICAL COUNT FREQUENCY
- HIGH SPEED SYNCHRONOUSLY LOAD - OVER 15O MHz SYNCHRONOUS LOAD FREQUENCY
- INTERNAL COUNT ENABLE
- ASYNCHRONOUS MASTER RESET
- 5O Ω OR FANOUT OF 1O ON EACH OUTPUT WIRE OR CAPABILITY
- SEPARATE CURRENT SWITCH EMITTER FOLLOWER V_{CC} PINS - ELIMINATE NOISE COUPLING
- TEMPERATURE COMPENSATION
- INTERNAL PULL DOWN FOR DIRECT LOW COST WIRING
- SINGLE -5.2 VOLT POWER SUPPLY
- HERMETIC CERAMIC 16 PIN DIP
- COMPLEX MULTI-GATE CHIP REDUCES PACKAGE COUNT AND POWER

PIN NAMES

P_E	PARALLEL LOAD ENABLE, LOADS LOW
P_N	PARALLEL INPUTS
C_P	CLOCK INPUT, CLOCKS ON POSITIVE GOING TRANSITION
C_E	COUNT ENABLE, LOW TO COUNT
M_R	MASTER RESET, FORCES ALL Q-OUTPUTS LOW
T_C	TERMINAL COUNT, LOW WITH COUNT OF '9' HIGH OTHERWISE

ORDER INFORMATION - SPECIFY U6B95H10XX FOR 16 PIN DUAL IN-LINE PACKAGE WHERE XX IS 9X FOR 0°C TO +75°C TEMPERATURE RANGE.

FAIRCHILD
SEMICONDUCTOR

ELECTRICAL SPECS D. C. $0^{\circ}C - 75^{\circ}C$ $V_{EE} = -5.2V$

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
V_{OH}	OUTPUT HIGH LEVEL	-920	-860	-800	mV	F. O. = 1
V_{OH}	OUTPUT HIGH LEVEL	-970	-910	-850	mV	F. O. = 5
V_{OH}	OUTPUT HIGH LEVEL	-1010	-950	-890	mV	50Ω to -2. 0V + 5 pf to V_{CC}
V_{OL}	OUTPUT LOW LEVEL	-1780	-1690	-1600	mV	F. O. = 1
V_{OL}	OUTPUT LOW LEVEL	-1830	-1740	-1650	mV	F. O. = 5
V_{OL}	OUTPUT LOW LEVEL	-1810	-1720	-1630	mV	50Ω to -2. 0V + 5 pf to V_{CC}
V_{IHX}	INPUT THRESHOLD HIGH	-1140	-	-	mV	MIN. INPUT VOLTAGE FOR HIGH LOGIC
V_{ILX}	INPUT THRESHOLD LOW	-	-	-1450	mV	MAX. INPUT VOLTAGE FOR LOW LOGIC
I_{IN} (HIGH)	INPUT CURRENT HIGH		2. 25	3. 16	mA	V_{IN} = -900 mV
I_{IN} (LOW)	INPUT CURRENT LOW		1. 75	2. 46	mA	V_{IN} = -1700 mV
I_{PS}	POWER SUPPLY CURRENT	-	100	-	mA	

ELECTRICAL SPECS A. C.

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
Tpd	CLOCK TO OUTPUT (AII)		3. 6		nS	
Tpd	CLOCK TO T_C		3. 6		nS	
Tpd	M_R TO OUTPUT		5. 0		nS	
Tpcd	P_E PRIOR TO CLOCK		1. 5		nS	
Tpch	P_E HOLD AFTER CLOCK		1. 0		nS	
Tecd	C_E PRIOR TO CLOCK		1. 5		nS	C_E MAY ONLY CHANGE WHEN C_P IS HIGH
Tech	C_E HOLD AFTER CLOCK		1. 0		nS	
Tcpw	CLOCK PULSE WIDTH		2. 5		nS	
Trw	RESET PULSE WIDTH		4		nS	
fc	COUNT FREQUENCY		160		MHz	
trtf	RISE, FALL TIME	1. 5	2. 5		nS	
It	TRANSIANT INPUT CURRENT		2. 5	3. 5	mA	

LOGIC SYMBOL

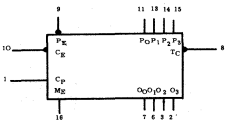


FIG 1

CONNECTION DIAGRAM DIP (TOP VIEW)

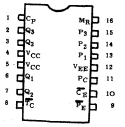


FIG 2

95H16

4-BIT SYNCHRONOUS BINARY COUNTER

FAIRCHILD TEMPERATURE COMPENSATED ECL

GENERAL DESCRIPTION

The 95H16 is a high speed synchronously presettable 4-Bit Binary counter. It is synchronously presettable, multifunction MSI building block useful for a large number of counting, digital, integration, and conversion applications. Up to 9 devices can be cascaded with no speed degradation using the standard 95OO gates. With 95HOO gates a multidecade synchronous load counter to over 15O MHz can be built. Typical count frequency is over 18O MHz.

Features include assertion inputs and outputs on each of the 4 master slave counting flip flop. Terminal count is generated internally in a manner that allows synchronous loading at nearly the speed of the basic counter. When the parallel load feature is not needed, the CE input may be used as a clock gate regardless of clock input level. Availability of all these features on one chip significantly improves the reliability, performance and power consumption of high speed systems.

- HIGH SPEED COUNT - 18O MHz TYPICAL COUNT FREQUENCY
- HIGH SPEED SYNCHRONOUSLY LOAD - OVER 15O MHz SYNCHRONOUS LOAD FREQUENCY
- INTERNAL COUNT ENABLE
- ASYNCHRONOUS MASTER RESET
- 5O Ω OR FANOUT OF 1O ON EACH OUTPUT WIRE OR CAPABILITY
- SEPARATE CURRENT SWITCH EMITTER FOLLOWER V_{CC} PINS - ELIMINATE NOISE COUPLING
- TEMPERATURE COMPENSATION
- INTERNAL PULL DOWN FOR DIRECT LOW COST WIRING
- SINGLE - 5.2 VOLT POWER SUPPLY
- HERMETIC CERAMIC 16 PIN DIP
- COMPLEX MULTI-GATE CHIP REDUCES PACKAGE COUNT AND POWER

PIN NAMES

P_E	PARALLEL LOAD ENABLE
P_N	PARALLEL INPUTS
C_P	CLOCK INPUT, CLOCKS ON POSITIVE TRANSITION
C_E	COUNT ENABLE, LOW TO COUNT
M_R	MASTER RESET, FORCES ALL OUTPUTS LOW
T_C	TERMINAL COUNT, LOW WITH 15(H,H,H,H,) HIGH OTHERWISE

ORDER INFORMATION - SPECIFY U6B95H16 XX FOR 16 PIN DUAL IN-LINE PACKAGE

WHERE XX IS 9X FOR 0°C TO +75°C TEMPERATURE RANGE

FAIRCHILD
SEMICONDUCTOR

ELECTRICAL SPECS D. C. $0^{\circ}C - 75^{\circ}C$ $V_{EE} = -5.2V$

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
V_{OH}	OUTPUT HIGH LEVEL	-920	-860	-800	mV	F.O. = 1
V_{OH}	OUTPUT HIGH LEVEL	-970	-910	-850	mV	F.O. = 5
V_{OH}	OUTPUT HIGH LEVEL	-1010	-950	-890	mV	50Ω to -2.0V+ 5 pf to V_{CC}
V_{OL}	OUTPUT LOW LEVEL	-1780	-1690	-1600	mV	F.O. = 1
V_{OL}	OUTPUT LOW LEVEL	-1830	-1740	-1650	mV	F.O. = 5
V_{OL}	OUTPUT LOW LEVEL	-1810	-1720	-1630	mV	50Ω to -2.0V+ 5 pf to V_{CC}
V_{IHX}	INPUT CURRENT HIGH	-1140	-	-	mV	MIN. INPUT VOLTAGE FOR "HIGH" LOGIC
V_{ILX}	INPUT CURRENT LOW	-	-	-1450	mV	MAX. INPUT VOLTAGE FOR "LOW" LOGIC
I_{IN} (HIGH)	INPUT CURRENT HIGH		2.25	3.16	mA	V_{IN} = -900 mV
I_{IN} (LOW)	INPUT CURRENT LOW		1.75	2.46	mA	V_{IN} = -1700 mV
I_{PS}	POWER SUPPLY CURRENT		100		mA	

ELECTRICAL SPECS A. C.

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
Tpd	CLOCK TO OUTPUT (AII)		3.6		nS	
Tpd	CLOCK TO T_C		3.6		nS	
Tpd	M_R TO OUTPUT		5.0		nS	
Tpcd	P_E PRIOR TO CLOCK		1.5		nS	
Tpch	P_E HOLD AFTER CLOCK		1.0		nS	
Tecd	C_E PRIOR TO CLOCK		1.5		nS	C_E MAY ONLY CHANGE
Tech	C_E HOLD AFTER CLOCK		1.0		nS	WHEN C_P IS HIGH
Tcpw	CLOCK PULSE WIDTH		2.5		nS	
Trw	RESET PULSE WIDTH		4		nS	
fc	COUNT FRQUENCY		160		MHz	
Trtf	RISE, FALL TIME	1.5	2.5		nS	
It	TRANSIANT INPUT CURRENT		2.5	3.5	mA	

LOGIC SYMBOL

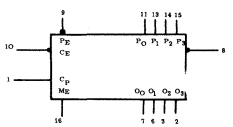


FIG 1

CONNECTION DIAGRAM DIP (TOP VIEW)

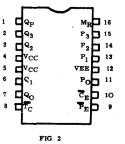


FIG 2

95L22 • 95L23 • 95L24

LOW POWER HIGH SPEED GATES

FAIRCHILD TEMPERATURE COMPENSATED ECL

GENERAL DESCRIPTION – The 95L22, 95L23 and 95L24 are low power temperature compensated ECL OR/NOR Gates employing a nonsaturating current switch, emitter follower configuration to achieve high speed. The elements are intended for the design of high speed central processors, terminals, instrumentation and digital communications systems.

All 9500 series elements incorporate a unique temperature compensation network. This insures that significant parameters such as logic levels, noise margin and speed remain relatively constant over a wide temperature range. High input impedance and open outputs allow effective usage of terminated line technology and large wired-OR ties. Package pin locations are chosen to reduce internal noise generation and crosstalk.

The devices are packaged in the hermetic CERAMIC, 16 pin Dual In-Line Package and specified for operation over the temperature range 0°C to 75°C.

- **VERY HIGH SPEED . . . 2.0 ns PER GATE**
- **LOW POWER DISSIPATION OF 20 mW/GATE (TYP.)**
- **SEPARATE CURRENT SWITCH AND EMITTER FOLLOWER V_{CC} PINS – ELIMINATES NOISE COUPLING**
- **TEMPERATURE COMPENSATION**
- **INTERNAL HI–Z INPUT PULLDOWN RESISTORS**
- **COMMON ENABLE INPUTS**
- **LOW CROSSTALK AND NOISE GENERATION**
- **EXTENSIVE WIRED–OR CAPABILITY**
- **50 Ω LINE DRIVING CAPABILITY**
- **COMPLEMENTARY OR/NOR OUTPUTS (95L22, 95L23)**
- **SINGLE –5.2 V POWER SUPPLY**
- **HERMETIC CERAMIC 16 PIN DUAL IN-LINE PACKAGE**

ORDER INFORMATION – Specify U6B95L22XXX for 16 pin Dual In-Line Package where XXX is 59X for the 0°C to +75°C temperature range for 95L22 gate. Substitute 95L23 or 95L24 for other elements.

CIRCUIT SCHEMATIC

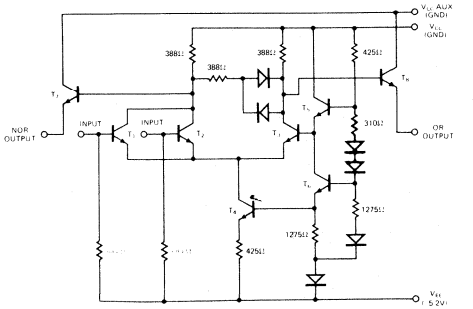
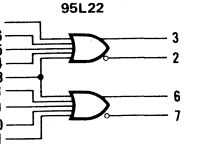


Fig. 1

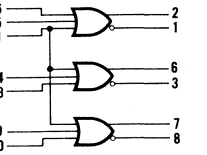
LOGIC DIAGRAM AND PIN CONNECTION

95L22



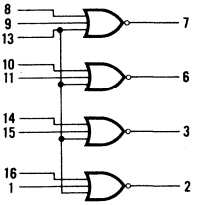
Dual 4 OR/NOR
(with enable)

95L23



Triple 2 OR/NOR
(with enable)

95L24



Quad 2 NOR
(with enable)

On all elements Pins 4 and 5 are circuit ground, V_{CC}. Pin 12 is V_{EE}, –5.2 V

Fig. 2

FUNCTIONAL DESCRIPTION — The 9500 Series Temperature Compensated ECL Gates are based on the current switch-emitter follower (CSEF), or emitter coupled (ECL), configuration of Figure 1. Additional circuit complexity compared with conventional ECL is incorporated to improve system operating characteristics. This includes temperature compensation networks to insure that logic levels and thresholds, set by the on chip bias driver, are essentially independent of temperature. A current source in the tail of the differential amplifier equalizes ONE and ZERO level noise margins by removing the NOR side saturation knee, and also improves saturation temperature dependency.

Defining logic "ONE" as V_{OH} = −960 mV (typ) and logic "ZERO" as V_{OL} = −1720 mV (typ), the elements perform the logical NOR and OR functions. The opposite definition specifies NAND/AND operation. All parameters specified in the characteristics are defined by the algebraic maximum and minimum limits.

Gate pin configurations are indicated in Fig. 2. An input enable line common to all gates in each package is provided for additional logical flexibility.

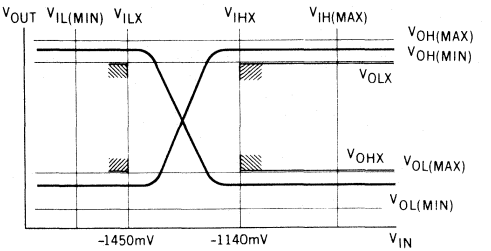
ABSOLUTE MAXIMUM RATINGS (above which useful life may be impaired)

Storage Temperature	−65° C to +150° C
Junction Temperature	+150° C
Supply Voltage V_{EE} (Continuous)	−6 Volts
Supply Voltage V_{EE} (Pulsed)	−8 Volts
Input Voltage	GND to V_{EE} (max)
Output Current	40 mA

D.C. ELECTRICAL CHARACTERISTICS (Operating Temperature Range: T_A = 0°C to 75°C, V_{CC} = GND, V_{EE} = −5.2 V)

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS	
		MIN.	TYP.	MAX.			
V_{OH}	Output Voltage High		−960		mV	50 Ω to −2.0 V	$V_{IN} = V_{IL}$ = −1700 mV for NOR Gate $V_{IN} = V_{IH}$ = −900 mV for OR Gate
V_{OL}	Output Voltage Low		−1720		mV	50 Ω to −2.0 V	$V_{IN} = V_{IL}$ = −1700 mV for OR Gate $V_{IN} = V_{IH}$ = −900 mV for NOR Gate
V_{OHX}	Output Voltage High at $V_{IN} = V_{IX}$ (Threshold)	−1040			mV	50 Ω to −2.0 V	See Fig. 3 $V_{IN} = V_{ILX}$ = −1450 mV for NOR Gate $V_{IN} = V_{IHX}$ = −1140 mV for OR Gate
V_{OLX}	Output Voltage Low at $V_{IN} = V_{IX}$ (Threshold)			−1615	mV	50 Ω to −2.0 V	See Fig. 3 $V_{IN} = V_{ILX}$ = −1450 mV for OR Gate $V_{IN} = V_{IHX}$ = −1140 mV for NOR Gate
V_{IHX}	Guaranteed Input High Threshold Voltage	−1140			mV		Guaranteed Input High Threshold Voltage
V_{ILX}	Guaranteed Input Low Threshold Voltage			−1450	mV		Guaranteed Input Low Threshold Voltage
$V_{IN(H)}$	Input Current High		0.14	0.30	mA		V_{IN} = −900 mV to Common Enable Input
$V_{IN(H)}$	Input Current High		0.06	0.20	mA		V_{IN} = −900 mV to Other Inputs Sequentially
$V_{IN(L)}$	Input Current Low		.035	.125	mA		V_{IN} = −1700 mV to Each Input Sequentially
I_{PS}	Power Supply Current 95L22 95L23 95L24	 7.0 9.0 11	 10.5 13 16	 15 18 22	mA		V_{EE} = −5.2 V, V_{CC} = GND All Inputs and Outputs Open

NOISE MARGIN SPECIFICATION POINTS



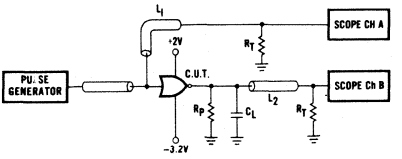
Corner points indicated on the transfer characteristics represent the worst case points (thresholds) at which the device will start to switch. The values V_{ILX} and V_{IHX} define the maximum width of the transition region.

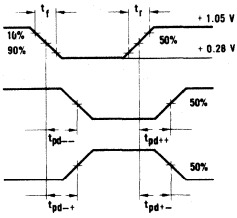
Fig. 3

AC ELECTRICAL CHARACTERISTICS (T_A = 0°C to 75°C)

SYMBOL	CHARACTERISTICS	LIMITS 0°C TYP.	LIMITS 25°C MIN.	LIMITS 25°C TYP.	LIMITS 25°C MAX.	LIMITS 75°C TYP.	UNITS	CONDITIONS
t_{pd}	Propagation Delay							
	10% – 50%						ns	See Fig. 4
	t_{pd} – –	2.0		2.0	3.0	2.2		P_L = 50 Ω to –2 V
	t_{pd} + +	2.0		2.0	3.0	2.2		C_L <5 pF
	t_{pd} – +	2.0		2.0	3.0	2.2		$t_r = t_f$ = 2.2 ns (10 – 90%)
	t_{pd} + –	2.0		2.0	3.0	2.2		
t_f	Fall Time 10% – 90%	3.0		3.0	4.5	3.0	ns	
t_r	Rise Time 10% – 90%	3.0		3.0	4.5	3.0		

SWITCHING TIME TEST CIRCUIT AND WAVEFORM





$t_r = t_f$ = 2.2 ns (10% - 90%)
Jig setup with no circuit under test.
$V_{CC} = V_{CC(AUX)}$ = +2.0 V
V_{EE} = –3.2 V

L_1 and L_2 = equal length 50 Ω impedance lines
$R_L = R_T$ = 50 Ω Termination of Scope C
C_L = Jig and Stray Capacitance <5.0 pF

Logic levels for Fig. 5 is nominal values at 50 Ω fanout determined by indicated power supplies. These values chosen to permit use of scope 50 Ω termination to ground.

Decoupling 0.1 μF from GND to V_{EE}.

Fig. 4

APPLICATION

INTERCONNECTION RECOMMENDATIONS – All high speed ECL circuits demand that special precautions be taken for optimum system performance. A ground plane must be provided for a good, low impedance, ground current return path and to transform interconnections into microstrip transmission lines. The voltage supply line should be well decoupled with small ceramic capacitors throughout each card between V_{EE} and the ground plane and by including at least one larger tantalum capacitor per card.

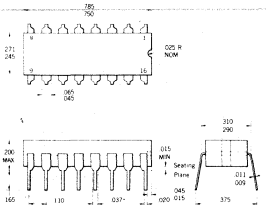
Typical microstrip lines have a characteristic impedance between 50 and 150 ohms with the lower being more desirable in ECL systems. Microstrip interconnections may be terminated by a resistor to a −2 volt supply. Alternately, a 2 resistor divider network may be used with R_1 = 1.6 R connected to ground and R_2 = 2.6 R connected to V_{EE}.

The high impedance 95L00 devices may be wired using series type termination, but must have additional 510Ω resistors from each output to V_{EE} or terminate through the appropriate value resistor −2.00 volts. The high impedance inputs allow high fanouts, and slight (<3 ns) and open outputs allow wire-ORing to greater than 30 with degradation. Care must be taken to avoid glitches in the threshold region of the waveform occuring at certain combinations of line length and series resistor value.

A single terminated wire running over a ground screen can be used for backpanel interconnections up to 4 or 5 inches in length, but terminated coaxial cables or terminated twisted pairs of wire are required for longer interconnections.

LINE DRIVING CAPABILITY – The 9500 series ECL circuits are capable of driving fairly long lines if the previous recommendations are followed. 50 ohm coaxial cables 10 feet in length or longer and properly terminated may be driven with almost no degradation in the waveform. The normal delay due to the finite speed of the signal traveling down the cable will be encountered in addition to a slight decrease in signal swing. This decrease caused by the attenuation of the cable (about 40 mV for 10 feet of 50 ohm coax) will lower the noise immunity of the receiving circuit by the same amount. Care must be exercised to ensure the ground potentials at the driving and receiving ends of a line are equal and no differential noise is present.

PHYSICAL DIMENSIONS
16 LEAD SSI DUAL IN-LINE



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin plated kovar
Package weight is 2.0 grams
*The .037/.027 dimensions does not apply to the corner leads

9528

HIGH SPEED DUAL D FLIP-FLOP

FAIRCHILD TEMPERATURE COMPENSATED ECL

GENERAL DESCRIPTION — The 9528 is a high speed, temperature compensated ECμL dual D (data) flip-flop compatible with all other members of the 9500 series of ECμL circuits. The device is versatile and permits easy implementation of high speed counters, registers, and control circuits.

All 9500 series elements incorporate a unique temperature compensation network. This insures that significant parameters such as logic levels, noise margins and speed remain relatively constant over a wide temperature range. Input and output two kilohm pulldown resistors eliminate the necessity for external termination of lines up to six or eight inches and permit unused inputs to be left open. Package pin locations are chosen to reduce internal noise generation and crosstalk.

The device is packaged in the hermetic ceramic 16 pin dual in-line package and specified for operation over the temperature range 0°C to +75°C.

- **160 MHz OPERATION**
- **SEPARATE CURRENT SWITCH AND EMITTER FOLLOWER V_{CC} PINS — ELIMINATES NOISE COUPLING**
- **TEMPERATURE COMPENSATION**
- **INTERNAL PULLDOWN RESISTORS**
- **MASTER-SLAVE CIRCUIT**
- **SEPARATE DIRECT SET AND CLEAR INPUTS**
- **BOTH COMMON AND SEPARATE CLOCK INPUTS**
- **WIRED-OR CAPABILITY ON OUTPUTS**
- **50 Ω LINE DRIVING CAPABILITY**
- **SINGLE —5.2 VOLT POWER SUPPLY**
- **HERMETIC CERAMIC 16 PIN DUAL IN-LINE PACKAGE**

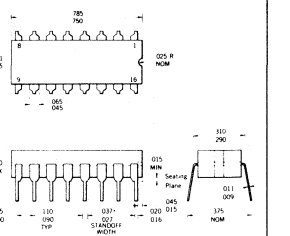
ABSOLUTE MAXIMUM RATINGS (above which useful life may be impaired)

Storage Temperature	−65°C to +150°C
Junction Temperature	+150°C
Supply Voltage V_{EE} (Continuous)	−6.0 Volts
Supply Voltage V_{EE} (Pulsed)	−8.0 Volts
Input Voltage	GND to V_{EE} (max)
Output Current	40 mA

ORDER INFORMATION

Specify U6B9528XXX for 16 pin Dual In-Line Package where XXX is 59X for the 0°C to +75°C temperature range for 9528 flip-flop.

PHYSICAL DIMENSIONS
16 Lead Dual In-Line



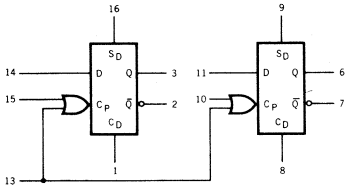
NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin plated kovar
Package weight is 2.0 grams
The .027/.037 dimensions does not apply to the corner leads

FUNCTIONAL DESCRIPTION — The 9528 Dual D (data) Flip-Flop uses the non-saturating, current switch-emitter follower circuit configuration to achieve high speed. In addition series gating and other current mode design techniques are incorporated to implement the circuits with minimum propagation delays and minimum power dissipation.

Each D Flip-Flop consists of both a master and a slave. While the clock is LOW the slave is held steady, but the information on the D input is permitted to enter the master. The next clock transition from LOW to HIGH locks the master in its present state making it insensitive to the D input and connects the slave to the master causing the new information to be reflected on the outputs. The following clock transition from HIGH to LOW again locks the slave and permits information to flow into the master. Logic races are avoided by offsetting the master and slave thresholds to avoid simultaneous switching when low speed edges are encountered in the system.

The internal clock is the OR of two clock inputs, one common to both flip-flops. The outputs will only switch following a LOW to HIGH transition of the ORed clock (unless the direct set or clear inputs are activated). The ORed clock permits the use of one input as a clock pulse input and the other as an active low enable. If one clock input is held HIGH, clock pulses on the other input will not be seen by the flip-flop. To maintain synchronous operation, however, the clock input used as an enable should only be changed while the clock is HIGH.

Fig. 1 — LOGIC DIAGRAM



V_{CC} = GND (Pins 4 & 5)
V_{EE} = −5.20 V (Pin 12)

TRUTH TABLE

SYNCHRONOUS OPERATION

D TABLE	
D_n	$Q_n + 1^*$
L	L
H	H
$^*S_D$ - C_D = Low	

ASYNCHRONOUS OPERATION

S_D - C_D TABLE			
C_D	S_D	Q	$\overline{Q}$
L	L	See D Table	See D Table
L	H	H	L
H	L	L	H
H	H	Not Allowed	

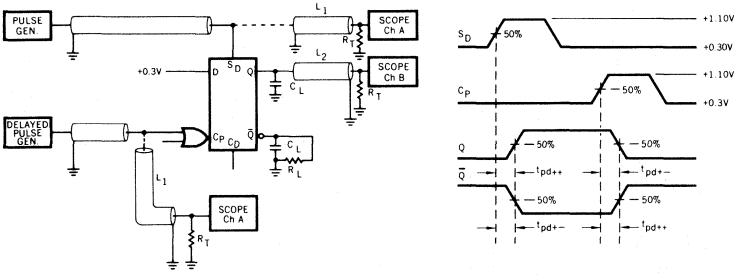
D.C. ELECTRICAL CHARACTERISTICS (T_A = 0°C to +75°C, V_{CC} = GND, V_{EE} = −5.2 V)

SYMBOL	CHARACTERISTIC	LIMITS									UNITS	CONDITIONS
		0°C			+25°C			+75°C				
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
V_{OH}	Output High Voltage	−905	−850	−795	−905	−850	−795	−895	−840	−785	mV	FO = 1 Gate
		−945	−890	−835	−945	−890	−835	−945	−890	−835	mV	FO = 5 Gates
		−980	−925	−870	−980	−925	−870	−980	−925	−870	mV	R_L = 50 Ω to −2.0 V
V_{OL}	Output Low Voltage	−1755	−1670	−1585	−1755	−1670	−1585	−1755	−1670	−1585	mV	FO = 1 Gate
		−1795	−1710	−1625	−1795	−1710	−1625	−1795	−1710	−1625	mV	FO = 5 Gates
		−1785	−1700	−1615	−1785	−1700	−1615	−1785	−1700	−1615	mV	R_L = 50 Ω to −2.0 V
V_{IHX}	Input High Threshold Voltage	−1140			−1140			−1140			mV	Guaranteed Input High
V_{ILX}	Input Low Threshold Voltage			−1450			−1450			−1450	mV	Guaranteed Input Low
$I_{IN(1)}$	Input Current at V_{IH}		2.30	3.15		2.25	3.10		2.15	3.00	mA	V_{IH} = 900 mV to each
	Common Clock Input		4.60	6.30		4.50	6.20		4.30	6.00		input sequentially
$I_{IN(0)}$	Input Current at V_{IL}		1.80	2.40		1.75	2.35		1.65	2.25	mA	V_{IL} = 1700 mV to each
	Common Clock Input		3.60	4.80		3.50	4.70		3.30	4.50		input sequentially
I_{PS}	Power Supply Current	46	62	84	51	64	85	52	66	90	mA	All inputs open

A.C. ELECTRICAL CHARACTERISTICS (T_A = 0°C to +75°C)

SYMBOL	CHARACTERISTIC	LIMITS									UNITS	CONDITIONS
		0°C			+25°C			+75°C				
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
I_T	Transient Input Current					2.5	3.5				mA	See Fig. 5
	Common Clock					3.5	4.5				mA	
t_{pd}	Clock Input											V_{CC} = 2.0 V
	t_{pd++}		3.6			3.6	4.8		3.6		ns	V_{EE} = −3.2 V
	t_{pd+-}		3.6			3.6	4.8		3.6		ns	See Fig. 2 & 3
	S_D & C_D Input											R_L = 50 Ω to Gnd
	t_{pd++}		3.6			3.6	4.8		3.6		ns	C_L < 5 pF
	t_{pd+-}		3.6			3.6	4.8		3.6		ns	$t_r = t_f$ = 2.5 ns
	Toggle Rate				110	160					MHz	See Fig. 4

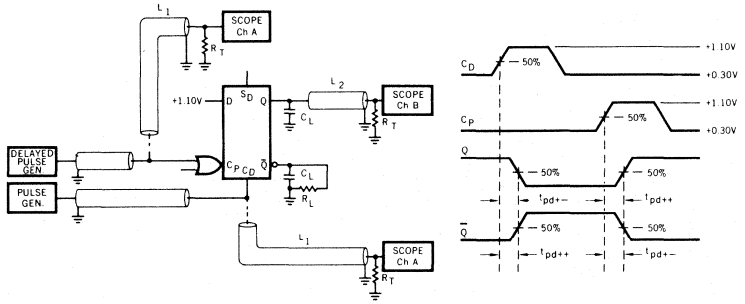
SWITCHING TIME TEST CIRCUITS AND WAVEFORMS



CONDITIONS

V_{CC} = +2.0 V
V_{EE} = −3.2 V
R_L = 50 Ω = R_T (Scope input impedance)
C_L = Jig and stray capacitance < 5 pF
L_1 = L_2 equal 50 Ω impedance lines
Input signal $t_r = t_f$ = 2.5 ns (10% - 90%)
with no circuit under test

Fig. 2 — S_D ASYNCHRONOUS INPUT SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

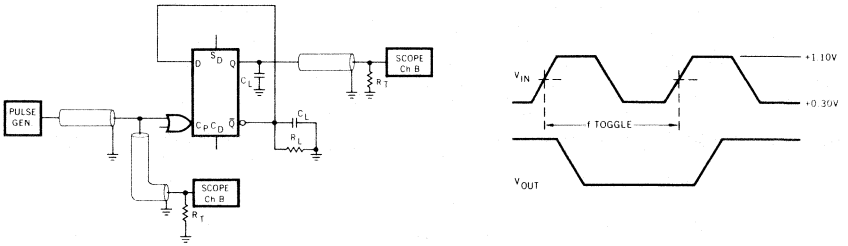


CONDITIONS

V_{CC} = +2.0 V
V_{EE} = −3.2 V
R_L = 50 Ω = R_T (Scope input impedance)
C_L = Jig and stray capacitance < 5 pF
L_1 = L_2 equal 50 Ω impedance lines
Input signal $t_r = t_f$ = 2.5 ns (10% - 90%)
with no circuit under test

Fig. 3 — C_D ASYNCHRONOUS INPUT SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

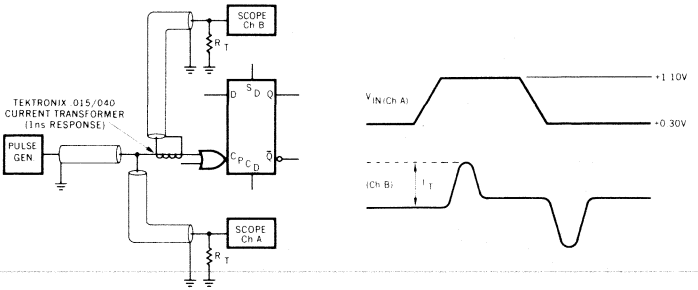
SWITCHING TIME TEST CIRCUITS AND WAVEFORMS (continued)



CONDITIONS

V_{CC} = +2.0 V
V_{EE} = −3.2 V
R_L = 50 Ω = R_T (Scope input impedance)
C_L = Jig and stray capacitance < 5 pF
Pulse Gen. — EH 122 or equivalent

Fig. 4 — TOGGLE RATE TEST CIRCUIT AND WAVEFORMS



This test provides a measure of the average value of C_{IN}.

CONDITIONS

V_{CC} = +2.0 V
V_{EE} = −3.2 V
R_T = 50 Ω (Scope input impedance)
Input signal t_r = t_f = 2.5 ns (10% - 90%) with no circuit under test

Fig. 5 — TRANSIENT INPUT CURRENT TEST CIRCUIT AND WAVEFORMS

95H28

VERY HIGH SPEED
DUAL D FLIP-FLOP
FAIRCHILD TEMPERATURE COMPENSATED ECL

GENERAL DESCRIPTION

The 95H28 is a very high speed temperature compensated ECL dual D (data) flip-flop compatible with all other members of the 9500 series of ECL circuits. The deivce is versatile and permits easy implementation of high speed counters, registers, and control circuits.

FUNCTIONAL DESCRIPTION

Each D Flip-Flop consists of both a master and a slave. While the clock is LOW the slave is held steady, but the information on the D input is permitted to enter the master. The next clock transition from LOW to HIGH locks the master in its present state making it insensitive to the D input and connects the slave to the master causing the new information to be reflected on the outputs. Logic races are avoided by offsetting the master and slave thresholds to avoid simultaneous switching when low speed edges are encountered in the system.

The internal clock is the OR of two clock inputs, one common to both flip-flops. The ORed clock permits the use of one input as a clock pulse input and the other as an active low enable.

- 220 MHZ TYPICAL OPERATION
- SEPARATE CURRENT SWITCH AND EMITTER FOLLOWER V_{cc} PINS - ELIMINATES NOISE COUPLING
- TEMPERATURE COMPENSATION
- INTERNAL PULLDOWN RESISTORS
- MASTER SLAVE CIRCUIT
- SEPARATE DIRECT SET AND CLEAR INPUTS
- BOTH COMMON AND SEPARATE CLOCK INPUTS
- WIRED OR CAPABILITY ON OUTPUTS
- 50Ω LINE DRIVING CAPABILITY
- SINGLE - 5.2 VOLT POWER SUPPLY
- HERMETIC CERAMIC 16 PIN DUAL IN-LINE PACKAGE

PIN NAMES

D	DATA INPUT TO MASTER
C_P	CLOCK INPUTS
Q	SLAVE OUTPUT
$\overline{Q}$	SLAVE COMPLIMENT OUTPUT
S_P	SET DIRECT INPUT
C_P	CLEAR DIRECT INPUT

ORDER INFORMATION - SPECIFY U6B95H28 XX FOR 16 PIN DUAL IN-LINE PACKAGE WHERE XX IS 9X FOR 0 C TO + 75 C TEMPERATURE RANGE

FAIRCHILD
SEMICONDUCTOR

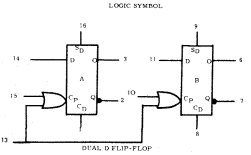
DC ELECTRICAL CHARACTERISTICS ($T_A = 0^\circ C$ TO $+75^\circ C$, V_{CC} = GND $V_{EE} = -5.2V$)

SYMBOL	CHARACTERISTIC	LIMITS 0°C-75°C MIN	TYP	MAX	UNITS	CONDITIONS
V_{OH}	OUTPUT HIGH VOLTAGE	-920	-860	-800	mV	FO= 1 GATE
		-970	-910	-850	mV	FO= 5 GATES
		-1010	-950	-890	mV	R_L=50Ω TO - 2.0V
V_{OL}	OUTPUT LOW VOLTAGE	-1780	-1690	-1600	mV	FO= 1 GATE
		-1850	-1740	-1650	mV	FO= 5 GATES
		-1810	-1720	-1630	mV	R_L = 50Ω TO - 2.0V
V_{IHX}	INPUT HIGH THRESHOLD VOLTAGE	-1140			mV	GUARANTEED INPUT HIGH
V_{ILX}	INPUT LOW THRESHOLD VOLTAGE			-1450	mV	GUARANTEED INPUT LOW
$I_{IN(I)}$	INPUT CURRENT AT V_{IH}		2.25	3.15	mA	V_{IH}=-900 mV TO EACH INPUT SEQUENTIALLY
$I_{IN(O)}$	INPUT CURRENT AT V_{II}		1.75	2.35	mA	V_{IL}=-1700 mV TO EACH INPUT SEQUENTIALLY
I_{PS}	POWER SUPPLY CURRENT		64		mA	ALL INPUTS OPEN

EC ELECTRICAL CHARACTERISTICS ($T_A = 0^\circ C$ TO $+75^\circ C$)

SYMBOL	CHARACTERISTIC	LIMITS 0°C MIN	TYP	MAX	+25°C MIN	TYP	MAX	+75°C MIN	TYP	MAX	UNITS	CONDITIONS
I_T	TRANSIENT INPUT CURRENT					2.5	3.5				mA	SEE FIG. 5
	COMMON CLOCK					3.5	4.5				mA	9528 DATA SHEET
t_{pd}	CLOCK INPUT											V_{CC} = 2.0V
	t_{pd++}		3.6			2.8	4.8		3.6		ns	V_{EE} = -3.2V
	t_{pd+-}		3.6			2.8	4.8		3.6		ns	SEE FIG. 2&3
	S_D&C_D INPUT											R_L = 50Ω to GND
	t_{pd++}		3.6			2.4	4.8		3.6		ns	C_L < 5 pF
	t_{pd+-}		3.6			2.4	4.8		3.6		ns	$t_r = t_f$ = 2.5 ns
	TOGGLE RATE					220					MHZ	SEE FIG. 4
												9528 DATA SHEET

LOGIC SYMBOL



DUAL D FLIP-FLOP

FIG. 1

CONNECTION DIAGRAM DIP (TOP VIEW)

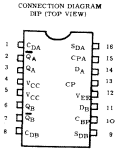


FIG. 2

95H29
VERY HIGH SPEED J-K FLIP-FLOP
FAIRCHILD TEMPERATURE COMPENSATED ECL

GENERAL DESCRIPTION — The 95H29 is a High Speed Edge-Triggered J-K flip-flop with both direct set and clear inputs. The J and K functions are the active low AND of three inputs. The clock is the active high OR of three inputs. With these inputs this device may be used effectively in counters, registers, and other applications where data must be stored or shifted at a high rate.

An additional use of the 95H29 is as a frequency prescaler and controlled divider for frequencies over 200 MHz.

FEATURES

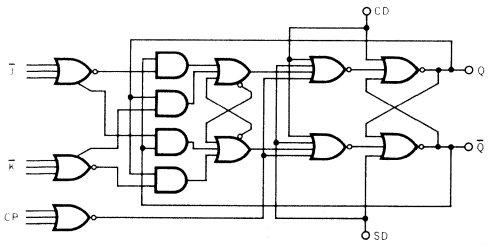
- 210 MHz TYPICAL OPERATION
- ASYNCHRONOUS DIRECT SET AND CLEAR
- EDGE TRIGGERED (NON-ONES-CATCHING)
- SEPARATE CURRENT SWITCH & EMITTER FOLLOWER V_{CC} PINS
- TEMPERATURE COMPENSATION
- INTERNAL PULLDOWN RESISTORS
- 50Ω LINE DRIVING CAPABILITY
- SINGLE −5.2 VOLT POWER SUPPLY
- HERMETIC CERAMIC 16 PIN DIP

PIN NAMES

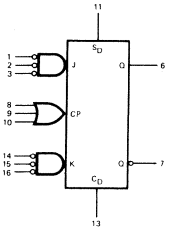
$\overline{J}$	Synchronous Set
$\overline{K}$	Synchronous Reset
CP	Clock Input
S_D	Asynchronous Set Direct
C_D	Asynchronous Clear Direct
Q	True Output
$\overline{Q}$	Component Output

ORDER INFORMATION — Specify U6B95H2959X for 16 pin Dual In-Line Package and 0°C to 75°C Temperature Range.

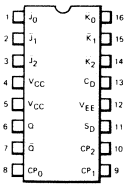
LOGIC DIAGRAM



LOGIC SYMBOL



CONNECTION DIAGRAM
DIP (TOP VIEW)



Pins 4 and 5 = V_{CC} = GND
Pin 12 = V_{EE} = −5.2 V

FAIRCHILD
SEMICONDUCTOR

FUNCTIONAL DESCRIPTION – The 95H29 is a very high speed $\overline{JK}$ flip-flop whose design has been optimized for maximum speed. The multiple $\overline{J}$, $\overline{K}$ and Clock inputs permit its use in most register and counter applications without extra gates.

The master-slave design offers the advantage of a DC threshold on the clock input initiating the transition of the outputs, so that careful control of clock pulse rise and fall times is not required.

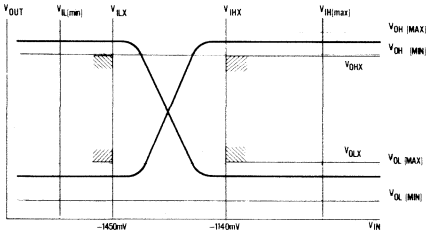
Data is accepted by the master while the clock is low. Data present just prior to the rising edge of the clock (as specified by the set up time) is trapped in the master and transferred to the slave on the rising edge of the clock. When the clock is high, the $\overline{J}$ and $\overline{K}$ inputs are inhibited.

The asynchronous inputs provide ability to control the state of the flip-flop independent of static conditions of the clock and synchronous inputs. Both asynchronous set and clear are provided. The set or clear pin being high, absolutely guarantees that one output will be high, but if opposing data is present at the synchronous inputs and the flip-flop is clocked, the low output may momentarily spike high synchronous with a positive transition of the clock. If the clock is suspended during the time when the asynchronous inputs are activated, no spike will occur.

D.C. ELECTRICAL CHARACTERISTICS (Operating Temperature Range: T_A = 0°C to 75°C, V_{CC} = GND, V_{EE} = –5.2 V)

SYMBOL	CHARACTERISTIC	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	CONDITIONS	
V_{OH}	Output Voltage High	–920 –970 –1010	–860 –910 –950	–800 –850 –890	mV	FO = 1 Gate FO = 5 Gates 50Ω to –2.0 V	$V_{IN} = V_{IL}$ = –1700 mV for NOR Gate $V_{IN} = V_{IH}$ = –900 mV for OR Gate
V_{OL}	Output Voltage Low	–1780 –1830 –1790	–1690 –1740 –1720	–1600 –1650 –1630	mV	FO = 1 Gate FO = 5 Gates 50Ω to –2.0 V	$V_{IN} = V_{IH}$ = –900 mV for NOR Gate $V_{IN} = V_{IL}$ = –1700 mV for OR Gate
V_{IHX}	Guaranteed Input High Threshold Voltage	–1140			mV	Guaranteed Input High Threshold Voltage	
V_{ILX}	Guaranteed Input Low Threshold Voltage			–1450	mV	Guaranteed Input Low Threshold Voltage	
$V_{IN(H)}$	Input Current High		2.40	3.45	mA	V_{IN} = –900 mV to S_D(11) & C_D(13) Inputs	
$V_{IN(H)}$	Input Current High		2.25	3.15	mA	V_{IN} = –900 mV to Other Inputs Sequentially	
$V_{IN(L)}$	Input Current Low		1.75	2.46	mA	V_{IN} = –1700 mV to Each Input Sequentially	
I_{PS}	Power Supply Current	36	46	62	mA	All Inputs & Outputs Open	

NOISE MARGIN SPECIFICATION POINTS



Corner points indicated on the transfer characteristics represent the worst case points (thresholds) at which the device will start to switch. The values V_{ILX} and V_{IHX} define the maximum width of the transition region.

TRUTH TABLE

SYNCHRONOUS

$\overline{J}_0$ $\overline{J}_1$ $\overline{J}_2$	$\overline{K}_0$ $\overline{K}_1$ $\overline{K}_2$	Q_{n+1}
L L L	L L L	$\overline{Q}_n$
L L L	One or More High	H
One or More High	L L L	L
One or More High	One or More High	Q_n

L = Low Logic Level
H = High Logic Level
Q_n = Present Output State
Q_{n+1} = Output State after next Clock

ASYNCHRONOUS

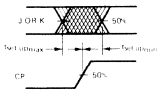
C_D	S_D	Q
L	L	Sync
L	H	H
H	L	L
H	H	Not Permitted

ABSOLUTE MAXIMUM RATINGS (above which useful life may be impaired)

Storage Temperature	–65°C to +150°C
Junction Temperature	+150°C
Supply Voltage V_{EE} (Continuous)	–6 V
Supply Voltage V_{EE} (Pulsed)	–8 V
Input Voltage	GND to V_{EE} (max)
Output Current	40 mA

A.C. ELECTRICAL CHARACTERISTICS (V_{CC} = Gnd, V_{EE} = -5.2 V, T_A = 25°C)

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		MIN.	TYP.	MAX.		
t_{pd+}	CP to Q or $\overline{Q}$	1.9	2.85	3.8	ns	See Fig. 3
t_{pd-}	CP to Q or $\overline{Q}$	1.9	2.85	3.8	ns	
t_r	Rise Time Q or $\overline{Q}$	1.2	2.4	3.6	ns	
t_f	Fall Time Q or $\overline{Q}$	1.2	2.4	3.6	ns	
t_{pd+}	S_D to Q	1.9	2.85	3.8	ns	See Fig. 4
	C_D to $\overline{Q}$	1.9	2.85	3.8	ns	
t_{pd-}	C_D to Q	1.9	2.85	3.8	ns	
	S_D to $\overline{Q}$	1.9	2.85	3.8	ns	
$f_{(min)}$	Minimum Clock Frequency	160	210		MHz	See Fig. 2
$t_{set\text{-}up}$	$\overline{J}$ or $\overline{K}$ to CP	1.0		-0.5	ns	See Fig. 1



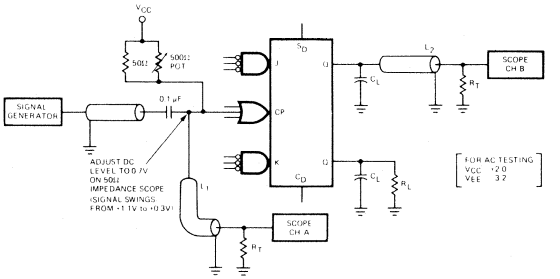
$t_{SET\text{-}UP}$ is the time that the $\overline{J}$ or $\overline{K}$ inputs must be present before the clock transition from low to high in order for the flip-flop to recognize the new data.

The negative value indicates that the data must remain after the clock transition.

For one flip-flop, there is one value of t_s. The limits of t_s max and t_s min cover the production spread of the parameter. For predictable performance data must be stable between those limits.

Fig. 1 TIME WAVEFORM AND DESCRIPTION

SWITCH TIME TEST CIRCUITS AND WAVEFORMS



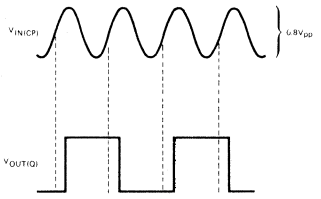


Fig. 2 MINIMUM CLOCK FREQUENCY

SWITCHING TEST CIRCUITS AND WAVEFORMS

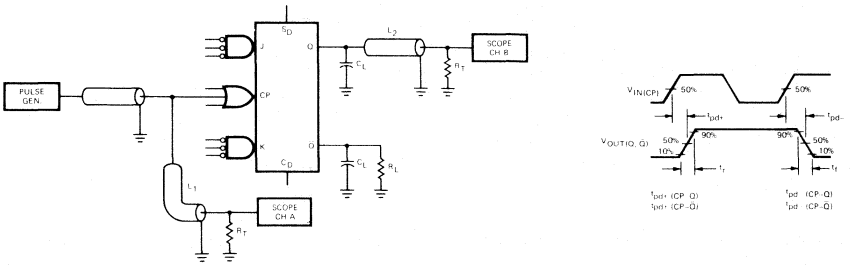


Fig. 3 CLOCK INPUT TO OUTPUT

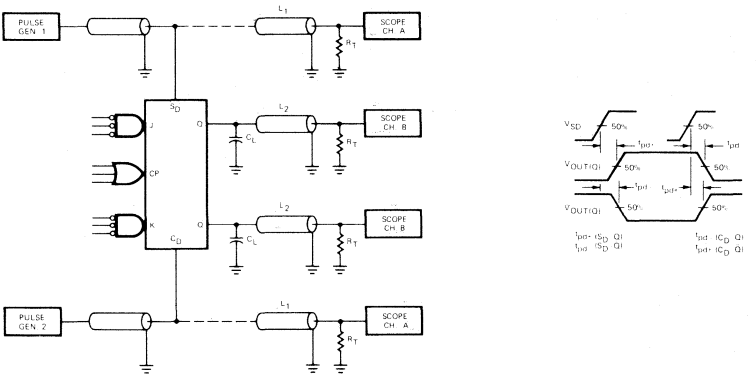
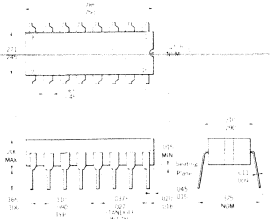


Fig. 4 ASYNCHRONOUS INPUT TO OUTPUT

PHYSICAL DIMENSIONS

6B — 16 LEAD SSI DUAL IN-LINE PACKAGE



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers.
They are purposely shipped with "positive" misalignment to facilitate insertion
Board drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin plated kovar
Package weight is 2.0 grams
*The .037/.027 dimension does not apply to the corner leads

C

9534

RESETTABLE QUAD "D" LATCH WITH I/O ENABLE

FAIRCHILD TEMPERATURE COMPENSATED ECL

GENERAL DESCRIPTION – The ECL 9534 quad D latch will store four bits of information simultaneously. Two common enable inputs and a common output enable allow maximum logic flexibility. A common Select input selects 'D' type or 'Set' type of operation. A common reset clears the device so that the 1's catching feature may be used when desired.

This element is designed as a storage buffer for high speed registers in arithmetic logic units and a data buffer in communication systems.

- **HIGH SPEED . . . 4.3 ns TYPICAL DATA DELAYS**
- **COMMON LATCH ENABLE**
- **COMMON MASTER RESET**
- **COMMON SELECT FOR 'D' OR 'SET'**
- **COMPLEX MULTIGATE CHIP REDUCES PACKAGE COUNT**
- **EASILY EXPANDED TO LARGE HIGH SPEED MEMORY**
- **WIRED OR CAPABILITY**
- **SEPARATE CURRENT SWITCH AND EMITTER FOLLOWER V_{CC} PINS – ELIMINATES NOISE COUPLING**
- **TEMPERATURE COMPENSATION**
- **INTERNAL PULLDOWN**
- **50 Ω LINE DRIVE CAPABILITY**
- **SINGLE –5.2 VOLT POWER SUPPLY**
- **HERMETIC CERAMIC 16 PIN DIP**

PIN NAMES

D_N	Data Inputs
Q_N	Data Output
S_1	Select, Data or 1's Catching
MR	Master Reset
$\overline{EO}$	Output Enable
$\overline{EI}$	Input Enable

ORDER INFORMATION – Specify U6B9534XXX for 16 pin Dual In-Line Package where XXX is 59X for 0°C to +75°C Temperature Range.

LOGIC SYMBOL

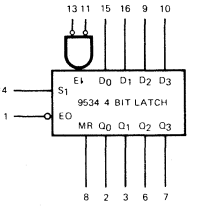


Fig. 1

CONNECTION DIAGRAM
DIP (TOP VIEW)

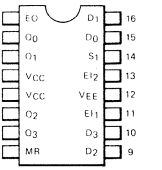


Fig. 2

LOGIC DIAGRAM (4 Each)

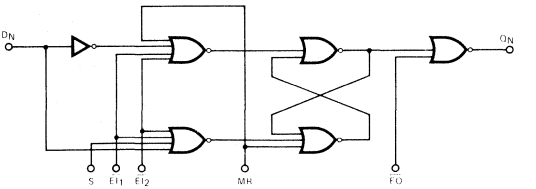


Fig. 3

FUNCTIONAL DESCRIPTION – Data can be entered into the latch whenever both input enable inputs ($\overline{E1}$) are low.

If either of the input enables ($\overline{E1}$) goes high the data present in the latch at that time is held and is no longer affected by the data input.

Data may be read out of the latches whenever the output enable ($\overline{E0}$) is low.

If the output enable goes high then the outputs are forced low, but the data is undisturbed. This function allows many 9534 latches to be wire ORed together and read out when selected. Information may be fed into the latch and stored while the outputs are held low.

If the S_1 input is raised the 9534 becomes a quad set-reset latch with separate sets (D_N) and a common reset (MR). In this mode (S_1 = high) if both input enables ($\overline{E1}$) are low the latches are ones catching. Again if either input enable ($\overline{E1}$) goes high the data present in the latch is held and is no longer affected by the data input.

If at any time the master rest (MR) goes high all latches are forced to "0". If the output enable goes high, only the outputs will be forced to "0". The data remains undisturbed.

D.C. ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (T_A = 0°C to 75°C, V_{EE} = −5.2 V)

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS	
		MIN.	TYP.	MAX.			
V_{OH}	Output High Voltage	−905 −945 −980	−850 −890 −925	−785 −835 −870	mV	FO = 1 Gate FO = 5 Gates 50 Ω to −2.0 V	V_{IN} = −0.900 V (D operation)
V_{OL}	Output Low Voltage	−1755 −1795 −1785	−1670 −1710 −1700	−1585 −1625 −1615	mV	FO = 1 Gate FO = 5 Gates 50Ω to −2.0 V	V_{IN} = −1.700 V (D operation)
V_{OHC}	Output High Corner Point (See Fig. 4)	−915 −955 −990			mV	FO = 1 Gate FO = 5 Gates 50 Ω to −2.0 V	V_{IN} = V_{IHX} (D Input) V_{IN} = V_{ILX} (EO Input)
V_{OLC}	Output Low Corner Point (See Fig. 4)			−1575 −1615 −1605	mV	FO = 1 Gate FO = 5 Gates 50 Ω to −2.0 V	V_{IN} = V_{ILX} (D Input) V_{IN} = V_{IHX} (EO Input)
V_{IHX}	Input High Level	−1140			mV	Guaranteed Input High Threshold Voltage	
V_{ILX}	Input Low Level			−1450	mV	Guaranteed Input Low Threshold Voltage	
$I_{IN(H)}$	Input Current at V_{IH}		2.25	3.15	mA	V_{IN} = −900 mV to Each Input Sequentially	
$I_{IN(L)}$	Input Current at V_{IL}		1.75	2.40	mA	V_{IN} = −1700 mV to Each Input Sequentially	
I_{PS}	Power Supply Current		80		mA	V_{EE} = −5.2 V, All Inputs Open	

NOISE MARGIN SPECIFICATION POINTS

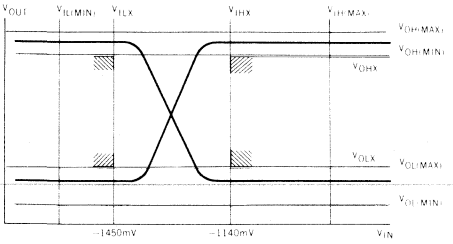


Fig. 4

Corner points indicated on the transfer characteristics represent the worst case points (thresholds) at which the device will start to switch. The values V_{ILX} and V_{IHX} define the maximum width of the transition region.

ABSOLUTE MAXIMUM RATINGS (above which useful life may be impaired)

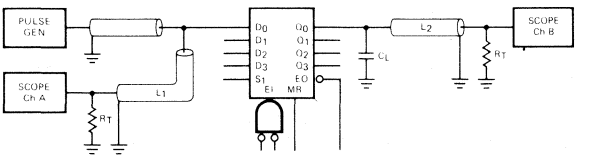
Storage Temperature	−65°C to +150°C
Junction Temperature	+150°C
Supply Voltage V_{EE} (Continuous)	−6 Volts
Supply Voltage V_{EE} (Pulsed)	−8 Volts
Input Voltage	GND to V_{EE} (max)
Output Current	40 mA

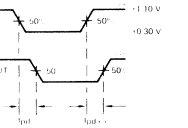
A.C. ELECTRICAL CHARACTERISTICS (V_{CC} = GND, V_{EE} = −5.2 V)

SYMBOL	CHARACTERISTIC	LIMITS 0°C MIN	0°C TYP	0°C MAX	25°C MIN	25°C TYP	25°C MAX	75°C MIN	75°C TYP	75°C MAX	UNITS	CONDITIONS
	Propagation Delay											
	DATA INPUT											
	t_{pd--}		4.3			4.3			4.6		ns	See Fig. 5
	t_{pd++}		4.3			4.3			4.6		ns	
	OUTPUT ENABLE											
	t_{pd-+}		3.4			3.4			3.6		ns	See Fig. 6
	t_{pd++}		3.4			3.4			3.6		ns	
t_{pd}	MR INPUT											
	t_{pd-+}		5.6			5.6			6.0		ns	See Fig. 7
	t_{pd+-}		5.6			5.6			6.0		ns	
	EI INPUT											
	t_{pd-+}		5.6			5.6			6.0		ns	See Fig. 8
	SELECT INPUT											
	t_{pd-+}		5.6			5.6			6.0		ns	See Fig. 9
	Transient Input Current					2.5	3.5				mA	
I_T	Master Reset					5.0	6.0				mA	See Fig. 10
	Output Enable					3.5	4.5				mA	

SWITCHING TIME CIRCUITS AND WAVEFORMS

DATA TO OUTPUT

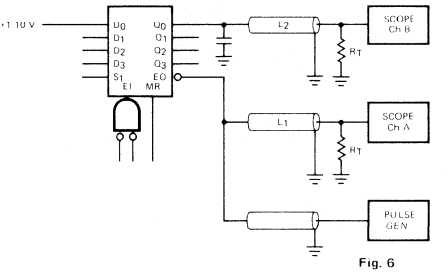


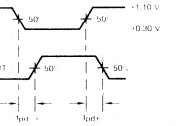


CONDITIONS
V_{CC} = +2.0 V
V_{EE} = −3.2 V
R_L = 50 Ω = R_T (Scope input impedance)
C_L = jig and stray capacitance = 5 pF
L_1 = L_2 equal 50 Ω impedance lines
Input signal t_r = t_f = 2.5 ns (10% - 90%)
With no circuit under test

Fig. 5

OUTPUT ENABLE TO OUTPUT





CONDITIONS
V_{CC} = +2.0 V
V_{EE} = −3.2 V
R_L = 50 Ω = R_T (Scope input impedance)
C_L = jig and stray capacitance = 5 pF
L_1 = L_2 equal 50 Ω impedance lines
Input signal t_r = t_f = 2.5 ns (10% - 90%)
With no circuit under test

Fig. 6

SWITCHING TIME CIRCUITS AND WAVEFORMS (Cont'd)

M.R. TO OUTPUT

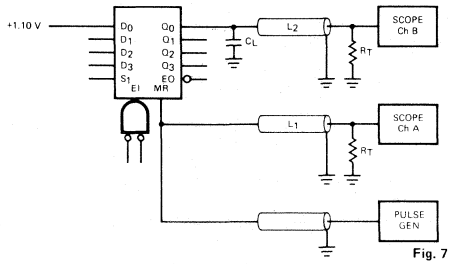
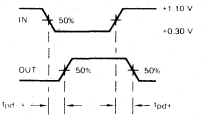


Fig. 7



CONDITIONS
- V_{CC} = +2.0 V
- V_{EE} = -3.2 V
- R_L = 50 Ω = R_T (Scope input impedance)
- C_L = jig and stray capacitance < 5 pF
- L_1 = L_2 equal 50 Ω impedance lines
- Input signal t_r = t_f = 2.5 ns (10% - 90%)
- With no circuit under test

INPUT ENABLE TO OUTPUT

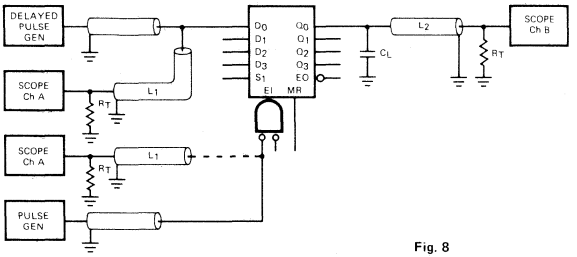
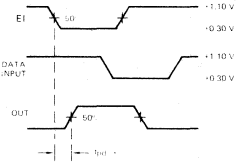


Fig. 8



CONDITIONS
- V_{CC} = +2.0 V
- V_{EE} = -3.2 V
- R_L = 50 Ω = R_T (Scope input impedance)
- C_L = jig and stray capacitance < 5 pF
- L_1 = L_2 equal 50 Ω impedance lines
- Input signal t_r = t_f = 2.5 ns (10% - 90%)
- With no circuit under test

SELECT TO OUTPUT

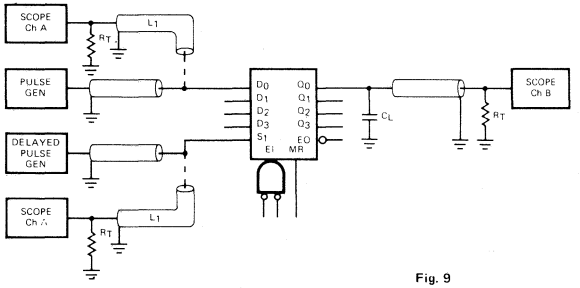
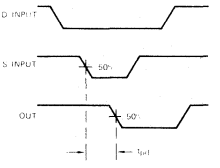


Fig. 9



CONDITIONS
- V_{CC} = +2.0 V
- V_{EE} = -3.2 V
- R_L = 50 Ω = R_T (Scope input impedance)
- C_L = jig and stray capacitance < 5 pF
- L_1 = L_2 equal 50 Ω impedance lines
- Input signal t_r = t_f = 2.5 ns (10% - 90%)
- With no circuit under test

TRANSIENT INPUT CURRENT

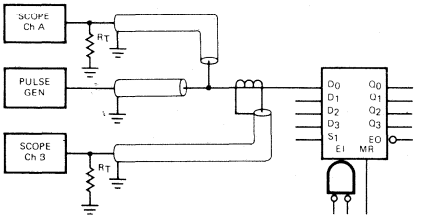
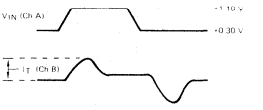


Fig. 10



This test provides a measure of the average value of C_{IN}

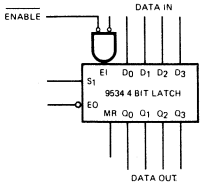
CONDITIONS
- V_{CC} = +2.0 V
- V_{EE} = -3.2 V
- R_T = 50 Ω (Scope input impedance)
- Input signal t_r = t_f = 2.5 ns (10% - 90%)
- With no circuit under test

APPLICATIONS – The 9534 quad latch is designed for all register applications encountered in high speed digital systems.

The 9534 has two modes of operation: as a 4-bit "D" type latch (Figure 11) or as a 4-bit Set-Reset type latch (Figure 12). The S (set) input determines which of these two modes the device operates in: S = "LOW" for "D" operation, S = "HIGH" for "S–R" operation.

An output enable (EO) is provided in addition to the input enables (EI). This permits both multiplexing of outputs (Figure 13) and demultiplexing of inputs (Figure 14). The Multiport Register in Figure 15 makes use of these features.

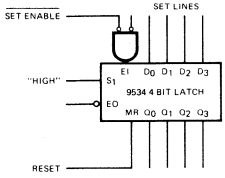
4 BIT STORAGE LATCH



The figure illustrates the use of the 9534 as a D type storage latch. Data is stored in the latch when the enable line is high.

Fig. 11

QUAD SET-RESET LATCH



This figure illustrates the use of the 9534 as a quad set-reset latch. If while the enable is low, a "HIGH" appears at an input (D_N) the latch sets, and stays set even if the input returns to a "LOW". A "HIGH" on the master reset removes all "HIGH's" from the latch.

Fig. 12

REGISTER MULTIPLEXING

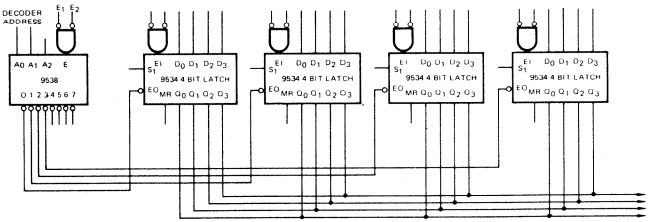


Fig. 13

REGISTER DEMULTIPLEXING

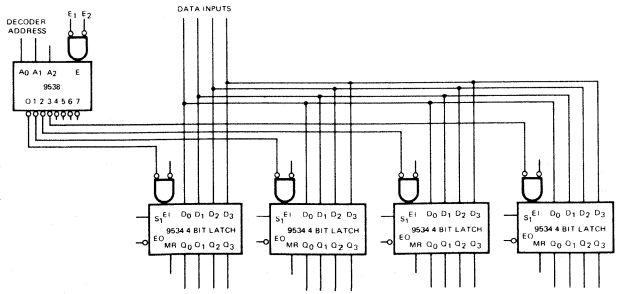
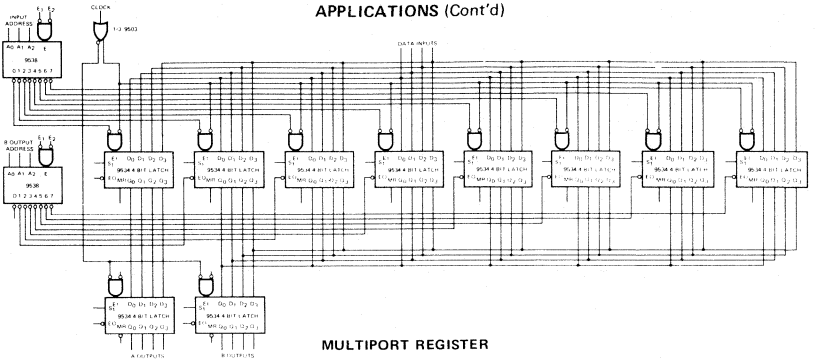


Fig. 14

APPLICATIONS (Cont'd)



MULTIPORT REGISTER

9534's may be used to form a multiport register for use in conjunction with an arithmetic unit. It is usually desirable for a multiport register to have two data outputs to simultaneously provide the two operands, A and B, and a data input for accepting the result of the operation. One of many possible variations is shown above.

The register uses eight master latches and two slave latches to provide dual-rank master-slave operation with the outputs changing following the "LOW" to "HIGH" transition of the clock. This fits nicely into a fully synchronous system where the address inputs come from sources also changing on the rising clock edge. The master-slave operation eliminates race conditions otherwise present when writing into and reading from the same location.

The multiport register shown allows the input (the result of the operation) to be read into any one of the eight locations. The A data output always comes from location 000 while the B data output may come from any of the other seven locations as selected by the 9538 decoder.

The system may easily be expanded to handle longer word lengths and a greater number of words by the addition of more 9534's and 9538's as well as 9581 multiplexers for additional output multiplexing. **Fig. 15**

INTERCONNECTION RECOMMENDATIONS

All high speed ECL circuits demand that special precautions be taken for optimum system performance. A ground plane must be provided for a good, low impedance, ground current return path and to transform interconnections into microstrip transmission lines. The voltage supply line should be well decoupled with small ceramic capacitors throughout each card between V_{EE} and the ground plane and by including at least one larger tantalum capacitor per card.

Typical microstrip lines have a characteristic impedance between 50 and 150 ohms with the lower being more desirable in ECL systems. For local interconnects the internal 2 kΩ resistors provide adequate termination but for optimum performance lines longer than 6 or 8 inches in length should be terminated in their characteristic impedance.

Lines up to 12 inches may be left unterminated if a degraded waveform can be tolerated with the resultant decrease in speed and increase in ringing.

Microstrip interconnections may be terminated by a resistor to a −2 volt supply. Alternately, a 2 resistor divider network may be used with R_1 = 1.6 R connected to ground and R_2 = 2.6 R connected to V_{EE}.

Series terminating resistors decrease noise immunity and slow rise and fall times, but can still be used if these effects are tolerable. In addition, care must be taken to avoid glitches in the threshold region of the waveform occurring at certain combinations of line length and series resistor value.

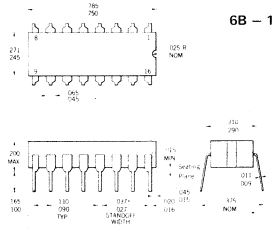
A single terminated wire running over a ground screen can be used for backpanel interconnections up to 4 or 5 inches in length, but terminated coaxial cables or terminated twisted pairs of wire are required for longer interconnections.

LINE DRIVING CAPABILITY

The 9500 series ECL circuits are capable of driving fairly long lines if the previous recommendations are followed. 50 Ω coaxial cables 10 feet in length or longer and properly terminated may be driven with almost no degradation in the waveform. The normal delay due to the finite speed of the signal traveling down the cable will be encountered in addition to a slight decrease in signal swing. This decrease caused by the attenuation of the cable (about 40 mV for 10 feet of 50 Ω coax) will lower the noise immunity of the receiving circuit by the same amount. Care must be exercised to ensure the ground potentials at the driving and receiving ends of a line are equal and no differential

PHYSICAL DIMENSIONS

6B – 16 LEAD SSI DUAL IN-LINE PACKAGE



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers.
They are purposely shipped with "positive" misalignment to facilitate insertion
Board drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.0 grams
*The .037/.027 dimension does not apply to the corner leads

9538

ONE OF EIGHT DECODER

FAIRCHILD TEMPERATURE COMPENSATED ECL

GENERAL DESCRIPTION – The 9538 is a high speed temperature compensated ECμL one of eight decoder compatible with all other members of the 9500 series of ECμL circuits. It provides in one package the ability to activate any one of eight lines by the binary address of three input lines. In addition this device may be used as a demultiplexer by connecting data to the enable inputs.

All 9500 series elements incorporate a unique temperature compensation network. This insures that significant parameters such as logic levels, noise margins and speed remain relatively constant over a wide temperature range. Input and output two kilohm pulldown resistors eliminate the necessity for external termination of lines up to six to eight inches and permit unused inputs to be left open. Package pin locations are chosen to reduce internal noise generation and crosstalk.

The device is packaged in the hermetic ceramic 16 pin dual in-line package and specified for operation over the temperature range 0°C to + 75°C.

- **HIGH SPEED 4.0 ns FROM SELECT INPUT TO OUTPUT LINE**
- **SEPARATE CURRENT SWITCH AND EMITTER FOLLOWER V_{CC} PINS–ELIMINATES NOISE COUPLING**
- **TEMPERATURE COMPENSATION**
- **INTERNAL PULLDOWN RESISTORS**
- **ENABLE INPUTS**
- **WIRED-OR CAPABILITY ON OUTPUT**
- **50 Ω LINE DRIVING CAPABILITY**
- **SINGLE -5.2 V POWER SUPPLY**
- **HERMETIC CERAMIC 16 PIN DUAL IN-LINE PACKAGE**

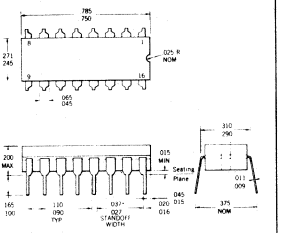
ABSOLUTE MAXIMUM RATINGS (above which useful life may be impaired)

Storage Temperature	-65°C to + 150°C
Junction Temperature	+ 150°C
Supply Voltage V_{EE} (Continuous)	-6 Volts
Supply Voltage V_{EE} (Pulsed)	-8 Volts
Input Voltage	GND to V_{EE} (max)
Output Current	40 mA

ORDER INFORMATION

Specify U6B9538XXX for 16 pin Dual In-Line Package where XXX is 59X for the 0°C to + 75°C temperature range.

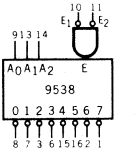
PHYSICAL DIMENSIONS
16 LEAD DUAL IN-LINE



Notes:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.0 grams
The .037/.027 dimensions does not apply to the corner leads.

Fig. 1

LOGIC SYMBOL



V_{CC} = GND (Pins 4 & 5)
V_{EE} = Pin 12

Fig. 2

FUNCTIONAL DESCRIPTION

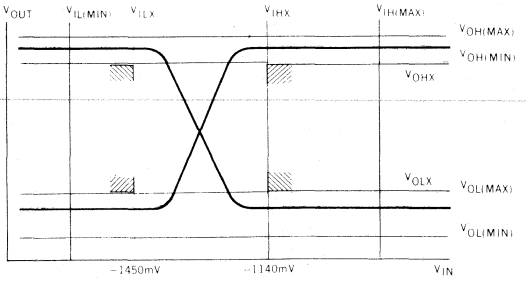
The 9538 decoder accepts three binary address inputs and under control of the enables, activates one of the eight active LOW outputs. Both of the active LOW enable input lines must be LOW to enable the outputs. In other words, if either of the enable inputs is HIGH all eight outputs remain HIGH. A truth table for the decoder is given in Figure 2.

The 9538 decoder may be used as a demultiplexer by connecting a data source to one of the enable inputs. The other enable input will function as a data enable line while inputs A_0, A_1 and A_2 determine which of the eight output lines the data is fed to. The data will not be inverted through the demultiplexer since both the input and the outputs are active low. The delay through the demultiplexer from either enable input to an output is only two gate delays.

TRUTH TABLE

INPUTS					OUTPUTS							
A_0	A_1	A_2	E_1	E_2	0	1	2	3	4	5	6	7
L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	L	H	H	H	H	H	H
L	H	L	L	L	H	H	L	H	H	H	H	H
H	H	L	L	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	L	H	H	H	H	H	L	H	H
L	H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	L	H	H	H	H	H	H	H	L
X	X	X	H	L	H	H	H	H	H	H	H	H
X	X	X	L	H	H	H	H	H	H	H	H	H
X	X	X	H	H	H	H	H	H	H	H	H	H

Fig. 3–NOISE MARGIN SPECIFICATION POINTS



Corner points indicated on the transfer characteristics represent the worst case points (thresholds) at which the device will start to switch. The values V_{ILX} and V_{IHX} define the maximum width of the transition region.

D.C. ELECTRICAL CHARACTERISTICS (T_A = 0°C to + 75°C, V_{CC} = Gnd, V_{EE} = -5.2 V)

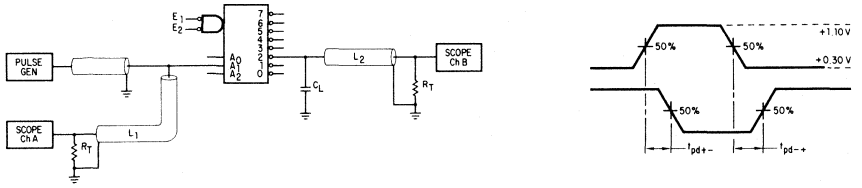
SYMBOL	CHARACTERISTIC	LIMITS									UNITS	CONDITIONS
		0°C			+ 25°C			+ 75°C				
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
V_{OH}	Output High Voltage	-915	-850	-785	-915	-850	-785	-905	-840	-775	mV	FO = 1 Gate
		-955	-880	-805	-955	-880	-805	-955	-880	-805	mV	FO = 5 Gates
		-990	-915	-840	-990	-915	-840	-990	-915	-840	mV	R_L = 50 Ω to -2.0 V
V_{OL}	Output Low Voltage	-1755	-1670	-1585	-1755	-1670	-1585	-1755	-1670	-1585	mV	FO = 1 Gate
		-1795	-1710	-1625	-1795	-1710	-1625	-1795	-1710	-1625	mV	FO = 5 Gates
		-1785	-1700	-1615	-1785	-1700	-1615	-1785	-1700	-1615	mV	R_L = 50 Ω to -2.0 V
V_{OHX}	Output High Voltage at V_{IN} (Threshold) V_{IHX} or V_{ILX} Applied to each. Select Line Sequentially.	-925			-925			-915			mV	FO = 1 Gate
		-965			-965			-965			mV	FO = 5 Gates
		-1000			-1000			-1000			mV	R_L = 50 Ω to -2.0 V See Fig. 3
V_{OLX}	Output Low Voltage at V_{IN} (Threshold) V_{IHX} or V_{ILX} Applied to each. Select Line Sequentially.			-1575			-1575			-1575	mV	FO = 1 Gate
				-1615			-1615			-1615	mV	FO = 5 Gates
				-1605			-1605			-1605	mV	R_L = 50 Ω to -2.0 V See Fig. 3
$I_{IN(1)}$	Input Current at V_{IH}		2.30	3.15		2.25	3.10		2.15	3.00	mA	V_{IH} = -900 mV to each Input Sequentially
$I_{IN(0)}$	Input Current at V_{IL}		1.80	2.40		1.75	2.35		1.65	2.25	mV	V_{IL} = -1700 mV to each Input Sequentially
I_{PS}	Power Supply Current		50		42	53	71		57		mA	All Inputs Open

A.C. ELECTRICAL CHARACTERISTICS (T_A = 0°C to + 75°C)

SYMBOL	CHARACTERISTIC	LIMITS						UNIT	CONDITIONS
		0°C	25°C			75°C			
		TYP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
t_{pd}	Propagation Delay								See Fig. 4 & 5
	Select Lines								R_L = 50 Ω to
	A_1	3.0		3.0	4.0		3.0	ns	Gnd
	A_0 & A_2	4.0		4.0	5.3		4.0	ns	$C_L \leqslant$ 5.0 pF
	Enable Lines	5.0		5.0	6.7		5.0	ns	$t_r = t_f$ = 2.5 ns
I_T	Transient Input Current			2.5	3.5			mA	See Fig. 6

SWITCHING TIME CIRCUITS AND WAVEFORMS

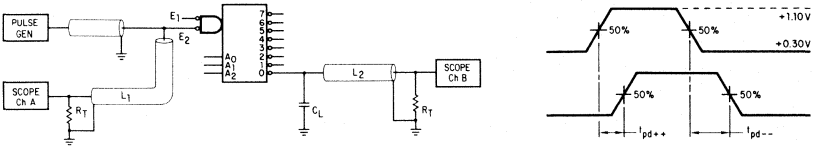
Fig. 4—SELECT LINES TO OUTPUT



CONDITIONS
V_{CC} = + 2.0 V
V_{EE} = -3.2 V
R_L = 50 Ω = R_T (Scope input impedance)
C_L = jig and stray capacitance < 5 pF
L_1 = L_2 equal 50 Ω impedance lines
Input signal $t_r = t_f$ = 2.5 ns (10% - 90%)
With no circuit under test

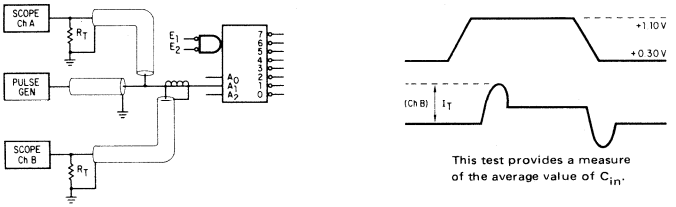
SWITCHING TIME CIRCUITS AND WAVEFORMS (CONT'D)

Fig. 5—ENABLE LINE TO OUTPUT



CONDITIONS
- V_{CC} = + 2.0 V
- V_{EE} = -3.2V
- R_L = 50 Ω = R_r (Scope input impedance)
- C_L = jig and stray capacitance < 5 pF
- L_1 = L_2 equal 50 Ω impedance lines
- Input signal t_r = t_f = 2.5 ns (10% - 90%)
- With no circuit under test

Fig. 6—TRANSIENT INPUT CURRENT TEST CIRCUIT AND WAVEFORMS



This test provides a measure of the average value of C_{in}.

CONDITIONS
- V_{CC} = + 2.0 V
- V_{EE} = -3.2 V
- R_r = 50 Ω (Scope input impedance)
- Input signal t_r = t_f = 2.5 ns (10% - 90%)
- With no circuit under test

95H39

HIGH SPEED 8-BIT MULTIPORT REGISTER
FAIRCHILD TEMPERATURE COMPENSATED ECL

GENERAL DESCRIPTION

This element is an 8 bit multiport master-slave register designed for the computer and communications system.

It is organized 8 words x 1 bit with three simultaneous outputs. The Z_O output is location O, O, O (O = Low on address lines) This output may be used for control information or as an operand or accumulator word bit in an A. L. U. The Z_A and Z_B outputs my be any of the eight locations or may be forced low by the A-Enable and B-Enable. Z_A and Z_B outputs are addressed by A-Address and B-Address inputs and my be used to supply operands for A.L.U.'s.

- VERY HIGH SPEED - < 6 N. SEC ADDRESS TO OUTPUT
- MULTIPLE OUTPUT FOR USE WITH A. L. U.
- MASTER-SLAVE OPERATION
- SEPARATE CURRENT SWITCH AND EMITTER FOLLOWER V_{CC} PINS ELIMINATES NOISE COUPLING
- TEMPERATURE COMPENSATION
- INTERNAL PULLDOWN
- 50Ω LINE DRIVE CAPACITY
- SINGLE - 5. 2 VOLT POWER SUPPLY
- HERMETIC CERAMIC 16 PIN DIP

FAIRCHILD
SEMICONDUCTOR

PIN NAMES

D DATA IN

C_P CLOCK PULSE

E_A OUTPUT 'A' ENABLE, CLOCK ENABLE

E_B OUTPUT 'B' ENABLE

A_N A ADDRESS

B_N B ADDRESS

Z_O LOCATION LO, LO, LO OUTPUT

$Z_{A,B}$ LOCATION ADDRESSED BY A, B OUTPUT (LOW WHEN DISABLED)

ORDER INFORMATION - SPECIFY U6B95H39XX FOR 16 PIN DUAL IN-LINE PACKAGE WHERE XX IS 9X FOR 0-75° C TEMPERATURE RANGE.

LOGIC OPERATION

Data present at the D_A input is loaded into the master while the clock is low. The output of the master is demultiplied into any one of the eight slave locations selected by the A-Address the moment the clock goes high. Registers on the master address prevent timing problems by permitting the A-Address to change immediately after the clock.

An additional feature of this device is the gating of the clock (cp) input with the A-Enable. Expansion up to 64 words may be accomplished by simply enabling the A_E and B_E with the output of a 9538 decoder. Operated in this manner only addressed devices will clock in new data. Because of this gating register selection should take place only while the clock is high.

In some uses the clock input may not be needed. Upon enabling a particular register the input data is loaded into the master. The disabling of this register transfers the data into the addressed slave.

DC ELECTRICAL CHARACTERISTICS (T_A 0°C - 75°C V_{EE} = -5.2 V)

SYMBOL	CHARACTERISTIC	LIMITS MIN	TYP	MAX	UNITS	CONDITIONS
V_{OH}	OUTPUT HIGH LEVEL	-920	-860	-800	mV	F.O. = 1
		-970	-910	-850	mV	F.O. = 5
		-1010	-950	-890	mV	50Ω to -2.0V± 5 pf to V_{CC}
V_{OL}	OUTPUT LOW LEVEL	-1780	-1690	-1600	mV	F.O. = 1
		-1830	-1740	-1650	mV	F.O. = 5
		-1810	-1720	-1630	mV	50Ω to -2.0V± 5 pf to V_{CC}
V_{ILX}	INPUT THRESHOLD LOW	-	-	-1450	mV	MAX INPUT VOLTAGE FOR "LOW" LOGIC
V_{IHX}	INPUT THRESHOLD HIGH	-1140	-	-	mV	MAX INPUT VOLTAGE FOR "HIGH" LOGIC
I_{IN} (HIGH)	INPUT CURRENT (HIGH)		2.25	3.16	mA	V_{IN} = -900 mV
IIN (LOW)	INPUT CURRENT (LOW)		1.75	2.46	mA	V_{IN} = -1700 mV
I_{PS}	POWER SUPPLY CURRENT		100		mA	

LOGIC SYMBOL

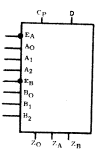


FIG 1

CONNECTION DIAGRAM
DIP (TOP VIEW)

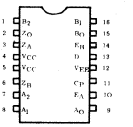


FIG 2

95H55

MSI 5-BIT COMPARATOR WITH ENABLE
FAIRCHILD TEMPERATURE COMPENSATED ECL

GENERAL DESCRIPTION

The 95H55 is a high speed expandable 5 Bit Comparator which provides comparisons between two 5 bit words and gives two outputs, "LESS THAN" and "GREATER THAN". "EQUAL TO" can be obtained by ORing the "LESS THAN" and "GREATER THAN" outputs. A high level on the Enable function forces both outputs low.

Features include easy expansion to larger word comparisons and very high speed operation. Experience gained in use of the TTL 9324 can be directly applied to the 95H55.

- HIGH SPEED - 1.0 ns INTERNAL GATE DELAYS
- "GREATER THAN" AND "LESS THAN" IN ONE DEVICE
- OUTPUT ENABLE INPUT IS ACTIVE LOW FOR EASE OF USE WITH OTHER MEMBERS OF THE 9500 FAMILY
- WIRE OR CAPABILITY
- 50 Ω AND FANOUT OF 10 ON EACH OUTPUT
- SEPARATE CURRENT SWITCH EMITTER FOLLOWER V_{CC} PINS - ELIMINATE NOISE COUPLING
- TEMPERATURE COMPENSATED
- INTERNAL PULL DOWN RESISTORS FOR DIRECT LOW COST WIRING
- SINGLE -5.2 VOLT POWER SUPPLY
- HERMETIC CERAMIC 16 PIN DIP

PIN NAMES

A_N	=	WORD A, WHERE A_0 = LEAST SIGNIFICAL BIT, A_5 MOST SIGNIFICANT BIT
E	=	OUTPUT ENABLE, FORCES OUTPUTS LOW WITH HIGH
$Q_{A>B}$	=	HIGH IF A > B, LOW IF A ≤ B
$Q_{B>A}$	=	HIGH IF B > A, LOW IF B ≤ A
B_N	=	WORD B

ORDER INFORMATION - SPECIFY U6B95H55XX FOR 16 PIN DUAL IN-LINE PACKAGE
WHERE XX IS 9X FOR 0°C TO +75°C TEMPERATURE RANGE

FAIRCHILD
SEMICONDUCTOR

ELECTRICAL SPECS D.C. $0^{\circ}C - 75^{\circ}C$ $V_{EE} = -5.2V$

SYMBOL	CHARACTERISTICS	MIN	TYP	MAX	UNITS	CONDITIONS
VOL	OUTPUT LOW LEVEL	-1780	-1690	-1600	mV	F.O. = 1
V_{OL}	OUTPUT LOW LEVEL	-1830	-1740	-1650	mV	F.O. = 5
V_{OL}	OUTPUT LOW LEVEL	-1810	-1720	-1630	mV	50Ω to -2.0V+ 5pf to V_{CC}
V_{OH}	OUTPUT HIGH LEVEL	-920	-860	-800	mV	F.O. = 1
V_{OH}	OUTPUT HIGH LEVEL	-970	-910	-850	mV	F.O. = 5
V_{OH}	OUTPUT HIGH LEVEL	-1010	-950	-890	mV	50Ω to -2.0V+ 5pf to V_{CC}
V_{ILX}	INPUT VOLTAGE LOW	-	-	-1450	mV	THRESHOLD VOLTAGE TO ASSURE V_{OH} AND V_{OL}
V_{IHX}	INPUT VOLTAGE HIGH	-1140	-	-	mV	
I_{IN} (LOW)	INPUT CURRENT LOW	-	1.75	2.4	mA	V_{IL} = -1700 mV EACH INPUT
I_{IN} (HIGH)	INPUT CURRENT HIGH	-	2.25	3.15	mA	V_{IH} = -900 mV EACH INPUT
I_{PS}	POWER SUPPLY CURRENT		85		mA	

ELECTRICAL SPECS A.C.

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
T_{DEO}	DELAY ENABLE TO OUTPUT		3.0		nS	50Ω to -2.0V 5 pf to V_{CC}
T_{DLSB}	DELAY LEAST SIGNIFICANT BIT (A_0, B_0 TO OUT)		6.0		nS	
T_{PMSB}	DELAY MOST SIGNIFICANT BIT (A_4, B_4 TO OUT)		6.0		nS	
I_t	TRANSIANT INPUT CURRENT		2.5	3.5	mA	

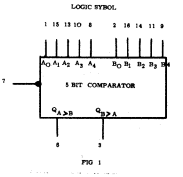


FIG 1

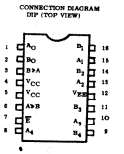


FIG 2

ECL/MSI 9578

QUAD EXCLUSIVE-OR WITH ENABLE/4-BIT COMPARATOR

FAIRCHILD TEMPERATURE COMPENSATED ECL

GENERAL DESCRIPTION – The 9578 provides four exclusive OR gates in one package using internal gating to achieve the logic function within approximately one gate delay. An additional enable gate is included so that all outputs may be held low if desired. With four of these devices a 16 bit compare function may be built with one gate delay. This element is useful in many applications such as data comparison, parity generation and checking, frequency mixing, decision and code conversion, etc.

By OR tying all outputs, the 9578 becomes a 4-Bit Comparator whose output is low only if the word on the A inputs matches the word on the B inputs or the Enable input is high.

The 9578 may be used as a Dual Differential Data-Bus Line Driver (see Application Section).

- **HIGH SPEED . . . 3.2 ns TYPICAL DELAY**
- **COMMON ENABLE**
- **WIRED OR CAPABILITY**
- **SEPARATE CURRENT SWITCH EMITTER FOLLOWER V_{CC} PINS –ELIMINATE NOISE COUPLING**
- **TEMPERATURE COMPENSATION**
- **INTERNAL PULLDOWN**
- **50 Ω LINE DRIVE CAPABILITY**
- **SINGLE –5.2 VOLT POWER SUPPLY**
- **HERMETIC CERAMIC 16 PIN DIP**

PIN NAMES

A_N, B_N	Inputs of Exclusive OR Function
C_N	Output of Exclusive OR Function
$\overline{E}$	Enable Input, Forces output LOW when held HIGH

ORDER INFORMATION – Specify U6B957859X for 16 pin Dual In-Line Package and 0°C to 75°C Temperature Range.

LOGIC DIAGRAM 1 of 4

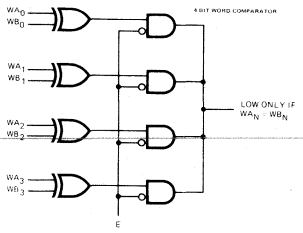


Fig. 3

LOGIC SYMBOL

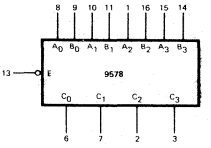
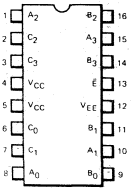


Fig. 1

CONNECTION DIAGRAM
DIP (TOP VIEW)



Pins 4 and 5 = V_{CC} = GND
Pin 12 = V_{EE} = –5.2 V

Fig. 2

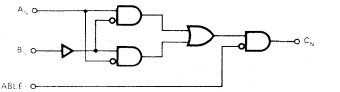
FAIRCHILD
SEMICONDUCTOR

FUNCTIONAL DESCRIPTION – Each of the 9578 Exclusive OR gates produce a HIGH output when its inputs are complementary. By OR tying the outputs of several of these gates, a comparator can be made which will be LOW only if the inputs to each of the Exclusive OR gates match. An additional feature of the 9578 is the Output Enable. By raising this input HIGH, all outputs are forced LOW regardless of any other input condition.

TRUTH TABLE

$\overline{E}$	A_N	B_N	C_N
H	X	X	L
L	L	L	L
L	L	H	H
L	H	L	H
L	H	H	L

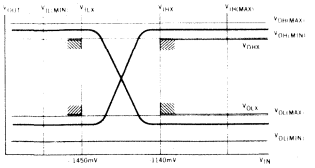
L = Low Logic Level
H = High Logic Level
X = Don't Care



D.C. ELECTRICAL CHARACTERISTICS – Over Operating Temperature Range (T_A = 0°C to 75°C, V_{EE} = –5.2 V)

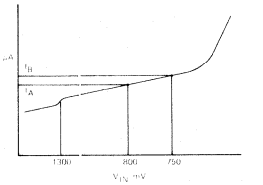
SYMBOL	CHARACTERISTIC	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	CONDITIONS	
V_{OH}	Output HIGH Voltage	–905 –945 –980	–850 –890 –925	–785 –835 –879	mV	FO = 1 Gate FO = 5 Gates 50 Ω to –2.0 V	V_{IN} = –0.900 V
V_{OL}	Output LOW Voltage	–1755 –1795 –1785	–1670 –1710 –1700	–1585 –1625 –1615	mV	FO = 1 Gate FO = 5 Gates 50 Ω to –2.0 V	V_{IN} = –1.700 V
V_{OHC}	Output HIGH Corner Point (See Fig. 4)	–915 –955 –990			mV	FO = 1 Gate FO = 5 Gates 50 Ω to –2.0 V	$V_{IN} = V_{IHX}$ $V_{IN} = V_{ILX}$
V_{OLC}	Output LOW Corner Point (See Fig. 4)			–1575 –1615 –1605	mV	FO = 1 Gate FO = 5 Gates 50 Ω to –2.0 V	$V_{IN} = V_{ILX}$ $V_{IN} = V_{IHX}$
V_{IHX}	Input HIGH Level	–1140			mV	Guaranteed Input HIGH Threshold Voltage	
V_{ILX}	Input LOW Level			–1450	mV	Guaranteed Input LOW Threshold Voltage	
$I_{IN(H)}$	Input Current at V_{IH}		2.25	3.15	mA	V_{IN} = –900 mV to Each Input Sequentially	
$I_{IN(H)}$	Input Current at V_{IH} (Enable)		2.25	3.85	mA	V_{IN} = –900 mV to Each Input Sequentially	
$I_{IN(L)}$	Input Current at V_{IL}		1.75	2.4	mA	V_{IN} = –1700 mV to Each Input Sequentially	
$I_{IN(L)}$	Input Current at V_{IL} (Enable)		1.75	2.60	mA	V_{IN} = –1700 mV to Each Input Sequentially	
I_{PS}	Power Supply Current		53	74	mA	V_{EE} = –5.2 V, All Inputs Open	
ΔI_{IN}	Input Saturation Test (Fig. 5)			50	μA	$\Delta I_{IN} = I_B - I_A$, I_A = I_{IN} @ V_{IN} = 800 mV I_B = I_{IN} @ V_{IN} = 750 mV	

Fig. 4. NOISE MARGIN SPECIFICATION POINTS



Corner points indicated on the transfer characteristics represent the worst case points (thresholds) at which the device will start to switch. The values V_{ILX} and V_{IHX} define the maximum width of the transition region.

Fig. 5. INPUT SATURATION TEST



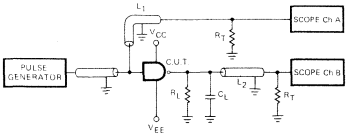
This test insures that the input transistor is not in saturation at V_{IN} = 750 mV. This represents a worst case condition with the driving gate at V_{OH} (min) = 750 mV (ie. for T_A = 75°C this is equivalent to driving gate into FO = 1 with its power supply at –5%).

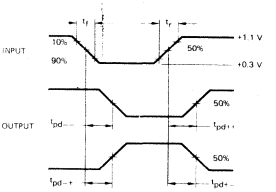
Saturation is defined as no increase in collector current for 20% increase in base drive current I_B. The effect is to increase t_{pd}.

AC ELECTRICAL CHARACTERISTICS (Operating Temperature: T_A = 0°C to 75°C, V_{CC} = GND, V_{EE} = −5.2 V)

SYMBOL	CHARACTERISTIC	LIMITS 0°C TYP.	25°C MIN.	25°C TYP.	25°C MAX.	75°C MIN.	75°C TYP.	75°C MAX.	UNITS	CONDITIONS
	Propagation Delay									
t_{pd}	t_{pd} ± A Inputs	2.6		2.6	3.5		2.7		ns	R_L = 50 Ω to −2.0 V
	t_{pd} ± B Inputs	3.2		3.2	4.3		3.3		ns	C_L <5.0 pF
	t_{pd} ± E Inputs	3.5		3.5	4.6		3.6		ns	$t_r = t_f$ = 2.5 ns
t_r, t_f	Rise and Fall Time	3.0	1.5	3.0	4.8		3.0		ns	
	Transient Input Current									
I_T	A Inputs			3.0	4.5				mA	See Fig. 6
	B Inputs			3.0	4.5				mA	
	E Inputs			6.0	9.0				mA	See Fig. 7

Fig. 6. SWITCHING TIME TEST CIRCUIT AND WAVEFORM

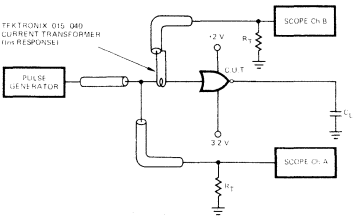


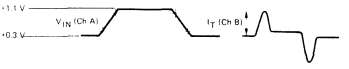


L_1 and L_2 = equal length 50 Ω impedance lines
$R_L = R_T$ = 50 Ω Termination of Scope
C_L = Jig and Stray Capacitance < 5.0 pF
$t_r = t_f$ = 2.5 ns (10% - 90%)

$V_{CC} = V_{CC}$ (AUX) = +2.0 V
V_{EE} = −3.2 V

Fig. 7. TRANSIENT INPUT CURRENT TEST CIRCUIT AND WAVEFORMS

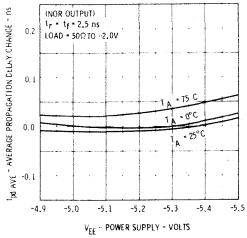




t_r = 2.5 ns (10% - 90%)

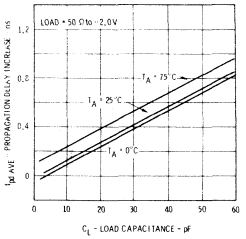
This test provides a measure of the average value of C_{IN}; also current mismatch in the line.
$V_{CC} = V_{CC}$ (AUX) = +2.0 V
V_{EE} = −3.2 V

TYPICAL AVERAGE PROPAGATION DELAY CHANGE VERSUS POWER SUPPLY



$$t_{pd}AVG = \frac{t_{pd}\ \text{rising} + t_{pd}\ \text{falling}}{2}$$

TYPICAL PROPAGATION DELAY INCREASE VERSUS LOAD CAPACITANCE

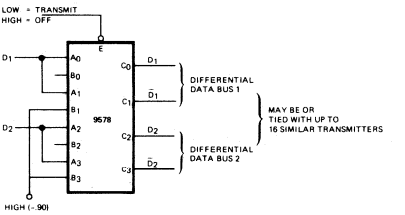


ABSOLUTE MAXIMUM RATINGS (above which useful life may be impaired)

Storage Temperature	−65°C to +150°C
Junction Temperature	+150°C
Supply Voltage V_{EE} (Continuous)	−6 Volts
Supply Voltage V_{EE} (Pulsed)	−8 Volts
Input Voltage	GND to V_{EE} (max)
Output Current	40 mA

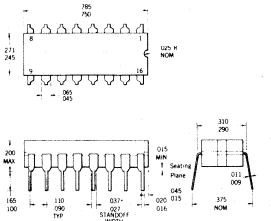
APPLICATION

DUAL DIFFERENTIAL DATA-BUS DRIVER



PHYSICAL DIMENSIONS

16 Lead Dual In-Line



NOTES
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin plated kovar
Package weight is 2.0 grams
The .037/.027 dimensions does not apply to the corner leads.

ECL/MSI 9579

QUAD 2-INPUT MULTIPLEXER WITH COMMON SELECT

FAIRCHILD TEMPERATURE COMPENSATED ECL

GENERAL DESCRIPTION – The 9579 is a Temperature Compensated ECL Quad 2-input Multiplexer, the logic equivalent of a 4 pole – 2 position switch. A common select line selects one of two groups of 4 data sources. This high speed switch operates within about one 9500 gate delay increasing reliability and saving power by delivering this function in one 16 pin package.

- **HI-SPEED . . . 2.6 ns DATA, 4.0 ns SELECT DELAY**
- **COMMON SELECT**
- **NO DATA INVERSION**
- **WIRED OR CAPABILITY**
- **SEPARATE CURRENT SWITCH EMITTER FOLLOWER V_{CC} PINS – ELIMINATE NOISE COUPLING**
- **TEMPERATURE COMPENSATION**
- **INTERNAL PULL DOWN**
- **50 Ω LINE DRIVE CAPABILITY**
- **SINGLE –5.2 VOLT POWER SUPPLY**
- **HERMETIC CERAMIC 16 PIN DIP**
- **COMPLEX MULTI-GATE CHIP REDUCES PACKAGE COUNT AND POWER**

PIN NAMES

A_N	Multiplexer Input Selected when S is HIGH
B_N	Multiplexer Input Selected when S is LOW
C_N	Multiplexed Output of A_N and B_N
S	Select Input, LOW Select B and HIGH Select A

ORDER INFORMATION – Specify U6B957959X for 16 pin Dual In-Line Package and 0°C to 75°C Temperature Range.

LOGIC DIAGRAM (1 of 4)

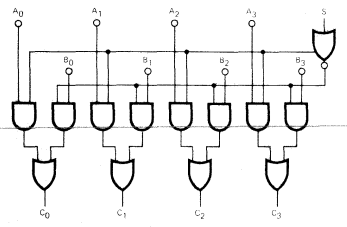


Fig. 3

LOGIC SYMBOL

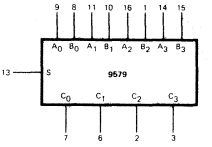
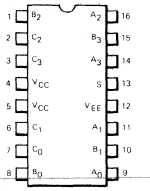


Fig. 1

CONNECTION DIAGRAM
DIP (TOP VIEW)



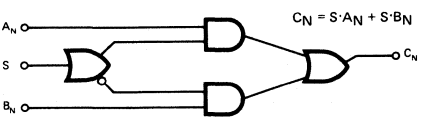
Pins 4 and 5 = V_{CC} = GND
Pin 12 = V_{EE} = –5.2 V

Fig. 2

FAIRCHILD SEMICONDUCTOR

FUNCTIONAL DESCRIPTION – The 9579 2-input multiplexer is designed with series gating and collector dotting to answer maximum speed with minimum power. It consists of four multiplexing circuits with a common select. No inversion of Data occurs.

The Data delay is similar to a standard 9500 gate delay so that optimum system speed is maintained. The Select input is buffered yielding an input loading identical to a standard 9500 gate. Partially because of this, the Select delay is typically 4.0 ns.



TRUTH TABLE

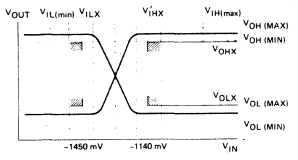
S	A_N	B_N	C_N
H	L	X	L
H	H	X	H
L	X	L	L
L	X	H	H

L = LOW Logic Level
H = HIGH Logic Level
X = Don't Care

D.C. ELECTRICAL CHARACTERISTICS – Over Operating Temperature Range (T_A = 0°C to 75°C, V_{EE} = –5.2 V)

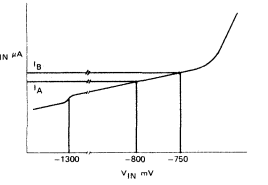
SYMBOL	CHARACTERISTIC	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	CONDITIONS	
V_{OH}	Output HIGH Voltage	–905 –945 –980	–850 –890 –925	–785 –835 –879	mV	FO = 1 Gate FO = 5 Gates 50 Ω to –2.0 V	V_{IN} = –0.900 V
V_{OL}	Output LOW Voltage	–1755 –1795 –1785	–1670 –1710 –1700	–1585 –1625 –1615	mV	FO = 1 Gate FO = 5 Gates 50 Ω to –2.0 V	V_{IN} = –1.700 V
V_{OHC}	Output HIGH Corner Point (See Fig. 4)	–915 –955 –990			mV	FO = 1 Gate FO = 5 Gates 50 Ω to –2.0 V	$V_{IN} = V_{IHX}$ $V_{IN} = V_{ILX}$
V_{OLC}	Output LOW Corner Point (See Fig. 4)			–1575 –1615 –1605	mV	FO = 1 Gate FO = 5 Gates 50 Ω to –2.0 V	$V_{IN} = V_{ILX}$ $V_{IN} = V_{IHX}$
V_{IHX}	Input HIGH Level	–1140			mV	Guaranteed Input HIGH Threshold Voltage	
V_{ILX}	Input LOW Level			–1450	mV	Guaranteed Input LOW Threshold Voltage	
$I_{IN(H)}$	Input Current at V_{IH}		2.25	3.15	mA	V_{IN} = –900 mV to Each Input Sequentially	
$I_{IN(L)}$	Input Current at V_{IL}		1.75	2.40	mA	V_{IN} = –1700 mV to Each Input Sequentially	
I_{PS}	Power Supply Current		53	74	mA	V_{EE} = –5.2 V, All Inputs Open	
ΔI_{IN}	Input Saturation Test (See Fig. 5)			50	μA	$\Delta I_{IN} = I_B - I_A$, $I_A = I_{IN}$ @ V_{IN} = 800 mV $I_B = I_{IN}$ @ V_{IN} = 750 mV	

Fig. 4 NOISE MARGIN SPECIFICATION POINTS



Corner points indicated on the transfer characteristics represent the worst case points (thresholds) at which the device will start to switch. The values V_{ILX} and V_{IHX} define the maximum width of the transition region.

Fig. 5 INPUT SATURATION TEST



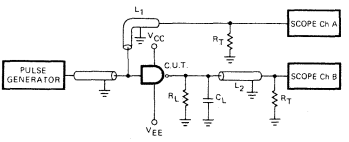
This test insures that the input transistor is not in saturation at V_{IN} = 750 mV. This represents a worst case condition with the driving gate at V_{OH} (min) = 750 mV (ie. for T_A = 75°C this is equivalent to driving gate into FO = 1 with its power supply at –5%).

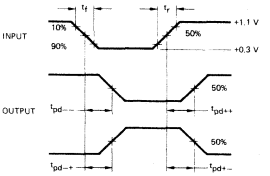
Saturation is defined as no increase in collector current for 20% increase in base drive current I_B. The effect is to increase t_{pd}.

AC ELECTRICAL CHARACTERISTICS (Operating Temperature: T_A = 0°C to 75°C, V_{CC} = GND, V_{EE} = −5.2 V)

SYMBOL	CHARACTERISTIC	LIMITS							UNITS	CONDITIONS
		0°C	25°C			75°C				
		TYP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
t_{pd}	Propagation Delay									
	t_{pd} (AVG) Data Inputs	2.6		2.6	3.5		2.7		ns	R_L = 50 Ω to −2.0 V
	t_{pd} (AVG) Select Inputs	4.0		4.0	5.3		4.2		ns	C_L < 5.0 pF
										$t_r = t_f$ = 2.5 ns
t_r, t_f	Rise and Fall Time	3.0	1.5	3.0	4.8		3.0		ns	See Fig. 6
I_T	Transient Input Current			2.5	3.5				mA	See Fig. 7

Fig. 6. SWITCHING TIME TEST CIRCUIT AND WAVEFORM

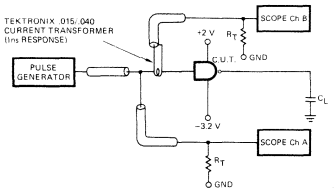


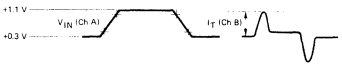


L_1 and L_2 = equal length 50 Ω impedance lines
$R_L = R_T$ = 50 Termination of Scope
C_L = Jig and Stray Capacitance < 5.0 pF
$t_r = t_f$ = 2.5 ns (10% - 90%)

$V_{CC} = V_{CC}$ (AUX) = +2.0 V
V_{EE} = −3.2 V

Fig. 7. TRANSIENT INPUT CURRENT TEST CIRCUIT AND WAVEFORMS

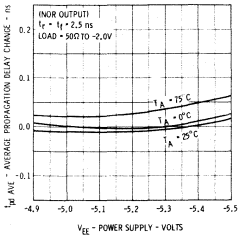




$t_r = t_f$ = 2.5 ns (10% - 90%)

This test provides a measure of the average value of C_{IN}; also current mismatch in the line.
$V_{CC} = V_{CC}$ (AUX) = +2.0 V
V_{EE} = −3.2 V

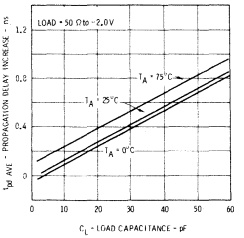
TYPICAL AVERAGE PROPAGATION DELAY CHANGE VERSUS POWER SUPPLY



Reference:
AC Electrical Characteristic

$$t_{pd\ AVG} = \frac{t_{pd\ rising} + t_{pd\ falling}}{2}$$

TYPICAL PROPAGATION DELAY INCREASE VERSUS LOAD CAPACITANCE

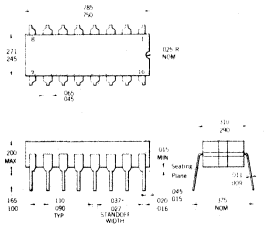


ABSOLUTE MAXIMUM RATINGS (above which useful life may be impaired)

Storage Temperature	−65° C to +150° C
Junction Temperature	+150° C
Supply Voltage V_{EE} (Continuous)	−6 Volts
Supply Voltage V_{EE} (Pulsed)	−8 Volts
Input Voltage	GND to V_{EE} (max)
Output Current	40 mA

PACKAGE INFORMATION

6B – 16 Lead SSI Dual In-Line Package



NOTES
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.0 grams

9581

EIGHT INPUT MULTIPLEXER

FAIRCHILD TEMPERATURE COMPENSATED ECL

GENERAL DESCRIPTION — The 9581 is a high speed, temperature compensated ECμL eight input multiplexer compatible with all other members of the 9500 series of ECμL circuits. It provides in one package the ability to select one bit of data from up to eight sources. In addition, the 9581 can be used as a universal function generator to generate any logic function of four variables.

All 9500 series elements incorporate a unique temperature compensation network. This insures that significant parameters such as logic levels, noise margins and speed remain relatively constant over a wide temperature range. Input and output two kilohm pulldown resistors eliminate the necessity for external termination of lines up to six to eight inches and permit unused inputs to be left open. Package pin locations are chosen to reduce internal noise generation and crosstalk.

The device is packaged in the hermetic ceramic 16 pin dual in-line package and specified for operation over the temperature range 0°C to +75°C.

- **HIGH SPEED . . . 3.0 ns FROM DATA INPUT TO OUTPUT**
- **SEPARATE CURRENT SWITCH AND EMITTER FOLLOWER V_{CC} PINS — ELIMINATES NOISE COUPLING**
- **TEMPERATURE COMPENSATION**
- **INTERNAL PULLDOWN RESISTORS**
- **ENABLE INPUTS**
- **WIRED-OR CAPABILITY ON OUTPUT**
- **50 Ω LINE DRIVING CAPABILITY**
- **SINGLE —5.2 V POWER SUPPLY**
- **HERMETIC CERAMIC 16 PIN DUAL IN-LINE PACKAGE**

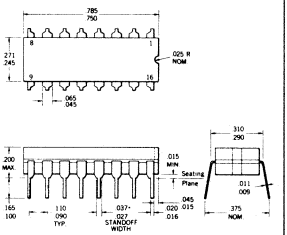
ABSOLUTE MAXIMUM RATINGS (above which useful life may be impaired)

Storage Temperature	−65°C to +150°C
Junction Temperature	+150°C
Supply Voltage V_{EE} (Continuous)	−6 Volts
Supply Voltage V_{EE} (Pulsed)	−8 Volts
Input Voltage	GND to V_{EE} (max)
Output Current	40 mA

ORDER INFORMATION

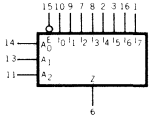
Specify U6B9581XXX for 16 pin Dual In-Line Package where XXX is 59X for the 0°C to +75°C temperature range.

PHYSICAL DIMENSIONS
16 LEAD DUAL IN-LINE



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin plated kovar
Package weight is 2.0 grams
The .037/.027 dimensions does not apply to the corner leads

LOGIC SYMBOL



V_{CC} = GND (Pins 4 & 5)
V_{EE} = −5.2 V (Pin 12)

Fig. 1

FUNCTIONAL DESCRIPTION

The 9581 eight input multiplexer uses the non-saturating, current switch-emitter follower circuit configuration to achieve high speed. In addition series gating and other current mode design techniques are incorporated to implement the circuits with minimum propagation delays and minimum power dissipation. Data encounters only one gate delay from one of the eight inputs to the output.

The 9581 is fundamentally a high speed semiconductor implementation of a single-pole eight-position switch. Three address lines select one out of the eight data inputs and feed this input to the output (Z). An active low enable forces the output LOW if held HIGH. The logic function provided at the output is:

$$Z = E \bullet (I_0 \bullet \overline{A}_0 \bullet \overline{A}_1 \bullet \overline{A}_2 + I_1 \bullet A_0 \bullet \overline{A}_1 \bullet \overline{A}_2 + I_2 \bullet \overline{A}_0 \bullet A_1 \bullet \overline{A}_2 + I_3 \bullet A_0 \bullet A_1 \bullet \overline{A}_2 + I_4 \bullet \overline{A}_0 \bullet \overline{A}_1 \bullet A_2 + I_5 \bullet A_0 \bullet \overline{A}_1 \bullet A_2 + I_6 \bullet \overline{A}_0 \bullet A_1 \bullet A_2 + I_7 \bullet A_0 \bullet A_1 \bullet A_2).$$

(Since the enable is an active low input, the E in the equation implies pin 15 must be LOW to activate Z).

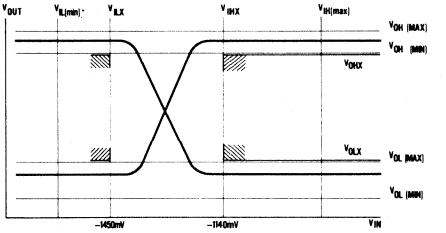
The 9581 provides the ability to select from or sequence eight data sources. It may therefore be used as a parallel to serial converter by sequentially advancing through the input address combinations.

The device may also be used as a universal logic element capable of generating any function of four variables by proper manipulation of the inputs. The wire-ORable outputs and the input enable permit easy expansion of several 9581's to form multiplexers with more than eight inputs.

Fig. 2 — TRUTH TABLE

INPUTS											OUTPUT
A_0	A_1	A_2	$\overline{E}$	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	Z
L	L	L	L	L	X	X	X	X	X	X	X	L
L	L	L	L	H	X	X	X	X	X	X	X	H
H	L	L	L	X	L	X	X	X	X	X	X	L
H	L	L	L	X	H	X	X	X	X	X	X	H
L	H	L	L	X	X	L	X	X	X	X	X	L
L	H	L	L	X	X	H	X	X	X	X	X	H
H	H	L	L	X	X	X	L	X	X	X	X	L
H	H	L	L	X	X	X	H	X	X	X	X	H
L	L	H	L	X	X	X	X	L	X	X	X	L
L	L	H	L	X	X	X	X	H	X	X	X	H
H	L	H	L	X	X	X	X	X	L	X	X	L
H	L	H	L	X	X	X	X	X	H	X	X	H
L	H	H	L	X	X	X	X	X	X	L	X	L
L	H	H	L	X	X	X	X	X	X	H	X	H
H	H	H	L	X	X	X	X	X	X	X	L	L
H	H	H	L	X	X	X	X	X	X	X	H	H
X	X	X	H	X	X	X	X	X	X	X	X	L

Fig. 3 — NOISE MARGIN SPECIFICATION POINTS (DATA LINES)



Corner points indicated on the transfer characteristics represent the worst case points (thresholds) at which the device will start to switch. The values V_{ILX} and V_{IHX} define the maximum width of the transition region.

D.C. ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $+75°C$, $V_{CC} = Gnd$, $V_{EE} = -5.2$ V)

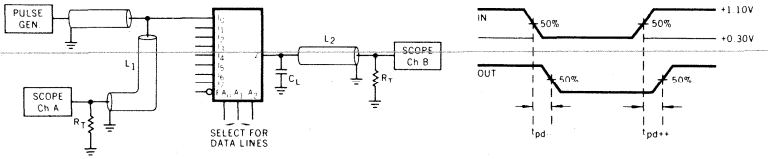
SYMBOL	CHARACTERISTIC	LIMITS 0°C MIN.	0°C TYP.	0°C MAX.	+25°C MIN.	+25°C TYP.	+25°C MAX.	+75°C MIN.	+75°C TYP.	+75°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	−905	−850	−795	−905	−850	−795	−895	−840	−785	mV	FO = 1 Gate
		−945	−890	−835	−945	−890	−835	−945	−890	−835	mV	FO = 5 Gates
		−980	−925	−870	−980	−925	−870	−980	−925	−870	mV	$R_L = 50\ \Omega$ to −2.0 V
V_{OL}	Output Low Voltage	−1755	−1670	−1585	−1755	−1670	−1585	−1755	−1670	−1585	mV	FO = 1 Gate
		−1795	−1710	−1625	−1795	−1710	−1625	−1795	−1710	−1625	mV	FO = 5 Gates
		−1785	−1700	−1615	−1785	−1700	−1615	−1785	−1700	−1615	mV	$R_L = 50\ \Omega$ to −2.0 V
V_{OHX}	Data Lines Output High Voltage at $V_{in} = -1140$ mV	−915			−915			−905			mV	FO = 1 Gate
		−955			−955			−955			mV	FO = 5 Gates
		−990			−990			−990			mV	$R_L = 50\ \Omega$ to −2.0 V See Fig. 3
V_{OLX}	Data Lines Output Low Voltage at $V_{in} = -1450$ mV			−1575			−1575			−1575	mV	FO = 1 Gate
				−1615			−1615			−1615	mV	FO = 5 Gates
				−1605			−1605			−1605	mV	$R_L = 50\ \Omega$ to −2.0 V See Fig. 3
V_{IHX}	Select Lines Input High Threshold Voltage	−1140			−1140			−1140			mV	Guaranteed Input High Voltage
V_{ILX}	Select Lines Input Low Voltage			−1450			−1450			−1450	mV	Guaranteed Input Low Voltage
$I_{IN(1)}$	Input Current at V_{IH}		2.30	3.15		2.25	3.10		2.15	3.00	mA	$V_{IH} = -900$ mV to each Input Sequentially
$I_{IN(0)}$	Input Current at V_{IL}		1.80	2.40		1.75	2.35		1.65	2.25	mA	$V_{IL} = -1700$ mV to each Input Sequentially
I_{PS}	Power Supply Current		48		40	50	67		55		mA	All Inputs Open

A.C. ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $+75°C$)

SYMBOL	CHARACTERISTIC	LIMITS 0°C TYP.	25°C MIN.	25°C TYP.	25°C MAX.	75°C MIN.	75°C TYP.	75°C MAX.	UNIT	CONDITIONS
t_{pd}	Propagation Delay									See Fig. 4, 5 & 6
	Data Lines	3.2		3.2	4.3		3.2		ns	$R_L = 50\ \Omega$ to Gnd
	Select Lines	5.5		5.5	7.5		5.5		ns	$C_L < 5.0$ pF
	Enable Lines	3.5		3.5	4.8		3.5		ns	$t_r = t_f = 2.5$ ns
I_T	Transient Input Current			2.5	3.5				mA	See Fig. 7

SWITCHING TIME CIRCUITS AND WAVEFORMS

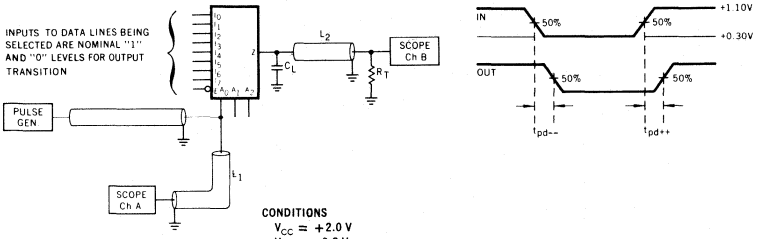
Fig. 4 — DATA LINES TO OUTPUT



CONDITIONS
$V_{CC} = +2.0$ V
$V_{EE} = -3.2$ V
$R_L = 50\ \Omega = R_T$ (Scope input impedance)
C_L = jig and stray capacitance < 5 pF
$L_1 = L_2$ equal 50 Ω impedance lines
Input signal $t_r = t_f = 2.5$ ns (10% - 90%)
With no circuit under test

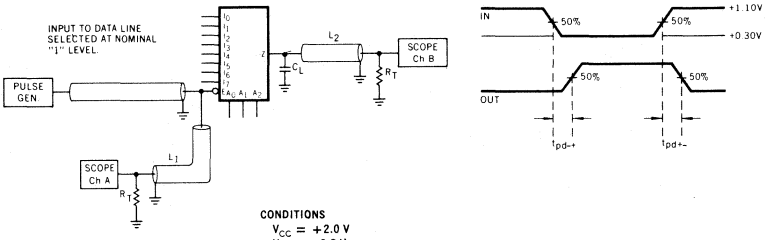
SWITCHING TIME CIRCUITS AND WAVEFORMS (CONT'D)

Fig. 5 — SELECT LINES TO OUTPUT



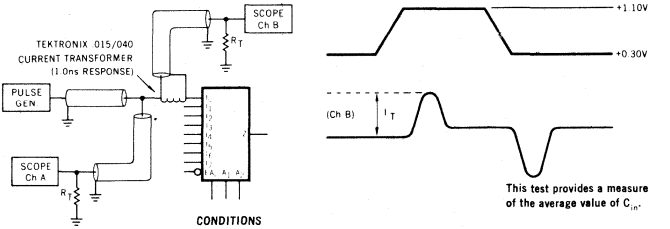
CONDITIONS
$V_{CC} = +2.0$ V
$V_{EE} = -3.2$ V
$R_L = 50\ \Omega = R_T$ (Scope input impedance)
C_L = jig and stray capacitance < 5 pF
$L_1 = L_2$ equal 50 Ω impedance lines
Input signal $t_r = t_f = 2.5$ ns (10% - 90%)
With no circuit under test

Fig. 6 — ENABLE TO OUTPUT



CONDITIONS
$V_{CC} = +2.0$ V
$V_{EE} = -3.2$ V
$R_L = 50\ \Omega = R_T$ (Scope input impedance)
C_L = jig and stray capacitance < 5 pF
$L_1 = L_2$ equal 50 Ω impedance lines
Input signal $t_r = t_f = 2.5$ ns (10% - 90%)
With no circuit under test

Fig. 7 — TRANSIENT INPUT CURRENT TEST CIRCUIT AND WAVEFORMS



CONDITIONS
$V_{CC} = +2.0$ V
$V_{EE} = -3.2$ V
$R_T = 50\ \Omega$ (Scope input impedance)
Input signal $t_r = t_f = 2.5$ ns (10% - 90%)
With no circuit under test

9582

MULTI-FUNCTION LINE RECEIVER/AMPLIFIER

FAIRCHILD TEMPERATURE COMPENSATED ECL

GENERAL DESCRIPTION – The 9582 is 3 differential input amplifiers. Both the true and complement outputs are temperature compensated to be compatible with other ECL 9500 products. With appropriate connection of the base pins the device will function as a differential line receiver; Schmitt trigger; high speed comparator; broad band video, I.F. or R.F. amplifier; or oscillator. V_{ref} is made available to allow use of this device as a high input impedance buffer gate.

FEATURES:

- **DIFFERENTIAL INPUT**
- **TRUE AND COMPLIMENT OUTPUT**
- **HIGH INPUT IMPEDANCE**
- **HIGH SPEED – 2.5 ns**
- **REFERENCE VOLTAGE AVAILABLE FOR GATE OR LINEAR OPERATION**
- **PACKAGE GAIN OVER 50 dB FOR LINE RECEIVER, VIDEO OR RF APPLICATION.**

PIN NAMES

A_N = Positive (Non-Inverting) Input of Amplifier N
$\bar{A}_N$ = Negative (Inverting) Input of Amplifier N
Q_N = True (Non-Inverting) Output of Amplifier N
$\bar{Q}_N$ = Compliment (Inverting) Output of Amplifier N
V_R = Reference Voltage

ORDER INFORMATION – Specify U6B9582XXX for 16 pin Dual In-Line Package, where XXX is 59X for the 0°C to 75°C temperature range.

LOGIC SYMBOL

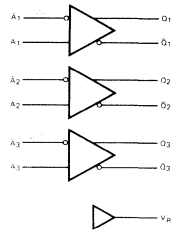


Fig. 1

CONNECTION DIAGRAM
DIP (TOP VIEW)

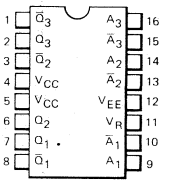
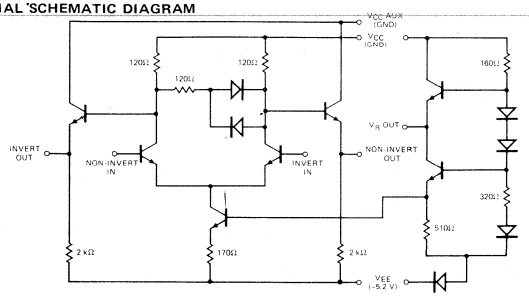


Fig. 2

PARTIAL SCHEMATIC DIAGRAM



For maximum Bandwidth, an additional R_L to V_{EE} of 220 ohms on each output will permit a bandwidth of >80 MHz at 3 dB.

Unused inputs must be grounded.

Fig. 3

FUNCTIONAL DESCRIPTION – The 9582 consists of three differential amplifiers with emitter-follower outputs and a bias (V_R) driver. This device is designed to be used as a line receiver in applications requiring a medium gain, high band-width limiting differential amplifier.

The ECL 9582 Triple line receiver is used primarily to receive data from balanced twisted pair lines, as indicated in Figure 4. Any 9500 gate with differential outputs may be used to drive the twisted pair line. The line is terminated in its characteristic impedance (around 125 ohms). A voltage divider is formed between the high-level gate output, the terminating resistor, and the pull-down resistor on the low-level gate output. The equivalent DC circuit is shown in Figure 5. The voltage swing across the terminating resistor (R_T) is typically 260 mV. Any input voltage swing in excess of 160 mV ensure the output levels due to the voltage gain of the 9582. The output of the line receiver is similar to a standard ECL 9500 gate. For worst-case pull-down resistors in the driving gate (2.0k ohms ±20%) and a V_{OH} min, the differential drop across an R_T of 100 ohms is ±185 mV.

Very long lines may be used with excellent results. The only restriction on line length (other than common mode noise) is series line resistance. The nominal voltage drop across R_T is actually shared with the series resistance of the twisted pair line. The resistance of No. 22 AWG wire averages about .016 ohms per foot, while No. 24 AWG wire averages about .026 ohms per foot. For very long lines, an additional voltage drop across R_T is easily obtained by paralleling additional pull-down resistors with those internal to the driver gate. For example, by paralleling a 2.0k ohm resistor with each output, the voltage drop across R_T is effectively doubled.

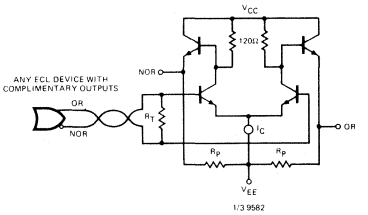
Extensive data have shown that a positive transient of 1.0 V or a negative, transient of 1.5 V may be introduced on the twisted pair line (i.e., between driver and receiver system grounds) before noise can propagate through another ECL device tied to the line receiver output. This method of data transmission is useful at frequencies to 100 MHz.

A twisted pair transmission line is recommended for clock distribution in high-speed systems since distribution skew time may be balanced out by adjusting line lengths. Propagation delay times are approximately 1.0 ns per eight inches of line.

In system design it is often convenient to organize information transfer with a data bus or "party-line" approach. In this application, one of many sources may "talk" to the common data line and multiple receivers may "listen". Figure 6 illustrates such a data bus utilizing ECL 9500 gates as drivers and ECL 9582 as line receivers. Note that the line is unbalanced, but this will in turn allow all drivers to be ORed together. Bandwidth of data distribution is excellent. The technique may be used to 100 MHz over the entire industrial temperature range. Noise immunity is also good due to the low impedance methods of transmission and the common mode rejection of the line receiver. The following results were obtained during an evaluation of the data bus shown in Figure 6 under the following conditions:

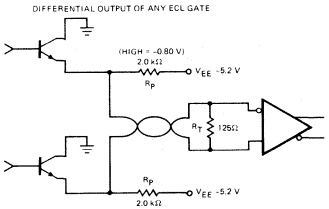
Number of driver gates: 10
Number of receivers: 10
Line length: 10 feet
Maximum operating frequency: 100 MHz
Total terminating resistance: 60 ohms, i.e., 120Ω at each end.
Differential power supply voltage from transmitter gate to receiver gate: ±5.0%

The Triple line receiver can also be used in many linear applications. The minimum differential voltage gain is 6 volt/volt, with a 3.0 dB bandwidth of typically 70 MHz for each differential amplifier. The device makes an excellent FM limiter with minimal phase shift. By employing feedback, both selective band-pass amplifiers and notch frequency rejection amplifiers may be built.



$100\Omega < R_T < 150\Omega$
Driver worst-case R_E = 2.2 kΩ @ R_T = 100Ω
Differential gain = 7.0 V/V
Common mode rejection > 60 dB
Common mode voltage rejection range
(voltages between driver and receiver grounds) = +1.5 V
-1.0 V

Fig. 4 TWISTED PAIR LINE RECEIVER



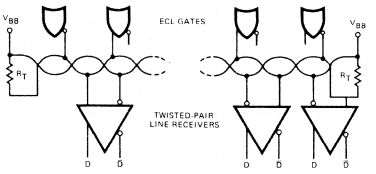
V_R = VOLTAGE DROP ACROSS R_T (TERMINATING RESISTOR)

$$V_R = \frac{(5.2\ V - 0.80\ V)\ (R_T)}{2\ k\Omega + R_T}$$

$$= \frac{(4.40)\ (125)}{2125}$$

$$= 260\ mV$$

Fig. 5 LINE RECEIVER DC EQUIVALENT CIRCUIT



System Design Criteria

1. A minimum of two emitter pull-down resistors is recommended in the driver gates.
2. R_T should be Z_{out} of the twisted pair line: 100 to 125 ohms
3. Either OR or NOR outputs may drive the line.
4. All driver gates are ORed together.
5. The line receiver output is Data or Data depending upon the input and output configurations.
6. V_{BB} should be able to source 6.0 mA or sink 7.0 mA total current. This is accomplished by the addition of a 500Ω resistor from V_R (Pin 11) to V_{EE}.

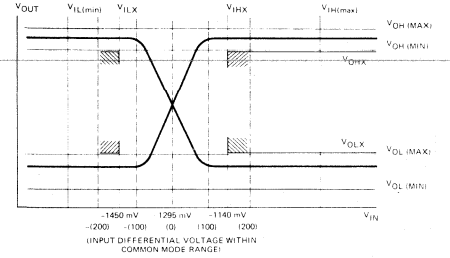
Fig. 6 DATA BUS DRIVING WITH ECL 9500

ABSOLUTE MAXIMUM RATINGS (above which useful life may be impaired)

Storage Temperature	−65°C to +150°C
Junction Temperature	+150°C
Supply Voltage V_{EE} (Continuous)	−6 Volts
Supply Voltage V_{EE} (Pulsed)	−8 Volts
Input Voltage	GND to V_{EE} (max)
Output Current	40 mA

DC ELECTRICAL CHARACTERISTICS (Operating Temperature Range 0°C to 75°C, V_{CC} = GND, V_{EE} = −5.2 V)

SYMBOL	CHARACTERISTIC	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	CONDITIONS (Measured with $\overline{\text{Inputs}}$: $\bar{A}_1$, $\bar{A}_2$, $\bar{A}_3$; connected to V_R)
V_{OH}	Output Voltage High	−900	−850	−800	mV	F.O. = 1 Gate V_{IL} = −1700 mV for NOR Gate
		−940	−890	−840	mV	F.O. = 5 Gates V_{IH} = −900 mV for OR Gate
		−975	−925	−875	mV	50Ω to −2.0 V
V_{OL}	Output Voltage Low	−1745	−1670	−1595	mV	F.O. = 1 Gate V_{IL} = −1700 mV for OR Gate
		−1785	−1710	−1635	mV	F.O. = 5 Gates V_{IH} = −900 mV for NOR Gate
		−1775	−1700	−1625	mV	50Ω to −2.0 V
V_{OHX}	Ouptut Voltage High at V_{IN} (threshold)	−910			mV	F.O. = 1 Gate V_{ILX} = −1450 mV for NOR Gate } To Each Input Sequentially
		−950			mV	F.O. = 5 Gates V_{IHX} = −1140 mV for OR Gate } To Each Input Sequentially
		−985			mV	50Ω to −2.0 V See Fig. 7
V_{OLX}	Ouptut Voltage Low at V_{IN} (threshold)			−1585	mV	F.O. = 1 Gate V_{ILX} = −1450 mV for OR Gate } To Each Input Sequentially
				−1625	mV	F.O. = 5 Gates V_{IHX} = −1140 mV for NOR Gate } To Each Input Sequentially
				−1615	mV	50Ω to −2.0 V See Fig. 7
I_{PS}	Power Supply Current	35	48	65	mA	All Inputs Open Except A_1, A_2, A_3 to V_R



Corner points indicated on the transfer characteristics represent the worst case points (thresholds) at which the device will start to switch. The values V_{ILX} and V_{IHX} define the maximum width of the transition region.

Fig. 7 NOISE MARGIN SPECIFICATION POINTS

FOR LINEAR APPLICATIONS OF THE 9582

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = GND, V_{EE} = -5.2 V)

PARAMETER (see definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Differential Voltage Gain		6.0	7.0		V/V
Bandwidth	Open output		70		MHz
Risetime	R_S = 50Ω		2.5		ns
Propagation Delay	R_S = 50Ω		2.4		ns
Input Resistance			1.3		kΩ
Input Capacitance				5.0	pF
Input Offset Current			7.0		μA
Input Bias Current			40		μA
Input Offset Voltage			5.0		mV
Input Voltage Range	Around V_R	±1.3			V
Common Mode Rejection Ratio	V_{cm} = ±1 V, f ≤ 100 kHz Around V_R	60			dB
Supply Voltage Rejection Ratio	ΔV_S = ±0.5 V	60			dB
Output Common Mode Voltage			-1.3		V
Output Voltage Swing		0.8			Vpp
Output Sink Current		1.3	2.0		mA
Output Source Current				40	mA
Output Resistance			10	20	Ω

DEFINITION OF TERMS

DIFFERENTIAL VOLTAGE GAIN – The ratio of the change in the differential output voltage to the change in voltage between the input terminals producing it.

BANDWIDTH – The frequency at which the differential gain is 3 dB below its low frequency value.

RISE TIME – The time required for an output voltage step to change from 10% to 90% of its final value.

PROPAGATION DELAY – The interval between the application of an input voltage step and its arrival at either output, measured at 50% of the final value.

INPUT RESISTANCE – The resistance seen looking into either input terminal with the other grounded.

INPUT OFFSET CURRENT – The difference between the currents into the two input terminals.

INPUT BIAS CURRENT – The average of the two input currents.

INPUT VOLTAGE RANGE – The range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.

COMMON MODE REJECTION RATIO – The ratio of a change in input common mode voltage to the resulting change in output offset voltage referred to the input.

SUPPLY VOLTAGE REJECTION RATIO – The ratio of a change in supply voltage to the resulting change in output offset voltage referred to the input.

OUTPUT COMMON MODE VOLTAGE – The average of the voltages at the two output terminals.

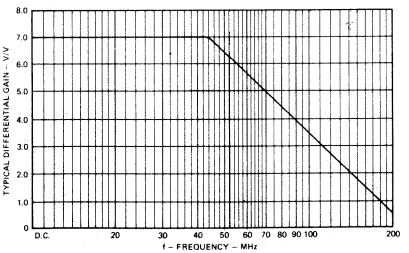
OUTPUT VOLTAGE SWING – The peak-to-peak output swing that can be obtained without clipping. This includes the unbalance caused by output offset voltage.

OUTPUT SINK CURRENT – The peak negative current available at either output of the amplifier.

OUTPUT SOURCE CURRENT – Peak positive current available at either output of the amplifier.

OUTPUT RESISTANCE – The resistance seen looking into either output terminal.

9582 LINE RECEIVER TYPICAL DIFFERENTIAL GAIN VERSUS FREQUENCY



A.C. ELECTRICAL CHARACTERISTICS (Temperature Range 0°C to +75°C, V_{CC} = GND, V_{EE} = –5.2 V)

SYMBOL	CHARACTERISTIC	LIMITS									UNITS	CONDITIONS
		0°C			+25°C			+75°C				
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
t_{pd}	Propagation Delay											
	t_{pd-} –		2.3			2.3	3.5		2.5		ns	See Fig. 10
			2.2			2.2	3.5		2.4		ns	R_L = 50Ω to –2.0 V
			2.4			2.4	3.5		2.6		ns	C_L <5.0 pF
			2.5			2.5	3.2		2.7		ns	$t_r = t_f \approx 2.5$ ns
t_r	Rise Time		3.0		1.5	3.0	4.5		3.0		ns	
t_f	Fall Time		3.0		1.5	3.0	4.5		3.0		ns	
I_T	Transient Input Current Standard Gate					2.5	3.5				mA	See Fig. 11

Fig. 8
TYPICAL AVERAGE PROPAGATION DELAY CHANGE VERSUS POWER SUPPLY

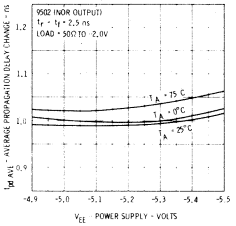
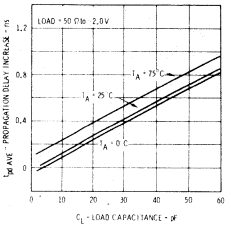
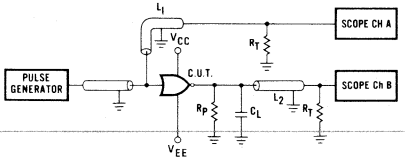


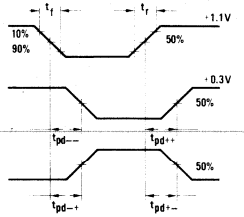
Fig. 9
TYPICAL PROPAGATION DELAY INCREASE VERSUS LOAD CAPACITANCE $t_{pd\ AVE}$ (OR OUTPUT)



$$t_{pd\ ave} = \frac{t_{pd\ rising} + t_{pd\ falling}}{2}$$

REFERENCE: A.C. ELECTRICAL CHARACTERISTICS



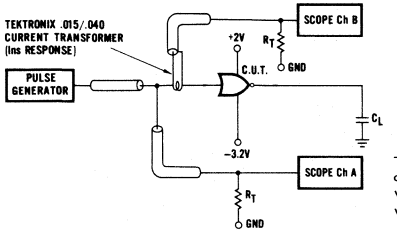


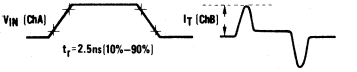
L_1 and L_2 = equal length 50Ω impedance lines
$R_L = R_T$ = 50Ω Termination of Scope
C_L = Jig and Stray Capacitance <5.0 pF

$t_r = t_f$ = 2.5 ns (10% – 90%) Jig setup with no circuit under test
$V_{CC} = V_{CC}$ (AUX) = +2.0 V
V_{EE} = –3.2 V

Fig. 10 SWITCHING TIME TEST CIRCUIT AND WAVEFORM

SWITCHING CHARACTERISTICS (Cont'd)





This test provides a measure of the average value of C_{IN}; also current mismatch in the line.

$V_{CC} = V_{CC}$ (AUX) = +2.0 V $R_T = 50\Omega$ (Scope input impedance)

$V_{EE} = -3.2$ V Input signal $t_r = t_f = 2.5$ ns (10% – 90%)

With no circuit under test

Fig. 11 TRANSIENT INPUT CURRENT TEST CIRCUIT AND WAVEFORMS

INTERCONNECTION RECOMMENDATIONS

All high speed ECL circuits demand that special precautions be taken for optimum system performance. A ground plane must be provided for a good, low impedance, ground current return path and to transform interconnections into microstrip transmission lines. The voltage supply line should be well decoupled with small ceramic capacitors throughout each card between V_{EE} and the ground plane and by including at least one larger tantalum capacitor per card.

Typical microstrip lines have a characteristic impedance between 50 and 150 ohms with the lower being more desirable in ECL systems. For local interconnects the internal 2 kΩ resistors provide adequate termination but for optimum performance lines longer than 6 or 8 inches in length should be terminated in their characteristic impedance.

Lines up to 12 inches may be left unterminated if a degraded waveform can be tolerated with the resultant decrease in speed and increase in ringing.

Microstrip interconnections may be terminated by a resistor to a –2 volt supply:

Alternately, a 2 resistor divider network may be used with $R_1 = 1.6$ R connected to ground and $R_2 = 2.6$ R connected to V_{EE}.

Series terminating resistors decrease noise immunity and slow rise and fall times, but can still be used if these effects are tolerable. In addition, care must be taken to avoid glitches in the threshold region of the waveform occurring at certain combinations of line length and series resistor value.

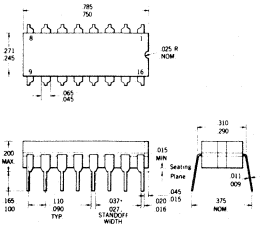
A single terminated wire running over a ground screen can be used for backpanel interconnections up to 4 or 5 inches in length, but terminated coaxial cables or terminated twisted pairs of wire are required for longer interconnections.

LINE DRIVING CAPABILITY

The 9500 series ECL circuits are capable of driving fairly long lines if the previous recommendations are followed. 50 ohm coaxial cables 10 feet in length or longer and properly terminated may be driven with almost no degradation in the waveform. The normal delay due to the finite speed of the signal traveling down the cable will be encountered in addition to a slight decrease in signal swing. This decrease caused by the attenuation of the cable (about 40 mV for 10 feet of 50 ohm coax) will lower the noise immunity of the receiving circuit by the same amount. Care must be exercised to ensure the ground potentials at the driving and receiving ends of a line are equal and no differential noise is present.

PACKAGE INFORMATION

6B – 16 LEAD DUAL IN-LINE



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin plated kovar
*The .037/.027 dimensions does not apply to the corner leads

ECL/MSI 95H84
2-BIT ADDER/SUBTRACTOR
FAIRCHILD TEMPERATURE COMPENSATED ECL

GENERAL DESCRIPTION – The 95H84 is a temperature compensated ECL/MSI circuit that performs addition and subtraction on a two bit word with full internal carry lookahead. For expansion to larger words no additional carry lookahead units are needed to maintain maximum speed.

The many possible applications of this device include: high speed arithmetic units for very large words, high speed adder/subtractor for serial machines, high speed multipliers for fast fourier transform computers, high speed function generators and code converters.

Add/Subtract delay for different size words is:

Word Size	Typical	Max.
3 – 6	10 ns	16 ns
7 – 12	12 ns	18 ns
13 – 20	14 ns	21 ns
21 – 30	16 ns	24 ns
31 – 42	18 ns	27 ns
43 – 56	20 ns	30 ns
57 – 72	22 ns	33 ns

- **HIGH SPEED . . . 1.5 ns INTERNAL GATE DELAYS**
- **ADDS AND SUBTRACTS WITH ONE DEVICE**
- **INTERNAL CARRY LOOKAHEAD FOR VERY LARGE WORDS**
- **SEPARATE CURRENT SWITCH EMITTER FOLLOWER V_{CC} PINS – ELIMINATE NOISE COUPLING**
- **TEMPERATURE COMPENSATION**
- **INTERNAL 2kΩ PULL DOWNS**
- **50Ω LINE DRIVE CAPABILITY**
- **SINGLE –5.2 VOLT POWER SUPPLY**
- **HERMETIC CERAMIC 16 PIN DIP**

PIN NAMES

A_0, B_0, A_1, B_1	Operand Inputs
F_0, F_1	Function Outputs
S	Subtract Select Line
C_{IN}, C_0	Carry In and Out
LA_{IN}, LB_{IN}	Carry Lookahead Inputs from Previous Unit
LA_0, LB_0	Carry Lookahead Outputs to Following Unit

ORDER INFORMATION – Specify U6B95H8459X for 16 pin dual in-line package and 0°C to 75°C temperature range.

LOGIC DIAGRAM

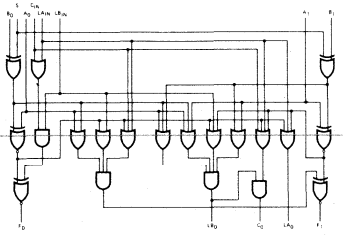


Fig. 3

LOGIC SYMBOL

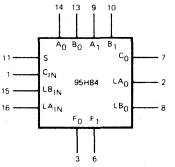
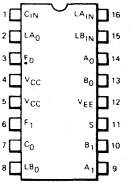


Fig. 1

CONNECTION DIAGRAM
DIP (TOP VIEW)



Pins 4 and 5 = V_{CC} = GND
Pin 12 = V_{EE} = –5.2 V

Fig. 2

FAIRCHILD
SEMICONDUCTOR

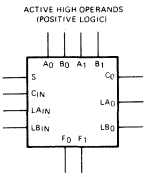
FUNCTIONAL DESCRIPTION — The 95H84 performs addition and one's complement subtraction (two's complement when a carry in is supplied) on a two bit word.

High speed is assured by internal carry lookahead, use of high speed internal gates and a novel multistage lookahead scheme which eliminates many interconnecting lines.

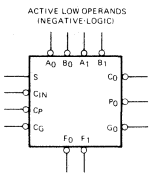
The 95H84 can be used with either Active High (Positive Logic) operands or Active Low (Negative Logic) operands. The logic symbols for both are shown below.

LOGIC SYMBOLS

ACTIVE HIGH OPERANDS (POSITIVE LOGIC)



ACTIVE LOW OPERANDS (NEGATIVE LOGIC)



LOGIC EQUATIONS — Active High Operands

$F_0 = A_0 \oplus B_0 \oplus S \oplus (LA_{IN} + C_{IN})LB_{IN}$

$F_1 = A_1 \oplus B_1 \oplus S \oplus [(S \oplus \overline{A}_0 \oplus B_0 + C_{IN} + LA_{IN})(A_0 + S \oplus B_0)(LB_{IN} + S \oplus \overline{A}_0 \oplus B_0)]$

$LA_0 = \overline{A}_1 \oplus B_1 \oplus S + LA_{IN} + \overline{A}_0 \oplus B_0 \oplus S$

$LB_0 = (A_1 + B_1 \oplus S)(\overline{A}_1 \oplus S \oplus B_1 + LB_{IN} + \overline{A}_0 \oplus B_0 \oplus S)(A_0 + A_1 + B_0 \oplus S)(A_0 + B_1 \oplus S + B_0 \oplus S)$

$C_0 = LB_0(LA_0 + C_{IN})$

MODE SELECTION — The 95H84 will add when the subtract line is low and will subtract (A – B) utilizing one's complement addition when the subtract line is high. Two's complement subtraction can be performed by supplying a carry in while subtracting. LA_{IN}, LB_{IN}, LA_0 and LB_0 are carry lookahead inputs and outputs with fast through delay for utilization in the high speed lookahead configuration. Whenever these inputs are not used, LA_{IN} should be low (left floating) and LB_{IN} should be high (.9 volts from a suitable source such as an unused ECL gate) and the carry in signal supplied to C_{IN}.

MODE SELECTION TABLE

Mode	S	Positive Logic C_{IN}*	Negative Logic C_{IN}*
Add	L	L	H
Subtract (one's complement)	H	L	H

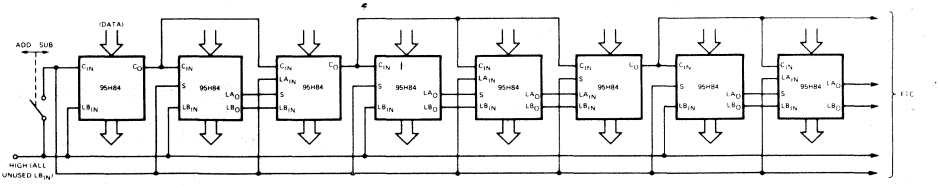
*Logic levels for no carry in (LB_{IN} = H, LA_{IN} = L)

APPLICATIONS

The 95H84 can be connected in a novel high speed lookahead scheme which does not require an additional lookahead logic unit. The adders are connected as shown below.

High speeds are obtained by using lookahead signals to generate partial sums in adder groups simultaneously with carriers propagating between these partial sum groups, thus allowing an optimum relationship between the number of bits and delay as shown in the Delay Table.

ADD/SUBTRACT (Two's Complement)

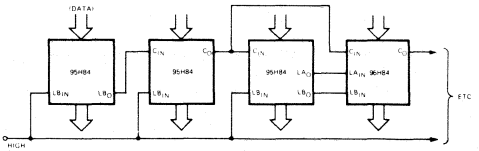


The adders are arranged in succession/larger groups. The units within these groups receive lookahead signals generated from prior units within the group to form a partial sum. By starting with one unit in the first group and progressively increasing the group size by one, carry inputs from previous groups arrive just as the lookahead signals have propagated through the group to form a final sum.

The last unit of the group therefore generates the carry for the next group in only one carry delay from the input carry.

The add/subtract scheme shown above performs two's complement subtraction by supplying carry in the subtract mode if A–B ≥ 0 in a carry out is present and F_{OUT} equals the binary output of the difference, while if A–B < 0 no carry out is present and F_{OUT} is the two's compliment of the difference.

ADD ONLY (Typical 10ns for 8-Bits)



When adding only (with no carry in) the carry from the first stage can be obtained from LB_0 approximately 2ns faster than from C_0.

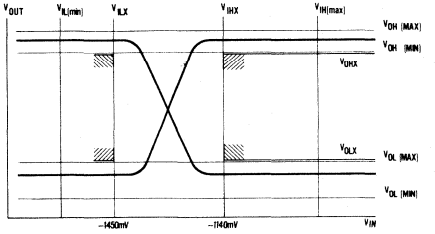
D.C. ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (T_A = 0°C to 75°C, V_{EE} = –5.2 V)

SYMBOL	CHARACTERISTIC	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	CONDITIONS	
V_{OH}	Output High Voltage	–930 –970 –1010	–860 –910 –950	–800 –850 –890	mV	FO = 1 Gate FO = 5 Gates 50Ω to –2.0 V	V_{IN} = –0.900 V
V_{OL}	Output Low Voltage	–1780 –1830 –1810	–1690 –1740 –1720	–1600 –1650 –1630	mV	FO = 1 Gate FO = 5 Gates 50Ω to –2.0 V	V_{IN} = –1.700 V
V_{OHC}	Output High Corner Point (See Fig. 4)	–940 –980 –1020			mV	FO = 1 Gate FO = 5 Gates 50Ω to –2.0 V	V_{IN} = V_{IHX} V_{IN} = V_{ILX}
V_{OLC}	Output Low Corner Point (See Fig. 4)			–1590 –1640 –1620	mV	FO = 1 Gate FO = 5 Gates 50Ω to –2.0 V	V_{IN} = V_{ILX} V_{IN} = V_{IHX}
V_{IHX}	Input High Level	–1140			mV	Guaranteed Input High Threshold Voltage	
V_{ILX}	Input Low Level			–1450	mV	Guaranteed Input Low Threshold Voltage	
$I_{IN(H)}$	Input Current at V_{IH} Enable Input		2.25 2.65	3.15 3.85	mA	V_{IN} = –900 mV to Each Input Sequentially	
$I_{IN(L)}$	Input Current at V_{IL} Enable Input		1.75 2.00	2.40 2.65	mA	V_{IN} = –1700 mV to Each Input Sequentially	
I_{PS}	Power Supply Current	72.8	93	114.8	mA	V_{EE} = –5.2 V, All Inputs Open	

A.C. ELECTRICAL CHARACTERISTICS (V_{CC} = GND, V_{EE} = –5.2 V)

SYMBOL	CHARACTERISTIC	0°C TYP.	25°C MIN.	25°C TYP.	25°C MAX.	75°C TYP.	UNITS	CONDITIONS
t_{pd}	C_{IN} to C_0 LA_{IN} to LA_0 LB_{IN} to LB_0	2.2		2.3	3.1	2.5	ns	Output R_L = 50Ω to –2.0V C_L ≤ 5 pF Input t_r, t_f = 2.2 ns, 10%–90%
	A_0, A_1, B_0, B_1 to F_0, F_1, LA_0, LB_0	4.4		4.6	6.2	4.9	ns	
	A_0, A_1, B_0, B_1 to C_0	6.0		6.2	8.3	6.5	ns	
	C_{IN} – F_0, F_1	6.0		6.2	8.3	6.5	ns	
	S to F_0, F_1, LA_0, LB_0, C_0	8.0		8.3	10.7	8.5	ns	
t_r t_f	Output Rise Time (10%–90%) Output Fall Time (10%–90%)	2.4	1.4	2.4	3.6	2.4	ns	

NOISE MARGIN SPECIFICATION POINT



Corner points indicated on the transfer characteristics represent the worst case points (thresholds) at which the device will start to switch. The values V_{ILX} and V_{IHX} define the maximum width of the transition region.

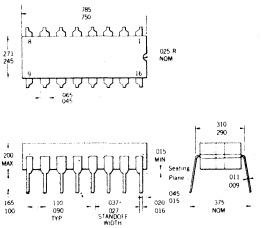
Fig. 4

ABSOLUTE MAXIMUM RATINGS (above which useful life may be impaired)

Storage Temperature	−65°C to +150°C
Junction Temperature	+150°C
Supply Voltage V_{EE} (Continuous)	−6 V
Supply Voltage V_{EE} (Pulsed)	−8 V
Input Voltage	GND to V_{EE} (max)
Output Current	40 mA

PACKAGE INFORMATION

6B – 16 LEAD SSI DUAL IN-LINE PACKAGE



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.0 grams
* The .037/.027 dimension does not apply to the corner leads.

95H90

VERY HIGH SPEED ÷ 10 / 11 PRESCALER

FAIRCHILD TEMPERATURE COMPENSATED ECL

GENERAL DESCRIPTION – The ECL 95H90 prescaler is a high speed ECL MSI device designed specifically for the communication and instrumentation manufacturer. In its simplest use it will divide any clock frequency up to 320 MHz, by 10. By using the 95H90, with other control logic a divide by "N" counter can be constructed.

By keeping all the high speed logic manipulation "on chip," a dramatic decrease in power and increase in reliability and wire-ability are made available at much lower cost than a comparable SSI function.

FEATURES

- **HIGH SPEED . . . 320 MHz (TYP.)**
- **÷10/11 ENABLE**
- **HIGH SPEED RESET**
- **SEPARATE CURRENT SWITCH EMITTER FOLLOWER V_{CC} PINS – ELIMINATE NOISE COUPLING**
- **TEMPERATURE COMPENSATION**
- **INTERNAL PULL DOWN**
- **50 Ω LINE DRIVE CAPABILITY**
- **SINGLE –5.2 VOLT POWER SUPPLY**
- **HERMETIC CERAMIC 16 PIN DIP**
- **COMPLEX MULTI-GATE CHIP REDUCES PACKAGE COUNT & POWER**
- **LOW CLOCK FEED-THROUGH OF ONLY 70 mV (TYP.)**
- **SMALL SIGNAL INPUT IMPEDANCE POSITIVE REAL FOR ALL FREQUENCIES**

PIN NAMES

$\overline{CP}_1$, $\overline{CP}_2$	Dual "OR" Clock Inputs (Active High)
$\overline{PE}_1$, $\overline{PE}_2$	Prescale by 11 (eleven) "AND" Enable Inputs (Active Low)
MS	Asynchronous Master Set (Active High)
Q_4	Assertion Output
$\overline{Q}_4$	Negative Output

ORDER INFORMATION

Specify U6B95H90XXX for 16 pin Dual In-Line package where XXX is 59X for the 0°C to +75°C and 56X for the –20°C to 100°C temperature range.

LOGIC SYMBOL

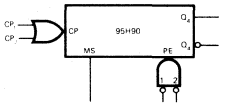


Fig. 1

CONNECTION DIAGRAM DIP (TOP VIEW)

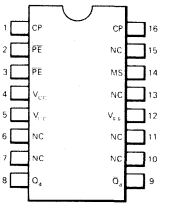


Fig. 2

LOGIC DIAGRAM

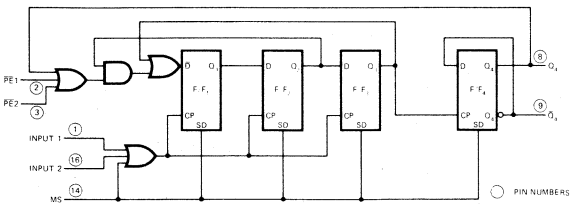


Fig. 3

COUNT SEQUENCE

Q_1	Q_2	Q_3	Q_4
H	H	H	H
L	H	H	H
L	L	H	H
L	L	L	H
H	L	L	H
H	H	L	H
L	H	H	L
L	L	H	L
L	L	L	L
H	L	L	L
H	H	L	L

NOTE: **"HHHH" is set state** and additional state for ÷11 mode.

FUNCTIONAL DESCRIPTION

The Device acts as a controllable (divide by 10/divide by 11) prescaler, accepting clock pulses of up to 320 MHz. Output Q_4 is low for 5 incoming clock pulses and high for the subsequent 5 or 6 incoming clock pulses, the decision between the two modes is made by the state of the two active low PE inputs. If both $\overline{PE}_1$ and $\overline{PE}_2$ are low 5.4 ns before the rising edge of Q_4, then Q_4 will stay high for 6 incoming clock pulses (divided by 11), if either $\overline{PE}_1$ or $\overline{PE}_2$ is high before the rising edge of Q_4, the output will stay high for 5 clock pulses (divided by 10).

The two input "OR" clock inputs can be used to combine two independent clock sources or one input can act as a clock enable (active low).

A master set is provided to initialize the prescaler. This input, when activated, overrides the clock and forces the prescaler into the HHHH state with Q_4 forced high and $\overline{Q}_4$ forced low. The prescaler will divide by 11 the first count cycle after being master set.

NOTE:
When using the 95H90 simply as a modulo 10 prescaler, the $\overline{Q}$ output may be connected to a $\overline{PE}$ input.

95H90 MODE SELECTION TABLE

$\overline{PE}_1$	$\overline{PE}_2$	PRESCALER MODULO
		Divide By
L	L	11
L	H	10
H	L	10
H	H	10

D. C. ELECTRICAL CHARACTERISTICS (Operating Temperature Range: T_A = 0°C to 75°C) (V_{CC} = GND, V_{EE} = −5.2V)

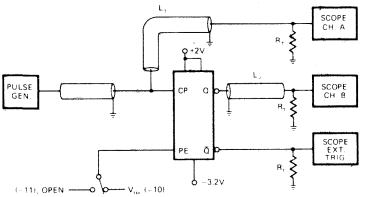
SYMBOL	CHARACTERISTIC	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	CONDITIONS
V_{OH}	Output Voltage High		−860 −910 −950		mV	FO= 1 Gate FO= 5 Gates R_L = 50 Ω to −2.0V V_{IN} = V_{IL} (−1700mV) or V_{IH} = (−900mV) as per Count Sequence
V_{OL}	Output Voltage Low		−1690 −1740 −1720		mV	FO= 1 Gate FO= 5 Gates R_L = 50 Ω to −2.0V V_{IN} = V_{IL} (−1700mV) or V_{IH} = (−900mV) as per Count Sequence
V_{OHC}	Output Voltage High at V_{IN} = V_{IX} (threshold)	−930 −970 −1010			mV	FO= 1 Gate FO= 5 Gates R_L = 50 Ω to −2.0V V_{IN} = V_{ILX} or V_{IHX} as per Count Sequence
V_{OLC}	Output Voltage Low at V_{IN} = V_{IX} (threshold)			−1605 −1655 −1635	mV	V_{IN} = V_{ILX} or V_{IHX} as per Count Sequence
V_{IHX}	Input High Threshold Voltage	−1140			mV	Guaranteed Input High Threshold Voltage
V_{ILX}	Input Low Threshold Voltage			−1450	mV	Guaranteed Input Low Threshold Voltage
$I_{IN(H)}$	Input Current High		2.40	3.65	mA	V_{IN} = −900mV to MS Input (Pin 14)
$I_{IN(H)}$	Input Current High		2.25	3.15	mA	V_{IN} = −900mV to other Inputs Sequentially
$I_{IN(L)}$	Input Current Low		1.75	2.40	mA	V_{IN} = −1700 mV to Each Input Sequentially
I_{PS}	Power Supply Current	66	90	119	mA	All Inputs Open

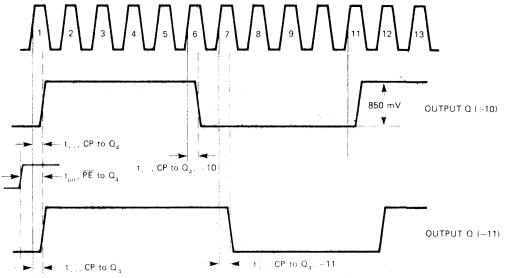
A.C. ELECTRICAL CHARACTERISTICS (T_A = 0°C to 75°C, V_{CC} = GND, V_{EE} = −5.2V)

SYMBOL	CHARACTERISTIC	LIMITS 0°C TYP.	25°C MIN.	25°C TYP.	25°C MAX.	75°C MIN.	75°C TYP.	75°C MAX.	UNITS	CONDITIONS
t_{pd}	Propagation Delay(50%-50%)									Output
	CP to Q_4, t_{pd++}	4.9		5.1	6.8		5.5		ns	R_L = 50Ω to −2.0V
	CP to Q_4, t_{pd--}	4.9		5.1	6.8		5.5		ns	C_L = 5.0pF
	MS to Q_4, t_{pd++}	5.3		5.7	7.6		6.5		ns	Input
	$\overline{PE}$ to Q_4, t_{pd++}(Note 1)	5.2		5.4			5.8		ns	$t_r = t_f$ = 2.2±0.1 ns (10%-90%)
t_r	Output Rise Time (10%-90%)	2.4	1.2	2.4	3.6		2.4		ns	
t_f	Output Fall Time (10%-90%)	2.4	1.2	2.4	3.6		2.4		ns	
t_{ri}=t_{fi}	Clock Input Transition Time	30			25			25	ns	Input t_r, t_f for correct operation
f_{max}	Maximum Clock Frequency	320	220	320			270		MHz	Sine Wave of 800mVpp about −1300mV

Note 1: See Functional Description and Top of Page 5

Fig. 4. SWITCHING TIME TEST CIRCUIT AND WAVEFORMS





CONDITIONS
V_{CC} = +2.0 V
V_{EE} = −3.2 V
R_L = 50 Ω = R_T (Scope input impedance)
C_L = Jig and stray capacitance <5 pF
L_1 = L_2 equal 50 Ω impedance lines
Input signal t_r = t_f = 2.5 ns (10% - 90%)
with no circuit under test

CLOCK PULSE CONDITIONS
V_{IH} = +1050 mV
V_{IL} = +280 mV
t_r = t_f = 2.2 ± 0.1 ns (10% - 90%)

ABSOLUTE MAXIMUM RATINGS (above which useful life may be impaired)

Storage Temperature	−65°C to +150°C
Junction Temperature	+150°C
Supply Voltage V_{EE} (Continuous)	−6 Volts
Supply Voltage V_{EE} (Pulsed)	−8 Volts
Input Voltage	GND to V_{EE} (max)
Output Current	40 mA

APPLICATIONS

Prescaler –In its simplest application, as a divide-by-ten prescaler, the 95H90 extends the frequency range of TTL frequency counters and phase locked systems to over 300 MHz (Figure 5). For this and other RF applications the input bias should be set close to the clock threshold ($R_2 \approx 3 \cdot R_1$). This improves AC-sensitivity but it also increases noise sensitivity. A preamplifier is often a better way to improve sensitivity (Figure 6), especially in frequency counters. Care should be taken to avoid overdriving the prescaler input which would saturate the input transistor and seriously degrade the frequency resolution. Excessive input voltages might also damage the device.

Fig. 5. Divide by ten RF prescaler

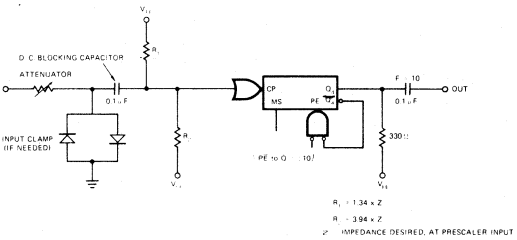
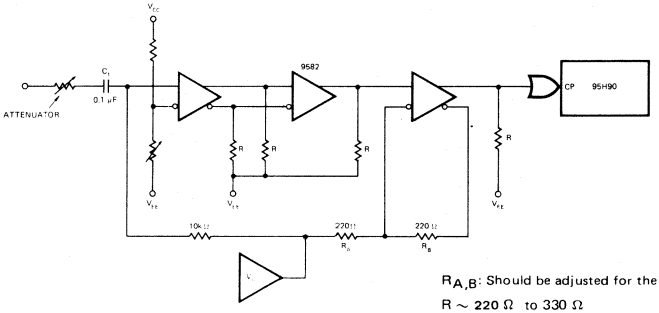


Fig. 6. Prescaler with RF preamplifier



$R_{A,B}$: Should be adjusted for the desired Hysteresis

R ~ 220 Ω to 330 Ω

Programmable Divider for Frequency Synthesizers – An integral part of most frequency synthesizers is a programmable divider. In a conventional design these become bulky, expensive and power consuming when implemented for frequencies above the TTL range. The 95H90 is especially designed for a technique called "pulse swallowing" which allows a simple high speed ECL divider (the 95H90) to be controlled by a relatively slow TTL-MSI presettable counter. This technique offers the advantage of prescaling (only the simple prescaler operates at the high input frequency) but it does not sacrifice resolution. The only drawback (usually not a limitation) is that there is a clearly defined minimum divide ratio below which the system does not function.

Pulse swallowing uses three functional blocks: (Figure 7)

(1) A variable modulo prescaler, controllable between modulo K and K+1 (typically 10/11, 20/21 or 100/101),

(2) A swallow counter which controls the prescaler, and

(3) A programmable counter.

The swallow counter determines the number of times that the prescaler divides by K+1, effectively swallowing one additional input pulse for each output pulse to the programmable counter. As an example, consider a divider (K = 10) that is programmed by decade switches. Inverting nine's complement decade switches are required, since the switch must ground the counter input in order to insert a zero. At the beginning of a divide cycle the swallow counter and the program counter are loaded with the nine's complement of the desired ratio and the count from there to their respective terminal states. If a ratio of 83 is desired, the swallow counter is preset to 6 and the program counter to 9991. The programmable counter will produce a terminal count output after 8 pulses from the prescaler, but since the swallow counter was preset to 6, the prescaler will have divided by 11 three times, by 10 the other five times. As a result, the output pulse will occur after 83 input pulses.

The prescaler modulo (K) is chosen to bring the prescaler output frequency into the range of TTL. Higher modulo (20/21, 100/101) prescalers can be implemented by additional flip-flops and counters.

An important speed parameter to be considered is the delay in the 10/11 prescaler control path. The delay through the ECL/TTL interfaces, the TTL logic, and back through the TTL/ECL interface must be less than $10/f_{in} - t_{pd}$ from Q_4 to PE.

APPLICATIONS *(Cont'd)*

Fig. 7. PULSE SWALLOWING PROGRAMMABLE DIVIDER

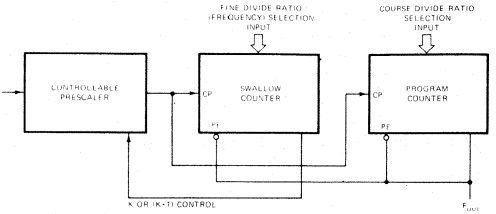
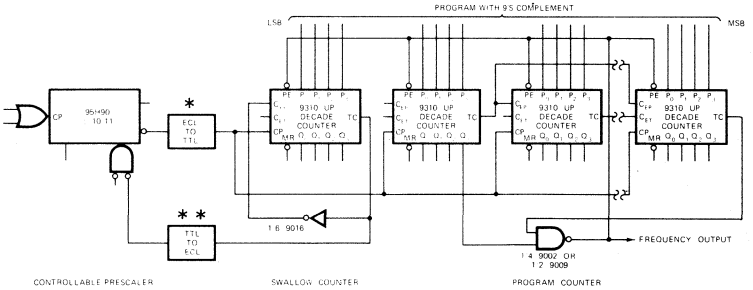
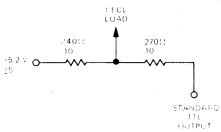


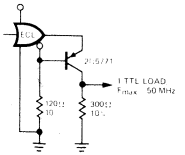
Fig. 8. HIGH SPEED PROGRAMMABLE DIVIDER (UTILIZING 10/11 PRESCALER)



***TTL to ECL, Common Power Supply.**



****ECL to TTL, Common Power Supply.**



INTERCONNECTION RECOMMENDATIONS

All high speed ECL circuits demand that special precautions be taken for optimum system performance. A ground plane must be provided for a good, low impedance, ground current return path and to transform interconnections into microstrip transmission lines. The voltage supply line should be well decoupled with small ceramic capacitors throughout each card between V_{EE} and the ground plane and by including at least one larger tantalum capacitor per card.

Typical microstrip lines have a characteristic impedance between 50 and 150 ohms with the lower being more desirable in ECL systems. For local interconnects the internal 2 kΩ resistors provide adequate termination but for optimum performance lines longer than 6 or 8 inches in length should be terminated in their characteristic impedance.

Lines up to 12 inches may be left unterminated if a degraded waveform can be tolerated with the resultant decrease in speed and increase in ringing.

Microstrip interconnections may be terminated by a resistor to a −2 volt supply: $R = \frac{Z_O}{1 - NZ_O/2000}$ where Z_O is the characteristic impedance of the line and N is the number of loads. Alternately, a 2 resistor divider network may be used with R_1 and 1.6 R connected to ground and R_2 = 2.6 R connected to V_{EE}.

Series terminating resistors decrease noise immunity and slow rise and fall times, but can still be used if these effects are tolerable. In addition, care must be taken to avoid glitches in the threshold region of the waveform occurring at certain combinations of line length and series resistor value.

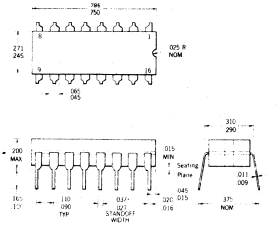
A single terminated wire running over a ground screen can be used for backpanel interconnections up to 4 or 5 inches in length, but terminated coaxial cables or terminated twisted pairs of wire are required for longer interconnections.

LINE DRIVING CAPABILITY

The 9500 series ECL circuits are capable of driving fairly long lines if the previous recommendations are followed. 50 ohm coaxial cables 10 feet in length or longer and properly terminated may be driven with almost no degradation in the waveform. The normal delay due to the finite speed of the signal traveling down the cable will be encountered in addition to a slight decrease in signal swing. This decrease caused by the attenuation of the cable (about 40 mV for 10 feet of 50 ohm coax) will lower the noise immunity of the receiving circuit by the same amount. Care must be exercised to ensure the ground potentials at the driving and receiving ends of a line are equal and no differential noise is present.

PACKAGE INFORMATION

6B — 16 LEAD SSI DUAL IN-LINE PACKAGE



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.0 grams
*The .037/.027 dimension does not apply to the corner leads

9595

DUAL HIGH SPEED ECL TO TTL CONVERTER

FAIRCHILD TEMPERATURE COMPENSATED ECL

GENERAL DESCRIPTION – The ECL 9595 is a high speed logic converter for use in systems using both the high speed of ECL and the many available functions of TTL. The 9595 requires the –5.2 volt V_{EE} supply of ECL and the +5 volt V_{CC} of TTL. The TTL fanout may be expanded by adding more pulldown current at the TTL output pin.

By allowing the logic converter to function as a logic gate the normally wasted time of logic conversion may be used in the logic implementation with the through delay generally less than that found in TTL circuits.

FEATURES:

- **HIGH SPEED . . . 6.0 ns**
- **FAN OUT 10 TTL LOADS WITH EXTERNAL PULL DOWN RESISTOR**
- **NO INVERSION THROUGH CONVERTER**
- **ECL INPUT TEMPERATURE COMPENSATED**
- **INTERNAL PULL DOWNS**
- **HERMETIC CERAMIC 16 PIN DIP**
- **FUNCTIONS AS DUAL 4 INPUT GATE**
- **TWO SEPARATE V_{CC} PINS ELIMINATE NOISE COUPLING**

ABSOLUTE MAXIMUM RATINGS (Above which useful life may be impaired)

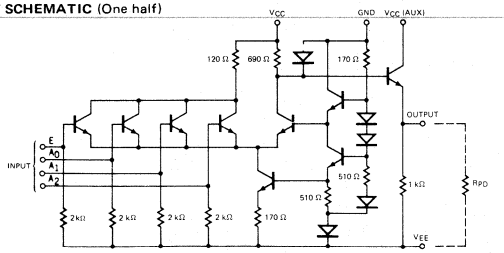
Storage Temperature	–65°C to +150°C
Junction Temperature	+150°C
Supply Voltage V_{EE} Continuous (Pulsed)	–6 Volts (–8 Volts)
Supply Voltage V_{CC} Continuous (Pulsed)	+6 Volts (+8 Volts)
Input Voltage	GND to V_{EE} (max)
Output Current	40 mA

PIN NAMES

A_N = OR Inputs to A Gate
Q_A = TTL Output of A Gate
B_N = OR Inputs to B Gate
Q_B = TTL Output of B Gate
E = Common Enable Input to A and B Gates

ORDER INFORMATION – Specify U6B9595XXX for 16 pin Dual In-Line Package where XXX is 59X for the 0°C to +75°C temperature range.

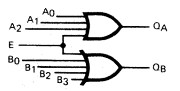
CIRCUIT SCHEMATIC (One half)



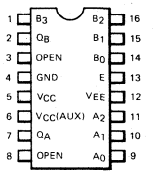
External Pull Down Resistor (R_{PD}) to V_{EE}:
(Recommended for best speed and noise immunity)

$3 \leq$ Fan Out ≤ 10
$R_{PD} = 360\ \Omega$

LOGIC SYMBOL

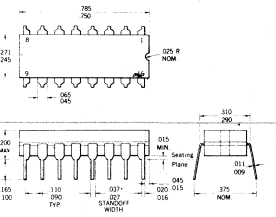


CONNECTION DIAGRAM
DIP (TOP VIEW)



PACKAGE INFORMATION

6B–16 LEAD SSI DUAL IN-LINE



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin plated kovar
Package weight is 2.0 grams
• The .037/.027 dimensions does not apply to the corner leads

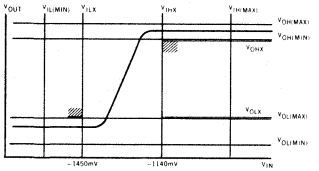
DC ELECTRICAL CHARACTERISTICS (Operating Temperature: $T_A = 0°C$ to $75°C$, $V_{CC} = V_{CC}$ (AUX) = +5.0 V ±5%, $V_{EE} = -5.2$ V ±5%.

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		MIN.	TYP.	MAX.		
V_{OH}	Output Voltage High	2.40	3.90		V	R_{PD} = 360 Ω to V_{EE}, See Fig. 5 V_{IN} = −1140 mV (V_{IHX}) or More Positive (for V_{OH})
V_{OL}	Ouput Voltage Low	−2.0	−1.5	0.4	V	F.O. = 1 (I_S = 1.6 mA), No External R_{PD}, See Fig. 5 V_{IN} = −1450 mV (V_{ILX}) or More Negative (for V_{OL})
$I_{IN(H)}$	Input Current High		2.25	3.10	mA	V_{IH} = −900 mV
$I_{IN(L)}$	Input Current Low		1.75	2.35	mA	V_{IL} = −1700 mV
I_{PS}	Power Supply Current	28	37	44	mA	All Inputs Open

AC ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V_{CC} = V_{CC}$ (AUX) = +5.0 V, $V_{EE} = -5.2$ V)

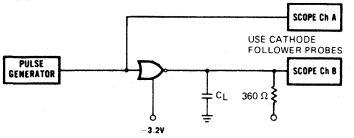
SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		MIN.	TYP.	MAX.		
t_{pd}	Propagation Delay		6.0	8.0	ns	See Fig. 6
t_r	Rise Time	3.0	6.0	8.0	ns	$C_L < 5.0$ pF
t_f	Fall Time	3.0	6.0	8.0	ns	$t_r = t_f$ = 2.5 ns (10%–90%)
I_T	Transient Input Current		2.0	3.5	mA	See Fig. 7
	Enable Line	2.8	2.8	5.7	mA	

Fig. 5 – NOISE MARGIN SPECIFICATION POINTS



Corner points indicated on the transfer characteristics represent the worst case points (thresholds) at which the device will start to switch. The values V_{ILX} and V_{IHX} define the maximum width of the transition region.

Fig. 6. SWITCHING TIME TEST CIRCUIT AND WAVEFORM



$t_r = t_f$ = 2.5 ns (10% - 90%)
Jig setup with no circuit under test
$V_{CC} = V_{CC}$ (AUX) = +5.0 V
V_{EE} = −5.2 V
C_L = Jig and Stray Capacitance <5.0 pF

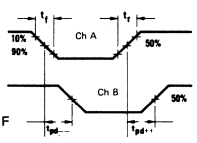
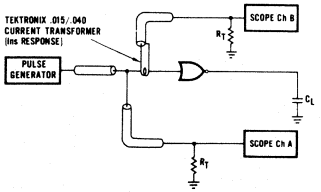
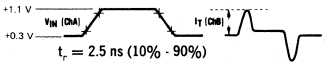


Fig. 7. TRANSIENT INPUT CURRENT TEST CIRCUIT AND WAVEFORMS





This test provides a measure of the average value of C_{IN}; also current mismatch in the line.
$V_{CC} = V_{CC}$ (AUX) = +5.0 V
V_{EE} = −5.2 V
R_T = 50 Ω Termination of Scope
C_L = Jig and Stray Capacitance <5.0 pF

95 400

64-BIT SCRATCH PAD MEMORY
FULLY DECODED 16 WORDS × 4 BITS
FAIRCHILD TEMPERATURE COMPENSATED ECL

GENERAL DESCRIPTION

The 95400 is a very high speed 64 bit memory organized 16 words by 4 bits. Internal decoding is employed with the 16 words selected through four address lines. A chip select input, read/write control line, and OR-tieable outputs are also provided.

The 16x4 organization was chosen as optimum for small high speed scratchpad applications. For word capacities in excess of 26, the 9538 decoder will permit expansion with very little decrease in overall speed.

HIGH SPEED .... 12 ns TYPICAL ACCESS TIME
LARGE CAPACITY - 64 BITS
OPTIMIZED FOR SMALL WORDS - 16 x 4
HIGH SPEED CHIP ENABLE FOR EASE OF EXPANSION
WIRED OR CAPABILITY
TEMPERATURE COMPENSATION
DATA INPUTS AND OUTPUTS OPEN FOR EASE OF EXPANSION: 50Ω LINE DRIVE CAPABILITY
SINGLE - 5.2 VOLT POWER SUPPLY
HERMETIC CERAMIC 16 PIN DIP
COMPLEX MULTI-GATE CHIP REDUCES PACKAGE COUNT & POWER

PIN NAMES

A_N = ADDRESS LOCATION

I_N = WORD INPUT

O_N = WORD OUTPUT

W_E = ENABLE (WRITE)

C_S = CHIP SELECT

NOTE
CHIP SELECT HAS INTERNAL 50 k PULLDOWN RESISTOR
ALL OTHER INPUTS OPEN.

ORDER INFORMATION - SPECIFY U6B95 400 XX FOR 16 PIN DUAL IN-LINE PACKAGE WHERE XX IS 9 X FOR 0°C TO + 75°C TEMPERATURE RANGE.

FAIRCHILD
SEMICONDUCTOR

D.C. (a) 0°C - 75°C V_{EE} = -5.2

A.C. (a) 25°C

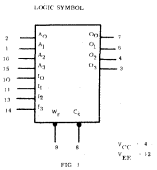
DC ELECTRICAL SPECIFICATIONS

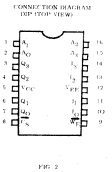
SYMBOL	CHARACTERISTIC	MIN	TYPE	MAX	UNITS	CONDITIONS
V_A	OUTPUT LOW LEVEL	-1780	-1690	-1600	mV	F.O. = 1
V_{AC}	OUTPUT LOW LEVEL	-1830	-1740	-1650	mV	F.O. = 5
V_{OL}	OUTPUT LOW LEVEL	-1810	-1720	-1630	mV	50Ω TO -2.0V + 5 pf TO V_{cc}
V_{OH}	OUTPUT HIGH LEVEL	-920	-860	-800	mV	F.O. = 7
V_{OH}	OUTPUT HIGH LEVEL	-970	-910	-850	mV	F.O. = 5
V_{OH}	OUTPUT HIGH LEVEL	-1010	-950	-890	mV	50Ω TO -2.0V + 5 pf TO V_{cc}
V_{ILX}	INPUT THRESHOLD LOW	-	-	-1450	mV	
V_{IHX}	INPUT THRESHOLD HIGH	-1140	-	-	mV	
$I_{N(LOW)}$	INPUT CURRENT (LOW)				uA	
$I_{IN(HIGH)}$	INPUT CURRENT (HIGH)	5	20	50	uA	ALL INPUTS EXCEPT CHIP SELECT (-900)
$I_{IN(HIGH)}$		30	100	140	uA	CHIP SELECT - 900
I_{PS}	POWER SUPPLY CURRENT		100		mA	

NOTE: OUTPUT LEVEL NOT DEFINEDED DURING WRITE MODE

AC ELECTRICAL SPECIFICATIONS

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS
t_{ACS}	CHIP SELECT ACCESS TIME	-	6	9	nS
t_{RCS}	CHIP SELECT RECOVERING TIME	-	6	9	nS
t_{AA}	ADDRESS ACCESS TIME	-	12	18	nS
t_{WC}	TIME WRITE CYCLE	-	18	-	nS
t_W	WRITE PULSE WIDTH	-	10	-	nS
t_{WSD}	DATA SET UP PRIOR WRITE	-	2	-	nS
t_{WRD}	DATA HOLD AFTER WRITE	-	5	-	nS
t_{NSA}	ADDRESS SET UP PRIOR TO WRITE	-	6	-	nS
t_{WHA}	ADRESS HOLD AFTER WRITE	-	6	-	nS
I_{IN}	INPUT CAPACITANCE	-	4	-	pf





DESIGN INFORMATION

easy ECL

9500 SYSTEM APPLICATION AND WIRING RULES

INTRODUCTION

High speed is essential in many real-time data processing and communications systems. In addition, the cost of information processing on large digital computers is inversely proportional to the square root of the machine's speed. These system requirements have prompted the design of the Fairchild 9500 Temperature Compensated ECL family. This series offers standard gate propagation delays of 2 to 3 ns, high-speed gates with propagation delays of 1 to 2 ns and internal MSI gates with typical delays of 1.5 ns.

To achieve speeds faster than 3 ns, the use of nonsaturating circuitry is essential. This is attained with ECL by maintaining a narrow logic swing. Keeping transistors out of saturation eliminates the long turn-off delay caused by excess stored charge. This, together with ECL logic advantages such as wired-OR and complementary outputs, permits system speeds four to ten times faster than conventional or Schottky TTL.

The penalties that must be paid for high speed are generally more restrictive wiring rules regardless of logic family, ECL or TTL. The necessity of terminating connecting lines and considering capacitive loading effects on high fan-out, short lines has been minimized in the design of the 9500 ECL family. Power per package has been optimized in a trade-off of gate-power and ease of wiring. The advantages of ECL are in the implementation and use of MSI. ECL's greater logic flexibility also means fewer gates per function for most systems. This implies that if an ECL and TTL logic family is each used in an efficient manner to process a given amount of data, the power requirements of the ECL system would be lower than those of the TTL system.

THE 9500 SERIES

9500 Series ECL elements have been designed with unique temperature compensation circuitry and other features aimed at extending the advantages of high speed to a wide range of low cost applications. This is achieved by simplifying the application and usage rules traditionally associated with ECL.

At gate propagation delays faster than 4 ns, package interconnections begin to look like transmission lines. Unless these conditions are handled correctly, reflections or crosstalk can cause unreliable system operations. This is common to all high speed logic forms including TTL.

9500 elements have been designed for use on standard two-sided printed circuit boards. Higher performance can be achieved with a ground plane or with multilayer boards which convert printed wiring into a controlled impedance system of high speed transmission lines. ECL input and output impedances are compatible with optimum transmission line requirements.

9500 BASIC GATE OPERATION

In the basic ECL gating circuit shown in Figure 1, T4 acts as a constant current source while T5 establishes a reference voltage for T3. Current must flow through T1, T2 or T3. If both inputs are LOW, T1 and T2 are OFF and current flows through T3 and R2 bringing the voltage on the collector of T3 negative, but not low enough to saturate the transistor. This negative voltage is reflected on the OR output as a LOW by transistor T8, an emitter follower. Little current flows through R1, forcing the NOR output HIGH. If either input is HIGH, most of the current flows through R1 instead of R2, forcing the NOR output LOW and the OR output HIGH. 2-kilohm resistors are included on the inputs and outputs to provide pulldown and to permit short interconnections without external resistors. These resistors also permit unused inputs and outputs to be left unconnected with no degradation in performance. These 2-kilohm resistors have been replaced with 50-kilohm resistors on the 95L22, L23 and L24 gates. This allows high fan-out and series terminations. The rest of the circuitry is used to generate the reference voltage and to provide temperature compensation for both the reference and output voltages. Separate V_{CC} (ground) pins are provided for the input circuitry reducing noise problems when driving unbalanced loads.

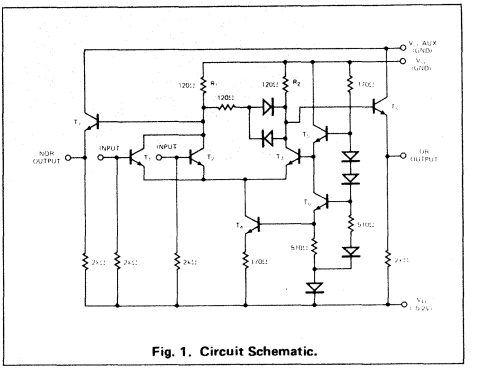


Fig. 1. Circuit Schematic.

9500 series circuits employ a unique temperature compensation network making the output HIGH and LOW levels and the input threshold level almost insensitive to temperature. This is extremely significant in maintaining full system noise immunity over all operating temperatures. In addition, interfacing circuits with different power dissipation, and thus different operating temperatures, does not decrease the noise immunity. A detailed description of the compensation action is provided in Fairchild Application Note APP-206.

The 9500 Series flip-flops and MSI elements use the same basic gating circuit with temperature compensation, but in addition make use of series gating and other ECL design techniques to achieve the required logical functions with minimum propagation delays and minimum power dissipation. All input and output levels for these devides are identical to the gate input and output levels.

All 9500 series outputs are buffered, using an emitter follower to make all outputs wire-ORable. The isolation provided by these output buffers makes it impossible to affect the state of a flip-flop or latch. Backlatching is therefore impossible.

Device Descriptions

Logic configurations, pin connections and loading for the basic elements in the 9500 series ECL family are shown in Figure 3. Positive logic is assumed.

ONE (HIGH) = −0.900 V., ZERO (LOW) = −1.700 V. All active LOW inputs and outputs are indicated by a small circle.

Gates

The simplest building block in the ECL family is the NOR gate. Nine are available in three gate configurations: the dual 4-input gates, the triple 2-input gates and the quad 2-input gates. The OR output from each gate is available on the dual and triple units. For each of the dual, triple and quad gate configuration three types of gates are available:

Basic 2.4-ns 9500 gates —	9502 dual, 9503 triple, 9504 quad
Basic 1.6-ns 95H00 gates —	95H02 dual, 95H03 triple, 95H04 quad
High input impedance, high-speed lower power gates —	95L22 dual, 95L23 triple, 95L24 quad

In addition, each device is equipped with a common enable input controlling all the gates in the package. If the enable line is held HIGH, all NOR outputs are forced LOW and all OR outputs HIGH. Alternatively, the NOR gates may be viewed as AND gates with active LOW inputs, as indicated in Figure 2.

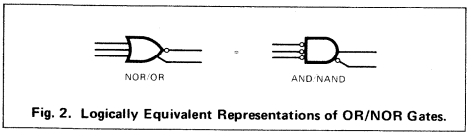


Fig. 2. Logically Equivalent Representations of OR/NOR Gates.

Selecting Gate Types

Standard 9500 gates should be used whenever possible because: 1. they have the lowest cost, and 2. they allow use of the easiest wiring.

High-speed gates should be used in areas of a system where speed is critical, such as register switching and clock driving.

The high input impedance low power gates should be used whenever maximum fan-out (>10) or wire-OR is needed. These gates also permit power savings and special wiring by allowing series terminations to be used.

Low power gates should also be used whenever overall system power is critical. The main disadvantage of these gates is their fan-out sensitivity and the need for external resistors for every output. These gates are similar to the internal gates found in the MSI elements.

Standard devices will satisfy most system requirements with only a small percentage of high-speed and high input impedance gates being needed.

All MSI elements are supplied with internal low-power gates and internal 2 k ohm pulldown resistors so that circuits can be wired directly without additional components and still maintain reasonable package power levels.

Two additional gate building blocks can be used to reduce package count and delay. These are the 9505 OR-AND and the 9507 quad AND gates. A specific advantage of the 9505 is the high-speed ANDing of four OR gates by collector dotting and wire ORing. The 9507 quad AND uses series gating to attain the positive logical AND and achieves an 8-input NAND function by dotting the complement outputs.

9595 ECL to TTL Interface

Another special gate found in the 9500 family is the 9595 ECL to TTL interface element. This device is logically organized as two OR gates, one 3-input and one 4-input. Like the basic gates, the 9595 has a common enable input. With an ECL logic "1" this enable input forces the outputs to a TTL logic "1". With the additional gate inputs and the 6 ns typical conversion delay, a hybrid system of ECL and TTL (or ECL and TTL-level MOS) can be constructed utilizing the optimum speeds and advantages of each.

The 9595 can also be used as a computer interface element. In this case both outputs should be connected together to give a maximum drive of 80 mA with both gates driven in parallel through the enable input.

Line Receiver: 9582

The 9582 consists of three differential input amplifiers. Both the true and complement outputs are temperature compensated to be compatible with other ECL 9500 products. With appropriate connection of the base pins the device will function as a differential line receiver, Schmitt trigger, high-speed comparator, broad-band video, IF or RF amplifiers, or as an oscillator. V_{ref} is made available to allow use of this device as a high input impedance buffer gate.

Dual D Flip-Flop: 9528 (160 MHz), 95H28 (260 MHz),

The dual D flip-flops will function in high speed counting, shifting or data storage applications. Each flip-flop is provided with asynchronous set direct and clear direct inputs as well as both assertion and negation outputs. Each flip-flop consists of both a master and a slave. While the clock is LOW the slave is held steady, but the information on the D (data) input is permitted to enter the master. The next clock transition from LOW to HIGH locks the master in its present state, making it insensitive to the D input, and connects the slave to the master, causing the new information to be reflected on the outputs. The following clock transition from HIGH to LOW again locks the slave and permits new information to flow into the master.

The internal clock is the OR of two clock inputs, one common to both flip-flops. The outputs will only switch following a LOW to HIGH transition of the ORed clock (unless either the set direct or clear direct input is activated). The ORed clock permits the use of one input as a clock pulse input and the other as an active LOW enable. If one clock input (the enable line) is held HIGH, clock pulses on the other input will not be seen by the flip-flop. To maintain synchronous operation however, this enable should only be changed while the clock is HIGH.

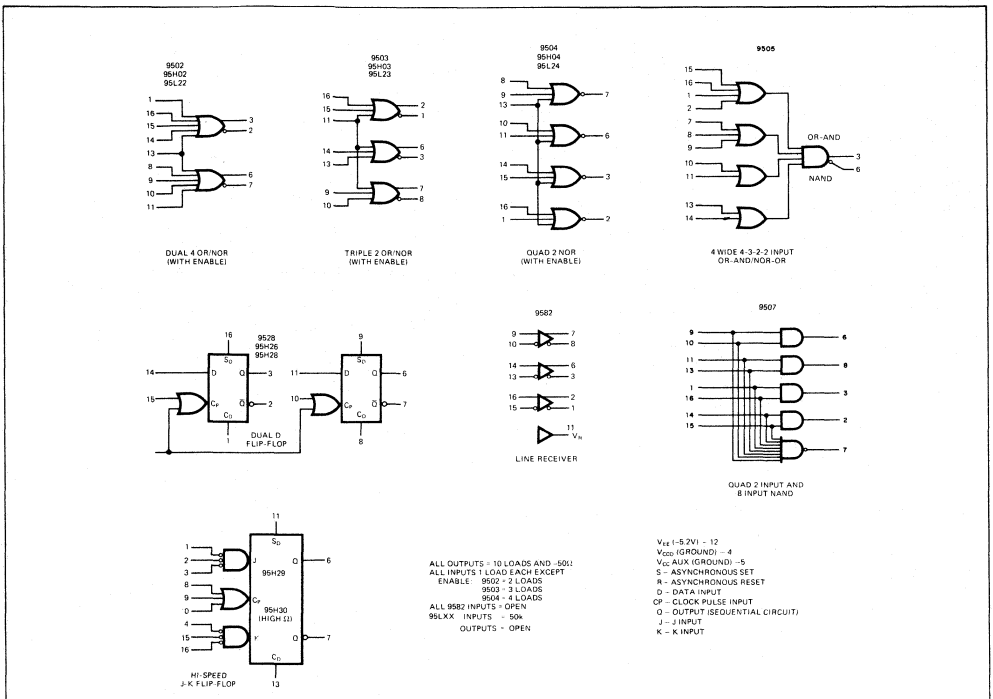


Fig. 3. 9500 Series Basic ECL Circuits.

J-$\overline{K}$ Flip-Flops – 95H29 (260MHz),

The 95H29 is a high-speed, edge-triggered J-$\overline{K}$ master-slave flip-flop with both direct set and clear inputs. The J-$\overline{K}$ and Clock functions are the active low AND of three inputs. With these inputs this device can be used effectively in counters, registers and other applications where data must be stored or shifted at a high rate. In addition, the full frequency range can be used effectively as a prescaler and controlled divider for frequencies up to 260 MHz.

Loading

The input and output loading for the 9500 series ECL circuits is given in Figure 3. As indicated, outputs are capable of delivering the DC currents required by a fairly large number of inputs, but a degradation in the AC performance must be expected if many loads are driven from one output.

For optimum performance, limiting the fan-outs to fewer than those specified as maximum is desirable. The number of loads an output can satisfactorily drive depends on the length of interconnecting lines, the impedance of the lines, terminations used and the required performance. The information given on the data sheets will permit the designer to determine a more stringent set of fan-outs applicable to his specific interconnection configurations and performance requirements.

Each output that is wire-ORed together can be considered as one additional input load. So, if three outputs are wire-ORed together, the fan-out should be decreased by two. For high impedance devices only AC fan-out need be considered. With the high capacity output found in the standard high speed 9500 ECL driving the high input impedance, lower power gates, the maximum AC fan-out with slight speed degredation will be about 10 load units. For the high speed low power devices, six standard gate AC and DC loads and one 50 ohm, shunt-terminated line will be the maximum for full speed performance. With series termination schemes this fan-out may be increased to a maximum of 16, or 4 per series load.

APPLICATION

OR/NOR Gate Flexibility

In addition to offering high speed, 9500 series ECL gates add a new freedom to logic design. Wire-ORing outputs is permitted, and both the OR function and the NOR function may be implemented directly. Tying gate outputs together results in a true wired-OR function, i.e., if either output is a ONE, the function is ONE. This is different from the so-called wired-OR function achieved by tying DTL gate outputs together; really a wired-AND function.

Of the 16 possible functions of two variables, A and B, six are trivial: 1, 0, A, $\overline{A}$, B and $\overline{B}$. Simple implementations of the other 10 are shown in Figure 4. They may all be implemented with no more than two gate delays. If both assertion and negation inputs are available, any of these 10 functions may be implemented with only one gate delay. Only a single gate package is required to implement any of the function.

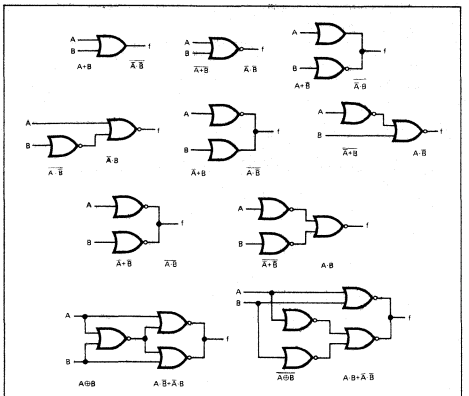


Fig. 4. Implementation of the 10 Non-trivial Functions of Two Variables.

9500 series ECL gates are provided with common enable inputs. The enable input may be used as an additional data input if one particular variable is required as an input to each gate, or if a variable is required as an input to some of the gates in the package and is redundant as an input to the others. The enable input is used in this way in some of the examples in the following section. This section gives examples of functions implemented using SSI elements, complex gates, and MSI elements. The MSI elements make ECL sub-nanosecond speeds usable with ordinary wiring rules.

High Speed Adder Using SSI

ECL gates permit the implementation of very high speed adders. Ripple adders require the least circuitry, but are too slow for longer word lengths to be included in a high-speed ECL system. The most commonly used technique for increasing the speed of an adder is the use of carry generate (CG) and carry propagate (CP) signals.

These two signals are generated by each adder stage and are only a function of the operands and not of the incoming carry. A carry lookahead unit accepts these signals from a number of adder stages and generates the carries directly.

A single adder stage is shown in Figure 5A, and a carry lookahead unit for four stages is shown in Figure 5B. Figure 5C shows the units interconnected to form a 4-bit adder. The carry generate (CG) and carry propagate (CP) signals are generated in one gate delay. The carries in two more gate delays and the sum outputs follow one additional gate delay later. This results in four gate delays for an addition. The number of delays in the adder from the A and B inputs to the S output (three delays) can be reduced, but the total addition time would not be shortened. The Boolean equations for the adder and carry lookahead are shown in Table 1.

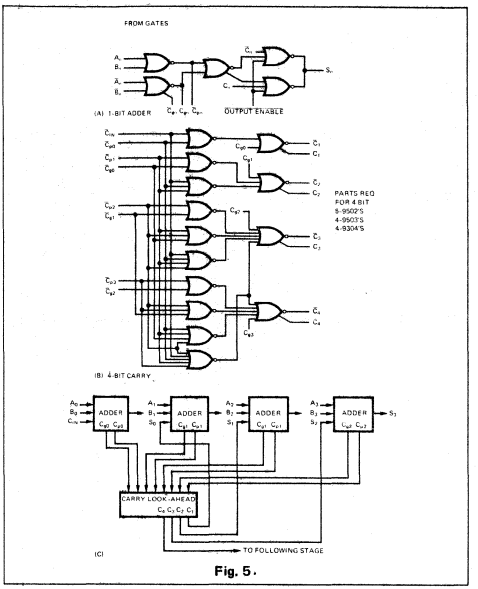


Fig. 5.

$$C_p = A + B$$

$$C_G = A \cdot B = \overline{\overline{A} + \overline{B}}$$

$$S = (A \cdot \overline{B} + \overline{A} \cdot B) \cdot C + (A \cdot \overline{B} + \overline{A} \cdot B) \cdot \overline{C}$$

$$= \overline{[(\overline{A} + \overline{B}) + (A + B) + C]} + \overline{[(\overline{A} + \overline{B}) + (A + B) + \overline{C}]}$$

$$C_1 = C_{p0} + C_{in} \cdot C_{p0} = C_{p0} + (\overline{C_{in}} + \overline{C_{p0}})$$

$$C_2 = C_{g1} + C_{p0} \cdot C_{g1} + C_{in} \cdot C_{p0} \cdot C_{p1}$$

$$C_3 = C_{g2} + C_{g1} \cdot C_{p2} + C_{g0} \cdot C_{p1} \cdot C_{p2} + C_{in} \cdot C_{p0} \cdot C_{p1} \cdot C_{p2}$$

$$C_4 = C_{g3} + C_{g2} \cdot C_{p3} + C_{g1} \cdot C_{p2} \cdot C_{p3} + C_{g0} \cdot C_{p1} \cdot C_{p2} \cdot C_{p3} + C_{in} \cdot C_{p0} \cdot C_{p1} \cdot C_{p2} \cdot C_{p3}$$

Etc.

The implementation is straightforward. The *enable* lines on two 9502 gates are used to expand the gates to 5-input gates. C_{P2} is required as an input to both gates anyway. The extra input to the gate generating C_3 is redundant, but again allows the enable to function as a fifth input to the other gate in the package.

An adder for a longer word length may be constructed by rippling between 4-bit sections and adding two gate delays for each additional 4-bit section. But adding a second level of carry lookahead would result in a faster adder. This requires generating an additional carry generate and carry propagate output from each 4-bit section and running these into an identical carry lookahead unit.

The ripple adder should be given a closer look before it is discarded. Figure 6 shows a 4-bit ripple adder where the carry propagates through each section in only one gate delay. Every other stage accepts an active LOW carry input and generates an active HIGH carry directly — while each of the remaining stages generates an active LOW carry from an active high carry input. Both the active low and active high carry are still needed to generate the sum, but more gate delays may be used to do this. The ripple adder shown will add two 4-bit numbers in five gate delays, only one delay more than required by the carry lookahead adder.

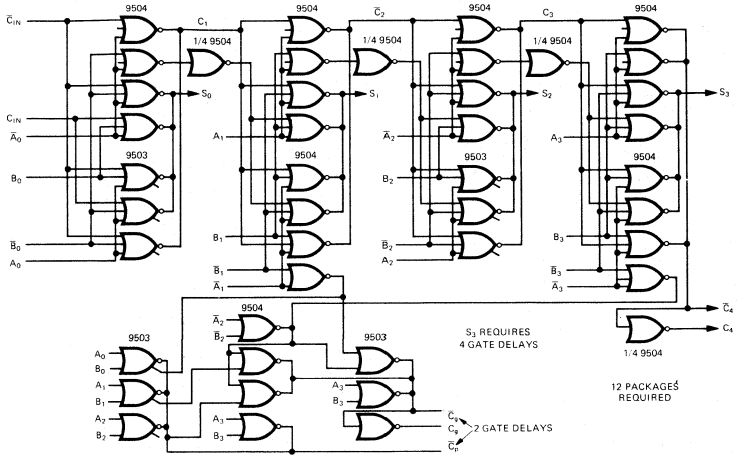


Fig. 6. 4-Bit Ripple Adder with Carry Generate and Carry Propagate Output.

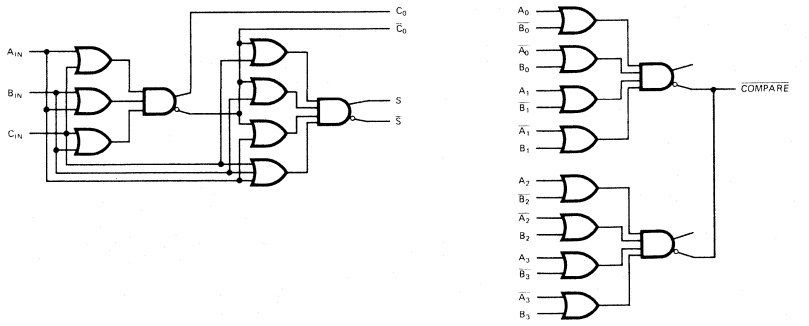
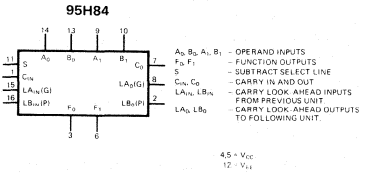


Fig. 7.

Carry lookahead may now be used between 4-bit sections. The required carry generate and carry propagate signals are generated by the circuit in Figure 6 in two gate delays. Four of these ripple adders used in conjunction with the lookahead unit in Figure 5B will add two 16-bit numbers in nine gate delays.

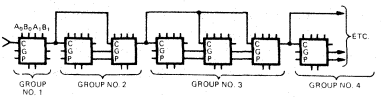
9505 Adder-Comparator

Another adder that can be implemented with two packages uses a pair of 9505s (Figure 7a). This device is recommended whenever one needs to add only 2 or 3 bits together. The 9505 also can be used to construct comparators (Figure 7b).



Add/Subtract

ACTIVE HIGH BLOCK DIAGRAM



GROUP	NUMBER OF BITS	TOTAL NUMBER OF GATE DELAYS	ADD/SUB SPEED AT 2.0 ns PER GATE (TYPICAL)
1	1–2	2	4
2	3–6	5	10
3	7–12	6	12
4	13–20	7	14
5	21–30	8	16
6	31–42	9	18
7	43–56	10	20
8	57–72	11	22

FOR 8 BITS THE CONFIGURATION BELOW ALLOWS A TYPICAL ADD TIME OF 10 ns ADD ONLY

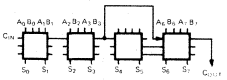


Fig. 8. 95H84 MSI 2-Bit Adder

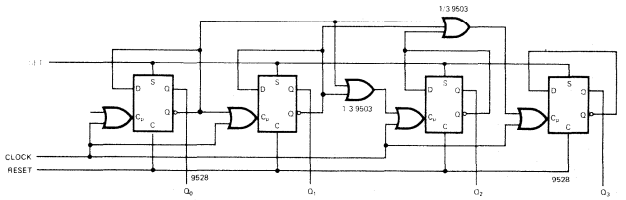


Fig. 9. Synchronous Binary Counter.

95H84 2-Bit Adder-Subtractor

For adding 2-bit words the 95H84 will provide the highest speed combined with minimum package count. As shown in Figure 8, the 95H84 performs both addition and subtraction on two bits with full internal carry lookahead, expandable between units. No additional carry lookahead unit is required. It can be implemented to add or subtract two 64-bit words within 22 ns at a power comparable to a TTL adder with carry lookahead units.

Counters

High-speed counters can be implemented easily with 9528 dual D flip-flops. Figure 9 shows a fully synchronous binary counter. Toggle flip-flops are formed by connecting the D input of each flip-flop to the $\overline{Q}$ output. The first flip-flop must toggle on every clock pulse. By using the two ORed clock inputs as a clock input and an active LOW enable, the second flip-flop is made to toggle on rising clock edges only if the first flip-flop is a ONE ($\overline{Q}$ LOW). Similarly, the third flip-flop only toggles if both $\overline{Q_0}$ and $\overline{Q_1}$ are LOW, etc.

While most high-speed applications require a synchronous counter, a ripple counter will function as well in certain applications and can be implemented with fewer external gates and less clock loading. Figure 10 shows such a counter. The "divide-by-64" (Terminal count) output is as fast as if decoded from a synchronous 64 counter. Only two transitions are of interest: from 011111 (least significant bit) to 111111 (most significant bit) and from this state to 000000. These transitions depend on the first (least significant) bit, and the more significant flip-flops have more than enough time to settle.

The D flip-flop is well suited for use in shift counters. The resulting count sequence is not binary, naturally, but this is of no consequence in many applications.

A shift counter of length 2^n-1 (n = number of stages) is easy to implement as shown in Figure 11. For n = 6 the counter will pass through 63 states by toggling the first flip-flop whenever the last flip-flop is ZERO (Q_5 LOW). The other flip-flops function as normal D flip-flops. As can be seen by examining the count sequence in Figure 11, the one missing state is the persistent 111111 state. A gate is used to reset the first flip-flop if the counter should accidentally enter this state. The reset line, as shown, sets the counter to the 100000 state and thus 000000 becomes the terminal state. This choice is arbitrary.

The feedback used for this shift counter will function properly for the following values of n (numbers of stages) less than 25: n = 2, 3, 4, 6, 7, 15 and 22. Other values require a different feedback arrangement.

The counter may be made to count by 64 (2^n) by modifying the feedback to include the 111111 state as shown in Figure 12.

Figure 13 shows a combination of the synchronous binary and shift counters. Each pair of flip-flops is connected as a count-by-4 shift counter and is permitted to count when all less significant pairs are in the 01 state. The resulting count sequence also is shown.

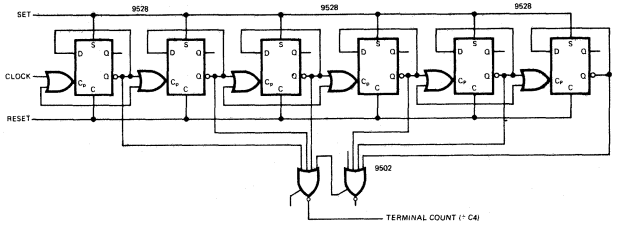
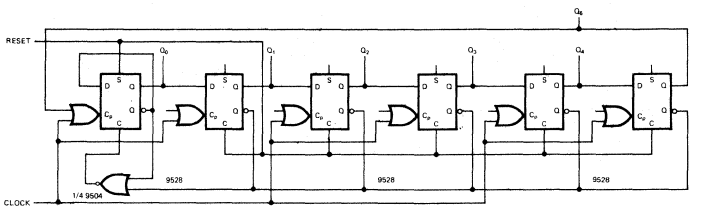


Fig. 10. Divide-by-64 Ripple Counter. (As fast as synchronous counter.)



COUNT SEQUENCE

1 0 0 0 0 0	1 1 0 1 0 0	1 0 1 0 1 1
0 1 0 0 0 0	0 1 1 0 1 0	1 1 0 1 0 1
1 0 1 0 0 0	1 0 1 1 0 1	1 1 1 0 1 0
0 1 0 1 0 0	1 1 0 1 1 0	0 1 1 1 0 1
1 0 1 0 1 0	0 1 1 0 1 1	0 0 1 1 1 0
0 1 0 1 0 1	0 0 1 1 0 1	1 0 0 1 1 1
0 0 1 0 1 0	0 0 0 1 1 0	1 1 0 0 1 1
1 0 0 1 0 1	1 0 0 0 1 1	1 1 1 0 0 1
1 1 0 0 1 0	1 1 0 0 0 1	1 1 1 1 0 0
0 1 1 0 0 1	1 1 1 0 0 0	0 1 1 1 1 0
0 0 1 1 0 0	0 1 1 1 0 0	1 0 1 1 1 1
1 0 0 1 1 0	1 0 1 1 1 0	1 1 0 1 1 1
0 1 0 0 1 1	0 1 0 1 1 1	1 1 1 0 1 1
0 0 1 0 0 1	0 0 1 0 1 1	1 1 1 1 0 1
0 0 0 1 0 0	0 0 0 1 0 1	1 1 1 1 1 0
1 0 0 0 1 0	0 0 0 0 1 0	0 1 1 1 1 1
0 1 0 0 0 1	1 0 0 0 0 1	0 0 1 1 1 1
0 0 1 0 0 0	1 1 0 0 0 0	0 0 0 1 1 1
1 0 0 1 0 0	0 1 1 0 0 0	0 0 0 0 1 1
0 1 0 0 1 0	0 0 1 1 0 0	0 0 0 0 0 1
1 0 1 0 0 1	0 1 0 1 1 0	0 0 0 0 0 0
		1 0 0 0 0 0

Fig. 11. Synchronous 63-Shift Counter.

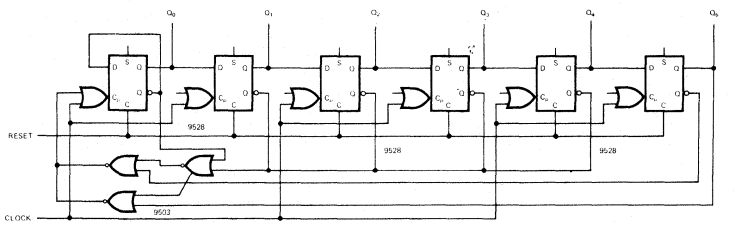


Fig. 12. Synchronous 64-Shift Counter.

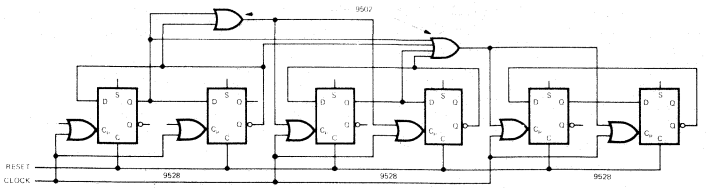
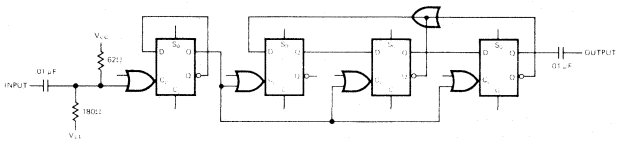


Fig. 13. Synchronous 64-Counter.



High-Speed Prescalers: 9528/95H28

High-Speed Prescalers: 9528/95H28

This easy-to-implement prescaler, Figure 14, has many applications in digital instruments and communications. By using only two integrated circuits the operating range of 10 to 30-MHz counters may be extended well into the VHF range. The prescaler also can be incorporated in digital phase-lock loop systems in communications equipment. The integrated circuits used to build the prescaler shown are 9528/95H28 dual D, temperature-compensated flip-flops.

The circuit will accept AC input voltages from 0.15V RMS to 0.5V RMS. If a greater input range is desired, either an attenuator or preamplifier can be inserted before the 9528's.

The logic configuration of this prescaler is straightforward. It consists of a divide-by-two toggle stage clocking a divide-by-five shift counter. The advantages of this configuration are: an output duty cycle of 60/40 (good for driving slower speed TTL logic), a single flip-flop on the input to reduce the loading of the driving circuitry if desired, and no lockup states.

High-Speed Prescaler: 95H90

The ECL 95H90 prescaler, Figure 15, is a high-speed ECL/MSI element designed specifically for the communication and instrumentation manufacturer. In its simplest use it will divide any clock frequency up to 250 MHz by 10. By using the 95H90 with other control logic a divide by 10/11 logic control element allows a divide by "N" counter to be constructed with a maximum frequency above 250 MHz. Typically maximum clock frequency for the 95H90 is 340 MHz.

By keeping all the high speed logic manipulation "on chip," a dramatic decrease in power and increase in reliability and wireability are made available at much lower cost than that of a comparable SSI function.

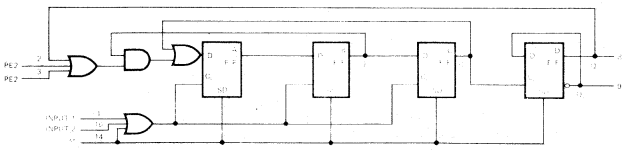


Fig. 15. 95H90 Logic Diagram.

Multiplexers/Decoders

The 9500 ECL product line includes many devices that can be used as multiplexers and demultiplexers or decoders. A simple 2-input multiplexer can be implemented using two (or more) 9504 gates. (Figure 16).

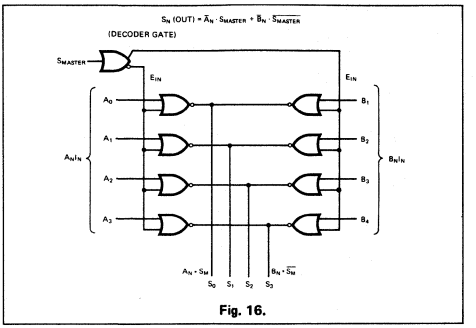


Fig. 16.

This type of multiplexer can be expanded to either of two 16-bit words with more decoders (i.e., 3-input, 4-input, etc.) or more NOR gates.

The MSI equivalent of this logic function is found in the 9579 quad 2-input multiplexer (Figure 17). The advantage of the 9579 over the SSI equivalent is lower power and higher speed, as well as fewer connections.

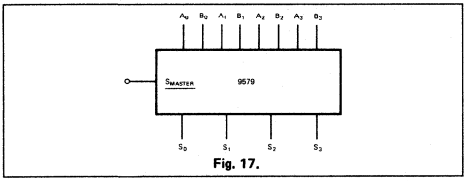


Fig. 17.

A special triple 2-input multiplexer, the 9580 combines several features. These are: 1. separate select on each output, 2. common enable on all outputs, disabling low for OR tying, and 3. inversion through the multiplexer. By using the wired-OR on the inverted outputs, a logical NAND may be obtained. Figure 18 illustrates this with gates in place of multiplexers.

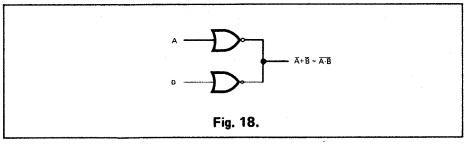
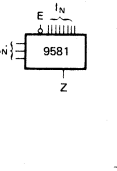


Fig. 18.

8-Input Multiplexer: 9581

The 9581 multiplexer is fundamentally a high-speed semiconductor implementation of a single-pole eight-position switch. Three address lines select one of the eight data inputs and feed this input to output (Z). An active LOW enable input forces the output LOW if held HIGH. Data encounters only one gate delay from one of the eight data inputs to the output. A truth table for the device is given in Figure 19.

The multiplexer also can be used as a universal logic block capable of generating any function of four variables. To generate an arbitrary function of A, B, C and D; three of the variables (A, B and C for example) should be connected to the address input lines A_0, A_1 and A_2. The desired function is achieved by wiring each of the eight data inputs to either a LOW (open input), a HIGH (-.89 volts), the fourth variable (D), or the negation of the fourth variable ($\overline{D}$).

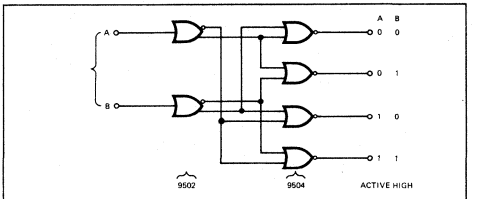


INPUTS											OUTPUT
A_0	A_1	A_2	E	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	Z
L	L	L	L	L	X	X	X	X	X	X	X	L
L	L	L	L	H	X	X	X	X	X	X	X	H
H	L	L	L	X	L	X	X	X	X	X	X	L
H	L	L	L	X	H	X	X	X	X	X	X	H
L	H	L	L	X	X	L	X	X	X	X	X	L
L	H	L	L	X	X	H	X	X	X	X	X	H
H	H	L	L	X	X	X	L	X	X	X	X	L
H	H	L	L	X	X	X	H	X	X	X	X	H
L	L	H	L	X	X	X	X	L	X	X	X	L
L	L	H	L	X	X	X	X	H	X	X	X	H
H	L	H	L	X	X	X	X	X	L	X	X	L
H	L	H	L	X	X	X	X	X	H	X	X	H
L	H	H	L	X	X	X	X	X	X	L	X	L
L	H	H	L	X	X	X	X	X	X	H	X	H
H	H	H	L	X	X	X	X	X	X	X	L	L
H	H	H	L	X	X	X	X	X	X	X	H	H
X	X	X	H	X	X	X	X	X	X	X	X	L

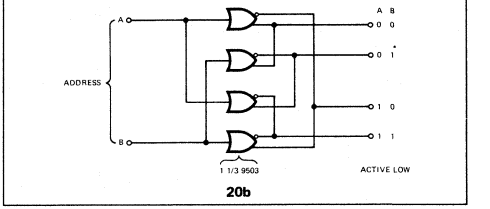
Fig. 19. 9581 Truth Table

Decoding: Using the 9503 and 9504 Gates

For decoding or demultiplexing, the true and complement outputs and the wire-OR features can be used to make a decoder in one gate delay. For example Figure 20a is a 2 to 4-line, active low decoder. If added delay can be tolerated, then the 2 to 4-line, active high decoder of Figure 20b can be used. In 20b the 9504 enable will force all inputs low for OR tying or serve as the "data in" line for demultiplexing.



20a



20b

3-Line, 8-Line Decoder: 9538

The 9538 decoder accepts three binary address inputs, and under control of the enables, activates one of the eight active LOW outputs. Both of the active LOW enable input lines must be LOW to enable the outputs. In other words, if either of the enable inputs is HIGH, all eight outputs remain HIGH. A truth table for the decoder is given in Figure 21.

The 9538 decoder can be used as a demultiplexer by connecting a data source to one of the enable inputs. The other enable input will function as a data enable line, while inputs A_0, A_1 and A_2 determine which of the eight output lines the data is fed to. The data will not be inverted through the demultiplexer since both the input and the outputs are active low. The delay through the demultiplexer from either enable input to an output is only two gate delays.

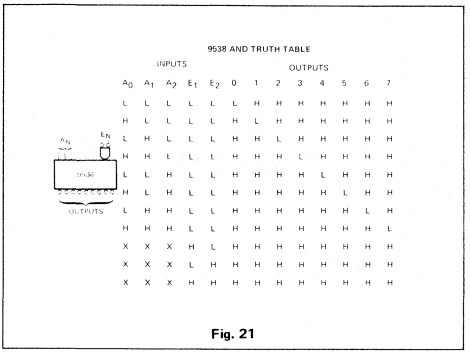


Fig. 21

Exclusive OR, Parity Checking

Using standard OR gates: If both assertion and negation inputs are available, an exclusive-OR may be implemented in only one gate delay, Figure 4.

This function is made available in the 9578 Quad Exclusive-OR gate, Figure 22. An additional feature of this product is the output enable.

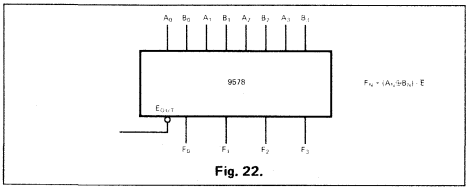


Fig. 22.

With this device a 4-bit comparator is made by OR-tying the four outputs. This output will be low only if $A_N \equiv B_N$, otherwise it is high.

An addressable comparator may be constructed using two or more 9578's and a decoder gate. Figure 23.

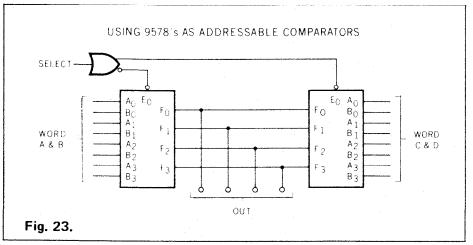


Fig. 23.

For parity checking, several 9578's may be connected together to yield a fast logic block (Figure 24).

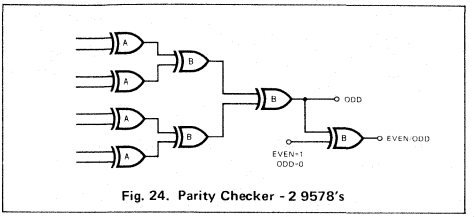


Fig. 24. Parity Checker - 2 9578's

The 9578 will function as an RF Mixer for $F_1 + F_2$ to over 150 MHz. In this application an RF spectrum analyzer will display a text book wave form.

WIRING RULES

General

It is possible to use 9500 in a variety of board constructions ranging from the simple PC or wired board without ground plane to the relatively complex multilayer PC board with ground plane on which all of the connections are terminated transmission lines. 9500 speeds and circuit features have been chosen so that most system manufacturers will find that the system design approach which gives them optimum cost/performance will lie somewhere between these two extremes, where both unterminated and terminated microstrip lines can be used over ground planes. 95H00 speeds are up to 50% faster and must use more restrictive wiring rules. For this reason, double-sided boards with ground planes are recommended for this high-speed logic.

I. Double-Sided PC Or Wired Board *Without Ground Plane*

Although a board with a ground plane gives the most reliable performance, it is possible to operate simple systems on a single board without a ground plane according to the following rules:

(1) Use PC or wired board with maximum size of 3 x 4 inches.

(2) Keep interconnects less than 8 inches total line length. Greater lengths may be used for some applications where increased ringing is tolerable.

(3) Use a common ground line of equal length or shorter than the common data line between interconnecting devices.

(4) Bypass each device at the package. The two V_{CC} pins (4 and 5) are joined together to ground via a 0.02 μF capacitor to V_{EE} (pin 12) at -5.2 V.

(5) Since interconnects must be very short for operation without a ground plane, the radial form interconnection shown in Figure 26a will be most practical.

(6) Minimize interconnections between two or more boards and use a controlled impedance line such as RG-174 50-ohm coax or twisted pair (see Figure 26 for terminations) if any length greater than 8 inches is

encountered. For larger systems of several boards, it is advisable to use ground plane construction.

(7) For distribution of high frequency (such as clock pulses), terminated 50-ohm coax or twisted pair can be used, secured to the board with adhesive or cable ties.

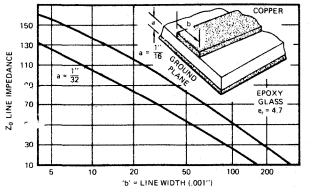


Fig. 25. Characteristic Impedance for Microstrip.

II. Double-Sided PC (Wired) Board *with ≥60% Ground Plane*

Relatively large systems of 100 or more packages can operate reliably using boards on which a ground plane is plated on one side. With a ground plane present, the conductors on the opposite surface of the board appear electrically as microstrip transmission lines with a specific characteristic impedance Z_0 (typically 85–150 ohms). See Figure 25. Ideally, for minimum reflections, both source resistance R_S and load resistance R_L should each equal Z_0. However, this is not always practical or necessary in a real system where interconnections between source and load are often short enough so that the circuit rise times are longer than the interconnecting line delays. Any reflections are masked in the rising edge of the input waveform and do not seriously affect logic operation. It is on this basis that 9500 rise times of 2.5 to 3.0 ns and on-chip pulldown resistors allow reliable operation with unterminated lines on PC boards of 6 to 8-inch sides. Here interconnections are generally less than 9500 rise times. The following rules will help establish optimum performance for ground plane microstrip unterminated or terminated connections:

Printed circuit interconnections become microstrip transmission lines when backed up by a ground plane. Thus, the standard equations describing transmission line behavior apply. This means a characteristic impedance can be associated with a line, and reflections will occur unless the line is terminated in this impedance. Typical microstrip transmission lines have a characteristic impedance between 50 and 150 ohms. It can be calculated by the following equation developed by H. R. Kaupp ("Characteristics of Microstrip Transmission Lines," IEEE transactions on Electronic Computers, Vol. EC-16, No. 2, April 1967, pp. 185-193):

$$Z_0 = \frac{87}{\sqrt{E_r + 1.41}} \times \ln \frac{5.98\,h}{0.8w + t}$$

where Z_0 = Characteristic Impedance
E_r = Dielectric Constant (4.7 for epoxy-glass) (4.5 for phenolic-glass)
w = Width of line
t = Thickness of line
h = Thickness of dielectric

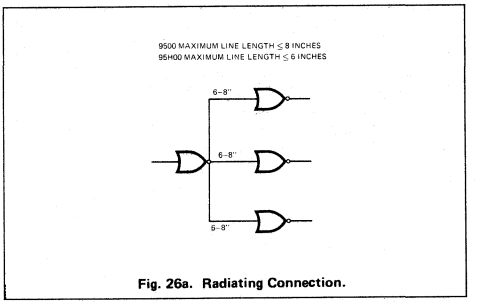


Fig. 26a. Radiating Connection.

This type of connection is preferable for unterminated lines and should be kept short (1-2 inches) for minimum inductive effects. For terminated inputs the maximum fan-out current must not be exceeded.

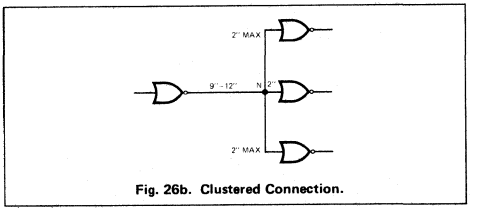


Fig. 26b. Clustered Connection.

This type of connection can be used with or without terminated lines. For terminated lines it is preferable to keep the lines from node N to each input equal in length, very short and terminated at N. Distributed connections should be used if the lines from node N to input exceed one inch.

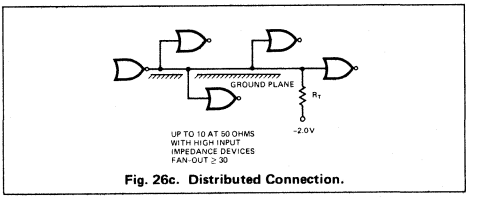


Fig. 26c. Distributed Connection.

This type of connection is preferred for long terminated lines such as clock runs. Termination should be made at the last input. For unterminated connections, the input nearest the source will be slowest in operation because of multiple reflections from the other loads. This is especially true when line length approaches the 8-inch limit of unterminated connections.

(1) Unterminated Load Distribution

In general, any connection arrangements can be used within the maximum unterminated D.C. fan-out of 20, providing all connections are no more than eight inches from source to load and the propagation delay is within the rise times of 9500. The shorter the interconnections, the less the probability of undesirable effects such as ringing and crosstalk. For 95H00, unterminated connections must be less than 5 inches from the source.

It may be possible to use up to 12 inches on unterminated line (8 inches with 95H00) with clustered loads with no undesirable effects. Wire ORing can always be carried out providing sources are less than 2 inches apart. Otherwise, logic timing must be considered. Each OR input appears as one logic load to the other outputs. *If critical timing paths are encountered, the simple single resistor terminated to -5.2 V (the technique shown in Figure 27a) will provide optimum speed.* The value of this resistor should be selected to load the outputs with a total D.C. current of 30 mA. Other resistors on gate inputs and outputs must be considered to prevent exceeding the 40 mA maximum current rating.

(2) Terminated Load Distribution

For distribution of high-speed signals such as clock pulses, where minimum delays are required or where intolerable reflections are incurred in interconnections that are more than 8 inches (5 inches with 95H00), it is desirable to terminate the microstrip line in its equivalent impedance. *Figure 27b* shows the various forms of interconnection that can be used on terminated lines with more than one input. The Data Buss interconnection method should be used for more complicated arrangements where more than one data source is present and large areas of data distribution are required. (Figure 29.)

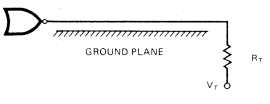


Fig. 27a. Single-Resistor Termination.

This enables the use of a single resistor terminated to -2V. For some applications for up to a fan-out of 5, a single resistor to V_{EE} may be used. The maximum fan-out current should not be exceeded for the later termination. In this case, a typical application would be in terminating a distributed load clock run of 6 to 12 inches.

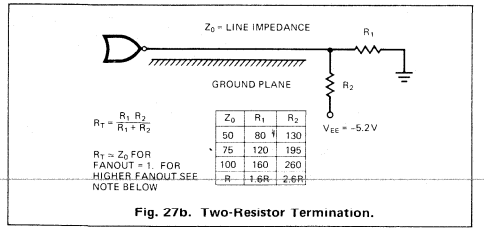


Fig. 27b. Two-Resistor Termination.

This avoids bringing -2V onto the board. *NOTE* that as fan-out increases beyond 4 at the end of line, as in *Figure 27b,* the paralleling of the internal 2-kilohm pulldown resistor at each input required that R_2 be increased to maintain correct termination. For example, FO = 6, Zo = 100, then R_1 = 160, R_2 = 1.17 kilohms.

System fan-outs of more than 4 at the end of a terminated line are uncommon. If a higher number of clustered loads at the end of a terminated line is desired, the lowest line impedance (m 50) should be used and the correct R_2 calculated.

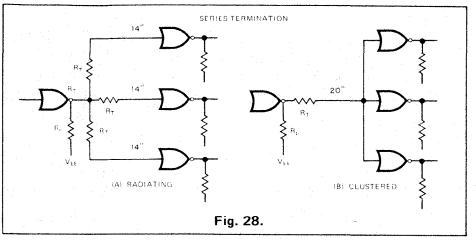


Fig. 28.

(3) Series Termination

Series termination can be used with the high input impedance 95L00 devices whenever lines longer than 8 inches are needed and it is undesirable to terminate the load ends of each line. The technique shown in Figure 28a allows radiating type connections up to 14 inches on each leg. In Figure 28b connections over 20 inches can be used. In this case, a reflection will occur from the gate load but will be absorbed by the series termination resistor at the source.*

A good rule for calculating the value of the series terminating resistor (R_T) is to subtract 5 ohms from the loaded transmission line impedance. For example, a 75-ohm line, minus 5 ohms, yields a series termination resistor value of 70 ohms. A standard value resistor (68 ohms) would be close enough. For a 50-ohm line, a 43-ohm standard resistor is a good choice.

The value of the pulldown resistor (R_P) should be a minimum of 150 ohms, but can be optimized around other values, depending upon the desired speed, power or fan-out. Driving a 50-ohm transmission line (series terminated with 40 ohms) with an 0.85-volt logic swing requires a surge current capacity of 8.8 mA. This requirement is met with an R_P of 500 ohms to V_{EE}.

Better speeds can be obtained when driving three 50-ohm, series-terminated lines with an R_P of 1/2 to 1/3 the 510-ohm value. But the additional decrease in fall time speed may present more problems, such as ringing.

Generally, the series termination speed will be slower than the shunt. This is caused by degradation of the rise and fall times with the series resistor and the capacitive load. But series termination allows the use of radiating type lines to drive several locations on back panels, as opposed to shunt type terminations which would require additional gate outputs. For certain types of connections this additional wiring advantage offsets the slower speed.

*NOTE: This technique should not be used to drive low input impedance 9500 or 95H00 devices. The additional pulldown current of the 2-kilohm input resistor will lower the noise margin by 100 to 300 mV, which is totally unacceptable.

(4) Data Buss Termination (Wired OR)

This kind of interconnection is usually required when data must be distributed over a large area to a number of loads. These loads may stem from two or more sources

that are located in different parts of the system, such as between boards. Care should be taken in logic timing to ensure that sources are not activated simultaneously. Since a system malfunction results when any load receives both source data outputs at odd time intervals, due to line delays, the following precautions must be taken:

(a) ORed connections may always be made within 2 inches of each other. For any greater distance, differences in logic timing must be considered but may be placed anywhere on the line. Each OR output is effectively one gate load. When using high input impedance 95L00 devices, wire ORing greater than 30 is possible with slight speed degradation (1.5-3.0).

(b) If the distance between any of the sources and either end of the line is greater than 8 inches (5 inches with 95H00), the line must be terminated at the more distant end. If both ends are at least 8 inches from any source, both ends must be terminated as shown in Figure 29. For this double termination, the interconnecting line impedance should be as high as is practical (e.g., 100 to 150 ohms), since each source will be driving into an equivalent load of half the line impedance. If a 50-ohm line has a double termination, it is possible to provide increased drive by paralleling two adjacent gates in a single package. Because of current hogging conditions between sources, however, maximum fan-out should be limited to 30 standard gates for single terminations or to 15 for double 50-ohm (i.e., 25-ohm) terminations. Generally, the high input impedance devices should be used for double termination schemes.

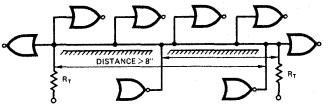


Fig. 29. Data Buss Termination.

If both ends are at least 8 inches from any source, the line requires double termination for best performance.

(5) Decoupling

A minimum of one small (0.01 μF) ceramic capacitor should be used for every five to ten packages, and at least one large (2-20 μF) tantalum capacitor per board should be used between V_{EE} and ground (V_{CC}). Capacitors should be used liberally around the highest frequency components, such as flip-flops. When using boards with large areas of ground and power planes, then the 0.01 μF ceramic capacitor can be reduced in value or eliminated.

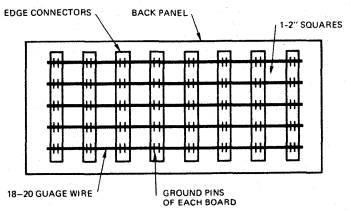


Fig. 30. Backpanel Ground Screen.

(6) Back Panel Wiring (Figure 30)

A ground screen can be constructed on the back panel of the system that interconnects with the board ground planes. This will provide an adequate screen for any data line passing over it between boards. The terminated line arrangements should be used as described above in the paragraph on terminated load distribution.

(7) Line Driving

The two basic modes most commonly used for line driving are differential and single-ended. The differential mode is generally superior to the single-ended mode in terms of noise immunity. Both coaxial cable and twisted pair can be used in these modes, with coax providing superior performance at greater expense.

(a) Coaxial Cable

For differential driving, Figure 31a shows a method of termination which must use coax of 75 ohms or higher with 9500 circuits to avoid exceeding the maximum current ratings. Differential drive through 2 coax lines will yield the highest possible speed with maximum noise rejection. In this mode each coax is terminated in its characteristic impedance to -2V, as if it were used in the single-ended mode.

The single-ended mode is shown in Figure 31b. It can use 50 or 75 ohms with appropriate termination. Over 10 feet of 50-ohm or 75-ohm cable may be driven without serious attenuation.

(b) Twisted Pair

Figures 31c and 31d show differential and single-ended modes respectively for twisted pair cable. Up to about 20 feet can be driven without serious attenuation.

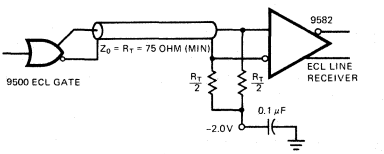


Fig. 31a. Differential Transmission Coax.

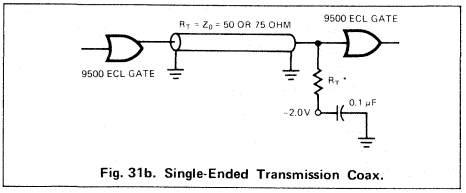


Fig. 31b. Single-Ended Transmission Coax.

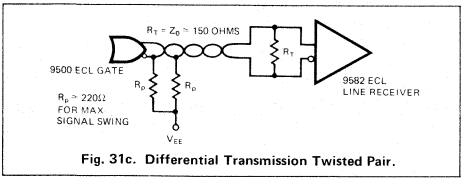


Fig. 31c. Differential Transmission Twisted Pair.

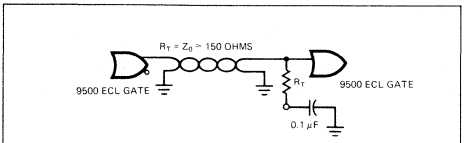


Fig. 31d. Single Ended Transmission Twisted Pair.

NOISE CONSIDERATIONS

Noise is classified under two categories of unwanted signals:
(a) Externally generated noise
(b) Internally generated noise

I. External Noise

This is due to external influences in the system such as motors, fluorescent lighting or power lines. External noise can best be attenuated by standard means of good cabinet design and power line filtering. A full description of this kind of noise is beyond the scope of this discussion. The design of 9500 ECL maintains a constant noise margin sufficient to prevent false logic levels caused by external noise. The percent noise margin of 9500 is at least as good as that of standard TTL logic, and the low impedance lines associated with ECL are generally immune to RF noise.

II. Internal Noise

Internal noise is attributable to the operation of the system itself. For convenience these types of noise are classified as follows:

(1) Reflections and Ringing
(2) Crosstalk
(3) Power Distribution

By allocating connector pins spaced above ground and connected both internally to the board ground plane and externally to the cross wires, an effective ground screen is formed. Data wires passing directly over the screen form transmission lines (Zo $\simeq$ 150 ohms) and can be treated as such. Values of Zo can vary ±50% or more. If excessive, ringing and reflections can be limited by ferrite beads slipped over data wires near the connector pins.

(1) Reflections and Ringing

The conditions which cause reflections or ringing can best be shown by this example:

Line Delay Greater Than Half Rise Time
$T_D > 0.5\ t_r$ (Figure 32a).

This diagram shows the unterminated line conditions under which large reflections can occur. If the design rules for terminated lines are followed, however, extreme amplitudes of greater than 20% logic swing should seldom be encountered. For the majority of such interconnections, the amplitude will be 5% or less, even for a relatively poor termination. Generally, the undershoot of a reflected wave front is a greater problem than overshoot, since undershoot causes temporary reduction in noise immunity as the waveform excursion approaches the logic threshold. A 20% reflection represents a 50% loss of noise immunity for a time as long as the undershoot exists. Overshoot has to be considerable (25% or more) to risk driving the load circuit input transistors into saturation. Therefore, it is not a problem if reasonably good terminations are achieved.

Line Delay = Half Rise Time
$T_D = 0.5\ t_r$ (Figure 32b)

For this condition, in which the electrical delay length of the line approaches that of the circuit rise time, the reflections get closer together and are generally referred to as ringing, since this is how they appear on an oscilloscope. Ringing may be a problem when stretching the unterminated design rule line length to a maximum of 8 inches or more. What constitutes tolerable undershoot or overshoot will be different for various systems. Generally the 20% of logic swing rule of thumb applies.

Line Delay Less Than Half Rise Time
$T_D < .5 t_r$ (Figure 32c)

For this condition, the line appears to be capacitive, rise times are slightly slower and ringing is minimal. Thus, unterminated wiring rules apply, and few noise problems are encountered. The internal pulldown resistors ensure adequate fall times. For lines between 4 and 8 inches, *in cases where speed and timing are critical*, a single resistor to V_{EE} will insure maximum frequency of operation. Maximum output current must not be exceeded (Figure 27a).

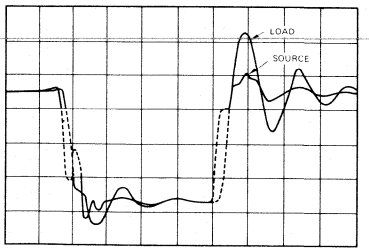


Fig. 32a. Line reflections at $T_D > .5\ t_r$, unterminated line, four gates clustered at 12 inches from source, 10ns/0.2V/cm.

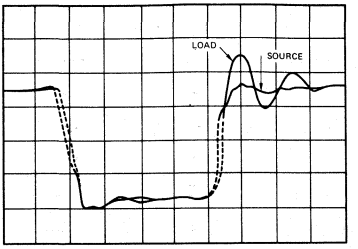
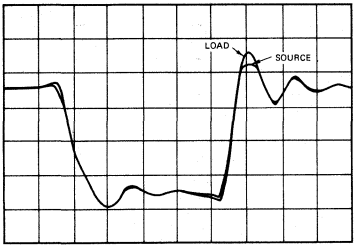


Fig. 32b. Line ringing at $T_D = 0.5\ t_r$, unterminated, four gates clustered at 8 inches from source, 10ns/0.2V/cm.



***T_D = Propagation Delay of Line, t_r = Pulse Rise Time.**

Fig. 32c. Line Ringing at $T_D < .5\ t_r$, unterminated, three gates radiating on 2-inch stubs, 5ns/0.2V/cm.

(2) Crosstalk

Crosstalk is the unwanted coupling of one signal path to another by mutual capacitance or inductance. Because of the high frequencies involved, the following nominal amount of care in board layout should be observed:

Keep adjacent data paths no less than one board thickness or one line thickness apart, whichever is greater.

Do not allow more than 2 to 6 inches of parallel runs when adjacent data paths are this close.

Generally, the inherent good noise immunity and low impedance of 9500 will minimize crosstalk. Separate V_{CC} ground pins for emitter follower and current switches of each 9500 circuit reduce on-chip crosstalk to a negligible level. A large area of ground plane ensures low crosstalk.

(3) Power Distribution

The following rules should be adopted for safe performance.

(a) Voltage drops on V_{EE} lines between gates should be minimized by using maximum conductor area for current to be carried, or by ring connection around the board.

(b) Connections to ground or ground plane must be as short as possible.

(c) Since 9500 logic levels are a function of supply voltages, supply variations are best kept to ±5%, which is normal for most industrial systems. A significant improvement in system noise immunity can be gained with 9500, especially under worst-case conditions, if power supply variations are kept to ±2% or less. This is because levels are directly controlled by the supply voltages.

(d) Use decoupling capacitors as stated in the wiring rules.

9500 SYSTEM THERMAL CONSIDERATIONS

When 9500 ECL is operated in still air or in unknown air movement, the permissible range of ambient temperature operation is 0°C to 75°C with ±5% power supplies. With ±2% power supplies and a minimum of 500 linear feet per minute airflow, 9500 ECL meets all DC specs from 0°C to +125°C. Above 100°C with ⩾ 500 linear feet per minute airflow, AC performance (T_{PD}) must be derated by 33%.

SPECIAL CLOCK CIRCUITS

General

Crystal oscillators and monostable multivibrators are two types of special circuits often encountered in high-speed digital systems. To use a digital gate as an oscillator, it must be biased into its linear operating region and have a high input impedance (> 2 kΩ). The 9582 line receiver satisfies these conditions.

Fundamental Crystal Oscillator (Figure 33a)

The fundamental crystal oscillator requires no tank circuit. The 9582 serves simply as an amplifier, with the crystal in the series mode functioning as a bandpass filter. C_A is the fine frequency adjustment, but if small variations of frequency are not needed, it can be replaced with a short circuit.

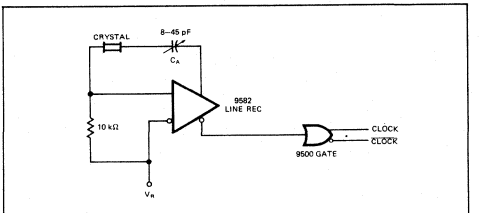


Fig. 33a. Fundamental Crystal Oscillator (1-20 MHz).

Overtone Crystal Oscillator (Figure 33b)

The overtone crystal oscillator employs an adjustable resonant tank circuit which insures operation at the desired crystal overtone.

C_1 and L_1 form the tank circuit, which has a resonant frequency adjustable from 30 MHz to 100 MHz with the values specified.

Overtone operation is accomplished by adjusting the tank circuit frequency to or near the desired frequency. The tank appears to be a shunt to all frequencies except those near resonance. Operation in this manner insures that the oscillator will always start at the correct overtone. C_A is the fine frequency tuning.

With both fundamental and overtone oscillators the gate serves the dual purpose of buffer and wave-shaper. The output of the first 9582, which is approximately a sine wave, is fed into the gate which shapes it into a square wave with rise and fall times of approximately 2.5 ns.

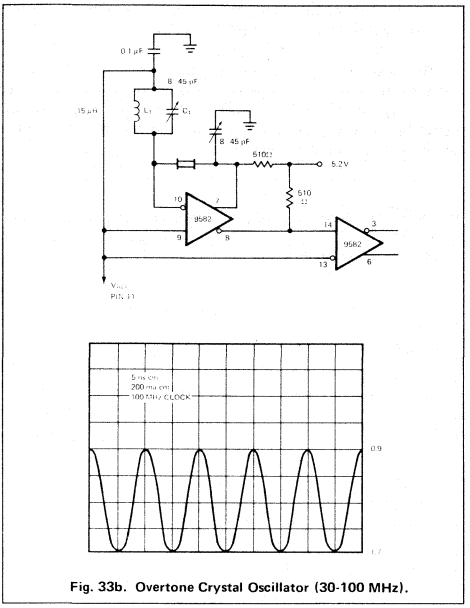


Fig. 33b. Overtone Crystal Oscillator (30-100 MHz).

Clock Restorer/Monostable

The circuit in Figure 34 can be used to restore clock pulses to standard rise and fall times and pulse width. This circuit also can be used to convert a change in logic level from "0" to "1" to a pulse with a well-defined width.

An advantage of this monostable is that the output pulse width is determined solely by delay D. Circuit operation can best be described by following the numbers and events on the circuit.

When the input goes positive (1) the complement output (2) becomes negative. Since the true output (3) had been LOW, the output of the delay line (4) is also LOW. With both inputs into gate 2 LOW, the complement output (5) goes HIGH, removing the control from the input. The input now can assume any state with no effect on the output pulse. The outputs of gate 2 will stay in this state until the logic "1" from the true output of gate 1 (3) arrives at the input of gate 2 (4). At this time gate 2 outputs will change state and control will be restored to the input (1). If the input is still up, it must return to logic "0" for at least "D" ns before the cycle can start again. Should it be at logic "0", at least "D" ns must elapse before it can be recycled.

The delay device used can range from a length of terminated coax or standard delay line to several gates in series. One gate, using its true output, can be used for a minimum pulse width. Caution should be exercised when using this minimal pulse, since it will not have a flat top. It will appear as 1/2 of a sine wave, with its width slightly greater than its rise/fall time.

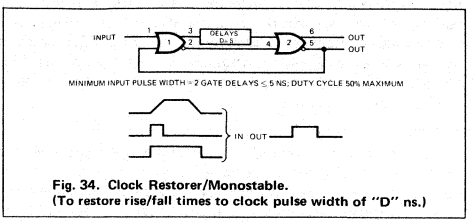


Fig. 34. Clock Restorer/Monostable.
(To restore rise/fall times to clock pulse width of "D" ns.)

LOGIC CONVERSION

General

The 9500 family can be interconnected with other ECL families with little difficulty. Because of superior output level control, and internal pulldown resistors, 9500 can be directly connected to MECL II, III without external components or terminating resistors. Conversion circuits are included for TTL and DTL levels. Generally a fan-out of one is recommended when converting from one circuit family to another. Also, lines into and out of the converter circuits should be short. When interfacing, some circuits will need a reference voltage centered on the 9500 logic swing. This may be derived from any standard 9500 gate simply by returning the complement output to its input with a line of less than 1 ns delay, as shown in Figure 35.

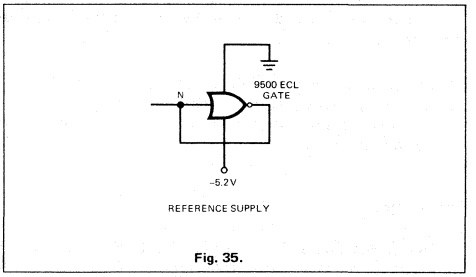


Fig. 35.

Interface Between Motorola MECL II, III 10K, and 9500

Wire directly without any external resistors. Limit fan-out between families to one.

Interface Between Texas Instruments ECL 2500 and 9500

V_{CC} must be common for both circuits. Two separate V_{EE}s are required. Wire directly without any external resistors. Use 9500 gate for TI 2500 reference voltage as shown in Figure 35. Fan-out may be four or more between 9500 and 2500 when operated in this manner.

ECL/TTL INTERFACE

Mixing 9500 series ECL and TTL logic families offers the design engineer a new level of freedom and opens the entire VHF frequency spectrum to the advantages of digital measurement, control and logic operation.

The chief advantages of emitter coupled logic are high speed, flexibility, design versatility and transmission line compatibility. But application and interfacing cost problems have traditionally discouraged the use of ECL in many areas, particularly in low-cost, less sophisticated systems. Using 9500 temperature-compensated ECL with new ECL/TTL interface devices and several new methods of interfacing with all TTL circuits promises to extend the advantages of ECL to many low-cost systems designs.

The interfacing method that may be most practical for smaller systems involves using a common supply of +5 to +5.2 volts. Care must be exercised with both logic families when using this technique to assure proper bypassing of the power supply to prevent any coupling of noise between circuit families. If only a few 9500 ECL packages are designed into a predominantly TTL system, the safest method is to use a 0.01-μF miniature ceramic capacitor across each 9500 device. This value capacitor has the highest Q, or bypassing efficiency. When larger systems are operated on a common supply, separate power busses to each logic family will help prevent problems. Otherwise, good high frequency bypassing techniques usually will be sufficient.

9500 devices are delivered with either high resistance (>20 kilohm) or low resistance (2 kilohm) pulldown resistors at their inputs. The low input resistance ECL devices (basic 9500 series) are generally easier to use. This is because these resistors can replace the costly external pulldown or termination resistors normally required and can improve stability by keeping the input impedance positive real, which eliminates oscillation. When using these Fairchild 9500 devices with short lines (less than 8 inches) no additional external components are needed.

All circuits described will operate with ± 5% ECL and ± 10% TTL power variations, except those with ECL and TTL on a common supply. In those cases a ± 5% supply will assure proper performance.

TTL to ECL

The easiest conversion is from TTL to ECL, and is best done with resistors. An ECL gate should be used as a buffer if high fanout is required. Resistors always will suffice because the amount of signal attenuation is compatible with the required DC offset. Additional factors to be considered are converter circuit delay and drive requirements. Figures 36a and 36b both assume an unloaded TTL gate as the standard TTL source.

The input capacitance of an ECL gate is about 5 pF. With the 2 to 4-ns transition times, this gives a peak input current of 1 to 3 mA. The resistor divider, when calculated to load the driving gate with about 5 mA, will have a delay of only 2 to 3 ns. Since this usually is faster than the TTL rise times, it is normally considered adequate.

If power is to be minimized and extra delay can be tolerated, the current through the converter circuit may be reduced. However, it is important to remember the internal 2-kilohm resistor between the ECL input and V_{EE} when using this type of circuit.

ECL to TTL

When interfacing between high voltage-swing logic such as TTL and low voltage-swing logic such as ECL, the more difficult conversion is from ECL to TTL. This requires a voltage amplifier to build up the 0.8-volt logic swing to a minimum of 2.5 volts. The circuits shown in Figures 36c and 36d or a 9595 may be used to interface from ECL to TTL.

The higher-speed converters usually have the lowest fanout —only one or two TTL gates. This fanout can be increased simply by adding a TTL buffer gate to the output of the converter. Another option, if the ultimate speed is required, is to use additional logic converters.

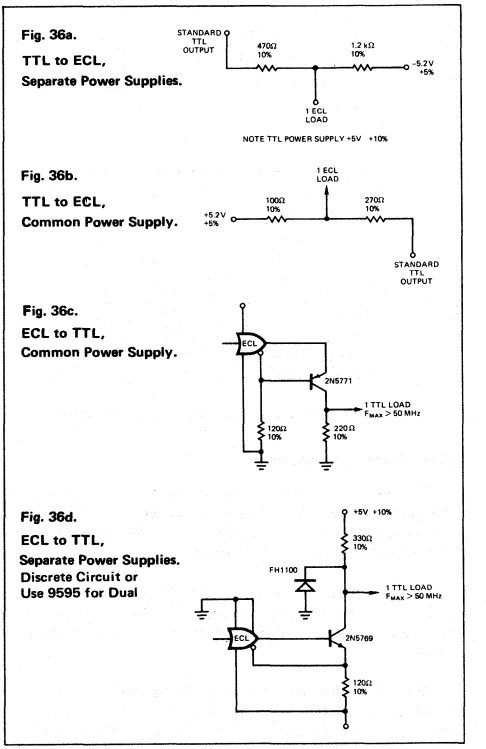


Fig. 36a. **TTL to ECL, Separate Power Supplies.**

Fig. 36b. **TTL to ECL, Common Power Supply.**

Fig. 36c. **ECL to TTL, Common Power Supply.**

Fig. 36d. **ECL to TTL, Separate Power Supplies. Discrete Circuit or Use 9595 for Dual**

CONCLUSION

Very high speed systems can be designed by using 9500 series ECL circuits. The temperature-compensated inputs and outputs and the good noise immunity of 9500 series systems provide reliable operation over a large temperature range. Speed is enhanced by the high speed of the basic gate, the low number of gate delays encountered in MSI circuits and by the relatively few and short interconnections required. The logic flexibility of ECL circuits and the availability of MSI functions permit systems to be implemented with a minimum number of packages, which in turn minimizes the required interconnections.

TEMPERATURE COMPENSATED ECL

THEORETICAL DESIGN

In the past, standard ECL circuits have caused problems in characterization at different temperature levels as well as system noise immunity loss due to temperature gradients. These problems were due to use of the low output impedance emitter follower which enabled the heavy load driving required in system applications. Standard ECL circuit logic levels and threshold are a function of temperature. The logic "1" level is a direct function of high current density V_{BE}. The logic "0" level and threshold are set by the resistors chosen with the bias voltage tracking at one half the logic "1" and logic "0" level temperature deltas.

The primary consideration in this paper is a new circuit shown in Figure 1 which offers temperature invarient levels and internal threshold. The primary advantages of this circuit are an increase in system noise margins due to the loss of temperature gradient effects, an increase in producibility due to the elimination of V_{BE} drifts due to process and hence a tighter control of logic level voltage spreads. The differences with respect to a normal ECL current sourced gate are the addition of two diodes in the bias driver and a network connected between the output device base nodes.

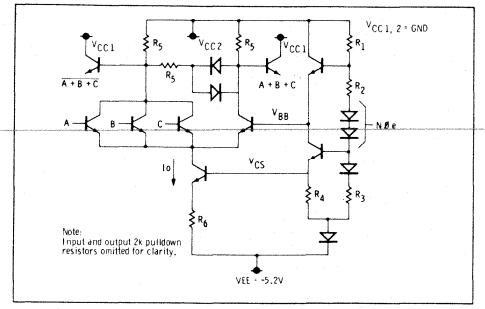


Fig. 1.

Threshold Level V_{BB}

Analysis of the new bias driver network shows that the V_{BB} level (threshold) can be expressed by the following equation.

$$V_{BB} = -\Phi e - \frac{R_1}{R_1+R_2+R_3}\left[|V_{EE}| - (N+2)\,\Phi e\right] \quad (1)$$

$$= -\Phi e\left[1 - \frac{(N+2)\,R_1}{R_1+R_2+R_3}\right] - \frac{R_1\,|V_{EE}|}{R_1+R_2+R_3} \quad (2)$$

N = number of diodes in bias chain at junction of R_2 and R_3

This implies that for V_{BB} to be temperature invarient all the terms involving Φ e (emitter-base forward voltage) must be removed. The result will be dependent solely on V_{EE}, resistor ratio and second order temperature effects.

$$\therefore\ 1 - \frac{(N+2)\,R_1}{R_1+R_2+R_3} = 0 \quad (3)$$

$$N+2 = \frac{R_1+R_2+R_3}{R_1} \quad (4)$$

$$\therefore\ V_{BB} = -\frac{|V_{EE}|}{N+2} \quad (5)$$

Analysis of the output voltages in terms of current source, current I_o results in the following equations, regardless of the input state, for V_H (logic high level) and V_L (logic low level).

Logic Low Level V_L

$$\frac{V_L+\Phi e}{R_5} + \frac{V_L+2\Phi e}{2R_5} = -I_o \quad (6)$$

$$\frac{3}{2}\frac{V_L}{R_5} + \frac{2\Phi e}{R_5} = -I_o \quad (7)$$

$$V_L = -(I_o + 2\Phi e)\,\frac{2R_5}{3} \quad (8)$$

$$V_L = -\frac{2R_5 I_o}{3} - \frac{4\Phi e}{3} \quad (9)$$

Logic High Level V_H

$$V_H = \frac{R_5}{2R_5}\left[V_L + 2\Phi e\right] - \Phi e \quad (10)$$

$$= \frac{V_L}{2} + \Phi e - \Phi e \quad (11)$$

$$= \frac{V_L}{2} \quad (12)$$

This implies that if V_H is temperature independent, then V_L must necessarily also be temperature independent. This is critical as the choice of network yielding temperature compensation must work with a single switching current source.

$$\text{Now } I_o = \left[\frac{R_3}{R_1 + R_2 + R_3}\left[|V_{EE}| - (2+N)\Phi e + 2\Phi e - 2\Phi e\right]\right]\frac{1}{R_6} \quad (13)$$

$$= \frac{R_3\,(|V_{EE}| - (2+N)\,\Phi e)}{R_6\,(R_1 + R_2 + R_3)} \quad (14)$$

$$V_L = \frac{-4\,\Phi e}{3} - \frac{2\,R_5 R_3\,(|V_{EE}| - (2+N)\,\Phi e)}{3\,(R_6)\,(R_1 + R_2 + R_3)} \quad (15)$$

$$= -\Phi e\left[\frac{4}{3} - \frac{2\,(N+2)\,R_5 R_3}{3\,(R_1+R_2+R_3)\,R_6}\right] - \frac{2\,R_5 R_3\,|V_{EE}|}{3\,R_6\,(R_1+R_2+R_3)} \quad (16)$$

If V_L is to be solely a function of V_{EE} then the terms in Φ must be made equal to zero.

$$\therefore \frac{2\,R_5 R_3}{3\,(R_1 + R_2 + R_3)\,R_6} = \frac{4}{3\,(2+N)} \quad (17)$$

$$\therefore V_L = \frac{-4\,|V_{EE}|}{3\,(2+N)} \quad (18)$$

$$\therefore V_H = \frac{V_L}{2} = \frac{-2\,|V_{EE}|}{3\,(2+N)} \quad (19)$$

As a result, with selected power supply voltage and operating levels, it is possible to adjust the number of diode drops (N in equations) to yield the required levels. ECL circuits have in general used the −5.2 volt power supply because of market acceptability and the fact that this power supply approaches the minimum which will allow two levels of vertical gating. In addition, V_H for most logic families has been in the −850 mV region for high speed circuits.

$$\therefore -.85 = -\frac{2}{3}\,\frac{(5.2)}{2+N} \quad (20)$$

$$\therefore (2+N) = \frac{5.2}{.85} \times \frac{2}{3} = \frac{10.4}{2.55} \approx 4 \quad (21).$$

The family of circuits developed by Fairchild uses a total of four diodes in the bias driver to obtain a fully compensated circuit set. The voltage dependence for the logic levels and threshold is shown below.

$$V_H = -\frac{|V_{EE}|}{6} \quad (22)$$

$$V_L = -\frac{|V_{EE}|}{3} \quad (23)$$

$$V_{BB} = -\frac{|V_{EE}|}{4} \quad (24)$$

A comparison of transfer characteristics between temperature compensated and incompensated ECL gates is shown in Figures 2 and 3. An indication of the control of the levels and threshold is given by the transfer characteristic (V_{IN} vs V_{OUT}).

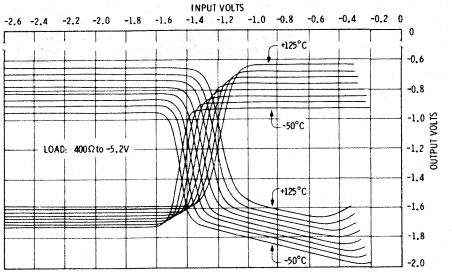


Fig. 2. Transfer characteristics of uncompensated ECL (shown for temperature range −50°C to +125°C in increments of 25°C).

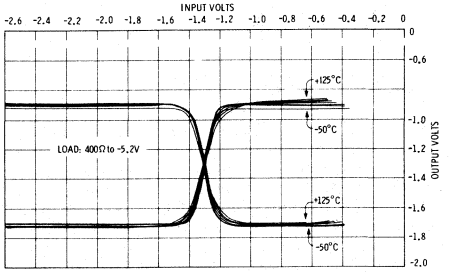


Fig. 3. Transfer characteristics of 9500 temperature compensated ECμL (shown for temperature range −50°C to +125°C in increments of 25°C).

COLD TEMPERATURE OPERATION

It should be noted that at cold temperatures the compensating cross connect network composed of two diodes and a resistor has insufficient forward bias to guarantee current flow. When this occurs, it can be shown that the levels change as a function of temperature and track at the normal V_{BE} rate towards the threshold.

$$V_H = -\Phi e \quad (25)$$

$$V_L = -\Phi e - R_5 I_o \quad (26)$$

$$= -\Phi e\,\frac{R_5 R_3\left[|V_{EE}| - (2+N)\,\Phi e\right]}{R_6\,(R_1+R_2+R_3)} \quad (27)$$

It has previously been shown (page 2 equation 17) that for the compensation to work, the following equations are true.

$$\frac{R_5 R_3}{R_6\,(R_1+R_2+R_3)} = \frac{2}{2+N} \qquad N = 2 \text{ (two diodes)} \quad (28)$$

$$\therefore V_L = -\Phi e - 1/2\left[|V_{EE}| - 4\,\Phi e\right] \quad (29)$$

$$= -\frac{|V_{EE}|}{2} + \Phi e \quad (30)$$

The important consideration now is whether the loss of noise immunity is equal on the logic "1" and logic "0" levels and whether the threshold of the new levels is still $V_{BB} = V_{EE}/4$.

An examination of the new V_H and V_L equations indicates the high level will decrease at the diode temperature tracking

rate and the low level will increase at the diode tracking rate. In addition, if we define $V_{BB} = (V_H + V_L) / 2$, then

$$V_{BB} = -\frac{\left[|V_{EE}|/2 + \Phi e - \Phi e\right]}{2} \quad (31)$$

$$= -\frac{|V_{EE}|}{4} \quad (32)$$

This guarantees both the normal operating range and the sub zero centigrade region have the same V_{BB} which implies noise immunity will be defined solely by the driving gate's temperature (i. e. fixed if above 0°C ambient decreasing from the fixed value for $T_A < 0°C$). It also guarantees that the input signal will always be centered with respect to V_{BB} resulting in the same gate delays over the entire temperature range (−50°C to 75°C). The loss of signal swing at −50°C is insufficient to increase the unit delays due to the high overdrive situation normally existing in ECL circuits.

SATURATION PERFORMANCE

Another serious consideration for any ECL derived circuit is the performance limiting parameters at high temperature. The most significant parameter here is saturation because saturation at light levels affects the circuit speed by causing storage. Upon gross saturation, the logic levels are adversely affected. Figures 2 and 3 should be reviewed at this time and it will be noted the temperature compensated circuit shows slight level shift due to saturation on both the logic "1" and logic "0" levels. This is caused by the interaction between the low level and the high level due to the diode-resistor cross connect network.

Figure 4 shows both circuits with the indicated voltage movement of both the voltage and temperature. For the sake of comparison, it will be assumed the two circuits are equivalent at one junction temperature (i. e. 25°C T_j). This implies that the logic swings, processing (i. e. V_{BE}'s), and forward bias on the base collector junction would be equal at this temperature. The requirement of equal base-collector bias is reasonable even though the internal collector voltages would be different nominally. The 9500 series gate would have a lower V_H under these conditions, but V_L is also lower by the same amount so for equal signal swings the collector-base junctions would be equally biased.

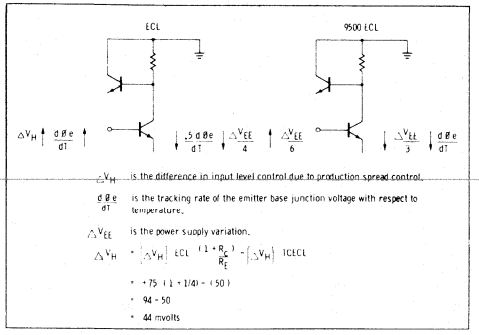


Fig. 4.

If we assume equal power supply control tolerance and worst case movements as shown to accentuate saturation, we could derive an equation relating the 9500 gate temperature increase (T_2) to the ECL gate temperature increase (T_1) in terms of V_{EE}.

$$V_{BC}(T_1) = V_{BC}(T_2) + K_2(T_2 - T_1) \quad (33)$$

$$V_{BC}(T_1) + K_2(T_1) = V_{BC}(T_2) + K_2(T_2) = V_{BCO} \quad (34)$$

where V_{BCO} defines the forward bias which results in a loss of speed due to storage at a fixed temperature (i. e. 25°C T_j). If we let V_{BCN} be the 25°C T_j normal forward bias, then

$$V_{BCN} + \Delta V_{BC}(T_1) + K_2(T_1) = V_{CBN} + \Delta V_{BC}(T_2) + K_2\ T_2 \quad (35)$$

$$\therefore \left[\Delta V_H + 1.5 K_1 T_1 + \Delta \frac{V_{EE}}{4}\right] + K_2(T_1) = K_1(T_2) + \Delta \frac{V_{EE}}{2} + K_2(T_2) \quad (36)$$

$$\Delta V_H + (1.5 K_1 + K_2)(T_1) = (K_1 + K_2)(T_2) + \Delta \frac{V_{EE}}{4} \quad (37)$$

$$(T_2) = \frac{(\Delta V_H - \Delta V_{EE}|4)}{K_1 + K_2} + \frac{(1.5 K_1 + K_2)(T_1)}{K_1 + K_2} \quad (38)$$

For most devices $K_1 \approx 1.5$ mV/°C, $K_2 \approx 2.2$ mV/°C

$$(T_2) = \frac{(\Delta V_H - \Delta V_{EE}|4)}{3.7} + 1.20(T_1) \quad (39)$$

Figure 5 shows the composite curves increase in junction temperature until saturation is reached vs. power supply tolerance for varying saturation temperature rise-of a standard ECL circuit. This type of worst case, considering levels due to production spread, V_{EE} and temperature, usually yields devices that saturate at 75 to 100°C T_j for standard ECL. If we assume a typical 85°C and ± 5% power supplies, it can be seen that this region of operation lies within the area where the temperature compensated 9500 gate would be superior.

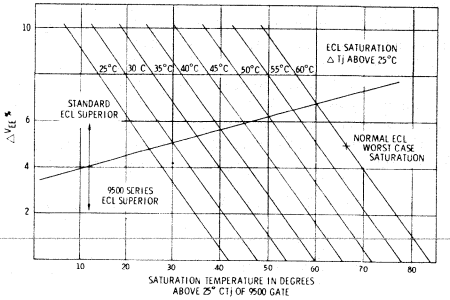


Fig. 5. Saturation comparison of 9500 ECμL gates and standard ECL.

Figure 5 also shows that the system designer now has the ability to control his device performance with power supply regulation. 10% – 20% improvements in the saturation temperature at the junction could be obtained by using a 9500 gate and controlling the power supplies to ± 2% regulation or better. The alternate approach with a standard ECL device would be to incorporate a stud-mounted package or other heat sink

design to minimize the junction temperature rise above ambient. System fabricators have increasingly found this latter solution to be cumbersome and expensive when compared to power supply regulation.

It should be noted that no mention of an additional forward bias due to an OR tied output driving the gate was made in this analysis. The addition of this worst case would cause a performance reduction in both gates.

By computing the effect on the ECL gate, the new maximum junction temperature could be computed and the equivalent 9500 gate saturation junction temperature could be located on Figure 5. This is possible due to the analysis looking at ΔT_j from a 25°C T_j where all things were equal. The new V_H resulting from the OR tie would increment the inputs equally on each gate because of the equal output impedance. This additional variable reduces the upper temperature limit for saturation on both products.

SYSTEM NOISE IMMUNITY

System noise immunity is also a function of production spread in levels and threshold, power supply tolerance and system temperature gradients if the levels have a temperature dependence. Unlike the saturation problem which occurs worst case when both gates are hot (driver and receiver), noise immunity is worst for a normal ECL gate when the system temperature gradient between driver and receiver is maximum.

ECL Gate

$$V_H = -\Phi e \ (\pm 75\ mV) \quad (40)$$

$$V_{BB} = -\Phi e - \frac{1}{8}(|V_{EE}| - 2\Phi e) \ (\pm 50\ mV) \quad (41)$$

$$V_L = -\Phi e - \frac{1}{4}(|V_{EE}| - 2\Phi e) \ (\pm 100\ mV) \quad (42)$$

The important thing to notice here is that the logic "1" level has no V_{EE} dependence as the bias driver and V_L do. V_{BB} is centered nominally, but it can be shown that the worst case noise immunity on the logic "0" level is lower than on the logic "1" level. If we define noise immunity as the separation of V_{BB} and V_H or V_L under worst case conditions, equations for the noise immunities can be written. This assumes equal threshold widths for both products, not an unreasonable assumption given the same device geometries and process.

$$V_{N1} = \frac{3}{4}\Phi e(hot) - \Phi e(cold) + \frac{|V_{EE}|(1-n)}{8} - \Delta V_{BB} - \Delta V_H \quad (43)$$

$$V_{N0} = \frac{1}{2}\Phi e(hot) - \frac{3}{4}\Phi e(cold) + \frac{|V_{EE}|(1-3n)}{8} - \Delta V_L - \Delta V_{BB} \quad (44)$$

Assuming a 60°C temperature gradient with a 25°C T_j at cold temperatures, V_{EE} = −5.2 volts ± 5% ΔV_{BB} = ± 50mV, ΔV_H ± 75mV, and ΔV_L ± 100mV, we could obtain some worst case noise immunities

for Φe = 0.85 volts and K_1 = 1.5 mV/°C

$$V_{N1} = -280 + 617 - 50 - 75 = 212\ mV \quad (45)$$

$$V_{N0} = -257 - 100 - 50 + 552 = 145\ mV \quad (46)$$

Threshold width for an ECL type gate at high current densities is typically 240 mV from unity gain to unity gain point. It would seem that only 20 – 30 mV of practical noise immunity is left on the "0" level and an OR tie still hasn't been considered. An additional problem with this circuit is that logic signals can be skewed because the temperature gradient can cause speed degradation in a large temperature gradient system.

9500 Gate

$$V_H = -|V_{EE}| \quad (47)$$

$$V_{BB} = -\frac{|V_{EE}|}{4} \quad -5.2 \text{ volt logic supply} \quad (48)$$

$$V_L = -\frac{|V_{EE}|}{3} \quad (49)$$

$$\therefore V_{N0} = \frac{|V_{EE}|}{12}(1 - 7n) - \Delta V_L - \Delta V_{BB} \quad (50)$$

$$V_{N1} = |V_{EE}|(1 - 5n) - \Delta V_{BB} - \Delta V_H \quad (51)$$

Again using ± 5% power supplies and the production spreads of the compensated gate (ΔV_L = ± 75 mV, ΔV_{BB} = ± 40 mV and ΔV_H = ± 50 mV), some noise margins can be calculated.

$$V_{N1} = \frac{5200}{12}(.75) - 40 - 50 \quad (52)$$

$$= 325 - 90$$

$$= 235\ mV$$

$$V_{N0} = \frac{5200}{12}(.65) - 75 - 40 \quad (53)$$

$$= 282 - 115$$

$$= 167\ mV$$

In both cases the noise immunity is better by 20 mV worst case and additional noise immunity could be obtained with tighter power supply control for the compensated 9500 gate. A standard ECL gate with ΔT_j = 60°C and ΔV_{EE} = ± 2% would have V_{N1} = 231 mV and V_{N0} = 204 mV; the 9500 gate would have V_{N0} = 257 mV and V_{N1} = 300 mV. The equalization of both logic "1" level and logic "0" level noise immunity would require the threshold to be offset 30 mV above the mean of the two nominal levels to obtain optimum performance for both circuits. The effects of OR ties have not been considered in this analysis but a large tie on the driven input does adversely effect both the saturation and the logic "0" level noise immunity.

This comparison illustrates that in systems applications requiring ± 5% power supplies and a 60°C ΔT_j because of package power level difference and system thermal hot spots, the temperature compensated gate is superior in available noise immunity. In addition, it is possible to increase this margin of extra noise immunity by tighter power supply control rather than by thermal equalization as required with standard ECL. The power supply tolerance and ΔT_j are representative of the ECL user's requirements and indeed the large computer houses frequently have better than ± 5% power supply control. If anything, in a system using MSI elements and gates, the ΔT_j would probably be larger than 60°C unless a custom design was made forcing package power levels to be the same. The superior performance of the 9500 gate is then accomplished by shifting the control from thermal to electronic with a resultant increase in saturation junction temperature which also allows higher operating junction temperatures.

APPLICATIONS OF THE 9538

INTRODUCTION

The ECL/MSI 9538 is a 1-out-of-8 ultra high speed decoder designed for use in high performance digital equipment. This device is compatible with all other 9500 ECL elements and offers the same high speed systems design advantages. These include temperature compensation to maintain noise margin across the full operating range, input-output circuits designed to insure freedom from oscillation, and wiring rules to permit the use of low-cost board layout and interconnection techniques (Ref. 1 and 2). The 9538 has applications in memory expansion, register and peripheral selection, serial to parallel conversion in excess of 100 MHz and general high speed decoding functions.

DESCRIPTION

The logic diagram with pin locations for the 9538 decoder is shown in Figure 1. The 9538 accepts three binary address inputs and, under control of the enable lines, activates one of eight active-level LOW outputs. The A_0 terminal of the decoder is considered the least significant so that an input configuration such as $A_0 = 1$, $A_1 = 0$, $A_2 = 0$ would select Output 1 to be LOW. Both of the active-level LOW enable inputs must be low to enable the outputs. If either of the enable inputs is HIGH, all eight outputs remain HIGH. A truth table for the decoder is given in Figure 2.

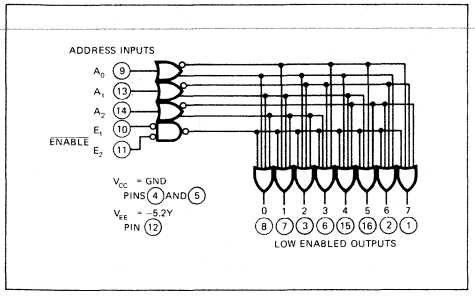


Fig. I. 9538 Logic Diagram

INPUTS					OUTPUTS							
A_0	A_1	A_2	E_1	E_2	0	1	2	3	4	5	6	7
L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	L	H	H	H	H	H	H
L	H	L	L	L	H	H	L	H	H	H	H	H
H	H	L	L	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	L	H	H	H	H	H	L	H	H
L	H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	L	H	H	H	H	H	H	H	L
X	X	X	H	L	H	H	H	H	H	H	H	H
X	X	X	L	H	H	H	H	H	H	H	H	H
X	X	X	H	H	H	H	H	H	H	H	H	H

Fig. 2. 9538 Truth Table

Three levels of series gating are used to implement the 9538 thus providing very high speed – typically 3.5 ns select to output delay, for medium power dissipation – typically 275 mW with a –5.2 volt power supply. All inputs and outputs are terminated in 2kohm resistors. These resistors provide pull-down currents required for extra inputs and outputs OR-tied to the line, insure a positive real Zin over all frequencies, and eliminate the need for external resistors for termination of short lines or on unused inputs. All device outputs are designed to permit driving a 50 ohm coaxial line and a fan-out of 10 unit loads simultaneously, when desired.

APPLICATIONS

The 9538 is an extremely versatile functional building block. The high speed and relatively simple wiring rules make it suitable for use in a wide range of low cost, high speed systems. General applications of MSI decoders are described in other Fairchild publications (Ref. 3 and 4). Some of the more significant uses in high performance systems are summarized on the following pages.

The 9500 family is recommended for use with V_{CC} = ground and $V_{EE} = -5.2$ volts. However, if suitable decoupling precautions are taken, these devices can be operated in a TTL

system with conventional positive supply rail in association with suitable interface circuits (Ref. 5).

DEMULTIPLEXING

The 9538 decoder may be used as a demultiplexer by connecting a data source to one of the enable inputs. The other enable input will function as a data enable line while inputs A_0, A_1 and A_2 determine which of the eight output lines the data is fed to. The data will not be inverted through the demultiplexer since both the input and outputs are active low.

In the example of Figure 3, with inputs and enable addressed as indicated, the data signal from the source will appear uninverted at output #2.

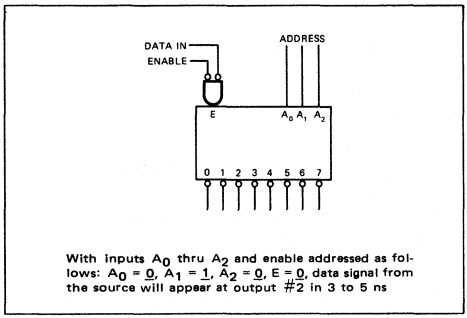


Fig. 3. 9538 as Demultiplexer

Many applications are possible using this principle. Figure 4 shows the decoder serving as a clock demultiplexer. The clock, under control of the address, switches to the appropriate register, counter or memory. For correct operation the clock signal need only be framed by the address inputs with the address set up prior to applying the clock. Up to ten 9500 ECL input loads can be driven by one decoder output.

Utilization of the demultiplexing capability of the 9538 in a serial-parallel conversion application is shown in Figure 5. This configuration also employs the 9581 MSI 8-input multiplexer and 9528 dual-D 150 MHz flip-flop for extremely high speed digital data transmission.

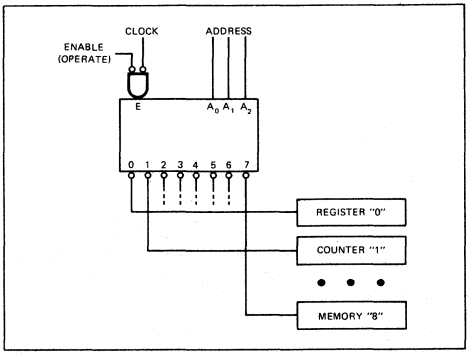


Fig. 4. Clock Demultiplexer

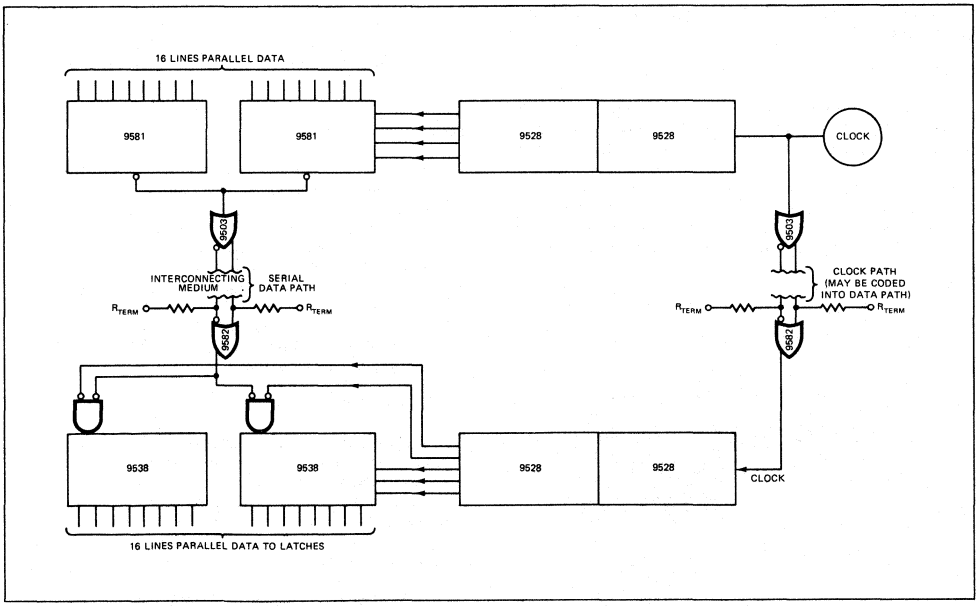
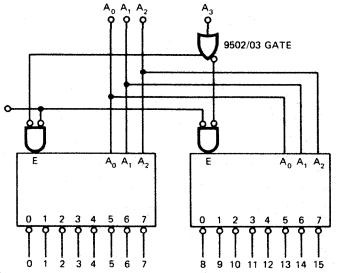


Fig. 5. Serial to Parallel — Parallel to Serial Conversion



	OUTPUT SELECTION				
	BCD CODE				
DECIMAL DIGIT	8421	5421	EXCESS 3	EXCESS 3 GRAY	2421
0	0	0	3	2	0
1	1	1	4	6	1
2	2	2	5	7	2
3	3	3	6	5	3
4	4	4	7	4	4
5	5	8	8	12	11
6	6	9	9	13	12
7	7	10	10	15	13
8	8	11	11	14	14
9	9	12	12	10	15

Fig. 6. Decode Any 4-bit Code

Here 16 channels of data are converted to serial form at a 5-MHz clock rate for transmission at an 80-megabit rate along a single line. The data is converted back to 16-channel parallel form (at the same rate) at the other end of the line. Advantages of temperature compensated ECL over conventional ECL in this application are that any drift in device threshold or output level can result in "glitches" in the decode circuitry. Since these may be interpreted as errors, either the speed or the number of channels must be reduced. With 9500 ECL these variables are eliminated or reduced so that maximum capability is preserved.

CODE DECODING

The enable inputs permit use of two 9538 decoders to decode any four-bit weighted or unweighted code by selecting the appropriate outputs in the required sequence. Figure 6 shows the connection diagram and decode table for this application. The other enable inputs allow enabling of the function. Complete decode operation is completed in 6 – 8 ns.

For decoding of 8421 code in only 3 to 5 ns Figure 7 indicates a lower cost approach using one 9503 Triple 2-input OR/NOR gate package in place of the second 9538 element. The disadvantage of this scheme is the lack of an enable control for the whole function.

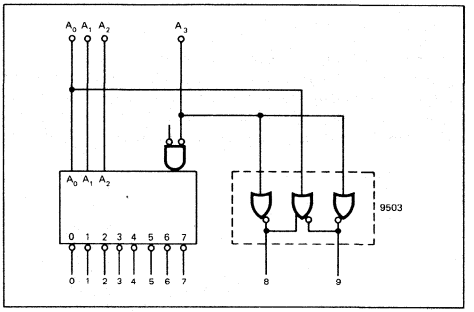


Fig. 7. Higher Speed Decode for 8421 Only

MEMORY DECODING

A major application for the 9538 is in address decoding of high speed memory systems.

The enable inputs allow the use of several 9538 decoders together to decode words of greater than four bits as illustrated in Figure 8. Here four packages are used to select 1 out of 32

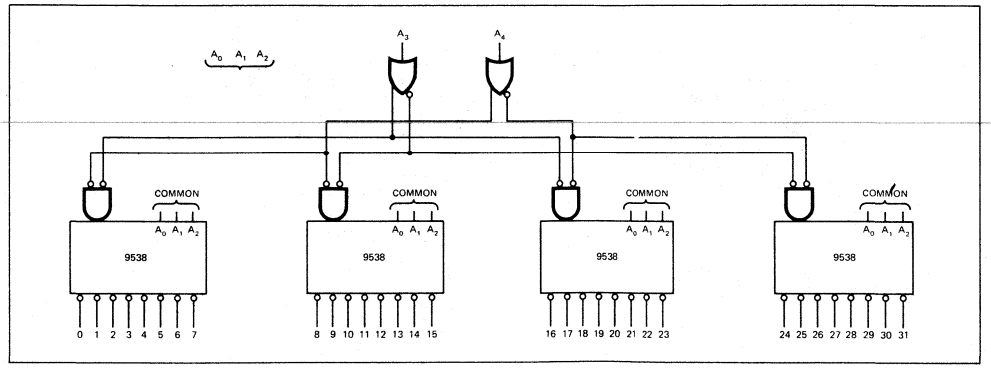


Fig. 8. 1-Out-of-32 Decoder

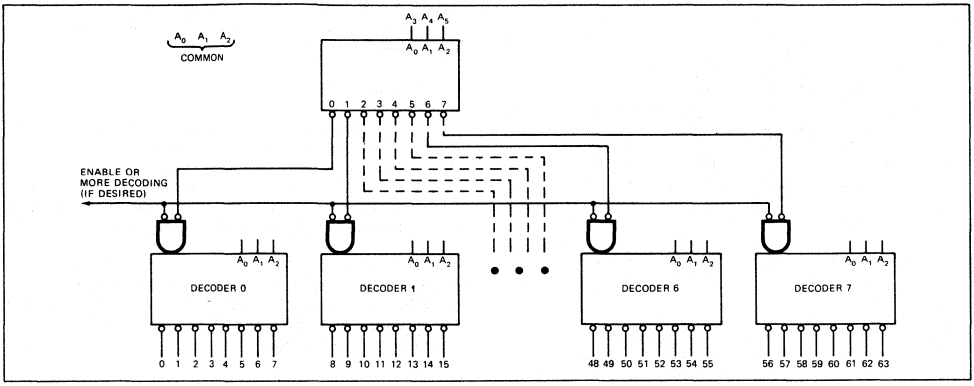


Fig. 9. 1-Out-of-64 Decoder

outputs in 6 – 8 ns from application of the address at inputs A_0 through A_4. This technique may be extended to a six-bit address by using the low output of the 9538 to select one decoder from a group of decoders. Figure 9 shows a 1-of-64 decoding scheme with select propagation delay of 7 to 10 ns. The remaining enable input may be used for overall control or wider decoding if desired.

The low propagation delay of the 9538 makes it particularly useful for high performance ECL semiconductor memory

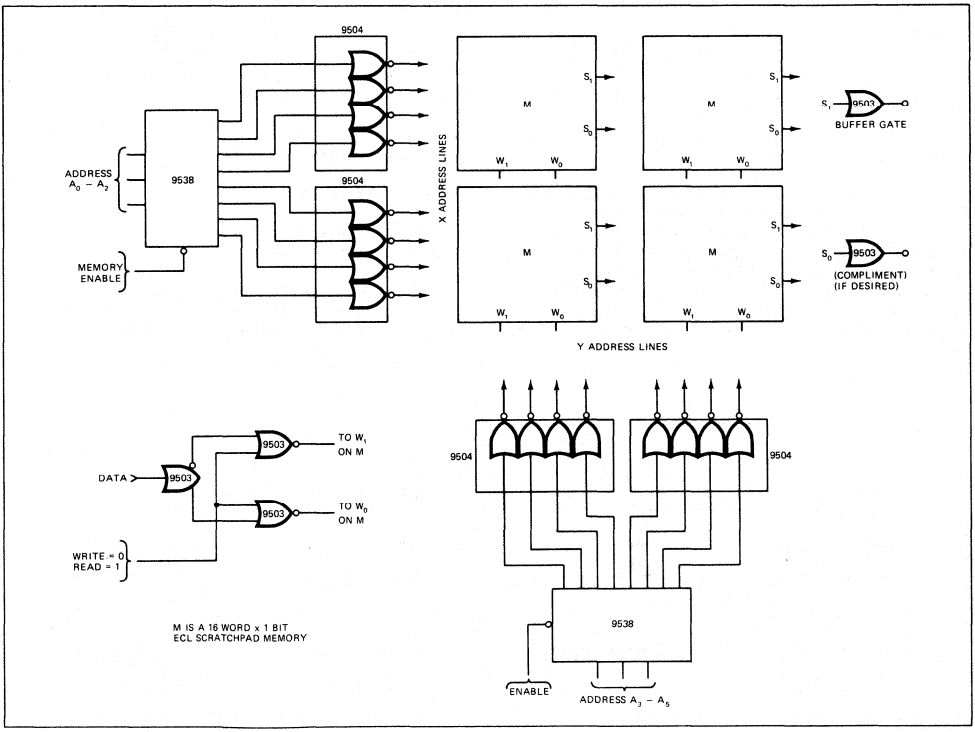


Fig. 10a. Decoding of 64 Word by 1-Bit Memory Array

configurations. Figure 10a shows the 9538 selecting a particular location in a 64-word by 1-bit memory plane constructed from four 16-word by 1-bit ECL scratchpad cells with a linear 4 x 4 x – y select. Each 9538 is connected to two 9504 Quad NOR (with common enable) gates serving as inverter and driver for the X and Y address lines of the memory elements. Wiring and sensing data is achieved with the 9503 Triple OR/NOR gates. Figure 10b shows a 64-word by 6-bit memory based on six of the stacks of Figure 8a. Using a 16-bit ECL scratchpad element with 5 – 6 ns access, the access time of the 64-word by 6-bit system would be typically 12 ns.

This same principle is extended to larger word sizes in Figure 11. Here each clock on the memory plane consists of one stack similar to Figure 10a. The capacity of this configuration is therefore 4K words by 1 bit, with a 20 ns typical access time. Each output of decoders addressed by A_0 through A_2 and A_6 through A_8 fans-out to eight 9504 gate inputs. No termination is required unless interconnecting lines exceed 8 inches. Decoders addressed by A_3 through A_5 and A_9 through A_{11} are connected to the common enable gate input on each

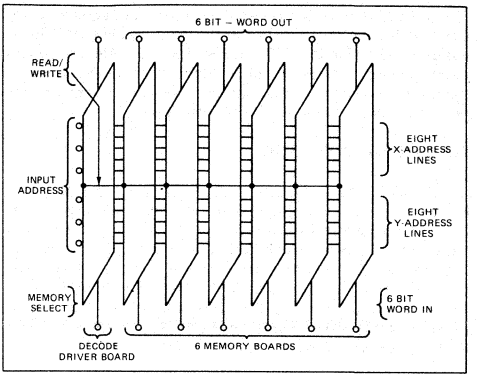


Fig. 10b. 64-Word by 6-Bit High Speed Scratchpad Using Basic Cell of Fig. 10a

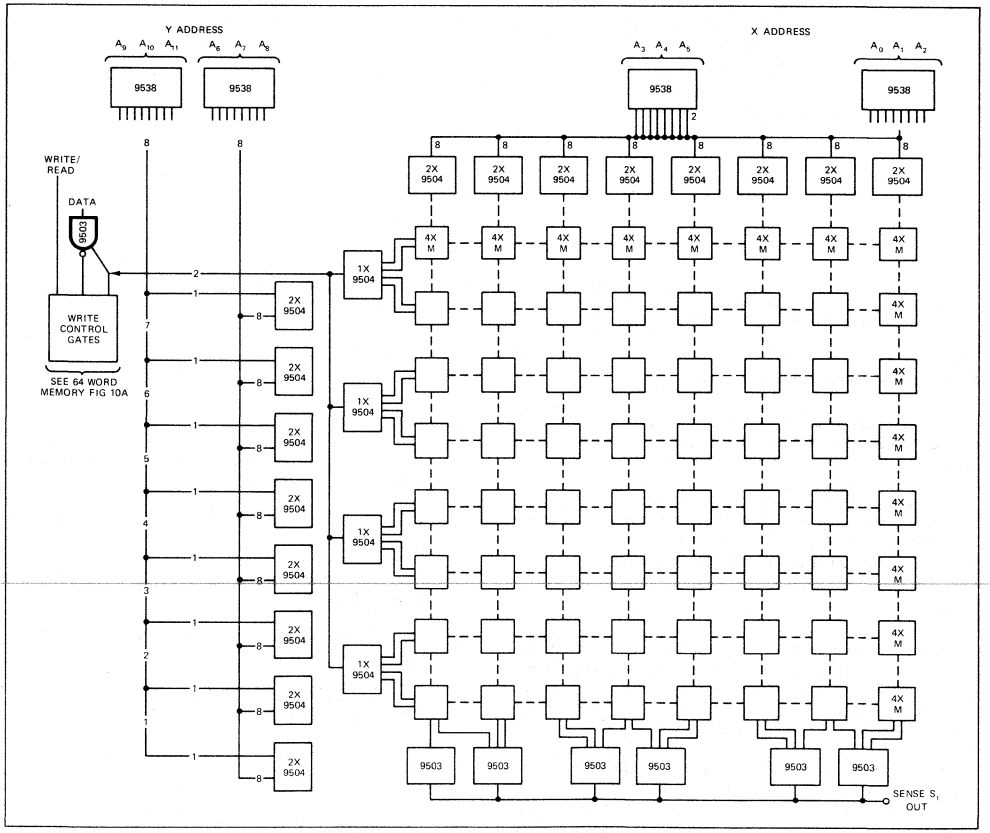
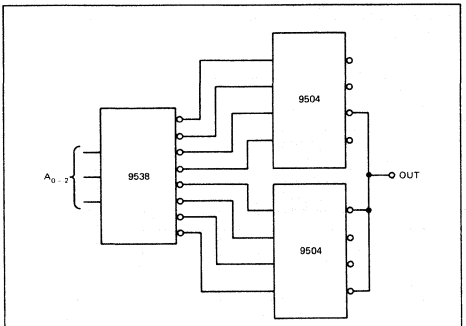


Fig. 11. 4K-Word X 1-Bit Memory

of two 9504 drivers. No external termination is required unless line length exceeds 12 inches in this case, as the enable input presents a heavier load. The 9504 driver outputs fan out to sixteen memory address inputs. 9504 gates are employed on the Read/Write control columns and for sensing sixteen memory outputs are tied to each 9503 gate input.

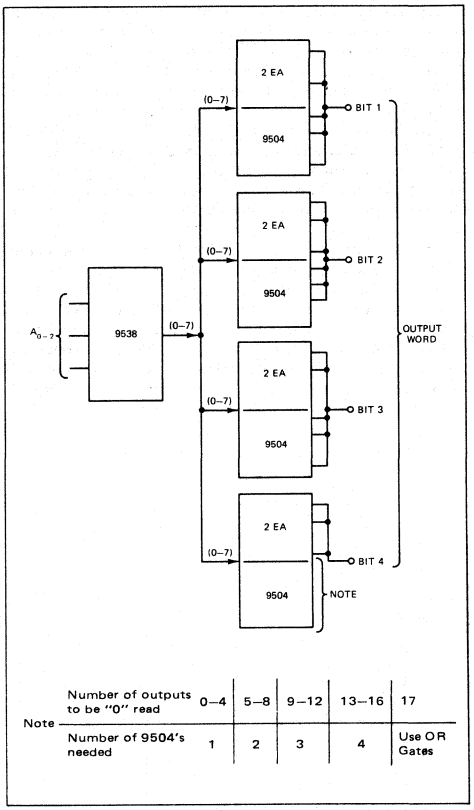
FUNCTION GENERATOR

The 9538 may also be used to construct a Read Only Memory or Function (minterm) Generator. By driving two 9504 Quad inverters from each output bit a simple 8-word x 1-bit function generator is achieved, Figure 12. This can be used for any control or display function where very high speed is required. Typical propagation delay of a ROM/Function Generator of 8 words by "N" bits will be less than 8 ns. A method of expanding the 8-bit ROM (Figure 12) to a 32-bit ROM (8 words x 4 bits) is shown in Figure 13.



"Wire OR" outputs addressed when "1" is desired. Example shown yields a logic "1" for address inputs of 010, 100, and 111 (A_2, A_1, A_0). Other addresses will yield a logic "0".

Fig. 12. 8 X 1 ROM/Function Generator



Note

Number of outputs to be "0" read	0–4	5–8	9–12	13–16	17
Number of 9504's needed	1	2	3	4	Use OR Gates

Fig. 13.

By use of the expansion schemes shown in Figures 8 and 9 a 32 or 64-word ROM is obtained with read times of only 3 ns more than the decode time.

The 9581 multiplexer may also be used for this function. The difference being that an 8 x "N" ROM would use either "N" 9581's or 1 9538 and "N" 9504's. The latter is the most economical, while the former uses fewer packages.

SUMMARY

This Application Brief has described the operation and major features of the 9538 1-out-of-8 ECL/MSI decoder. The device is particularly useful for memory address selection and provides functional building block capability for the 9500 Temperature Compensated ECL family.

The availability of ECL/MSI functions significantly reduces the cost of high performance systems implementation as it concentrates many operations on chip, thus eliminating many interconnections with associated delays and termination requirements.

REFERENCES

1. Fairchild Applications Brief #App. 157 – "9500 System Applications and Wiring Rules"
2. Fairchild Technical Paper #TP59 – "Temperature Compensated ECL"
3. Fairchild Application Bulletin #App 160 – "Applications of 9301 Decoder"
4. Fairchild Application Note #App 170 – "Applications of the 9311 Decoder"
5. Fairchild Applications Brief #App 179 – "Discrete ECL/TTL Interface Circuits"

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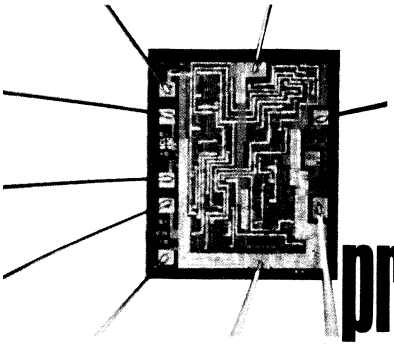
programmable divider performs at 140 MHz

Courtesy of Fairchild Semiconductor



programmable divider

Frequency synthesizers employed as local oscillators in TV, AM-FM and communication receivers will increase as long as new techniques continue to make them economically advantageous and crowding of the available spectrum requires their use.

Digital frequency synthesizers have become popular in applications that require generation of a large number (20 or more) of precise crystal-controlled frequencies. An integral part of such a synthesizer is the programmable divider and the most widely used logic family for high speed operation is nonsaturating emitter coupled logic (ECL). The technique to be discussed allows high-speed ECL to interface with TTL for the optimum speed/cost system performance.

To reduce system cost, a technique called "pulse swallowing" permits the designer to replace part of the ECL elements with TTL without sacrificing system speed (*Pulse Swallowing—A Logic Technique for High Speed Programmable Counters*, **EDN** Oct. 1, 1970). Further cost reduction can be realized by extensive use of MSI/TTL elements to obtain maximum logic function/package density. Pulse-swallowing also offers the capability of higher operating frequencies simply by introducing higher-speed and modulo prescalers.

Miscounting is also a problem frequently encountered when using any high-speed logic family at frequency extremes. Erroneous counting can be traced to a combination of problems. First, line reflections arise from improper terminations; and second; low-level dc noise immunity in past ECLs degraded with increasing temperature. To reduce these problems, temperature-compensated devices, such as the 9500 ECL family of Fairchild, are used and internal pull-down resistors reduce line reflections in runs up to 8 inches long.

Pulse Swallowing Briefly, pulse swallowing employs a variable modulo prescaler, typically 10/11, which is

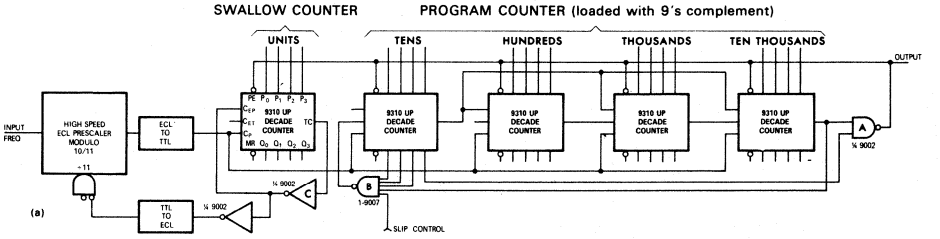


Fig. 1—**Two programmable dividers** provide division ratios in increments of one with minimum divide ratio of 90. Circuit (**a**) accepts up to 90 MHz input signals and (**b**) 140 MHz. Nine's complement applied to counter inputs determines the modulo for each counter.

In (**a**), gate A controls synchronous loading by detecting when the program divide counter is one count prior to terminal count (9 . . . 998). In (**b**), flip-flops **D** and **E** control the synchronous loading. Flip-flop **D** is set when the program counter is two clock pulses prior to terminal count. Thus, synchronous loading occurs on the next clock pulse. Also this pulse loads the program counter and sets flip-flop **E**. On the next clock pulse the swallow counter is loaded. The program counter is reloaded and flip-flops **E** and **D** are reset to zero. Loading and reloading of the program counter on two consecutive clock pulses allows the terminal count, if any, to stabilize before counting.

In circuit (**a**), the swallow counter makes the prescaler

performs at 140 MHz

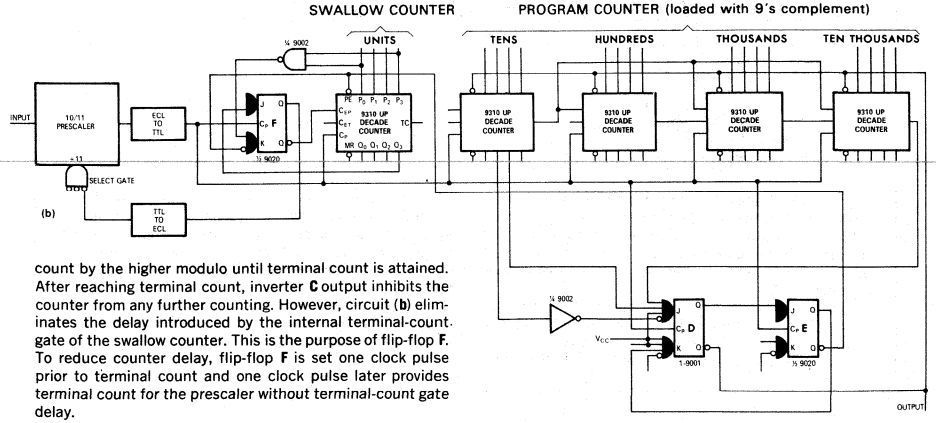
called a "swallow" counter, and a program counter. The divide ratio is developed by allowing the prescaler to divide by 11 at the beginning of each divide cycle until the swallow counter reaches its final value. This yields the units value of the divide ratio. Then the swallow counter directs the prescaler to divide by 10 for the remainder of the divide ratio. While the prescaler is dividing by 11, the extra pulse does not affect the program counter—in effect, the pulses are swallowed. Therefore, the counter controlling the prescaler is referred to as the swallow counter.

Both the swallow and program counters are loaded with values representing their respective part of the desired divide ratio, allowing them to count up to their maximum value at which time the initial values are reentered. This technique has the advantage of allowing only the prescaler to operate at the input frequency with no loss in resolution. The only disadvantage is that there is a minimum divide ratio—unimportant in most applications.

Programmable Divider Operation A programmable divider is essentially a counter that goes through only a part of its maximum number of possible states. A common method for selecting the number of states is to preset a specific value into the counter and allow it to count to its terminal state. Then the value is reentered and a new cycle begins. One state produces an output that occurs once every **N** input pulses—thus the input is divided by **N**. The preset value determines the desired divide ratio.

Two programmable dividers are illustrated in **Fig. 1**. The divider in **Fig. 1a** accepts signals up to 80 MHz and provides programmable division ratios in increments of one, with a minimum divide ratio of 90. The divider in **Fig. 1b** accepts up to 140 MHz signals and has the same minimum divide ratio. Of course, the maximum range of the divider depends on the counter length or the number of stages.

These dividers differ in the operating performance of the swallow counter and program counter because of



count by the higher modulo until terminal count is attained. After reaching terminal count, inverter **C** output inhibits the counter from any further counting. However, circuit (**b**) eliminates the delay introduced by the internal terminal-count gate of the swallow counter. This is the purpose of flip-flop **F**. To reduce counter delay, flip-flop **F** is set one clock pulse prior to terminal count and one clock pulse later provides terminal count for the prescaler without terminal-count gate delay.

the logic scheme used.

Basis for selecting the prescaler modulo is the lowest number that will yield reliable counting speeds within the range of the TTL programmable dividers. For high-input frequencies, there are methods available that extend the prescaler modulo to 20/21 or 40/41. A 20/21 prescaler will produce a 160 MHz programmable divider which will have the same general characteristics except the minimum divide ratio increases to 380.

Provision must be made for synchronous loading with the desired value that each counting cycle must attain. In **Fig. 1a**, this is accomplished by detecting when the program divide counter is one count prior to the terminal count and loading during the time period that normally represents the final count. A single NAND gate performs this function. In **Fig. 1b**, a two-stage shift counter controls the synchronous loading. This counter increases the operational speed two ways. First, the propagation delay of the two-input NAND gate is eliminated. Secondly, time is allowed for the terminal count signals to ripple through the stage when certain worst case numbers are loaded in parallel. When counting, the look-ahead circuitry prevents any restriction on speed.

Another parameter that limits the system's operating speed (besides the program divider operating speed) is the swallow-counter propagation delay. The swallow counter is clocked and its outputs must be stabilized so that the prescaler will divide by the correct modulo. Therefore, the counter and interface delays must be minimized. The techniques required to obtain a prescaler whose modulo can be changed from 10 to 11 and vice versa at the last moment will be discussed later.

The swallow counter in **Fig. 1b** commands the prescaler to count by the higher modulo until terminal count is reached. Then, the select line goes high, and the prescaler divides by ten, remaining in this condition until the parallel enable line is activated—beginning the divide cycle.

The internal terminal count gate of the swallow counter introduces a delay which is eliminated by the circuit in **Fig. 1b**. In this divider, the swallow counter performs the same function. However, the delay through the counter is reduced by the addition of a flip-flop. This flip-flop is set one clock pulse prior to terminal count, and one clock pulse later, it provides the terminal count for the prescaler without the terminal-count gate delay.

In some systems, such as frequency synthesizers, it is desirable to synchronize the beginning of each counting sequence of the programmable counter with some reference source. This is shown in **Fig. 1a** and easily incorporated in **Fig. 2b**. This "holding up" of the counter until the correct starting point is called "slip". For this function, an eight-input NAND gate detects when the program counter is two counts prior to the terminal

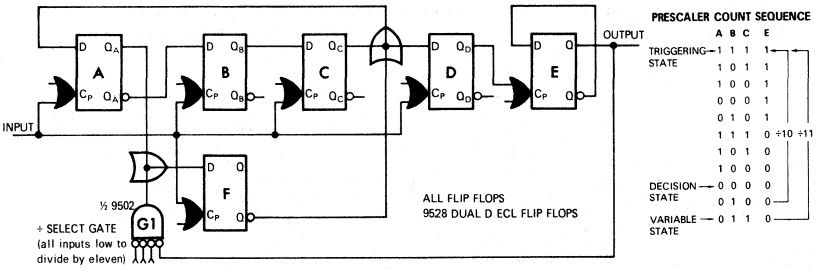


Fig. 2—**10/11 prescaler circuit** operates in excess of 160 MHz. Flip-flop **F** determines the 5/6 shift counter (flip-flops A, B and C) modulo. When input of **F** is not forced high, the counter divides by five and if forced high, a division by six takes place. Gate **G1** controls **F** through the OR tie.

Output Q_A clocks **E** which is connected in a toggle mode. This stage divides the counter output by two and simultaneously controls the counter modulo.

The prescaler can only divide by 10 or 11. When output of **E** is high, the gate conditions cannot be satisfied and the shift counter divides by 5 only. After five states, **E** is clocked again and its output goes low. Then the shift counter's modulo is controlled by the counter through the select gate. Since the TTL counters are clocked on a rising edge and since the output of **D** is high for five clock pulses, the counter has at least this number of states in which to respond. With this prescaler, the decision time allowed is 9 times the input period.

count and slips (holds) the counter until the synchronizing signal is present.

High-Speed 10/11 Prescaler The 10/11 prescaler, illustrated in **Fig. 2**, operates in excess of 160 MHz. In the prescaler design, decision time is the most critical parameter. This is the amount of time the TTL counter has available to respond to the prescaler output and to make a decision whether the prescaler should divide by the upper or the lower modulo. The prescaler must be designed so that its modulo can be changed at the last moment relative to the triggering edge of its output, thus providing maximum time for the propagation delays within the swallow counter.

Basically, the prescaler in **Fig. 2** consists of a three-stage synchronous shift counter, switchable between modulo 5 and 6, and a toggle flip-flop that divides the shift counter's output by two and simultaneously controls the shift counter's modulo to obtain the 10/11 divide modulo.

The 5/6 shift counter configuration was selected because changing from one divide ratio to the other is simple. More importantly, the count sequence for the modulo 6 configuration is identical to the modulo 5 sequence except for one state. This means that the shift counter modulo actually is determined only a short time before this state and at no other time. Correspondingly, the inputs to the select gate do not have to be in their final stabilized condition until this time. This important feature allows the swallow and program counter to operate much slower than the prescaler. The 5/6 shift counter output is derived essentially from the first stage output Q_A (flip-flop D is in parallel with flip-flop A), because this output makes the first transition after the variable state. This edge is used to trigger the following devices and allow them to respond before the next chance to change the shift counter modulo. This 5/6 configuration is also desirable because it requires no output decoding in either version, and no gates are required between the flip-flops to slow down operating speeds.

Addition of another flip-flop to the configuration of **Fig. 2a** forms a 20/21 prescaler (Fig. 3). With outputs of the two toggle flip-flops (E and G) in the 20/21 prescaler applied to the select gate, both must be in the zero state before the shift counter can divide by six. Therefore, the TTL counter is triggered by a rising edge and the shift counter divides by 5 three times until the outputs of both flip-flops are zero, then it divides by six if enabled by the swallow counter – modulo 20 or 21. Since the TTL counter is triggered at the beginning of the cycle, the TTL counter outputs should be valid by the time the shift counter can divide by six. With this additional flip-flop, the decision time allowed the TTL counter is more than doubled over the 10/11 configuration. The toggle flip-flop used to make the

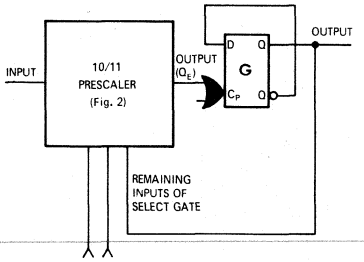


Fig. 3 – **A 20/21 prescaler** is formed by the addition of another flip-flop to Fig. 2. Outputs of both toggle flip-flops (D and E), applied to the select gate, must be in the zero state before the shift counter divides by six. Therefore, a rising edge of the shift counter triggers the flip-flops and the counter divides by 5 three times until both flip-flop outputs are zero, then it divides by six if enabled by the swallow counter.

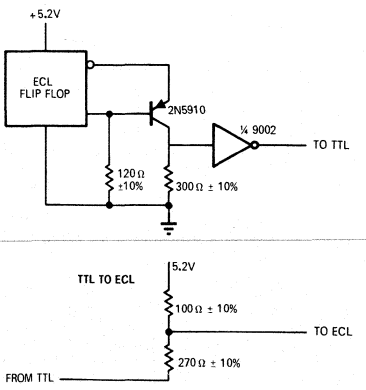


Fig. 4 – **Interfacing circuits** convert TTL-to-ECL or ECL-to-TTL circuits operating on a 5.2V dc supply.

20/21 prescaler may be TTL. However, the delay through the flip-flop and interface must be considered at the maximum operating frequency.

Interfacing Interface circuits provide the proper voltage level between the ECL and TTL devices. The delay through the interface must be minimum to increase the decision time allowed the MSI/TTL counter. Two circuits used for TTL/ECL interfacing are illustrated in **Fig. 3**.

The rising edge of the signal applied to the TTL counter must correspond to the rising edge of the 5/6 shift counter output to maintain the decision time required by the TTL swallow counter. Therefore, if an inverting interface is used, the output must be taken from the complement output of the last stage. For noninverting interface, the output must be taken from the nontrue output.

Physical Layout The prescaler construction is relatively straightforward. A ground plane construction was employed with voltage supply lines well decoupled throughout the boards using small ceramic capacitors. A capacitor was inserted between the ground plane and supply terminal of each package. In addition, one large tantalum capacitor was used on the board. The physical board layout was compact and none of the printed circuit traces was longer than eight inches. Consequently, with the exception of the clock line, no terminating resistors were required.

In this layout, the clock line required terminations for 160 MHz operation. However, this might not be required on a board laid out differently. At lower frequencies, clock terminations were not required. The clock was obtained from an ECL gate to insure good rise and fall times (a discrete block buffer also can be used).

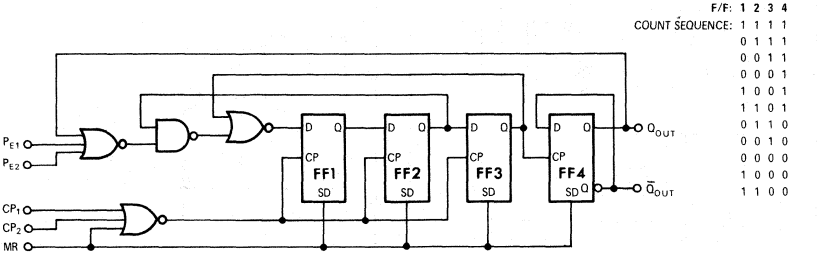


Fig. 5—**A monolithic 250 MHz prescaler** is currently in development at Fairchild Semiconductor. Designated the 9590, this MSI device (16-pin DIP) is built with high-speed ECL technology. Applications for this device include counters, frequency synthesizers and many other communications and instrumentation applications. In its simplest use, the 9590 will divide any clock frequency by 10 up to 250 MHz. With other control logic to form a divide by 10/11 configuration, a divide-by-"N" counter is possible with a maximum frequency of more than 250 MHz.

In the block diagram, **flip-flops 1, 2** and **3** are connected as a cross-coupled ring shift or Johnson counter. Flip-flop **4** is driven by flip-flop **3** and runs asynchronously. It toggles whenever Q3 makes a positive transition (0 to 1).

If both inputs **PE1** and **2** are floating, the counter will not skip the 111 state, and the prescaler will divide by 11. If one or both enable inputs are high, the Johnson counter goes directly from 110 to 011 state, thus skipping 111—division ratio is 10.

FAIRCHILD SEMICONDUCTOR

TTL
SSI & MSI

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FAIRCHILD SEMICONDUCTOR
TTL INTEGRATED CIRCUIT GUIDE

Where full data is included page numbers are given.
* indicates devices shown in product summary pp 152–157. Information on other devices available from your Fairchild Sales Office.

NUMERICAL INDEX OF DEVICES

	STANDARD		
	t_{pd} = 10 ns P_d = 10 mW per Gate		t_{pd} = 8 ns P_d = 10 mW per Gate
	0°C to + 75°C	−55° to +125°C	0°C to +75°C and −55° to +125°C
NAND Gates			
Quad 2-Input Positive NAND Gate	9N00/7400	9N00/5400	9002
Quad 2-Input Positive NAND Gate	9N01/7401	9N01/5401	
with Open-Collector Output	9N03/7403	9N03/5403	9012
Triple 3-Input Positive NAND Gate	9N10/7410	9N10/5410	9003
Dual 4-Input NAND Schmitt Trigger	9N13/7413*	9N13/5413*	
Dual 4-Input Positive NAND Gate	9N20/7420	9N20/5420	9004
Quad 2-Input High Voltage NAND Gate	9N26/7426	9N26/5426	
8-Input Positive NAND Gate	9N30/7430	9N30/5430	9007
NOR Gates			
Quad 2-Input Positive NOR Gate	9N02/7402	9N02/5402	
Quad 2-2-2-4-Input Positive NOR Gate			9015
Dual 4-Input Positive NOR with Strobe	9N23/7423*	9N23/5423*	
Dual 4-Input Positive NOR with Strobe	9N25/7425*	9N25/5425*	
Triple 3-Input NOR Gate	9N27/7427*	9N27/5427*	
AND Gates			
Quad 2-Input Positive AND Gate	9N08/7408	9N08/5408	
Quad 2-Input Positive AND (O.C.) Gate	9N09/7409	9N09/5409	
Triple 3-Input Positive AND Gate	9N11/7411	9N11/5411	
Triple 3-Input Positive AND (O.C.) Gate	9N12/7412*	9N12/5412*	
High Speed AND Gate			
Exclusive-OR/OR Gates			
Quad Exclusive-OR Gate	9N86/7486	9N86/5486	
Quad Exclusive-OR Gate with Inverted Outputs			9014
Quad 2-Input Positive OR Gate	9N32/7432*	9N32/5432*	
AND-OR-INVERT Gates and Expanders			
Expandable Dual 2-Wide 2-Input AND-OR-INVERT Gate	9N50/7450	9N50/5450	9005
Dual 2-Wide 2-Input AND-OR-INVERT Gate	9N51/7451	9N51/5451	
High Speed Expandable 2-2-2-3-Input AND-OR Gate			
Expandable 4-Wide 2-Input AND-OR-INVERT Gate	9N53/7453	9N53/5453	
4-Wide 3-2-2-3-Input AND-OR-INVERT Gate	9N54/7454	9N54/5454	
Expandable 4-Wide 2-Input AND-OR-INVERT Gate			
Expandable 4-Wide 2-2-2-3-Input AND-OR-INVERT Gate			9008
Dual 4-Input Expander	9N60/7460	9N60/5460	9006
High Speed Triple 3-Input Expander			
High Speed 4-Wide 3-2-2-3-Input AND-OR Expander			
4-2-3-2-Input AND-OR-INVERT Gate			
4-2-3-2-Input AND-OR-INVERT (O.C.) Gate			

LOW POWER	HIGH SPEED		SUPER HIGH SPEED	
t_{pd} = 20 ns P_d = 2 mW per Gate	t_{pd} = 6 ns P_d = 22 mW per Gate		t_{pd} = 3 ns P_d = 20 mW per Gate	
0°C to +75°C and −55° to +125°C	0°C to +75°C	−55° to +125°C	0° to +75°C	−55° to +125°C
9L00	9H00/74H00 9H01/74H01 9H10/74H10 9H20,22/74H20,22 9H30/74H30	9H00/54H00 9H01/54H01 9H10/54H10 9H20,22/54H20,22 9H30/54H30	9S00/74S00 9S03/74S03 9S20,22/74S20,22	9S00/54S00 9S03/54S03 9S20,22/54S20,22
	9H08/74H08 9H11/74H11 9H21/74H21*	9H08/54H08 9H11/54H11		
9L86				
9L54	9H50/74H50 9H51/74H51 9H52/74H52* 9H53/74H53* 9H54/74H54* 9H55/74H55* 9H60/74H60 9H61/74H61 9H62/74H62	9H50/54H50 9H51/54H51 9H52/54H52* 9H53/54H53* 9H54/54H54* 9H55/54H55* 9H60/54H60 9H61/54H61 9H62/54H62	9S64/74S64* 9S65/74S65*	9S64/54S64* 9S65/54S65*

TTL/SSI GATES FLIP-FLOPS (DATA NOT INCLUDED)

	STANDARD		
	t_{pd} = 10 ns P_d = 10 mW per Gate		t_{pd} = 8 ns P_d = 10 mW per Gate
	0° to +75°C	−55° to +125°C	0°C to +75°C and −55° to +125°C
Inverters and Buffers			
Hex Inverter	9N04/7404	9N04/5404	9016
Hex Inverter with Open-Collector Output	9N05/7405	9N05/5405	9017
Hex Inverter Buffer/Driver (O.C.)	9N06/7406*	9N06/5406*	
Hex Buffer/Driver (O.C.)	9N07/7407*	9N07/5407*	
Hex Inverter Buffer/Driver (O.C.)	9N16/7416*	9N16/5416*	
Hex Buffer/Driver (O.C.)	9N17/7417*	9N17/5417*	
Quad 2-Input NAND Buffer	9N37/7437*	9N37/5437*	
Quad 2-Input NAND Buffer (O.C.)	9N38/7438*	9N38/5438*	
Dual 4-Input Positive NAND Buffer	9N40/7440	9N40/5440	9009
Dual 4-Input Positive NAND Driver			
Flip-Flops			
J-K Flip-Flop	9N70/7470	9N70/5470	
	9N105/74105	9N105/54105	9001
J-K Master Slave Flip-Flop	9N72/7472	9N72/5472	
	9N104/74104	9N104/54104	9000
Other J-K Flip-Flops			
Dual J-K Flip-Flop			9020
			9022
			9024
Dual J-K Master Slave Flip-Flop	9N73/7473	9N73/5473	
	9N107/74107	9N107/54107	
Dual J-K Master Slave Flip-Flop with Preset and Clear	9N76/7476	9N76/5476	
Dual D-Type Edge-Triggered Flip-Flop	9N74/7474	9N74/5474	
Other Dual J-K Edge Triggered Flip-Flops			

* To be announced

LOW POWER	HIGH SPEED		SUPER HIGH SPEED	
t_{pd} = 20 ns P_d = 2 mW per Gate	t_{pd} = 6 ns P_d = 22 mW per Gate		t_{pd} = 3 ns P_d = 20 mW per Gate	
0°C to +75°C and −55° to +125°C	0° to +75°C	−55° to +125°C	0° to +75°C	−55° to +125
9L04	9H04/74H04 9H05/74H05	9H04/54H04 9H05/54H05	9S04/74S04 9S05/74S05	9S04/54S04 9S05/54S05
	9H40/74H40	9H40/54H40	9S40/74S40 9S140/74S140	9S40/54S40 9S140/54S140
9L24	9H71/74H71 9H72/74H72 9H101/74H101 9H102/74H102 9H73/74H73 9H78/74H78 ~~9H76/74H76~~	9H71/54H71 9H72/54H72 9H101/54H101 9H102/54H102 9H73/54H73 9H78/54H78 ~~9H76/54H76~~	9S109*	9S109*
	9H106/74H106 9H74/74H74 9H108/74H108* 9H103/74H103*	9H106/54H106 9H74/54H74 9H108/54H108* 9H103/54H103*	9S74/74S74* 9S112/74S112* 9S113/74S113* 9S114/74S114*	9S74/54S74* 9S112/54S112* 9S113/54S113* 9S114/54S114*

	9300/7400 Series Standard	93L Series Low Power	93H Series High Speed
Registers			
4-Bit Shift Register	9300	93L00	93H00
8-Bit Parallel to Serial Converter	93165/74165*		
8-Bit Serial to Parallel Converter	93164/74164*		
Dual 8-Bit Shift Register	9328	93L28	
8-Bit Multiple Port Register	9338/7494		
8-Bit Shift Register	9391/7491		
4-Bit Shift Register	9394		
4-Bit Shift Register	9394/7494		
4-Bit Right/Left Shift Register	9395/7495		
5-Bit Shift Register	9396/7496		
8-Bit Shift Register	93198/74198		
4-Bit Shift Register with Clock Enable			93H72*
Encoders			
8-Input Priority Encoder	9318	93L18	
Operators			
Dual Full Adder	9304		
5-Bit Comparator	9324	93L24	
4-Bit Arithmetic Logic Units	9340	93L40	
4-Bit Arithmetic Logic Units	9341/74181		
Carry Lookahead	9342/74182		
2-Bit × 4-Bit Full Multiplier	9344*		
12 Input Parity Checker/Generator	9348		
8-Bit Parity Generator/Checker	93180/74180*		
Full Adder	9380/7480		
2-Bit Full Adder	9382/7482		
4-Bit Full Adder	9383/7483		
Decoders/Demultiplexers			
One of Ten Decoder	9301	93L01	
Seven Segment Decoder	9307		
One of Sixteen Decoder	9311 (54154)	93L11	
One of Ten Decoder/Driver	9315/7441		
Seven Segment Decoder/Driver	9317		
Dual One of Four Decoder	9321	93L21	
BCD to Decimal Decoder/Driver	9325/74141*		
Seven Segment Decoder/Driver	9327		
One of Ten Decoder/Driver	9345/7445*		
One of Ten Decoder/Driver	93145/74145*		
Seven Segment Decoder/Driver	9337		
BCD to Decimal Decoder	9352/7442		
Excess −3 to Decimal Decoder	9353/7443		
Excess −3 Gray to Decimal Decoder	9354/7444		
BCD to Seven Segment Decoder/Driver	9357A/7446		
BCD to Seven Segment Decoder/Driver	9357B/7447		
BCD to Seven Segment Decoder	9358/7448		
BCD to Seven Segment Decoder	9359/7449*		

* To be announced

TTL/MSI

	9300/7400 Series Standard	93L Series Low Power
Multiplexers		
Dual 4 Input Multiplexer	9309	93L09
8 Input Multiplexer	9312	93L12
3 Input Digital Multiplexer /Open Collector	9313	
Quad 2 Input Multiplexer	9322	93L22
16 Input Multiplexer	93150/74150*	
8 Input Multiplexer	93151/74151*	
8 Input Multiplexer	93152/74152*	
Dual 4 Input Multiplexer	93153/74153*	
Latches		
Dual 4 Bit Latch	9308	93L08
4 Bit Latch	9314	93L14
8 Bit Addressable Latch	9334	
4 Bit Latch	9375/7475	
4 Bit Latch	9377/5477	

* To be announced

	9300/7400 Series Standard	93L Series Low Power
Counters		
Variable Modulo Counter	9305	
Up/Down BCD Counter	9306	
Decade Counter	9310	93L10
4 Bit Binary Counter	9316	93L16
Up/Down Decade Counter	93190/74190*	
Up/Down Binary Counter	93191/74191*	
Decade Counter	9350	
Binary Counter	9356	
Up/Down Decade Counter (Dual Clock)	9360/74192	
Up/Down Binary Counter (Dual Clock)	9366/74193	
Decade Counter	9390/7490	
Divide By Twelve Counter	9392/7492	
Binary Counter	9393/7493	
Code Converter		
BCD to Binary Converter	93184/74184*	

TTL/INTERFACE

Pulse Shapers

9600	Retriggerable, Resettable Monostable Multivibrator (One-Shot)
9601	Retriggerable Monostable Multivibrator (One-Shot)
9602	Dual Retriggerable, Resettable Multivibrator (One-Shot)

TTL/MEMORY

Random Access Read/Write Memories (RAM)

93433	16 Bit	16 Word × 1 Bit	Coincident Select	18 ns
93407	16 Bit	16 Word × 1 Bit	Coincident Select	18 ns
93435	64 Bit	16 Word × 4 Bit	Linear Select	22 ns
93403	64 Bit	16 Word × 4 Bit	Full Decode	40 ns
93400	256 Bit	256 Word × 1 Bit	3 of 6 Decode	70 ns
93410	256 Bit	256 Word × 1 Bit	Full Decode	40 ns
93415*	1024 Bit	1024 Word × 1 Bit	Full Decode	80 ns
93401	Decoder/Driver (For use with 93400)			20 ns

Read Only Memories (ROM)

93412*	256 Bit	32 Word × 8 Bit	Field Programmable	30 ns
93434	256 Bit	32 Word × 8 Bit	Mask Programmable	30 ns
93406	1024 Bit	256 Word × 4 Bit	Mask Programmable	50 ns

Associative/Content Addressable Memories (CAM)
Programmable Decoders

93402	16 Bit	4 Word × 4 Bit	Linear Select	25 ns

* To be announced

9300

MSI 4-BIT SHIFT REGISTER

A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

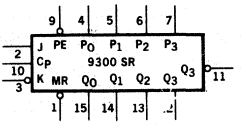
GENERAL DESCRIPTION — The 9300 Four Bit Shift Register is a high speed multi-functional sequential logic block which is useful in a wide variety of register and counter applications. As a register it may be used in serial-serial, shift left, shift right, serial-parallel, parallel-serial, and parallel-parallel data transfers. The circuit uses TTμL for high speed and high fanout capability, and is compatible with all devices in the CCSL group of digital integrated circuits.

- **15 MHz shift frequency**
- **Synchronous parallel entry**
- **J, $\overline{K}$ inputs to first stage**
- **Asynchronous common reset**
- **Typical power dissipation of 300 mW**
- **The input/output characteristics provide easy interfacing with Fairchild DTμL, LPDTμL, and TTμL families (CCSL).**
- **All ceramic "HERMETIC" 16 pin Dual In-Line package.**
- **Input diode clamping**

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7 V
Voltage Applied to Outputs for high output state	−0.5 V to +V_{CC} value
Input Voltage (D.C.)	−0.5 V to +5.5 V

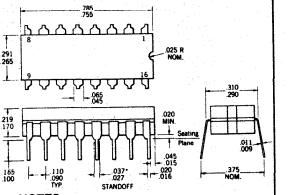
LOGIC SYMBOL



J_{CC} = PIN 16
GND = PIN 8

Fig. 3

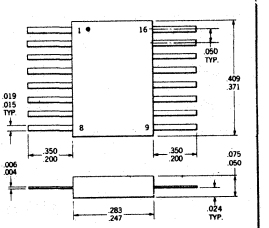
DUAL IN-LINE PACKAGE
16 Lead Dual In-Line



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" center
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for a conventional .020 inch diameter Lead
Package weight is 2.0 grams
Leads are tin-plated Kovar
*The .037 dimension does not apply .027 to the corner leads

Fig. 1

FLAT PAK
16 Lead BeO Cerpak



NOTES:
All dimensions in inches
Leads are gold-plated Kovar
Package weight is 0.4 gram

Fig. 2

ORDER INFORMATION

Specify U6B9300XXX for 16 pin Dual In-Line package or U4L for 16 pin Flat Package where XXX is 51X for the −55°C to +125°C temperature range, or 59X for the 0°C to +75°C temperature range.

FAIRCHILD
SEMICONDUCTOR

FUNCTIONAL DESCRIPTION

The logic symbol of Figure 2 provides an indication of the functional characteristics of the 9300 four bit shift register. Several special logical features of the 9300 design which provide a high degree of general usefulness are described below:

1. A $J\overline{K}$ input is provided to the first flip flop in the register. This type of input is the same as the more common JK input except that the low voltage level activates the $\overline{K}$ input. This provides the greater power of the JK type input for more general applications and at the same time the simple D type input that is most appropriate for a shift register can be easily obtained by simply tying the two inputs together.
2. There is no restriction on the activity of the J or $\overline{K}$ inputs for logical operation — except for the set up and release time requirements.
3. Parallel inputs for all four stages are provided. These will determine the next condition of the shift register synchronous with the clock input, whenever the Parallel Enable input is low. With the Parallel Enable input low the element appears as four common clocked D flip flops. When the Parallel Enable is high, or not connected, the shift register performs a one bit shift for each clock input. In both cases the next state of the flip flops occurs after the low to high transition of the clock input.
4. An internal clock buffer provides both reduced clock input loading, and the ability to gate the clock with only a single NAND gate.
5. The active high output is provided for all four stages and an active low output is provided for the last stage.
6. A master asynchronous clear input allows the setting to zero of all stages, independent of the condition of any other inputs.

TABLE I — TRUTH TABLE FOR SERIAL ENTRY
(PE = HIGH, MR = HIGH, (n + 1) indicates state after next clock)

J	$\overline{K}$	Q_0 at t_{n+1}
L	L	L
L	H	Q_0 at t_n (no change)
H	L	$\overline{Q}_0$ at t_n (toggles)
H	H	H

TABLE II — LOADING RULES (1 U.L. = 1 TTμL Gate Input Load)

INPUTS	LOADING
J, $\overline{K}$, $\overline{MR}$, P_0, P_1, P_2 & P_3	1 U.L.
$\overline{PE}$	2.3 U.L.
C_P	2 U.L.
OUTPUTS	**FANOUT**
Q_0, Q_1, Q_2, Q_3 & $\overline{Q}_3$	6 U.L.

TABLE III
ELECTRICAL CHARACTERISTICS ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$) (Part #U6B/4L930051X)

SYMBOL	CHARACTERISTICS	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS & COMMENTS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	$V_{CC} = 4.5\ V$, $I_{OH} = -0.36\ mA$
V_{OL}	Output Low Voltage		0.4		0.2	0.4		0.4	Volts	$V_{CC} = 5.5\ V$, $I_{OL} = 9.6\ mA$ $V_{CC} = 4.5\ V$, $I_{OL} = 7.44\ mA$
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current* J, K, MR, P_0, P_1, P_2 & P_3		−1.6 −1.24		−1.10 −0.97	−1.6 −1.24		−1.6 −1.24	mA mA	$V_{CC} = 5.5\ V$ $V_{CC} = 4.5\ V$ $V_F = 0.4\ V$
I_R	Input Leakage Current* J, K, MR, P_0, P_1, P_2 & P_3				15	60		60	μA	$V_{CC} = 5.5\ V$, $V_R = 4.5\ V$

TABLE IV
ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0\ V \pm 5\%$) (Part #U6B/4L930059X)

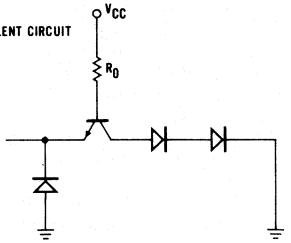
SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	$V_{CC} = 4.75\ V$, $I_{OH} = -0.36\ mA$
V_{OL}	Output Low Voltage		0.45		0.2	0.45		0.45	Volts	$V_{CC} = 5.25\ V$, $I_{OL} = 9.6\ mA$ $V_{CC} = 4.75\ V$, $I_{OL} = 8.5\ mA$
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current* J, $\overline{K}$, MR, P_0, P_1, P_2 & P_3		−1.6 −1.41		−1.0 −0.9	−1.6 −1.41		−1.6 −1.41	mA mA	$V_{CC} = 5.25\ V$ $V_{CC} = 4.75\ V$, $V_F = 0.45\ V$
I_R	Input Leakage Current* J, $\overline{K}$, MR, P_0, P_1, P_2 & P_3				15	60		60	μA	$V_{CC} = 5.25\ V$, $V_R = 4.5\ V$

*For CP and PE input currents, use load factors in Table II

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

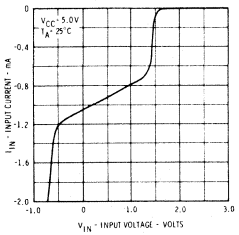
INPUTS

EQUIVALENT CIRCUIT

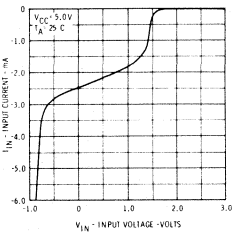


INPUT CURRENT VERSUS INPUT VOLTAGE

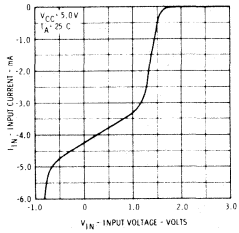
$\overline{MR}$, J, $\overline{K}$, P_0, P_1, P_2 & P_3



$\overline{PE}$

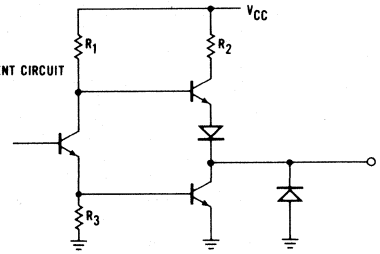


CP



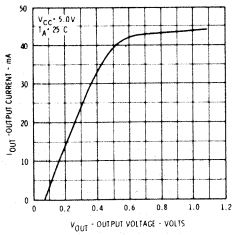
OUTPUTS

EQUIVALENT CIRCUIT

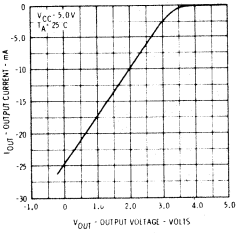


OUTPUT CURRENT VERSUS OUTPUT VOLTAGE
(Q_0, Q_1, Q_2, Q_3 AND $\overline{Q}_3$)

LOW STATE



HIGH STATE



SWITCHING CHARACTERISTICS ($T_A = 25°C$) (Part #U6B/4L930051X and U6B/4L930059X)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS & COMMENTS
t_{pd-}	Turn Off Delay		20	35	ns	$V_{CC} = 5.0$ V, $C_L = 15$ pF
t_{pd-}	Turn On Delay		25	45	ns	(See Fig. 6 & 7a)
f_{sr}	Shift Right Frequency	15	25		MHz	$V_{CC} = 5.0$ V, $C_L = 15$ pF (See Fig. 6 & 7c)
CP_{pw}	Clock Pulse Width	35	15		ns	
t_s	Set-up Time	35	17		ns	$V_{CC} = 5.0$ V
t_r	Release Time		16	0	ns	$C_L = 15$ pF,
$t_s(\overline{PE})$	Set-up Time for $\overline{PE}$	45	26		ns	(See Figs. 7a & 7b)
$t_r(\overline{PE})$	Release Time for $\overline{PE}$		25	10	ns	
$t_{pd-}(\overline{MR})$	Reset Time for $\overline{MR}$		35	65	ns	
$t_{rec}(\overline{MR})$	Recovery Time for $\overline{MR}$		20	35	ns	
$\overline{MR}_{pw}$	Min Reset Pulse Width		15	35	ns	

SET-UP TIME: t_s is defined as the minimum time required for the logic level to be present at the logic input prior to the clock transition from low to high in order for the flip-flop(s) to respond.

RELEASE TIME: t_r is defined as the maximum time allowed for the logic level to be present at the logic input prior to the clock transition from low to high in order for the flip-flop(s) not to respond.

RECOVERY TIME FOR $\overline{MR}$: $t_{rec}(\overline{MR})$ is defined as the minimum time required between the end of the reset pulse and the clock transition from low to high in order for the flip-flop(s) to respond to the clock.

Fig. 4
PROPAGATION DELAY — CLOCK TO Q_3 OR $\overline{Q}_3$ OUTPUT VS TEMPERATURE

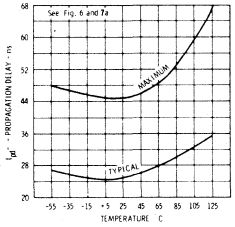
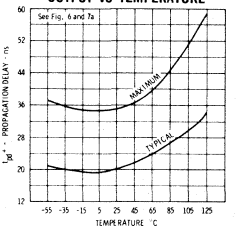
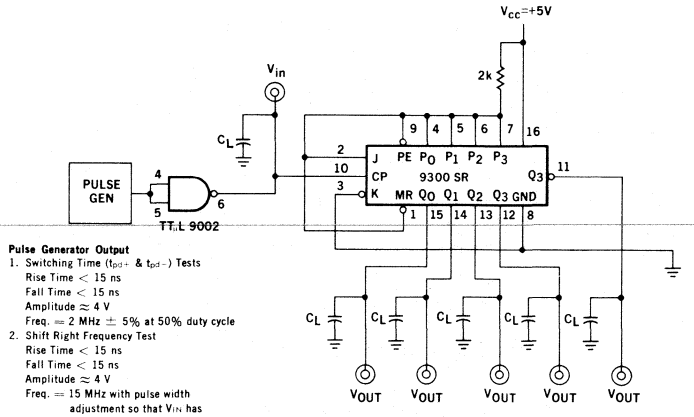


Fig. 5
PROPAGATION DELAY — CLOCK TO Q_3 OR $\overline{Q}_3$ OUTPUT VS TEMPERATURE





Pulse Generator Output
1. Switching Time (t_{pd+} & t_{pd-}) Tests
   Rise Time < 15 ns
   Fall Time < 15 ns
   Amplitude ≈ 4 V
   Freq. = 2 MHz ± 5% at 50% duty cycle
2. Shift Right Frequency Test
   Rise Time < 15 ns
   Fall Time < 15 ns
   Amplitude ≈ 4 V
   Freq. = 15 MHz with pulse width adjustment so that V_{IN} has duty cycle of approx. 50%.

Fig. 6 — SWITCHING TIME & SHIFT RIGHT FREQUENCY TEST CIRCUIT

Fig. 7a

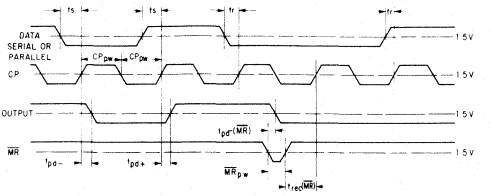


Fig. 7b

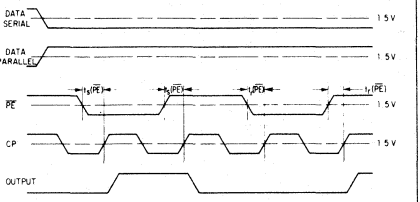
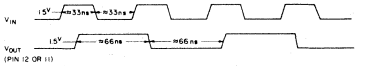


Fig. 7c



VOUT Frequency = ½ X VIN Frequency

Fig. 7 — SWITCHING TIME & SHIFT RIGHT FREQUENCY WAVEFORMS

APPLICATIONS — The 9300 has been designed to be useful in a wide variety of applications. The multifunctional capability of the Fairchild 9300 is illustrated by the applications shown below.

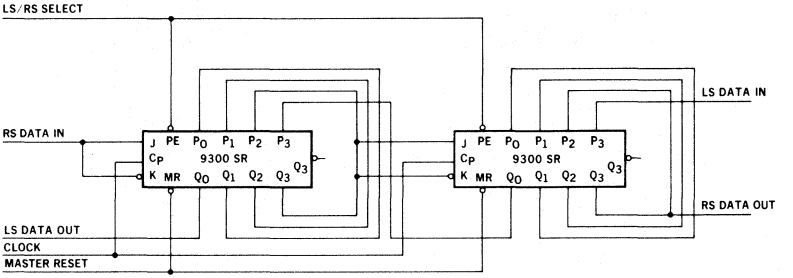


Fig. 8 — EIGHT BIT LEFT/RIGHT SHIFT REGISTER

This register shifts Left or Right on each shift clock, depending upon the condition of the LS/RS SELECT input. If this input is high, Right Shift occurs and if low, Left Shift occurs.

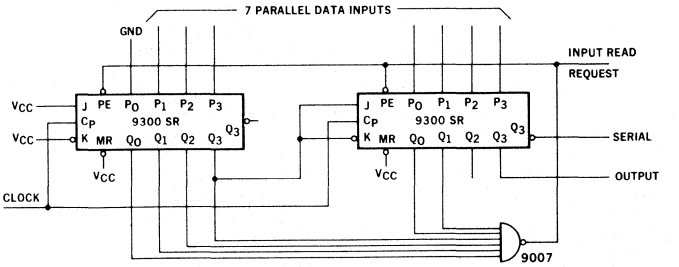


Fig. 9 — SEVEN BIT PARALLEL TO SERIAL CONVERTER

This parallel to serial converter uses a marker bit, to count the data bits shifted out, so that a parallel load enable is generated to load the next parallel word for conversion at the correct time.

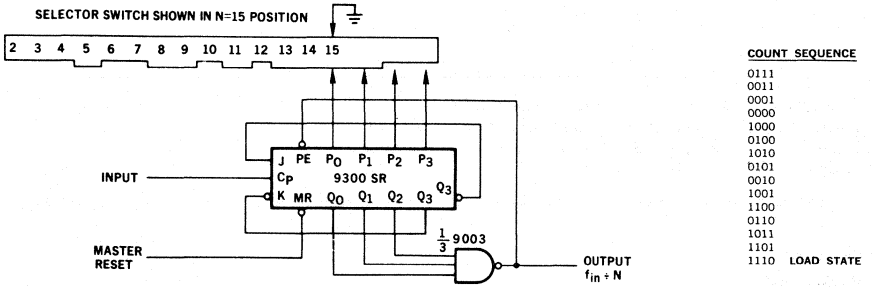


Fig. 10 — DIVIDE BY N COUNTER FOR N = 2 to 15

This counter produces an output pulse for every N input pulses, where the number N is determined by the setting of the slide selector switch as shown or by logic inputs to the parallel data lines from an external source.

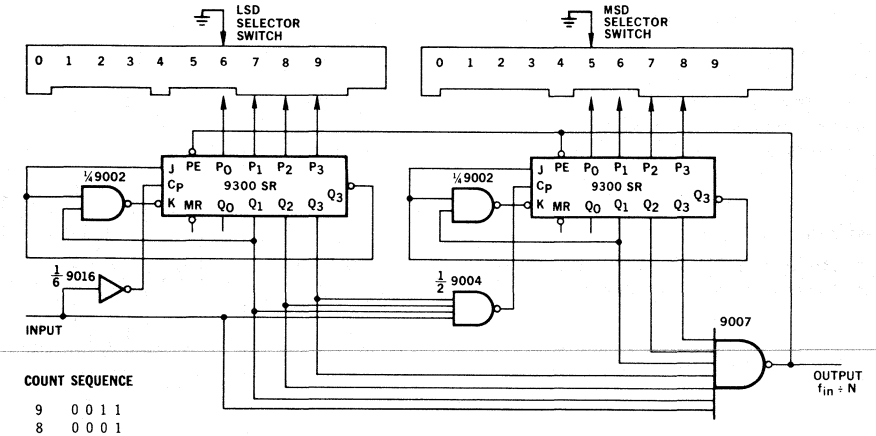


Fig. 11 — TWO DECADE PROGRAMMABLE DIVIDER

This circuit divides by any number "N" from 1 to 100. The selected N is one greater than is shown on the slide switches. As an example the switches are showing 56, therefore the circuit will divide by 57 with this setting.

9301

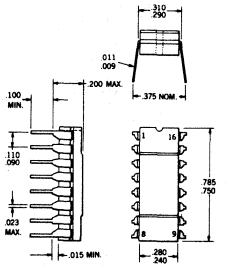
MSI ONE-OF-TEN DECODER

A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

GENERAL DESCRIPTION — The 9301 is a multipurpose decoder designed to accept four inputs and provide 10 mutually exclusive outputs. The circuit uses TTμL for high speed and high fan out capability, and is compatible with all members of the CCSL group of digital integrated circuits.

- **Multi-function capability**
- **Mutually exclusive outputs**
- **Guaranteed fanout of 10 TTμL loads over the full temperature range and supply voltage ranges**
- **High capacitive drive capability**
- **Demultiplexing capability**
- **Typical power dissipation of 145 mW**
- **The input/output characteristics provide easy interfacing with Fairchild DTμL, LPDTμL and TTμL families (CCSL).**
- **All ceramic "HERMETIC" 16-pin Dual In-Line* package**
- **Input clamp diodes limit high speed line termination effects**

PHYSICAL DIMENSIONS



NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.375) misalignment to facilitate insertion.
2. Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

Fig. 1

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7 V
Voltage Applied to Outputs for high output state	−0.5 V to +V_{CC} value
Input Voltage (D.C.)	−0.5 V to +5.5 V

LOGIC SYMBOL

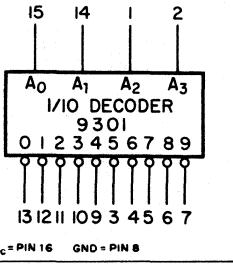


Fig. 2

ORDER INFORMATION

Specify U6B9301XXX for 16 pin Dual In-Line package where XXX is 51X for the −55°C to +125°C temperature range, or 59X for the 0°C to +75°C temperature range.

*Fairchild patent pending.

FAIRCHILD
SEMICONDUCTOR

FUNCTIONAL DESCRIPTION

The 9301 Decoder accepts four active high BCD inputs and provides ten mutually exclusive active low outputs, as shown by Figure 2. The active low outputs facilitate memory addressing when inverting drivers are used between decoder and memory elements such as the 9033.

The logic design of the 9301 ensures that all outputs are high when binary codes greater than nine are applied to the inputs.

The most significant A_3 input produces a useful inhibit function when the 9301 is used as a 1 out of 8 decoder. This is illustrated in the 1 out of 32 decoder shown in Figure 9.

The Truth Table and Loading Rules for the 9301 are shown in Table I and Table II.

TABLE I — TRUTH TABLE

A_0	A_1	A_2	A_3	0	1	2	3	4	5	6	7	8	9
L	L	L	L	L	H	H	H	H	H	H	H	H	H
H	L	L	L	H	L	H	H	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H	H	H
H	H	L	L	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	H	H	H	L	H	H	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
H	H	H	L	H	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = High Voltage Level
L = Low Voltage Level

TABLE II —

LOADING RULES (1 U.L. = TTμL Gate Input Load)

INPUTS	LOADING
A_0, A_1, A_2 & A_3	1 U.L.

OUTPUTS	FANOUT
0, 1, 2, 3, 4, 5, 6, 7, 8, & 9	10 U.L.

TABLE III —

ELECTRICAL CHARACTERISTICS ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$) (Part #U6B930151X)

SYMBOL	CHARACTERISTICS	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	$V_{CC} = 4.5\ V$, $I_{OH} = -0.6\ mA$
V_{OL}	Output Low Voltage		0.4		0.2	0.4		0.4	Volts	$V_{CC} = 4.5\ V$, $I_{OL} = 12.4\ mA$ $V_{CC} = 5.5\ V$, $I_{OL} = 16.0\ mA$
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		−1.6		−1.10	−1.6		−1.6	mA	$V_{CC} = 5.5\ V$, $V_F = 0.4\ V$
			−1.24		−0.97	−1.24		−1.24	mA	$V_{CC} = 4.5\ V$
I_R	Input Leakage Current				15	60		60	μA	$V_{CC} = 5.5\ V$, $V_R = 4.5\ V$
t_{pd+}	Turn Off Delay Input to Output				23	35			ns	$V_{CC} = 5.0\ V$
t_{pd-}	Turn On Delay Input to Output				20	30			ns	$C_L = 15\ pF$ See Fig. 8

TABLE IV —

ELECTRICAL CHARACTERISTICS (T_A = 0°C to +75°C, V_{CC} = 5.0 V ±5%) (Part #U6B930159X)

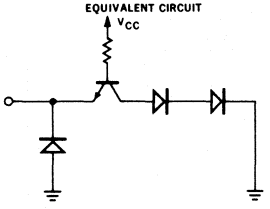
SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	0°C MAX.	+25°C MIN.	+25°C TYP.	+25°C MAX.	+75°C MIN.	+75°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	V_{CC} = 4.75 V, I_{OH} = −0.6 mA
V_{OL}	Output Low Voltage		0.45		0.2	0.45		0.45	Volts	V_{CC} = 4.75 V, I_{OL} = 14.1 mA V_{CC} = 5.25 V, I_{OL} = 16.0 mA
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		−1.6		−1.0	−1.6		−1.6	mA	V_{CC} = 5.25 V, V_F = 0.45 V
			−1.41		−0.9	−1.41		−1.41	mA	V_{CC} = 4.75 V
I_R	Input Leakage Current				15	60		60	μA	V_{CC} = 5.25 V, V_R = 4.5 V
t_{pd+}	Turn Off Delay Input to Output				23	35			ns	V_{CC} = 5.0 V
t_{pd-}	Turn On Delay				20	30			ns	C_L = 15 pF See Fig. 8

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

Fig. 3

INPUTS

EQUIVALENT CIRCUIT



INPUT CURRENT VERSUS INPUT VOLTAGE

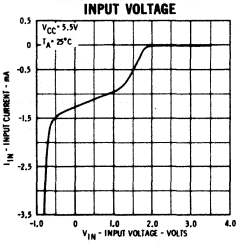
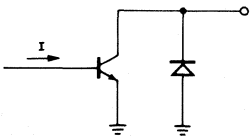


Fig. 4

OUTPUTS

EQUIVALENT CIRCUIT

OUTPUT LOW



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE OUTPUT LOW

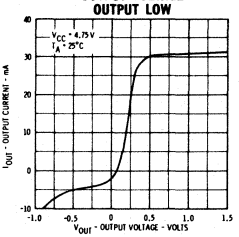
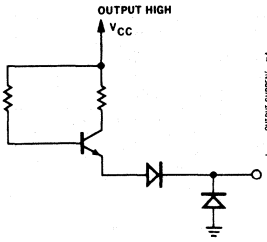
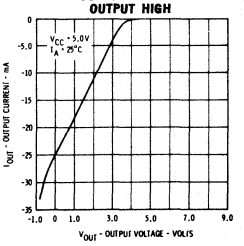


Fig. 5

OUTPUT HIGH



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE OUTPUT HIGH



SWITCHING PERFORMANCE

Fig. 6

TYPICAL TURN ON DELAY VERSUS TEMPERATURE

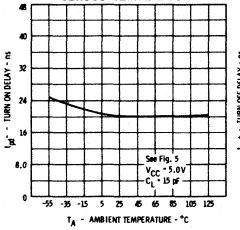
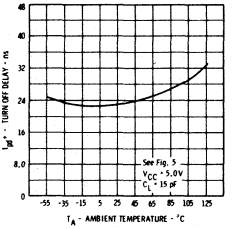
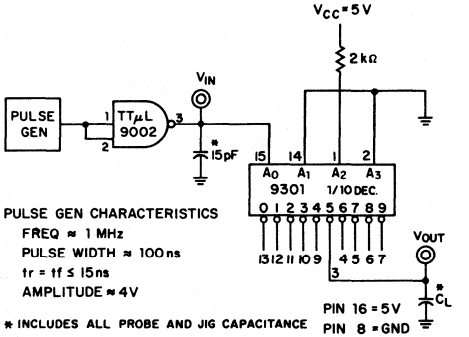


Fig. 7

TYPICAL TURN OFF DELAY VERSUS TEMPERATURE





PULSE GEN CHARACTERISTICS
- FREQ ≈ 1 MHz
- PULSE WIDTH ≈ 100 ns
- tr = tf ≤ 15 ns
- AMPLITUDE ≈ 4 V

* INCLUDES ALL PROBE AND JIG CAPACITANCE

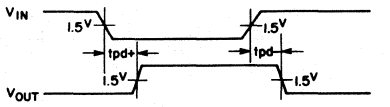


Fig. 8 — SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

APPLICATIONS — The 9301 decoder may be used for BCD to Decimal or 3 bit binary to octal conversion as well as many other applications. The general purpose nature of the 9301 is indicated by its use in the following applications.

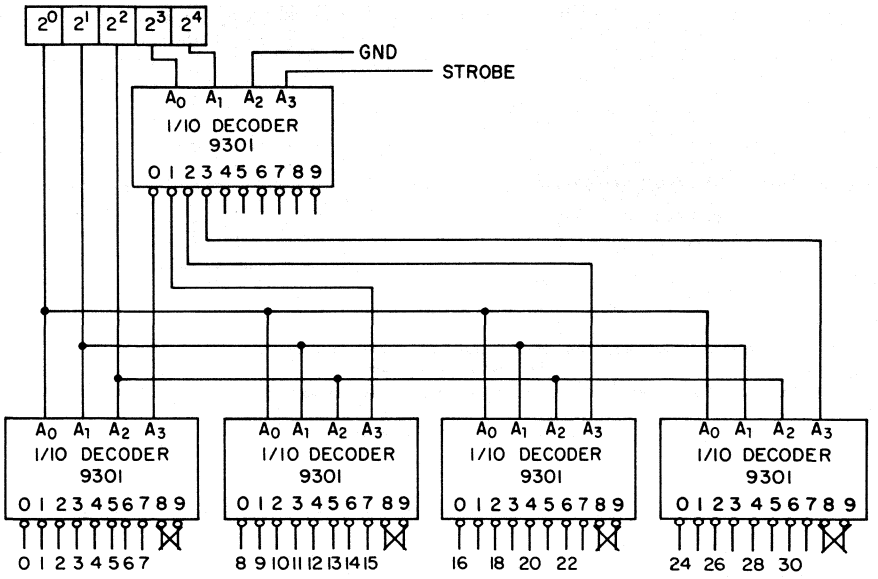
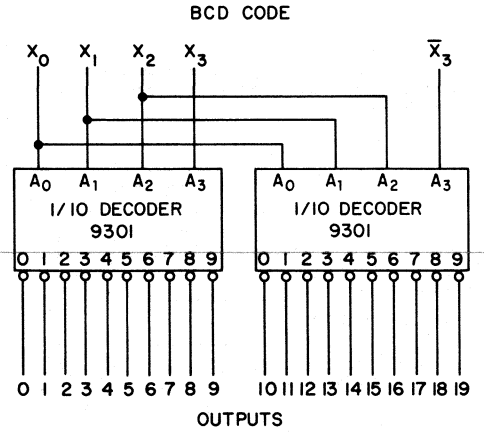


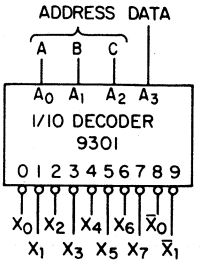
Fig. 9 — ONE-OUT-OF-THIRTY-TWO DECODING



DECIMAL DIGIT	OUTPUT SELECTION BCD CODE 8421	5421	EXCESS 3	4221
0	0, 18	0, 18	3	0, 18
1	1, 19	1, 19	4	1, 19
2	2	2	5	2
3	3	3	6	3
4	4	4	7	6
5	5	8, 10	8, 10	9, 11
6	6	9, 11	9, 11	14
7	7	12	12	15
8	8, 10	13	13	16
9	9, 11	14	14	17

Decode any BCD code using two 9301 elements. Any 4 bit BCD code may be decoded by selecting outputs as shown in the table.

Fig. 10 — DECODE ANY BCD CODE

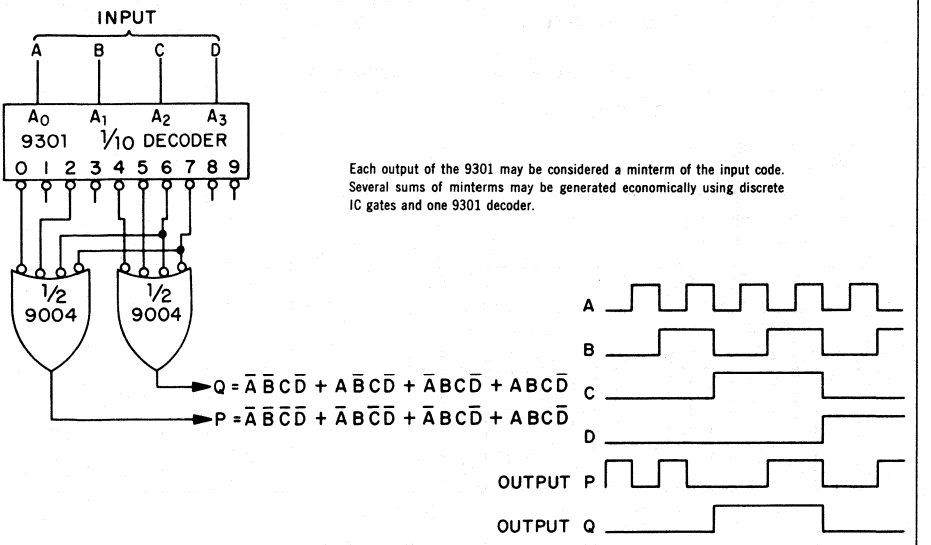


ADDRESS			OUTPUT
A	B	C	LINE
0	0	0	0
1	0	0	1
0	1	0	2
1	1	0	3
0	0	1	4
1	0	1	5
0	1	1	6
1	1	1	7

Data may be routed from a source to any of 8 outputs by addressing that output.
All non-addressed outputs remain high.

Complements of outputs 0 and 1 are available at outputs 8 and 9 respectively.

Fig. 11— DIGITAL DEMULTIPLEXER



Each output of the 9301 may be considered a minterm of the input code. Several sums of minterms may be generated economically using discrete IC gates and one 9301 decoder.

Fig. 12— MINTERM GENERATOR

9304

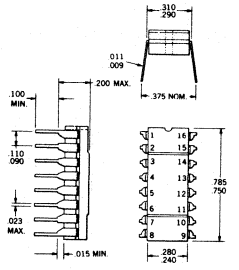
MSI DUAL FULL ADDER

A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

GENERAL DESCRIPTION — The 9304 consists of two independent, high speed, binary full adders. The adders are useful in a wide variety of applications including multiple bit parallel add/serial carry addition, parity generation and checking, code conversion, and majority gating. The circuit uses TTμL for high speed, high fanout operation and is compatible with all members of the CCSL group of digital integrated circuits.

- **Multi-function capability**
- **8ns carry propagation delay**
- **Complementary inputs and outputs available**
- **Typical power dissipation of 150 mW**
- **The input/output characteristics provide easy interfacing with Fairchild DTμL, LPDTμL and TTμL families (CCSL).**
- **All ceramic "HERMETIC" 16-pin Dual In-Line* package**
- **Input clamp diodes limit high speed termination effects**

PHYSICAL DIMENSIONS



NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.375) misalignment to facilitate insertion.
2. Board drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

Fig. 1

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7 V
Voltage Applied to Outputs for high output state	−0.5 V to +V_{CC} value
Input Voltage (D.C.)	−0.5 V to +5.5 V

LOGIC SYMBOL

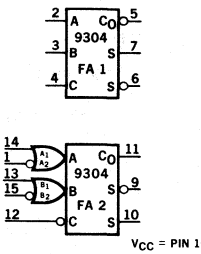


Fig. 2

ORDER INFORMATION

Specify U6B9304XXX for 16 pin Dual In-Line package where XXX is 51X for the −55°C to +125°C temperature range, or 59X for the 0°C to +75°C temperature range.

*Fairchild patent pending

FAIRCHILD SEMICONDUCTOR

FUNCTIONAL DESCRIPTION

The Fairchild 9304 logic block consists of two separate high speed carry dependent sum full adders. This design allows a minimum carry propagation time when the adders are used in ripple carry applications. The adders are identical except that adder 2 has provision for either active high or active low inputs at the A and B terminals. The adders produce a low carry and both low and high sum with active high inputs, a high carry and both high and low sum when active low inputs are used. This principle of duality is shown in Figure 12, where the adders are drawn as functional blocks.

The Truth Table and Loading Rules for the 9304 are shown in Table I and Table II.

TABLE I — TRUTH TABLES

ADDER 1					
INPUTS			OUTPUTS		
C	B	A	$\overline{C}_O$	$\overline{S}$	S
L	L	L	H	H	L
L	L	H	H	L	H
L	H	L	H	L	H
L	H	H	L	H	L
H	L	L	H	L	H
H	L	H	L	H	L
H	H	L	L	H	L
H	H	H	L	L	H

ADDER 2							
INPUTS					OUTPUTS		
$\overline{C}$	B_1	A_1	$\overline{B}_2$	$\overline{A}_2$	C_O	S	$\overline{S}$
L	L	L	L	L	H	H	L
L	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H
L	L	L	H	H	L	H	L
L	L	H	L	L	H	H	L
L	L	H	L	H	H	H	L
L	L	H	H	L	H	L	H
L	L	H	H	H	H	L	H
L	H	L	L	L	H	H	L
L	H	L	L	H	H	L	H
L	H	L	H	L	H	H	L
L	H	L	H	H	H	L	H
L	H	H	L	L	H	H	L
L	H	H	L	H	H	H	L
L	H	H	H	L	H	H	L
L	H	H	H	H	H	H	L
H	L	L	L	L	H	L	H
H	L	L	L	H	L	H	L
H	L	L	H	L	L	H	L
H	L	L	H	H	L	L	H
H	L	H	L	L	H	L	H
H	L	H	L	H	H	L	H
H	L	H	H	L	L	H	L
H	L	H	H	H	L	H	L
H	H	L	L	L	H	L	H
H	H	L	L	H	L	H	L
H	H	L	H	L	H	L	H
H	H	L	H	H	L	H	L
H	H	H	L	L	H	L	H
H	H	H	L	H	H	L	H
H	H	H	H	L	H	L	H
H	H	H	H	H	H	L	H

H = High Voltage Level
L = Low Voltage Level

TABLE II —

LOADING RULES (1 U.L. = TTμL Gate Input Unit Load)

INPUTS		LOADING
FA 1	A, B & C	4 U.L.
FA 2	$\overline{A}_2$, $\overline{B}_2$ & $\overline{C}$	4 U.L.
	A_1 & B_1	1 U.L.

OUTPUTS		FANOUT
FA 1	$\overline{C}_O$	7 U.L.
	$\overline{S}$	9 U.L.
	S	10 U.L.
FA 2	C_O	7 U.L.
	S	9 U.L.
	$\overline{S}$	10 U.L.

TABLE III —
ELECTRICAL CHARACTERISTICS ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$) (Part #U6B930451X)

SYMBOL	CHARACTERISTICS	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.2		2.4	2.7		2.4		Volts	$V_{CC} = 4.5\ V$, $I_{OH} = -1.2$ mA (Pins 7 & 9) $V_{CC} = 4.5\ V$, $I_{OH} = -1.08$ mA (Pins 6 & 10) $V_{CC} = 4.5\ V$, $I_{OH} = -0.84$ mA (Pins 5 & 11)
V_{OL}	Output Low Voltage		0.4		0.21	0.4		0.4	Volts	$V_{CC} = 5.5\ V$, $I_{OL} = 16$ mA (Pins 7 & 9) $I_{OL} = 14.4$ mA (Pins 6 & 10) $I_{OL} = 11.2$ mA (Pins 5 & 11) $V_{CC} = 4.5\ V$, $I_{OL} = 12.4$ mA (Pins 7 & 9) $I_{OL} = 11.2$ mA (Pins 6 & 10) $I_{OL} = 8.7$ mA (Pins 5 & 11)
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		−1.6		−1.1	−1.6		−1.6	mA	$V_{CC} = 5.5\ V$; $V_F = 0.4\ V$, $V_R = 5.5\ V$ on other inputs
$4\ I_F$	Input Load Current		−6.4		−4.4	−6.4		−6.4		
I_F	Input Load Current		−1.24		−0.97	−1.24		−1.24	mA	$V_{CC} = 4.5\ V$; $V_F = 0.4\ V$, $V_R = 5.5\ V$ on other inputs
$4\ I_F$	Input Load Current		−4.96		−3.88	−4.96		−4.96		
I_R	Input Leakage Current				15	60		60	μA	$V_{CC} = 5.5\ V$, $V_R = 4.5\ V$
$4\ I_R$	Input Leakage Current				60	240		240		Ground on other inputs
t_{pd+}	C to C_O				8	13			ns	$V_{CC} = 5.0\ V$ $C_L = 15$ pF See Fig. 11
t_{pd-}	C to C_O				8	13			ns	
t_{pd+}	A_i to $\overline{S}$				28	40			ns	
t_{pd-}	A_i to $\overline{S}$				25	35			ns	

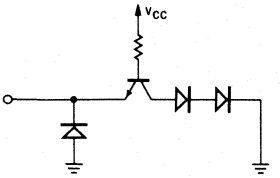
TABLE IV —
ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0\ V \pm 5\%$) (Part #U6B930459X)

SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	$V_{CC} = 4.75\ V$, $I_{OH} = -1.2$ mA (Pins 7 & 9) $V_{CC} = 4.75\ V$, $I_{OH} = -1.08$ mA (Pins 6 & 10) $V_{CC} = 4.75\ V$, $I_{OH} = -0.84$ mA (Pins 5 & 11)
V_{OL}	Output Low Voltage		0.45		0.21	0.45		0.45	Volts	$V_{CC} = 5.25\ V$, $I_{OL} = 16$ mA (Pins 7 & 9) $I_{OL} = 14.4$ mA (Pins 6 & 10) $I_{OL} = 11.2$ mA (Pins 5 & 11) $V_{CC} = 4.75\ V$, $I_{OL} = 14.1$ mA (Pins 7 & 9) $I_{OL} = 12.7$ mA (Pins 6 & 10) $I_{OL} = 9.85$ mA (Pins 5 & 11)
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		−1.6		−1.0	−1.6		−1.6	mA	$V_{CC} = 5.25\ V$, $V_F = 0.45\ V$
$4\ I_F$	Input Load Current		−6.4		−4.0	−6.4		−6.4		$V_R = 5.25\ V$ on other inputs
I_F	Input Load Current		−1.41		−0.9	−1.41		−1.41	mA	$V_{CC} = 4.75\ V$, $V_F = 0.45\ V$
$4\ I_F$	Input Load Current		−5.64		−3.6	−5.64		−5.64		$V_R = 5.25\ V$ on other inputs
I_R	Input Leakage Current				15	60		60	μA	$V_{CC} = 5.25\ V$, $V_R = 4.5\ V$
$4\ I_R$	Input Leakage Current				60	240		240		Ground on other inputs
t_{pd+}	C to C_O				8.0	15			ns	$V_{CC} = 5.0\ V$ $C_L = 15$ pF See Fig. 11
t_{pd-}	C to C_O				8.0	15			ns	
t_{pd+}	A_i to $\overline{S}$				28	45			ns	
t_{pd-}	A_i to $\overline{S}$				25	40			ns	

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

INPUTS

EQUIVALENT CIRCUIT



INPUT CURRENT VS INPUT VOLTAGE

FIG. 3 PINS 1, 2, 3, 4, 12, 15

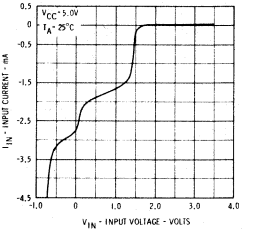
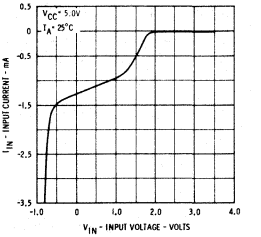
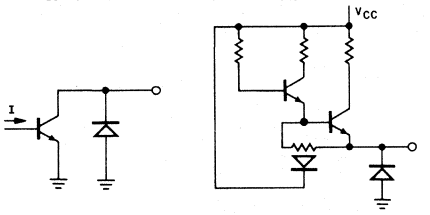


FIG. 4 PINS 13, 14



OUTPUTS

LOW STATE HIGH STATE



OUTPUT CURRENT VS OUTPUT VOLTAGE

FIG. 5 LOW STATE

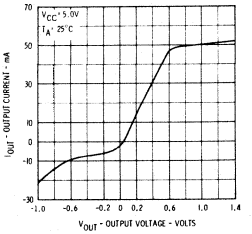


FIG. 6 HIGH STATE

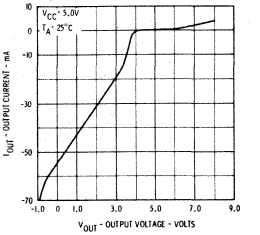


Fig. 7
TYPICAL CARRY TURN ON DELAY TIME VERSUS TEMPERATURE

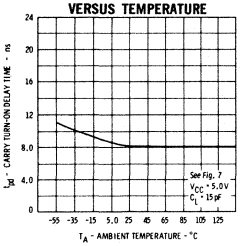


Fig. 8
TYPICAL CARRY TURN OFF DELAY TIME VERSUS TEMPERATURE

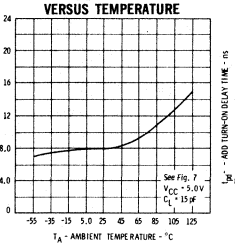


Fig. 9
TYPICAL ADD TURN ON DELAY TIME VERSUS TEMPERATURE

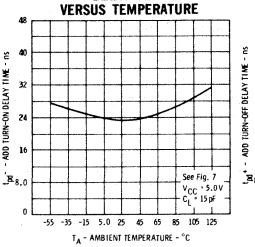
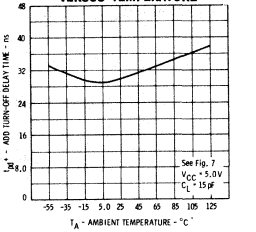
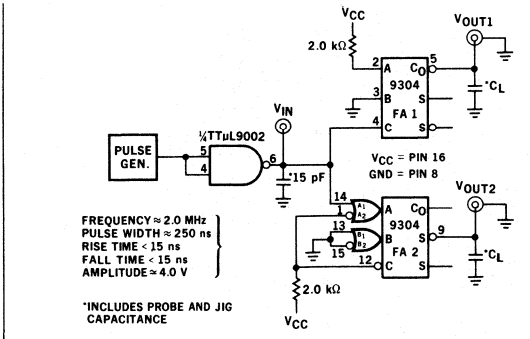


Fig. 10
TYPICAL ADD TURN OFF DELAY TIME VERSUS TEMPERATURE





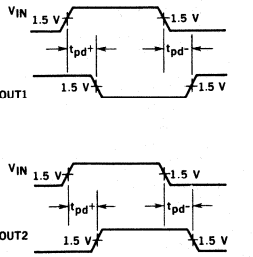


Fig.11— SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

APPLICATIONS — The 9304 dual adder has been designed to be useful in a wide variety of applications such as addition, parity generation and checking, code conversion, majority gating and other applications for which this combination of logic gates may be useful. The multifunctional capabilities of the Fairchild dual adder can be seen from reference to the applications shown.

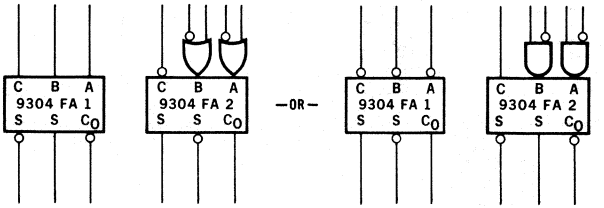


Fig.12— FUNCTIONAL BLOCK REPRESENTATION

The principle of duality allows 2 ways of representing each adder. The circuit is the same in both cases but the logic diagrams differ. The dual diagrams facilitate logic design and allow a greater understanding of the capabilities of the device.

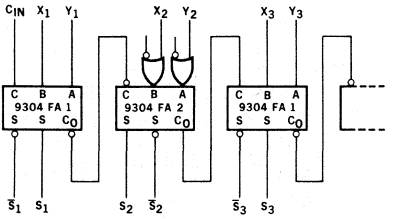


Fig.13— RIPPLE CARRY PARALLEL ADDITION

Shown above is a high speed ripple carry parallel addition scheme. Only one and-or-not gate relay is incurred at each stage allowing a typical addition speed of (N+1) x 8 ns, where N is the number of bits in the word. A similar scheme will work if the negation inputs are used, and the design acts as a subtractor when the complement of one variable is provided.

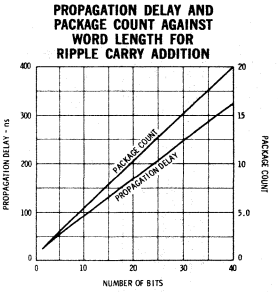


Fig. 14

The curve shows propagation delay of the ripple Carry Adder drawn in Figure 5. Plotted on the same diagram is a curve showing the low package count resulting from this Ripple Scheme.

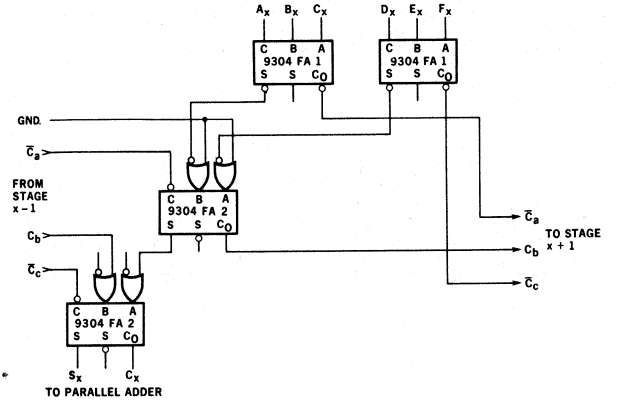


Fig. 15 — ADDITION OF SIX VARIABLES

The above design shows how the 9304 can be used in carry save arithmetic. Six input variable are reduced to two where they can be added in a parallel adder. Delay between inputs and outputs is typically 50 ns, allowing extremely high speed computation. Additional variables may be added or the concept can be extended to multiplication, division, and various other arithmetic operations.

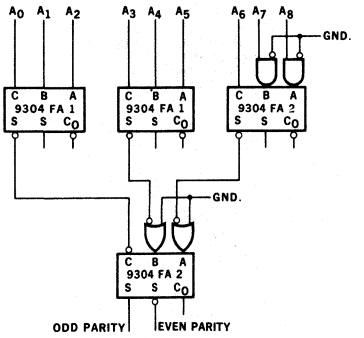


Fig. 16 — BYTE PARITY GENERATION OR CHECKING

The 9304 can be used for parity checking or generating. The above design uses 2 9304's to generate parity for an 8 bit byte or check parity over 9 bits. The delay from input to odd parity is typically 35 ns. Additional adder blocks can be used to generate or check parity over larger word lengths. The concept can also be used for hamming and cyclic code generation and checking.

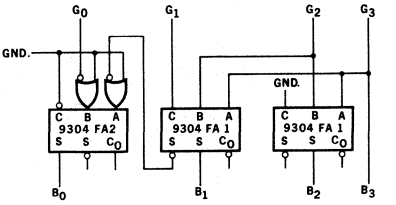


Fig. 17 — 4 BIT PARALLEL GRAY TO BINARY CONVERSION

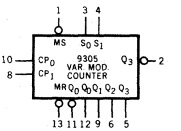
A 4 bit parallel binary to gray conversion is shown. The adders can also be used for other cyclic code manipulations.

TT μL/MSI 9305
VARIABLE MODULO COUNTER
A FAIRCHILD TTμL IC PRODUCT

GENERAL DESCRIPTION — The TTμL/MSI 9305 is a monolithic, high speed, variable modulo counter circuit, constructed with the Fairchild Planar* epitaxial process. It is a semisynchronous counter which can be programmed without extra logic to provide division or counting by either 2 and 4, 5, 6, 7, 8, or 10, 12, 14, 16. A binary count sequence can be obtained for all of the preceding counter modulos as well as 50% duty cycle output for dividers of 8, 10, 12, 14, 16. The device also features asynchronous overriding master reset and set inputs and the negation output of the final flip-flop output which allows the cascading of stages. The circuit uses TTμL for high speed, high fanout operation and is compatible with all other members of the TTμL family of digital integrated circuits.

- **VARIOUS BINARY COUNTING MODES**
  - **—MODULO 2 AND MODULO 5, 6, 7, 8**
  - **—MODULO 10 (8421 BCD), 12, 14, 16**
- **VARIOUS FREQUENCY DIVISION MODES WITH 50% DUTY CYCLE OUTPUT**
  - **—MODULO 8, 10, 12, 14, 16**
- **LOGIC SELECTION OF COUNTING MODE**
- **ASYNCHRONOUS MASTER RESET AND SET INPUTS**
- **MULTISTAGE COUNTING OPERATION**
- **TTμL COMPATIBLE**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**

LOGIC SYMBOL



V_{CC} = Pin 14
Gnd = Pin 7

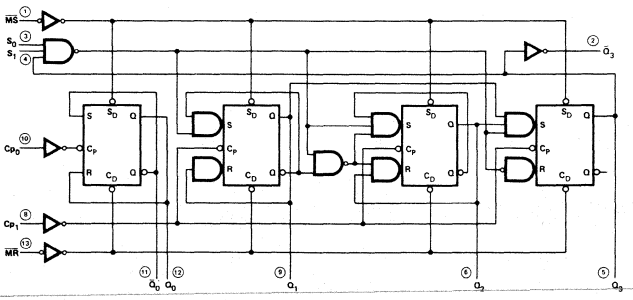
Fig. 1

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
Voltage Applied to Output when output is high	0 V to +V_{CC} value
Input Voltage (DC) (See Note 1)	−0.5 V to +5.5 V
Input Current (DC) (See Note 1)	−30 mA to +5 mA
Current into Output when output is low	30 mA

Note 1 — Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

LOGIC DIAGRAM



V_{CC} = Pin 14
Gnd = Pin 7

Fig. 2

ORDER INFORMATION — Specify U7A9305XXX for 14 pin Dual In-Line package where XXX is 51X for the −55°C to +125°C temperature range, or 59X for the 0°C to +75°C temperature range.

*Planar is a patented Fairchild process.

FAIRCHILD
SEMICONDUCTOR

FUNCTIONAL DESCRIPTION — The MSI 9305 consists of four master-slave flip-flops which are separated into two functional units, a single toggle stage and a three stage synchronous counter. All four flip-flops change state on the low to high transition of the clock. The three stage counter can be programmed with external connections as shown in Table 1 to provide modulo of either 5, 6, 7, or 8. This basic configuration allows synchronous binary counting by the last three stages and independent modulo 2 operation with the first single stage.

A four stage binary counter with a modulo of 10, 12, 14, or 16 is obtained by applying the incoming clock to the single toggle stage and feeding its negation output to the clock input of the three stage counter. A 4-stage divider with 50% duty cycle output is produced by feeding the incoming clock to the three stage counter and clocking the single stage with the Q_3 output. In either the binary or 50% division mode the modulo (10, 12, 14, 16) is determined by the external programming connections for the three stage counter. These 4-stage counters or dividers are not fully synchronous (semisynchronous) but have only one flip-flop ripple delay in either configuration. Counter modulos other than 10, 12, 14, 16 can be formed with a few extra gates as illustrated in the application section.

Several 9305 variable modulo counters programmed in any modulo can be connected together without extra logic to form asynchronous (ripple) type multistage counters. This is done by connecting the $\overline{Q}_3$ output of the less significant counter to the clock input of the following counter.

The master set and reset will asynchronously set or reset all four stages when activated. The active low reset input when low will clear the counter, overriding the clock and forcing the outputs ($Q_{0\text{-}3}$) low and outputs $\overline{Q}_0$, $\overline{Q}_3$ high. The active low set input when low will preset the counter, overriding the clock and forcing the outputs $Q_{0\text{-}3}$ high and outputs $\overline{Q}_0$, $\overline{Q}_3$ low. The master set provides a synchronous clear, since the first clock pulse following the asynchronous master set will reset all stages. This action is independent of the modulo programmed.

PIN FUNCTIONS

S_0, S_1	Select Inputs
CP_0	First Stage Clock Active High Going Edge Input
CP_1	Three Stage Clock Active High Going Edge Input
$\overline{MS}$	Master Set (Active Low) Input
$\overline{MR}$	Master Reset (Active Low) Input
Q_0	First Stage Output
$\overline{Q}_0$	Complementary First Stage Output
Q_1, Q_2, Q_3	Three Stage Counter Outputs
$\overline{Q}_3$	Complementary Last Stage Output

LOADING RULES

INPUTS	LOADINGS
CP_0, CP_1 $\overline{MS}$, $\overline{MR}$ S_0, S_1	1 U.L.

OUTPUTS	FANOUT AT LOGIC LEVEL	
	HIGH	LOW
Q_0, $\overline{Q}_0$, Q_1, Q_2, Q_3	16 U.L.	8 U.L.
$\overline{Q}_3$	20 U.L.	10 U.L.

(1 U.L. = 1 TTμL gate input load)

COUNTING MODE

The following are rules specifying the external connections required for various counter and divider modulo's.

PROGRAMMING CONNECTIONS FOR LAST THREE STAGES

S_0	S_1	MODULO
NC	NC	5
Q_1	NC	6
NC	Q_1	6
Q_2	NC	7
NC	Q_2	7
Q_1	Q_2	8
Q_2	Q_1	8

NC = No Connection

CONNECTIONS FOR MODULO 10, 12, 14, 16 BINARY COUNTERS AND 50% DUTY CYCLE DIVIDERS

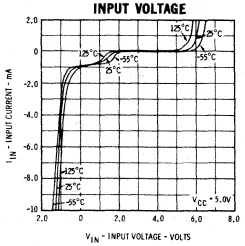
For Binary Counting $\overline{Q}_0$ connected to CP_1 Incoming clock to CP_0
For 50% Duty Cycle Output $\overline{Q}_3$ connected to CP_0 Incoming clock to CP_1

ASYNCHRONOUS MODE

$\overline{MS}$	$\overline{MR}$	Q_0	$\overline{Q}_0$	Q_1	Q_2	Q_3	$\overline{Q}_3$
L	H	H	L	H	H	H	L
H	L	L	H	L	L	L	H
H	H	COUNT*					

*As Determined by Programming Connections

TYPICAL INPUT AND OUTPUT CHARACTERISTICS



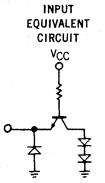
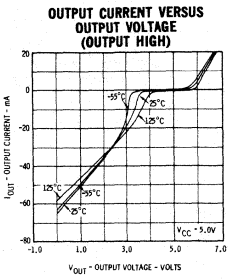


Fig. 3



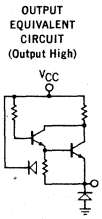
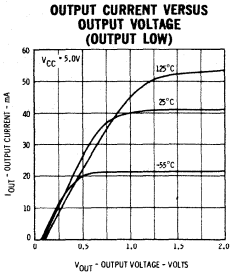


Fig. 4



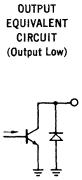


Fig. 5

ELECTRICAL CHARACTERISTICS* (T_A = −55°C to +125°C, V_{CC} = 5.0 V ±10%) (Part No. U7A930551X)

SYMBOL	CHARACTERISTIC	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	2.9		2.4		Volts	V_{CC} = 4.5 V I_{OH} = −1.2 mA (Pin 2) V_{CC} = 4.5 V I_{OH} = −0.96 mA (Pins 5, 6, 9, 11, 12)
V_{OL}	Output Low Voltage		0.4		0.29	0.4		0.4	Volts	V_{CC} = 5.5 V I_{OL} = 16.0 mA (Pin 2) I_{OL} = 12.8 mA (Pins 5, 6, 9, 11, 12) V_{CC} = 4.5 V I_{OL} = 12.4 mA (Pin 2) I_{OL} = 9.92 mA (Pins 5, 6, 9, 11, 12)
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F (all inputs)	Input Load Current		−1.6		−1.1	−1.6		−1.6	mA	V_{CC} = 5.5 V; V_F = 0.4 V
			−1.24		−0.85	−1.24		−1.24	mA	V_{CC} = 4.5 V; Input Selected
I_R (all inputs)	Input Leakage Current				10	60		60	μA	V_{CC} = 5.5 V V_R = 4.5 V
I_{PD}	V_{CC} Current	60			42	60		60	mA	V_{CC} = 5.0 V, Pin 13 = Gnd, All others open
t_{pd+} (CP_0 to $\overline{Q}_3$)	Switching Speed				55				ns	V_{CC} = 5.0 V, All outputs C_L = 15 pF Modulo 16 (S_0 to Q_1; S_1 to Q_2; $\overline{Q}_0$ to CP_1) Input CP_0
t_{pd-} (CP_0 to $\overline{Q}_3$)	Switching Speed				52				ns	
f_{max}	Maximum Frequency of Input Count Pulses			20	26				MHz	V_{CC} = 5.0 V, All outputs C_L = 15 pF Modulo 16 (S_0 to Q_1; S_1 to Q_2; $\overline{Q}_0$ to CP_1) Input CP_0

***Pulse Tested**

ELECTRICAL CHARACTERISTICS* (T_A = 0°C to +75°C, V_{CC} = 5.0 V ±5%) (Part No. U7A930559X)

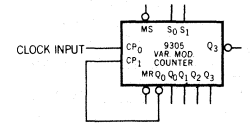
SYMBOL	CHARACTERISTIC	LIMITS 0°C MIN.	0°C MAX.	+25°C MIN.	+25°C TYP.	+25°C MAX.	+75°C MIN.	+75°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	2.9		2.4		Volts	V_{CC} = 4.75 V I_{OH} = −1.2 mA (Pin 2) V_{CC} = 4.75 V I_{OH} = −0.96 mA (Pins 5, 6, 9, 11, 12)
V_{OL}	Output Low Voltage		0.45		0.29	0.45		0.45	Volts	V_{CC} = 5.25 V I_{OL} = 16.0 mA (Pin 2) I_{OL} = 12.8 mA (Pins 5, 6, 9, 11, 12) V_{CC} = 4.75 V I_{OL} = 14.1 mA (Pin 2) I_{OL} = 11.3 mA (Pins 5, 6, 9, 11, 12)
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F (all inputs)	Input Load Current		−1.6		−1.0	−1.6		−1.6	mA	V_{CC} = 5.25 V, V_F = 0.45 V
			−1.41		−0.91	−1.41		−1.41	mA	V_{CC} = 4.75 V, Input Selected
I_R (all inputs)	Input Leakage Current				10	60		60	μA	V_{CC} = 5.25 V, V_R = 4.5 V
I_{PD}	V_{CC} Current		65		42	65		65	mA	V_{CC} = 5.0 V, Pin 13 = Gnd, All others open
t_{pd+} (CP_0 to $\overline{Q}_3$)	Switching Speed				55				ns	V_{CC} = 5.0 V, All outputs C_L = 15 pF Modulo 16 (S_0 to Q_i; S_i to Q_2; $\overline{Q}_0$ to CP_1) Input CP_0
t_{pd-} (CP_0 to $\overline{Q}_3$)	Switching Speed				52				ns	
f_{max}	Maximum Frequency of Input Count Pulses			20	26				MHz	V_{CC} = 5.0 V, All outputs C_L = 15 pF Modulo 16 (S_0 to Q_i; S_i to Q_2; $\overline{Q}_0$ to CP_1) Input CP_0

***Pulse Tested**

APPLICATIONS

COUNTER/DIVIDER CONFIGURATIONS

MODULO 10 COUNTER (BCD 8421 DECADE)



WAVEFORMS

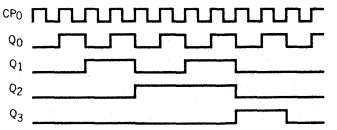
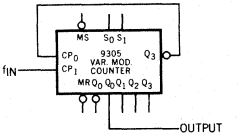


Fig. 6

MOD 10 DIVIDER, 50% DUTY CYCLE OUTPUT



WAVEFORMS

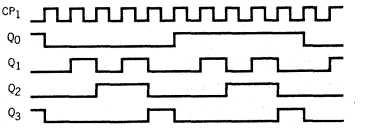
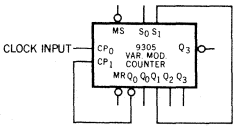


Fig. 7

MODULO 12 COUNTER



WAVEFORMS

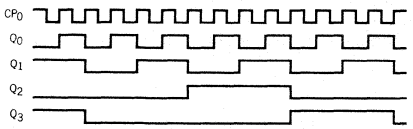
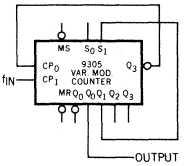


Fig. 8

MOD 12 DIVIDER, 50% DUTY CYCLE OUTPUT



WAVEFORMS

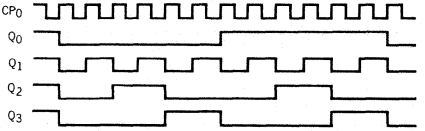
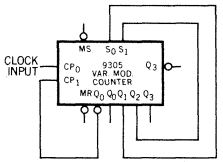


Fig. 9

MODULO 16 COUNTER (4 BIT BINARY COUNTER)



WAVEFORMS

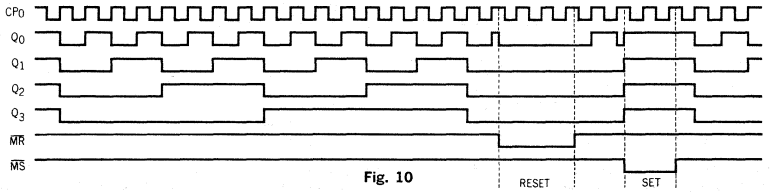
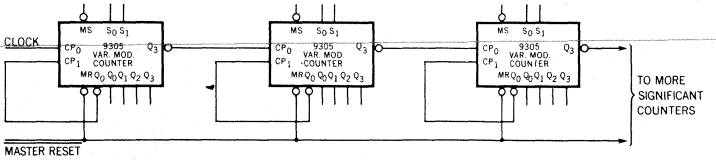


Fig. 10

MULTISTAGE COUNTING SCHEME

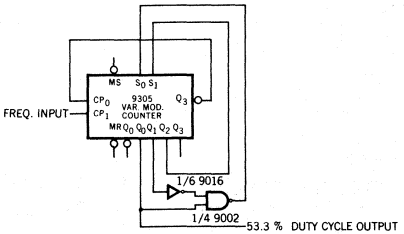


The connections required for a multistage ripple counter are shown above. The 9305 are programmed in this case to form BCD decades, however the same interconnections (Q_3 to clock of following stage) will permit multistage counting with the other counter modulos.

Fig. 11

APPLICATIONS (Cont'd.)

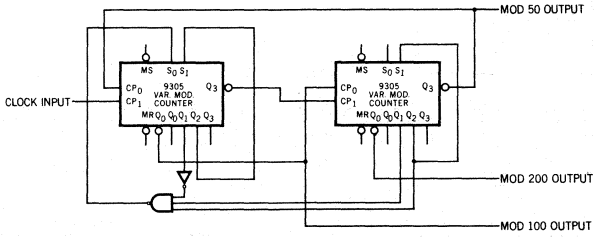
MOD 15 DIVIDER



This figure illustrates a modulo 15 divider that has a 53.3% duty cycle output. The nand gate and inverter permits the three stage counter to divide by seven or eight under control of Q_0, the output of the first stage. The first stage is clocked by the three stage counter and alternately switches the three stage counters modulo producing a mod 15 divider.

Fig. 12

MODULO 50, 100, 200 DIVIDER

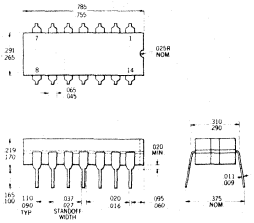


A modulo 50 counter is made by controlling the modulo of the three stage programmable counter of the first 9305 with the corresponding counter of the second 9305. The three stage counter of the first 9305 counts by seven, six times and then counts by eight once when one state is decoded of the seven programmed into the second 9305. The first stages of both 9305's divide this modulo 50 output and provide modulo 100 and modulo 200 outputs.

Fig. 13

PACKAGE INFORMATION

7A - 14 Lead MSI Dual In-Line



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020" diameter lead
Leads are tin-plated kovar
Package weight is 2.2 grams

9306

MSI UP/DOWN BCD COUNTER

A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

GENERAL DESCRIPTION — The 9306 is a high speed synchronous 8421 BCD up/down decade counter. It is a synchronously presetable, multifunctional MSI building block useful in a large number of counting, digital integration, and conversion applications. Seven decades of synchronous operation are obtainable with no external gating packages required through an internal carry look-ahead counting technique.

FEATURES:

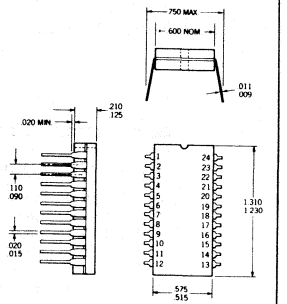
- **SYNCHRONOUS COUNTING AND PARALLEL ENTRY**
- **DECODED TERMINAL COUNT**
- **BUILT-IN CARRY/BORROW CIRCUITRY**
- **TYPICAL POWER DISSIPATION OF 350 mW**
- **THE INPUT/OUTPUT CHARACTERISTICS PROVIDE EASY INTERFACING WITH FAIRCHILD DTμL, LPDTμL, AND TTμL FAMILIES (CCSL).**
- **ALL CERAMIC HERMETIC 24 PIN DUAL IN-LINE PACKAGE**
- **INPUT DIODE CLAMPING**

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

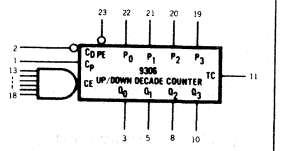
Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7 V
Voltage Applied to Outputs for high output state	−0.5 V to V_{CC} value
Input Voltage (D.C.)	−0.5 V to +5.5 V

ORDER INFORMATION — Specify U6N9306XXX for 24-pin Dual In-Line package where XXX is 51X for the −55°C to +125°C temperature range, or 59X for the 0°C to 75°C temperature range.

PHYSICAL DIMENSIONS



LOGIC DIAGRAM



V_{CC} — Pin 24
Gnd — Pin 12

FAIRCHILD
SEMICONDUCTOR

FUNCTIONAL DESCRIPTION — A clock buffer and inverter drives the four clocked RS master-slave flip flops in parallel, so that synchronous operation is obtained. When the clock input (CP) is low, the slave is steady, but data can enter the master via the R and the S inputs. During the low to high transition of CP, first the data inputs (R and S) are inhibited, so that a later change in the input data will not affect the master; secondly, the now trapped information in the master is transferred to the slave and is reflected at the outputs. When the transfer is completed both the master and the slave are steady as long as the clock input remains high, and regardless of the logic state at any other input to the device. During the high to low transition of the clock input, first the transfer path from master to slave are inhibited, leaving the slave steady in its present state, secondly, the data inputs (R and S) are enabled so that new data can enter the master. As a result of this synchronous operation higher clock frequency is possible and much less external logic is required in most applications. Mode selection is accomplished as shown in the table below. However, several restrictions are placed on the manner of selection. First, the transition of CE from high to low or of PE from low to high may only be done when CP is high. Second, any change of CD must be done only when CP is high. The remaining transitions may be made by following the setup and release times specified under "Switching Characteristics."

MODE SELECTION SCHEME

PE	CD	CE	Mode
0	0	0	presetting
0	0	1	presetting
0	1	0	presetting
0	1	1	presetting
1	1	1	count up
1	0	1	count down
1	1	0	no change
1	0	0	no change

Note: $CE = CE_0 \cdot CE_1 \cdot CE_2 \cdot CE_3 \cdot CE_4 \cdot CE_5$

LOADING RULES
(1 U.L. = 1 TTμL input gate load)

INPUT	FAN IN
CD, CE_0, CE_1, CE_2,	1 Unit Load
CE_3, CE_4, CE_5	1 Unit Load
CP, PE	2 Unit Loads
P_0, P_1, P_2, P_3	2/3 Unit Load
OUTPUT	**FAN OUT**
Q_0, Q_1, Q_2, Q_3, TC	6 Unit Loads

ELECTRICAL CHARACTERISTICS ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$)

SYMBOL	CHARACTERISTICS	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS & COMMENTS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	$V_{CC} = 4.5\ V$, $I_{OH} = -0.36\ mA$
V_{OL}	Output Low Voltage		0.4		0.2	0.4		0.4	Volts	$V_{CC} = 5.5\ V$, $I_{OL} = 9.6\ mA$ $V_{CC} = 4.5\ V$, $I_{OL} = 7.44\ mA$
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current E_0, E_1, E_2, E_3, E_4, E_5, CD		−1.6		−1.0	−1.6		−1.6	mA	
$2\ I_F$	Input Load Current CP, PE		−3.2		−2.0	−3.2		−3.2	mA	$V_{CC} = 5.5\ V$ $V_F = 0.4\ V$
$2/3\ I_F$	Input Load Current P_0, P_1, P_2, P_3		−1.07		−.7	−1.07		−1.07	mA	
I_R	Input Leakage Current E_0, E_1, E_2, E_3, E_4, E_5, CD		60		10	60		60	μA	
$2\ I_R$	Input Leakage Current CP, PE		120		20	120		120	μA	$V_{CC} = 5.5\ V$ $V_R = 4.5\ V$
$2/3\ I_R$	Input Leakage Current P_0, P_1, P_2, P_3		40		7	40		40	μA	

ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0\ V \pm 5\%$)

SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	CONDITIONS & COMMENTS
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	$V_{CC} = 4.75\ V$, $I_{OH} = -0.36\ mA$
V_{OL}	Output Low Voltage		0.45		0.2	0.45		0.45	Volts	$V_{CC} = 5.25\ V$, $I_{OL} = 9.6\ mA$
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	$V_{CC} = 4.75\ V$, $I_{OL} = 8.5\ mA$ Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current $E_0, E_1, E_2, E_3, E_4, E_5, CD$		−1.6		−1.0	−1.6		−1.6	mA	
$2\ I_F$	Input Load Current CP, PE		−3.2		−2.0	−3.2		−3.2	mA	$V_{CC} = 5.25\ V$ $V_F = 0.4\ V$
$⅔ I_F$	Input Load Current P_0, P_1, P_2, P_3		−1.07		−.7	−1.07		−1.07	mA	
I_R	Input Leakage Current $E_0, E_1, E_2, E_3, E_4, E_5, CD$		60		10	60		60	μA	
$2\ I_R$	Input Leakage Current CP, PE		120		20	120		120	μA	$V_{CC} = 5.25\ V$ $V_R = 4.5\ V$
$⅔ I_R$	Input Leakage Current P_0, P_1, P_2, P_3		40		7	40		40	μA	

SWITCHING CHARACTERISTICS ($T_A = 25°C$)

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	CONDITIONS & COMMENTS
t_{pd+} (Q)	Turn-Off Delay		20		ns	$V_{CC} = 5.0\ V$ $C_L = 15\ pF$ (Fig. 1)
t_{pd-} (Q)	Turn-On Delay		20		ns	
t_{pd+} (TC)	Turn-Off Delay for TC		40		ns	
t_{pd-} (TC)	Turn-On Delay for TC		30		ns	
t_s (CE)	Set-Up Time for CE		25		ns	$V_{CC} = 5.0\ V$ $C_L = 15\ pF$ (Fig. 2)
t_r (CE)	Release Time for CE		25		ns	
t_s	Set-Up Time for Data		15		ns	$V_{CC} = 5.0\ V$ $C_L = 15\ pF$ (Fig. 3)
t_r	Release Time for Data		15		ns	
t_s (PE)	Set-Up Time for PE		20		ns	
t_r (PE)	Release Time for PE		20		ns	

SET-UP TIME: t_s is defined as the minimum time required for the logic level to be present at the logic input prior to the clock transition from low to high in order for the flip-flop(s) to respond.

RELEASE TIME: t_r is defined as the maximum time allowed for the logic level to be present at the logic input prior to the clock transition from low to high in order for the flip-flop(s) not to respond.

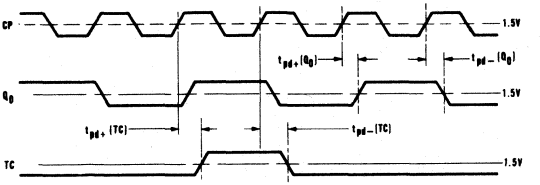


Fig. 1

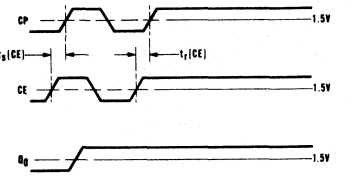


Fig. 2

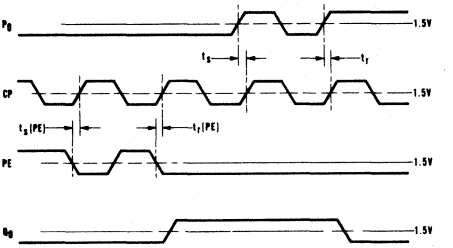


Fig. 3

APPLICATIONS

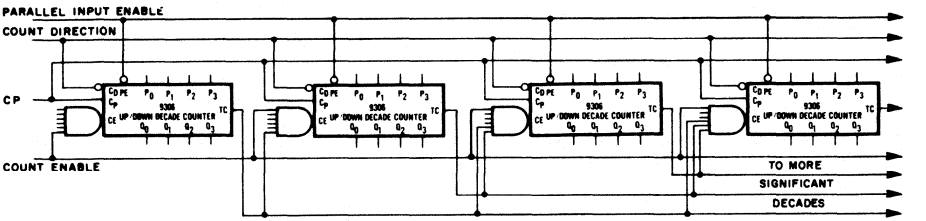


Fig. 4

9307

MSI SEVEN SEGMENT DECODER

A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

GENERAL DESCRIPTION — The 9307 is a Seven Segment Decoder designed to accept four inputs in 8421 BCD code and provide the appropriate outputs to drive a seven segment numerical display. The decoder can be used with seven segment incandescent lamp, neon, electro-luminescent, or CRT numeric displays. The 9307 is compatible with all other Fairchild CCSL devices.

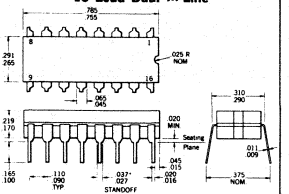
- **CCSL COMPATIBLE**
- **AUTOMATIC RIPPLE BLANKING FOR SUPPRESSION OF LEADING EDGE ZEROES**
- **LAMP INTENSITY MODULATION CAPABILITY**
- **LAMP TEST FACILITY**
- **BLANKING INPUT**
- **ACTIVE HIGH OUTPUTS**
- **ALL CERAMIC "HERMETIC" 16 PIN DUAL IN-LINE* PACKAGE**

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7 V
Voltage Applied to Outputs for high output state	−0.5 V to +V_{CC} value
Input Voltage (D.C.)	−0.5 V to +5.5 V

DUAL IN-LINE PACKAGE

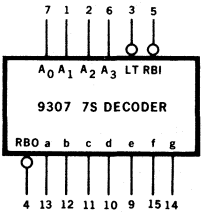
16 Lead Dual In-Line



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" center
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for a conventional .020 inch diameter Lead
Package weight is 2.0 grams
Leads are tin-plated Kovar
*The .037 dimension does not apply .027 to the corner leads

Fig. 1

LOGIC SYMBOL

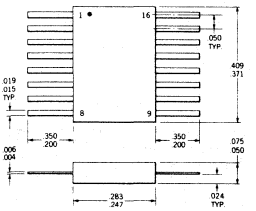


V_{CC}=PIN 16
GND=PIN 8

Fig. 3

FLAT PAK

16 Lead BeO Cerpak



NOTES:
All dimensions in inches
Leads are gold-plated Kovar
Package weight is 0.4 gram

Fig. 2

ORDER INFORMATION

Specify U6B9307XXX for 16 pin Dual In-Line package or U4L9307XXX for 16 pin Flat package where XXX is 51X for the −55°C to +125°C temperature range, or 59X for the 0°C to +75°C temperature range.

*Fairchild patent pending.

FAIRCHILD
SEMICONDUCTOR

The 9307 seven segment decoder accepts a 4 Bit BCD 8421 code input and produces the appropriate outputs for selection of segments in a seven segment matrix display used for representing the decimal numbers 0 - 9. The seven outputs (a, b, c, d, e, f, g) of the decoder select the corresponding segments in the matrix shown in Figure 4. The numeric designations chosen to represent the decimal numbers are shown in Figure 6, together with the resulting displays for input code configurations in excess of binary nine.

The decoder has active high outputs so that a buffer transistor may be used directly to provide the high currents required for incandescent displays. If additional base drive current is required external resistors may be added from the supply voltage to the seven segment outputs of the decoders. The value of this resistor is constrained by the 10 mA current sinking capability of the output transistors of the circuit.

The device has provision for automatic blanking of the leading and/or trailing edge zeroes in a multidigit decimal number, resulting in an easily readable decimal display, conforming to normal writing practice. In an eight digit mixed integer fraction decimal representation, using the automatic blanking capability, (0060.0300) would be displayed as (60.03). Leading edge zero suppression is obtained by connecting the Ripple Blanking Output (RBO) of a decoder to the Ripple Blanking Input (RBI) of the next lower stage device. The most significant decoder stage should have the RBI input grounded; and, since suppression of the least significant integer zero in a number is not usually desired, the RBI input of this decoder stage should be left open. A similar procedure for the fractional part of a display will provide automatic suppression of trailing edge zeroes.

The decoder has an active low input Lamp Test which overrides all other input combinations and enables a check to be made on possible display malfunctions. The RBO terminal of the decoder can be OR - tied with a modulating signal via an isolating buffer to achieve pulse duration intensity modulation. A suitable signal can be generated for this purpose by forming a variable frequency multivibrator with a cross coupled pair of DTμL gates.

Fig. 4
SEGMENT DESIGNATION

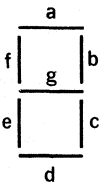


Fig. 5
TRUTH TABLE

LT	RB IN	A_0	A_1	A_2	A_3	a	b	c	d	e	f	g	RB OUT	
L	X	X	X	X	X	H	H	H	H	H	H	H	H	
H	L	L	L	L	L	L	L	L	L	L	L	L	L	0
H	H	L	L	L	L	H	H	H	H	H	H	L	H	0
	X	H	L	L	L	L	H	H	L	L	L	L	H	1
		L	H	L	L	H	H	L	H	H	L	H	H	2
		H	H	L	L	H	H	H	H	L	L	H	H	3
		L	L	H	L	L	H	H	L	L	H	H	H	4
		H	L	H	L	H	L	H	H	L	H	H	H	5
		L	H	H	L	H	L	H	H	H	H	H	H	6
		H	H	H	L	H	H	H	L	L	L	L	H	7
		L	L	L	H	H	H	H	H	H	H	H	H	8
		H	L	L	H	H	H	H	H	L	H	H	H	9
		L	H	L	H	L	L	L	H	H	L	H	H	10
		H	H	L	H	L	L	L	H	L	L	H	H	11
		L	L	H	H	L	H	H	L	L	H	H	H	12
		H	L	H	H	H	L	H	H	L	H	H	H	13
		L	H	H	H	L	L	L	H	H	H	H	H	14
H	X	H	H	H	H	L	L	L	L	L	L	L	H	15

H = HIGH VOLTAGE LEVEL
L = LOW VOLTAGE LEVEL
X = EITHER HIGH OR LOW VOLTAGE LEVEL

Fig. 6
NUMERICAL DESIGNATIONS

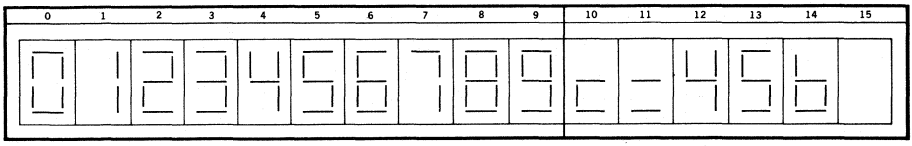


Table 1—Loading Rules (1 U.L. = 1 DTμL Gate Input Load)

Inputs	Loading (51X & 59X)	
	High State	Low State
A_0, A_1, A_2, A_3	1	1
$R_{B(IN)}$	1	1/2
LT	5	4.3

Outputs	Fan Out	
	51X	59X
a, b, c, d, e, f, g	8	7
$R_{B(OUT)}$	2.0	1.5

TABLE II —
ELECTRICAL CHARACTERISTICS ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$) (Part #U6B/4L930751X)

SYMBOL	CHARACTERISTICS	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	4.3 3.0		4.3 3.0	4.4 4.0		4.4 3.0		Volts	$V_{CC} = 4.5\ V$ $I_{OH} = 0.0\ mA$ (Pins 9-15) $V_{CC} = 4.5\ V$ $I_{OH} = -70\ \mu A$ (Pin 4) Inputs at threshold voltages (V_{IL} or V_{IH})
V_{OL}	Output Low Voltage		0.4		0.21	0.4		0.4	Volts	$V_{CC} = 5.5\ V$ $I_{OL} = 12.5\ mA$ (Pins 9-15) $I_{OL} = 3.1\ mA$ (Pin 4) $V_{CC} = 4.5\ V$ $I_{OL} = 10\ mA$ (Pins 9-15) $I_{OL} = 2.4\ mA$ (Pin 4) Inputs at threshold voltages (V_{IL} or V_{IH})
V_{IH}	Input High Voltage	2.1		1.9			1.7		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		1.4			1.1		0.8	Volts	Guaranteed input low threshold for all inputs
I_F (Pin 3) I_F (Pins 1, 2, 6, 7) I_F (Pin 5)	Input Load Current Input Load Current Input Load Current		−6.4 −1.5 −0.75			−6.4 −1.5 −0.75		−6.4 −1.5 −0.75	mA	$V_{CC} = 5.5\ V$ $V_F = 0.4\ V$ $V_R = 5.5\ V$ on other inputs
I_R (Pin 3) I_R (Pins 1, 2, 5, 6, 7)	Input Leakage Current Input Leakage Current					10 2.0		25 5.0	μA	$V_{CC} = 5.5\ V$ $V_R = 4.5\ V$ Ground on other inputs
I_A (Pins 9-15)	Available Output Current	−1.4		−1.4			−1.0		mA	$V_{OUT} = 0.85\ V$ $V_{CC} = 4.5\ V$ Inputs at threshold voltages (V_{IL} or V_{IH})
I_{SC} (Pins 9-15)	Short Circuit Current					−3.7			mA	$V_{OUT} = 0.0\ V$ $V_{CC} = 5.5\ V$
t_{pd+}	Switching Speed					500			ns	$V_{CC} = 5.0\ V$, See Figure 7 on page 5
t_{pd-}	Switching Speed					500			ns	

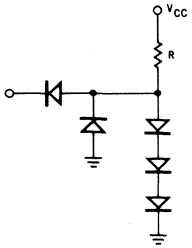
TABLE III —
ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0\ V \pm 5\%$) (Part #U6B/4L930759X)

SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	4.3 2.7		4.3 2.7	4.6 4.0		4.3 2.7		Volts	$V_{CC} = 4.75\ V$ $I_{OH} = 0.0\ mA$ (Pins 9-15) $V_{CC} = 4.75\ V$ $I_{OH} = -70\ \mu A$ (Pin 4) Inputs at threshold voltages (V_{IL} or V_{IH})
V_{OL}	Output Low Voltage		0.45		0.21	0.45		0.45	Volts	$V_{CC} = 5.25\ V$ $I_{OL} = 11.5\ mA$ (Pins 9-15) $I_{OL} = 2.75\ mA$ (Pin 4) $V_{CC} = 4.75\ V$ $I_{OL} = 10\ mA$ (Pins 9-15) $I_{OL} = 2.4\ mA$ (Pin 4) Inputs at threshold voltages (V_{IL} or V_{IH})
V_{IH}	Input High Voltage	2.0		2.0			2.0		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F (Pin 3) I_F (Pins 1, 2, 6, 7) I_F (Pin 5)	Input Load Current Input Load Current Input Load Current		−6.4 −1.5 −0.75			−6.4 −1.5 −0.75		−6.4 −1.5 −0.75	mA	$V_{CC} = 5.25\ V$ $V_F = 0.45\ V$ $V_R = 5.25$ on other inputs
I_R (Pin 3) I_R (Pins 1, 2, 5, 6, 7)	Input Leakage Current Input Leakage Current					25 5.0		50 10	μA	$V_{CC} = 5.25\ V$ $V_R = 4.5\ V$ Ground on other inputs
I_A (Pins 9-15)	Available Output Current	−1.4		−1.4			−1.0		mA	$V_{OUT} = 0.75\ V$ $V_{CC} = 4.75\ V$ Inputs at threshold voltages (V_{IL} or V_{IH})
I_{SC} (Pins 9-15)	Short Circuit Current					−4.0			mA	$V_{OUT} = 0.0\ V$ $V_{CC} = 5.5\ V$
t_{pd+}	Switching Speed					500			ns	$V_{CC} = 5.0\ V$, See Figure 7 on page 5
t_{pd-}	Switching Speed					500			ns	

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

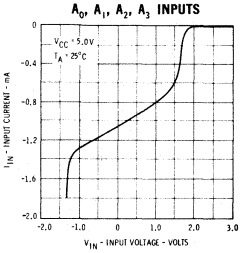
INPUTS

Equivalent Circuit

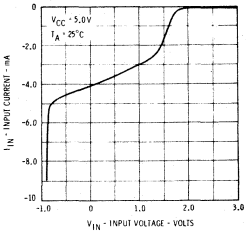


INPUT CURRENT VERSUS INPUT VOLTAGE

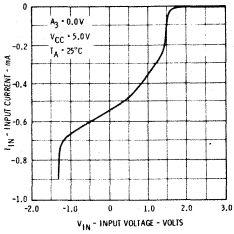
A_0, A_1, A_2, A_3 INPUTS



LT INPUT



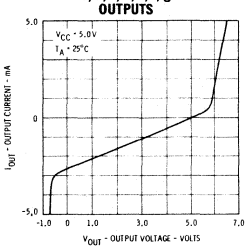
$RB_{(IN)}$ INPUT



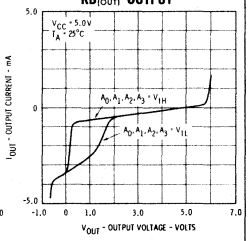
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE

U6B/4L930751X (−55°C to +125°C)
OUTPUT IN HIGH STATE

a, b, c, d, e, f, g OUTPUTS

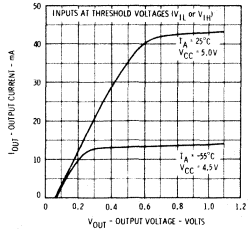


$RB_{(OUT)}$ OUTPUT

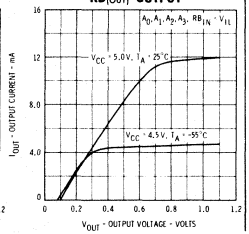


OUTPUT IN LOW STATE

a, b, c, d, e, f, g OUTPUTS

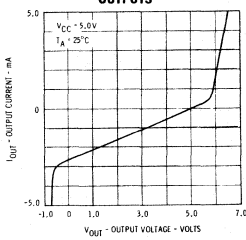


$RB_{(OUT)}$ OUTPUT

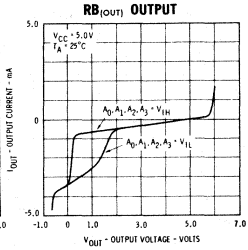


U6B/4L930759X (0°C to +75°C)
OUTPUT IN HIGH STATE

a, b, c, d, e, f, g OUTPUTS

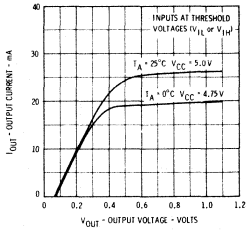


$RB_{(OUT)}$ OUTPUT

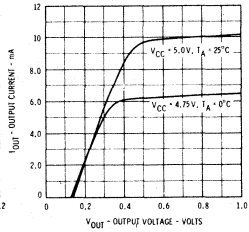


OUTPUT IN LOW STATE

a, b, c, d, e, f, g OUTPUTS



$RB_{(OUT)}$ OUTPUT



OUTPUTS

Equivalent Circuit

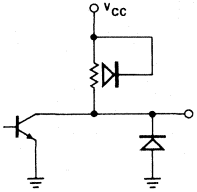
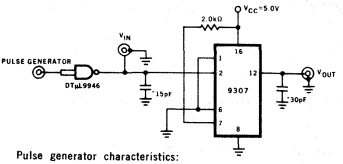
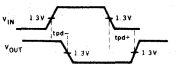


Fig. 7—SWITCHING CIRCUIT AND WAVEFORMS



Pulse generator characteristics:
Amplitude = 3.0 V
Freq. = 500 kHz
Pulse width = 1000 ns
$t_r = t_f \leq 15$ ns
*Includes probe and jig capacitance



APPLICATIONS

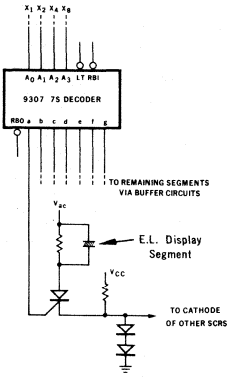


Fig. 8
9307 Seven Segment Decoder driving Electro-Luminescent Display.

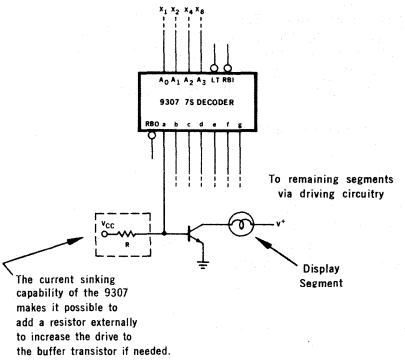


Fig. 9
9307 Seven Segment Decoder driving Incandescent lamp Display.

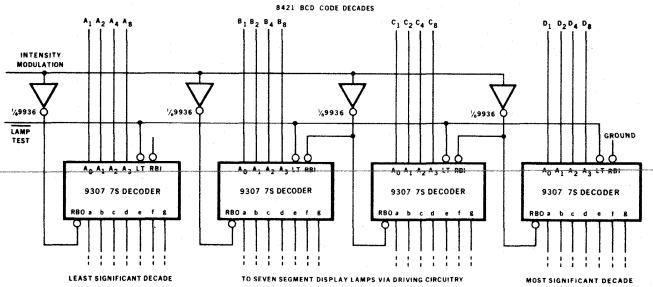


Fig. 10—FOUR DECADE SEVEN SEGMENT INTEGER DISPLAY SCHEME

This scheme incorporates automatic blanking of leading edge zeroes and intensity modulation using an external variable duty cycle signal.

9308
MSI DUAL FOUR-BIT LATCH
A FAIRCHILD TRANSISTOR-TRANSISTOR MICROLOGIC IC PRODUCT

GENERAL DESCRIPTION — The MSI 9308 is a Dual 4-Bit Latch designed for general purpose storage applications in high speed digital systems. The 9308 uses TTμL technology and is compatible with DTμL, TTμL, and MSI families. All inputs incorporate diode clamps to ground to reduce negative line transients. All outputs have active pull-up circuitry to provide high capacitive drive and low impedance outputs in both logic states to provide good A.C. noise immunity.

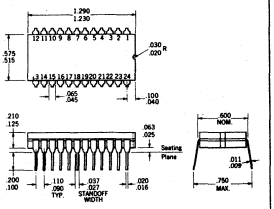
- **ACTIVE LEVEL LOW ENABLE GATE INPUTS**
- **OVERRIDING MASTER RESET**
- **25 ns THROUGH DELAY**
- **THE INPUT/OUTPUT CHARACTERISTICS PROVIDE DIRECT INTERFACING WITH FAIRCHILD DTμL, LPDTμL, TTμL, AND MSI FAMILIES**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **HIGH CAPACITIVE DRIVE CAPABILITY**
- **ALL CERAMIC HERMETIC 24-PIN DUAL IN-LINE PACKAGE**

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7 V
Input Voltage (D.C.)$_{\mathcal{F}}$(See Note 1)	−0.5 V to +5.5 V
Input Current (D.C.) (See Note 1)	−30 mA to +5 mA
Voltage Applied to Outputs (Output High)	−0.5 V to +V_{CC} value
Output Current (D.C.) (Output Low)	+30 mA

NOTE 1: Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

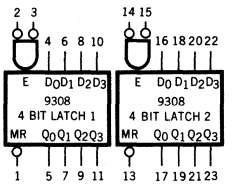
24 LEAD DUAL IN-LINE



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .600" centers. They are purposely shipped with "positive" misalignment to facilitate insertion
Leads are tin-plated kovar
Package weight is 6.5 grams

Fig. 1

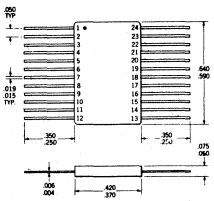
LOGIC DIAGRAM



V_{CC} = Pin 24
Gnd = Pin 12

Fig. 3

FLAT PACKAGE



NOTES:
All dimensions in inches
Leads are gold-plated kovar
Package weight is 0.8 gram

Fig. 2

ORDER INFORMATION — Specify U6N9308XXX for 24-pin Dual In-Line Package or U4M9308XXX for 24-pin Flat Package, where XXX is 51X for the −55°C to +125°C temperature range, or 59X for the 0°C to +75°C temperature range.

Electrical Characteristics on Page 3.

FAIRCHILD
SEMICONDUCTOR

FUNCTIONAL DESCRIPTION

LATCH OPERATION — Data can be entered into the latch when both of the enable inputs are low. As long as this logic condition exists, the output of the latch will follow the input. If either of the enable inputs goes high, the data present in the latch at that time is held in the latch and is no longer affected by data input.

The master reset overrides all other input conditions and forces the outputs of all the latches low when a low signal is applied to the master reset input.

Fig. 4 — TRUTH TABLE

$\overline{MR}$	$\overline{E}_0$	$\overline{E}_1$	D	Q_n	OPERATION
H	L	L	L	L	Data Entry
H	L	L	H	H	Data Entry
H	L	H	X	Q_{n-1}	Hold
H	H	L	X	Q_{n-1}	Hold
H	H	H	X	Q_{n-1}	Hold
L	X	X	X	L	Reset

X = Don't Care
L = Low Voltage Level
H = High Voltage Level
Q_{N-1} = Previous Output State
Q_N = Present Output State

Fig. 5 — LOADING RULES

INPUTS	LOADING
D_0, D_1, D_2, D_3	1.5 U.L.
$\overline{MR}, \overline{E}_0, \overline{E}_1$	1.0 U.L.

OUTPUTS	FAN OUT
Q_0, Q_1, Q_2, Q_3	9 U.L.

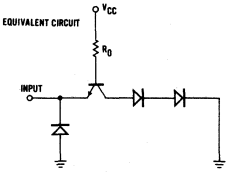
(1 U.L. = 1 TTμL Gate Input Load)

Pin Names:

D_0, D_1, D_2, D_3	Latch Inputs
$\overline{E}_0, \overline{E}_1$	AND Enable (active low) inputs
$\overline{MR}$	Master Reset (active low) input
Q_0, Q_1, Q_2, Q_3	Latch Outputs

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

Fig. 6 — INPUTS



INPUT CURRENT VERSUS INPUT VOLTAGE

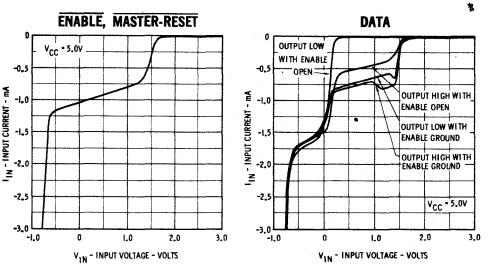
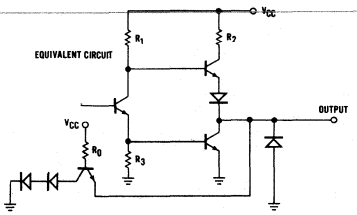


Fig. 7 — OUTPUTS



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE

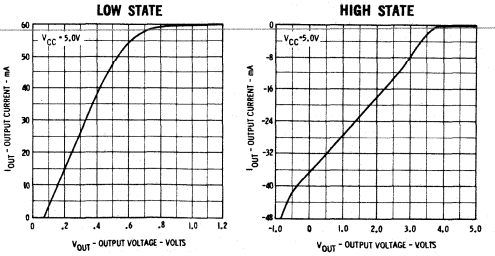


TABLE I —
ELECTRICAL CHARACTERISTICS ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$, See Note 1) (Part #U6N/4M930851X)

SYMBOL	CHARACTERISTIC	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	2.8		2.4		Volts	$V_{CC} = 4.5\ V$, $I_{OH} = -0.6\ mA$ Inputs at threshold voltages (V_{IL} or V_{IH}) (See Note 2)
V_{OL}	Output Low Voltage		0.4		0.21	0.4		0.4	Volts	$V_{CC} = 5.5\ V$, $I_{OL} = 14.4\ mA$ $V_{CC} = 4.5\ V$, $I_{OL} = 11.2\ mA$ Inputs at threshold voltages (V_{IL} or V_{IH}) (See Note 2)
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current $\overline{E_0}$, $\overline{E_1}$ and $\overline{MR}$ Inputs		−1.6		−1.1	−1.6		−1.6	mA	$V_{CC} = 5.5\ V$, $V_F = 0.4\ V$
$1.5\ I_F$	Input Load Current D Inputs		−2.6		−1.9	−2.6		−2.6	mA	$V_{CC} = 5.25\ V$, $V_F = 0.0\ V$ (See Note 3)
I_R	Input Leakage Current $\overline{E_0}$, $\overline{E_1}$ and $\overline{MR}$ Inputs				10	60		60	μA	$V_{CC} = 5.5\ V$, $V_R = 4.5\ V$
$1.5\ I_R$	Input Leakage Current D Inputs				15	90		90	μA	$V_{CC} = 5.5\ V$, $V_R = 4.5\ V$
I_{PD}	Power Supply Current		90		62	90		90	mA	$V_{CC} = 5.0\ V$ all outputs low inputs disabled

TABLE II —
ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0\ V \pm 5\%$, See Note 1) (Part #U6N/4M930859X)

SYMBOL	CHARACTERISTIC	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	3.1		2.4		Volts	$V_{CC} = 4.75\ V$, $I_{OUT} = -0.6\ mA$ Inputs at threshold voltages (V_{IL} or V_{IH}) (See Note 2)
V_{OL}	Output Low Voltage		0.45		0.21	0.45		0.45	Volts	$V_{CC} = 5.25\ V$, $I_{OUT} = 14.4\ mA$ $V_{CC} = 4.75\ V$, $I_{OUT} = 12.7\ mA$ Inputs at threshold voltages (V_{IL} or V_{IH}) (See Note 2)
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current $\overline{E_0}$, $\overline{E_1}$ and $\overline{MR}$ Inputs		−1.6		−1.0	−1.6		−1.6	mA	$V_{CC} = 5.25\ V$, $V_F = 0.45\ V$
$1.5\ I_F$	Input Load Current D Inputs		−2.6		−1.8	−2.6		−2.6	mA	$V_{CC} = 5.25\ V$, $V_F = 0.0\ V$ (See Note 3)
I_R	Input Leakage Current $\overline{E_0}$, $\overline{E_1}$ and $\overline{MR}$ Inputs				10	60		60	μA	$V_{CC} = 5.25\ V$, $V_R = 4.5\ V$
$1.5\ I_R$	Input Leakage Current D Inputs				15	90		90	μA	$V_{CC} = 5.25\ V$, $V_R = 4.5\ V$
I_{PD}	Power Supply Current		117		62	117		117	mA	$V_{CC} = 5.0\ V$ all outputs low inputs disabled

NOTES:
1: Units are pulse tested.
2: Output Voltages are guaranteed for either the input enabled or input disabled case.
3: This current is measured at $V_{IN} = 0.0\ V$ to insure that no current is being absorbed by the device internally. The maximum value given guarantees that the maximum instantaneous current that can flow out of the input at $V_{IN} = 0.4\ V$ is 2.4 mA.

A.C. CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 Volts, Pin 12 = Gnd)

CHARACTERISTIC	LIMITS				UNITS	CONDITIONS
	51 GRADE		59 GRADE			
	MIN.	MAX.	MIN.	MAX.		
t_{pd+} (Enable to Output) t_{pd-}		30 18		35 22	ns	See Figure 8
t_{pd+} (Data to Output) t_{pd-}		20 18		23 20	ns	See Figure 9
t_s "H" (High Data to Enable) t_s "L" (Low Data to Enable)	6.0 10		10 12		ns	See Figure 10 and See Figure 11
t_r "H" (High Data to Enable) t_r "L" (Low Data to Enable)	−4.0	 4.0	−8.0	 2.0	ns	See Figure 10 and See Figure 11
t_{PW} (Enable Pulse Width)	15		18		ns	See Figure 12
t_{PW} (Master Reset Pulse Width)	15		18		ns	See Figure 13
t_{pd-} (Master Reset to Output)		20		22	ns	See Figure 13
t_{rec} (Master Reset Recovery Time)	10		12		ns	See Figure 14

SET UP TIME: t_s is defined as the time required for the logic level to be present at the Data Input prior to the enable transition from Low to High in order for the latch to recognize and store the new data.

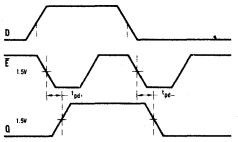
RELEASE TIME: t_r is defined as the time allowed for a new logic level to be present at the data input prior to the enable transition from Low to High in order for the latch not to respond to that new input logic level. A negative release time means the new logic level must not occur until after the enable transition.

RECOVERY TIME: t_{rec} is defined as the time that the Enable must remain Low after the Master Reset transition from Low to High in order for the latch to recognize and store High data.

A.C. CHARACTERISTICS

All delays are measured with V_{CC} = 5.0 V applied to Pin 24 and Pin 12 grounded. The active input is driven by a 9002 TTμL or equivalent gate with the output loaded with 15 pF (includes jig and probe). Outputs under test are loaded with 15 pF (includes jig and probe). Pins not referenced are not connected.

Fig 8 — t_{pd} (ENABLE TO OUTPUT)



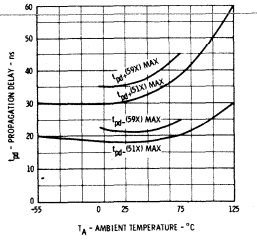
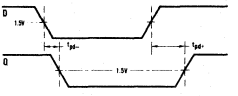
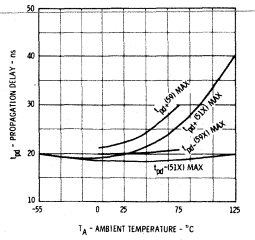


Fig. 9 — t_{pd} (DATA TO OUTPUT)

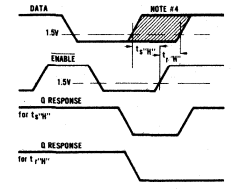


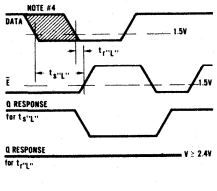
Other Conditions: E = Gnd

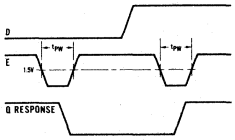


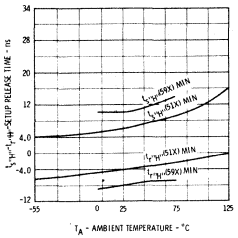
A.C. CHARACTERISTICS

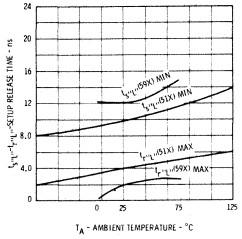
Fig. 10 — $t_{s''H''}$, $t_{r''H''}$ (DATA TO ENABLE) Fig. 11 — $t_{s''L''}$, $t_{r''L''}$ (DATA TO ENABLE) Fig. 12 — t_{PW} (MIN. ENABLE PULSE WIDTH)

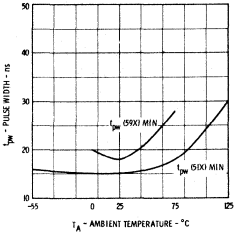






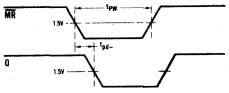






Note 4: If data changes during the shaded time, the state of the output cannot be predetermined.

Fig. 13 — t_{PW} (MIN. MASTER RESET PULSE WIDTH)
t_{pd-} (MASTER RESET TO OUTPUT)



Other Conditions: D = 4.5 V
E = Gnd

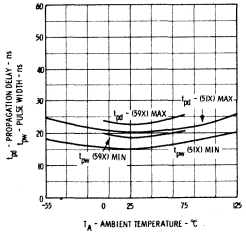
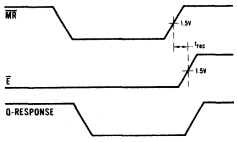
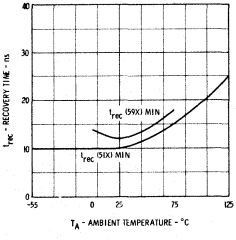


Fig. 14 — t_{rec} (MASTER RESET RECOVERY TIME)



Other Conditions: D = Open



APPLICATIONS

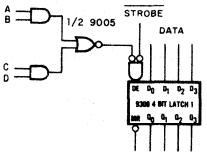


Fig. 15 — AND-OR ENABLE

The figure illustrates the logic for several AND conditions using an AND-OR-NOT Gate. This example shows the logic power of the active low inputs on the AND enable gate.

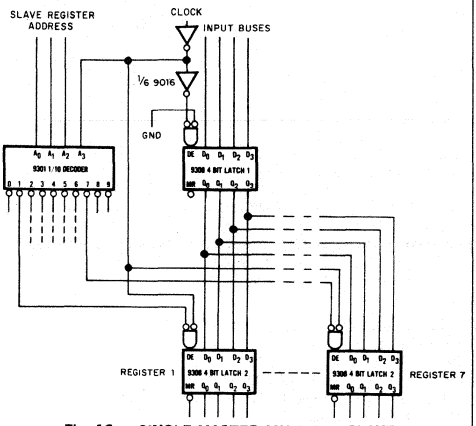


Fig. 16 — SINGLE MASTER MULTIPLE SLAVE FLIP-FLOP SCHEME

One 4-bit latch is acting as the master driving seven 4-bit latches acting as slaves. Which slave the information in the master is transferred to is determined by the 9301 decoder acting as a demultiplexer for the strobe or clock signal.

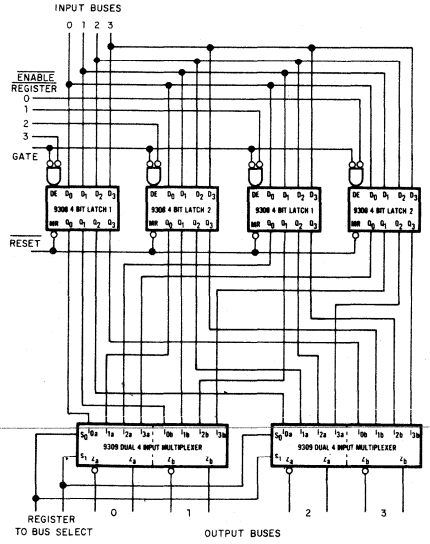


Fig. 17 — DUAL 4-BIT MULTIPLEXER USED TO GATE SELECTED REGISTER TO BUSS

The figure shows four 4-bit registers being switched to the approximate busses under control of the S_0, S_1 inputs of the multiplexer.

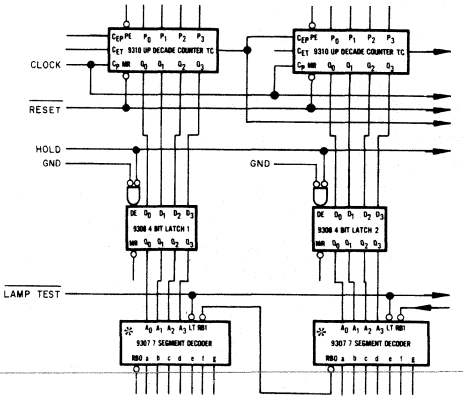


Fig. 18 — LATCH AS HOLDING REGISTER IN COUNTING & DISPLAY APPLICATION

The figure shows two 9310 synchronous decade counters in a typical counter design. At a specified time, the information from the counters is latched into the holding register, where it is held and displayed via the 9307 7-segment decoder until the next sample time.

*The MSI 9317 or MSI 9327 may also be used in this application.

9309

MSI DUAL FOUR-INPUT MULTIPLEXER

A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

GENERAL DESCRIPTION — The 9309 is a monolithic, high speed, dual four-input digital multiplexer circuit, constructed with the Fairchild Planar* epitaxial process. It consists of two multiplexing circuits with common input select logic, each circuit contains four inputs and fully buffered complementary outputs. In addition to operating as a multiplexer, the 9309 can generate any two function of three variables. Active pullups in the outputs ensure high drive and high speed performance. Because of its high speed performance and on-chip select decoding, the 9309 may be cascaded to multiple levels so that any number of lines can be multiplexed onto a single output buss. The circuit uses TTμL for high speed, high fanout operation and is compatible with all other members of the CCSL family of digital integrated circuits.

FEATURES

- **MULTIFUNCTION CAPABILITY**
- **25 ns THROUGH DELAY**
- **ON-CHIP SELECT LOGIC DECODING**
- **FULLY BUFFERED COMPLEMENTARY OUTPUTS**
- **THE INPUT/OUTPUT CHARACTERISTICS PROVIDE EASY INTERFACING WITH FAIRCHILD DTμL, LPDTμL, TTμL, AND MSI FAMILIES (CCSL).**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS.**

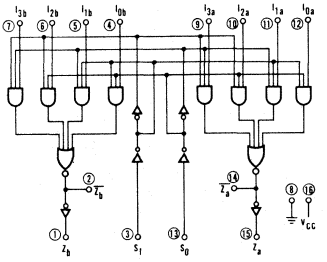
ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7 V
Voltage Applied to Output when output is high	0 V to +V_{CC} value
Input Voltage (DC) (See Note 1)	−0.5 V to +5.5 V
Input Current (DC) (See Note 1)	−30 mA to +5 mA
Current into Output when output is low	+30 mA

Note 1—either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

ORDER INFORMATION — Specify U6B9309XXX for 16-pin Dual In-Line package or U3L9309XXX for 16-pin Flatpak, where XXX is 51X for the −55°C to +125°C temperature range, or 59X for the 0°C to +75°C temperature range.

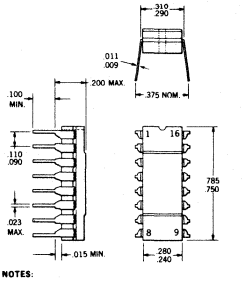
LOGIC DIAGRAM



9309
Dual four input multiplexer
Logic diagram

Fig. 4

DUAL IN-LINE PACKAGE



NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.375) misalignment to facilitate insertion.

Fig. 1

FLAT PACKAGE

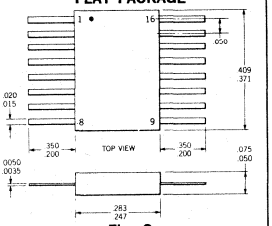


Fig. 2

LOGIC SYMBOL

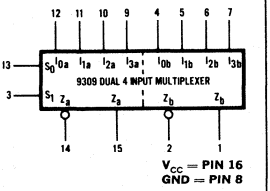


Fig. 3

*Planar is a patented Fairchild process.

FAIRCHILD
SEMICONDUCTOR

FUNCTIONAL DESCRIPTION

The 9309 dual four input multiplexer is a member of the Fairchild family of compatible Medium Scale Integrated (MSI) digital building blocks. It provides this family with the ability to select two bits of either data or control from up to four sources, in one package.

The 9309 dual four input multiplexer is the logical implementation of a two-pole four-position switch, with the position of the switch being set by the logic levels supplied to the two select inputs. Both assertion and negation outputs are provided for both multiplexers. The logic equations for the outputs are shown below:

$Z_a = I_{0a} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1a} \cdot \overline{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \overline{S}_0 + I_{3a} \cdot S_1 \cdot S_0$

$Z_b = I_{0b} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1b} \cdot \overline{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \overline{S}_0 + I_{3b} \cdot S_1 \cdot S_0$

A common use of the 9309 would be the moving of data from a group of registers to a common output buss. The particular register from which the data came would be determined by the state of the select inputs. A less obvious use is as a function generator. The 9309 can generate any two functions of three variables. This is useful for implementing random gating functions.

TRUTH TABLE

SELECT INPUTS		INPUTS				OUTPUTS	
S_0	S_1	I_{0a}	I_{1a}	I_{2a}	I_{3a}	Z_a	$\overline{Z}_a$
L	L	L	X	X	X	L	H
L	L	H	X	X	X	H	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	H	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	H	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	H	L
S_0	S_1	I_{0b}	I_{1b}	I_{2b}	I_{3b}	Z_b	$\overline{Z}_b$
L	L	L	X	X	X	L	H
L	L	H	X	X	X	H	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	H	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	H	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	H	L

L = low voltage level
H = high voltage level
X = either high or low logic level

LOADING RULES

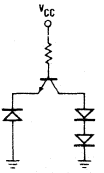
(1 U.L. = 1 TTμL gate input load)

INPUTS	LOADING
I_{0a}, I_{1a}, I_{2a}, I_{3a}, I_{0b}, I_{1b}, I_{2b}, I_{3b}, S_0, S_1	1 U.L.

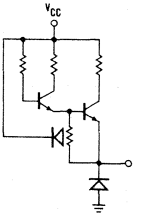
OUTPUTS	FANOUT AT LOGIC LEVEL HIGH	LOW
Z_a, Z_b	20 U.L.	10 U.L.
$\overline{Z}_a$, $\overline{Z}_b$	18 U.L.	9 U.L.

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

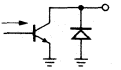
INPUT EQUIVALENT CIRCUIT



OUTPUT EQUIVALENT CIRCUIT (Output High)



OUTPUT EQUIVALENT CIRCUIT (Output Low)



INPUT CURRENT VERSUS INPUT VOLTAGE

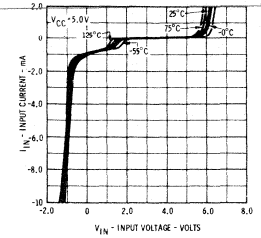


Fig. 5

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)

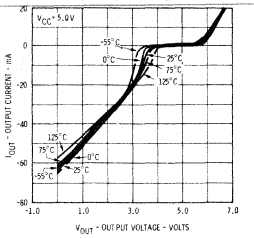


Fig. 6

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)

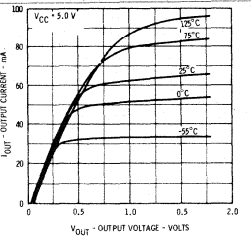


Fig. 7

ELECTRICAL CHARACTERISTICS* ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$) (Part No. UXX930951X)

SYMBOL	CHARACTERISTICS	LIMITS −55°C MIN.	MAX.	+25°C MIN.	TYP.	MAX.	+125°C MIN.	MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	$V_{CC} = 4.5\ V$ $I_{OH} = -1.2$ mA (Pins 1 & 15) $V_{CC} = 4.5\ V$ $I_{OH} = -1.08$ mA (Pins 2 & 14) Inputs at threshold voltages (V_{IL} or V_{IH}) as per truth table
V_{OL}	Output Low Voltage		0.4		0.21	0.4		0.4	Volts	$V_{CC} = 5.5\ V$ $I_{OL} = 16.0$ mA (Pins 1 & 15) $I_{OL} = 14.4$ mA (Pins 2 & 14) $V_{CC} = 4.5\ V$ $I_{OL} = 12.4$ mA (Pins 1 & 15) $I_{OL} = 11.2$ mA (Pins 2 & 14) Inputs at threshold voltages (V_{IL} or V_{IH}) as per truth table
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F (all inputs)	Input Load Current		−1.6		−1.1	−1.6		−1.6	mA	$V_{CC} = 5.5\ V$ $V_F = 0.4\ V$
			−1.24		−.85	−1.24		−1.24	mA	$V_{CC} = 4.5\ V$ Input selected
I_R (all inputs)	Input Leakage Current				15	60		60	μA	$V_{CC} = 5.5\ V$ $V_R = 4.5\ V$ Input not selected
I_{PDH}	V_{CC} Current		40		30	40		40	mA	$V_{CC} = 5.0\ V$ All inputs high
t_{pd+} (S_0 to Z_a)	Switching Speed				24	32			ns	$V_{CC} = 5.0\ V$, $C_L = 15$ pF, See Figure 8
t_{pd-} (S_0 to Z_a)	Switching Speed				24	32			ns	

*Pulse tested

ELECTRICAL CHARACTERISTICS* ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0\ V \pm 5\%$) (Part No. UXX930959X)

SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	MAX.	+25°C MIN.	TYP.	MAX.	+75°C MIN.	MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	$V_{CC} = 4.75\ V$ $I_{OH} = -1.2$ mA (Pins 1 & 15) $V_{CC} = 4.75\ V$ $I_{OH} = -1.08$ mA (Pins 2 & 14) Inputs at threshold voltages (V_{IL} or V_{IH}) as per truth table
V_{OL}	Output Low Voltage		0.45		0.21	0.45		0.45	Volts	$V_{CC} = 5.25\ V$ $I_{OL} = 16.0$ mA (Pins 1 & 15) $I_{OL} = 14.4$ mA (Pins 2 & 14) $V_{CC} = 4.75\ V$ $I_{OL} = 14.1$ mA (Pins 1 & 15) $I_{OL} = 12.7$ mA (Pins 2 & 14) Inputs at threshold voltages (V_{IL} or V_{IH}) as per truth table
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F (all inputs)	Input Load Current		−1.6		−1.0	−1.6		−1.6	mA	$V_{CC} = 5.25\ V$ $V_F = 0.45\ V$
			−1.41		−.91	−1.41		−1.41	mA	$V_{CC} = 4.75\ V$ Input selected
I_R (all inputs)	Input Leakage Current				15	60		60	μA	$V_{CC} = 5.25\ V$ $V_R = 4.5\ V$ Input not selected
I_{PDH}	V_{CC} Current		43		30	43		43	mA	$V_{CC} = 5.0\ V$ All inputs high
t_{pd+} (S_0 to Z_a)	Switching Speed				24	36			ns	$V_{CC} = 5.0\ V$, $C_L = 15$ pF, See Figure 8
t_{pd-} (S_0 to Z_a)	Switching Speed				24	36			ns	

*Pulse tested

A.C. CHARACTERISTICS

SWITCHING WAVEFORMS

All inputs are outputs of TTμL 9000 series gates loaded with 15 pF. All outputs are loaded with the same capacitance (referred to as C_L) and only with capacitance.

t_{pd}; S_0 to Z_a
CONDITIONS
Pins 3, 12 = GND.
Pin 11 = V_{CC}

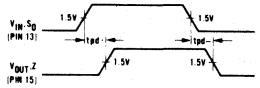


Fig. 8

t_{pd}; S_0 to $\overline{Z}_a$
CONDITIONS
Pins 3, 12 = GND.
Pin 11 = V_{CC}

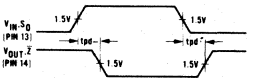


Fig. 9

t_{pd}; I_{a0} to $\overline{Z}_a$
CONDITIONS
Pins 3, 13 = GND.

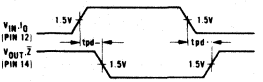


Fig. 10

SWITCHING CHARACTERISTICS

TURN OFF DELAY TIME VERSUS AMBIENT TEMPERATURE (S_0 to Z_a)

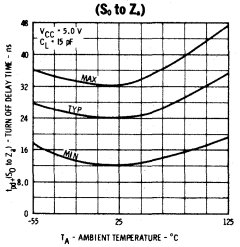


Fig. 11

TURN ON DELAY TIME VERSUS TEMPERATURE (S_0 to Z_a)

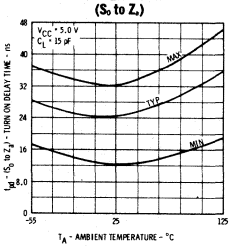


Fig. 12

TURN OFF DELAY TIME VERSUS AMBIENT TEMPERATURE (I_{0a} to $\overline{Z}_a$)

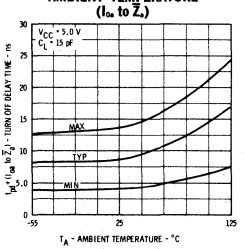


Fig. 13

TURN ON DELAY TIME VERSUS AMBIENT TEMPERATURE (I_{0a} to $\overline{Z}_a$)

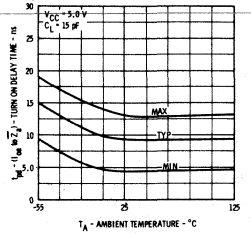


Fig. 14

TURN OFF DELAY TIME VERSUS AMBIENT TEMPERATURE (S_0 to $\overline{Z}_a$)

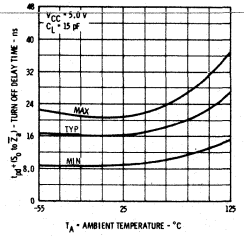


Fig. 15

TURN ON DELAY TIME VERSUS AMBIENT TEMPERATURE (S_0 to $\overline{Z}_a$)

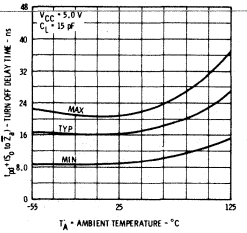


Fig. 16

APPLICATIONS

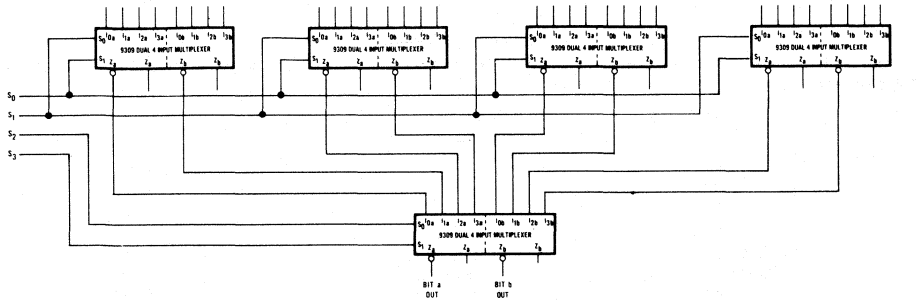
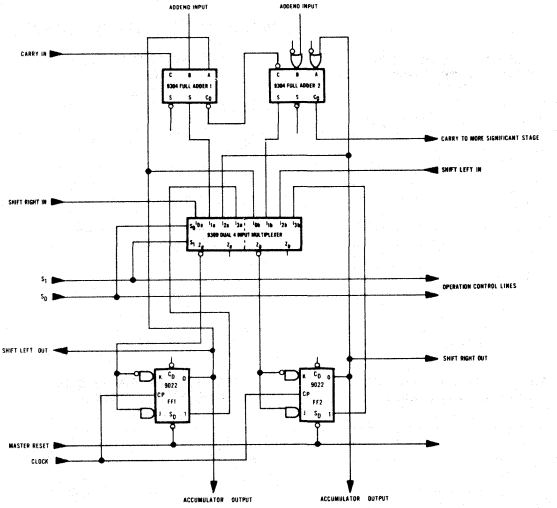


Fig. 12 — MULTIPLEXING TWO BITS FROM SIXTEEN SOURCES

This diagram shows the interconnection of five 9309 dual four bit multiplexers to provide switching of two bits of data from one of sixteen words onto a two bit data buss. The selection of which word will be transferred to the buss is made by the address supplied to the S_0, S_1, S_2 and S_3 inputs. As an example: if twelve bit words are to be transferred to a twelve bit buss, the above diagram would be repeated six times. Notice that the negative outputs are used at both levels resulting in the assertion output (negation of the negation) at a higher speed due to the fact that the through delay is less on the negation output.

If the word selecting address is held in four TTμL flip flops (two dual packages) enough load capability is available to select between sixteen, sixteen bit words.



OPERATION CODE LIST

S_0	S_1	INSTRUCTION
0	0	SHIFT LEFT
1	0	ADD
0	1	SHIFT RIGHT
1	1	COMPLEMENT

H = "1", L = "0"

Fig. 13 — GENERAL PURPOSE ACCUMULATOR

A fast, general purpose accumulator for computer applications is capable of: 1) shift left; 2) add; 3) shift right and 4) complement operations. Only three packages are required to construct two stages of the general purpose accumulator shown above.

The D input capability of the 9022 is utilized here to allow each flip flop of the accumulator to accept the data as presented by the 9309 multiplexer.

Under the operation code instructions the multiplexer provides an input to the 9022 from: 1) adjacent stage to the right for a shift left operation; 2) adjacent stage to the left for a shift right operation; 3) output of adders for add operation and 4) $\overline{Q}$ outputs of 9022 for the complement operation. The operation code at the right of Figure 13 shows the instruction codes to perform the various operations.

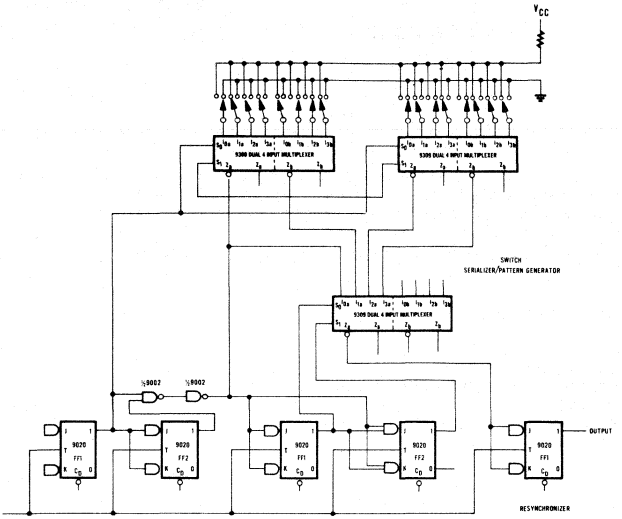
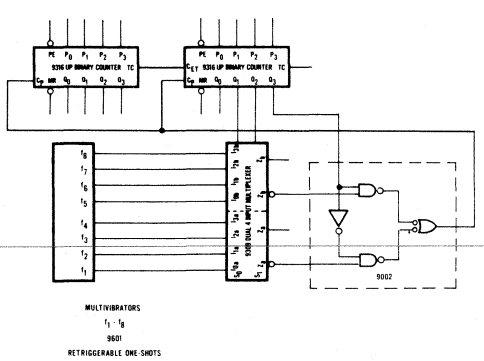


Fig. 14 — 16-BIT PATTERN GENERATOR

This application illustrates the use of 9309 and 9020 in the design of one channel of a 16 bit pattern generator. Each channel requires ½ 9020, ½ 9002 and 2½ 9309. Each channel consists of a switch serializer/pattern generator and resynchronizer sections with a modulo 16 binary counter common to all channels.

The two least significant bits and two most significant bits of the counter control the first and second stages of multiplexing respectively. In this manner four bits are multiplexed on each of the four lines from the first stage to the second stage. Every four clock times a new input line containing four multiplexed bits is selected by the second stage of the serializer thus serializing the 16 input bits from the switches.

The resynchronizer flip flop is used to eliminate decoding spikes.



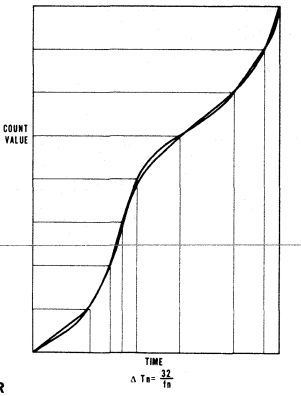


Fig. 15 — NON-LINEAR COUNTER

The rate of the non-linear counter depends on the multivibrator clock frequency selected under control of the three most significant bits of the counter. This makes the count rate a function of both the count value of counter and frequency of clock multivibrator selected.

Clock multiplexing is accomplished by a 9309 dual 4-input multiplexer and one 9002 quad gate. Eight line segments representing clock rates of the multivibrators may be adjusted in slope to approximate a non-linear function.

9310

MSI BCD DECADE COUNTER

A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

GENERAL DESCRIPTION — The 9310 is a high speed synchronous 8421 BCD decade counter. It is a synchronously presetable, multifunctional MSI building block useful in a large number of counting, digital integration, and conversion applications. Several decades of synchronous operation are obtainable with no external gating packages required through an internal carry look-ahead counting technique.

FEATURES:

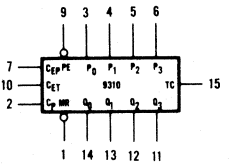
- **SYNCHRONOUS COUNTING AND PARALLEL ENTRY**
- **DECODED TERMINAL COUNT**
- **BUILT-IN CARRY CIRCUITRY**
- **TYPICAL POWER DISSIPATION OF 300 mW**
- **THE INPUT/OUTPUT CHARACTERISTICS PROVIDE EASY INTERFACING WITH FAIRCHILD DTμL, LPDTμL, AND TTμL FAMILIES (CCSL).**
- **ALL CERAMIC HERMETIC 16 PIN DUAL IN-LINE PACKAGE AND FLAT PACKAGE**
- **INPUT DIODE CLAMPING**

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7 V
Voltage Applied to Outputs for high output state	−0.5 V to V_{CC} value
Input Voltage (D.C.)	−0.5 V to +5.5 V

ORDER INFORMATION — Specify U6B9310XXX for 16-pin Dual In-Line Package, U3L9310XXX for 16-pin Flat Package where XXX is 51X for the −55°C to +125°C temperature range, or 59X for the 0°C to 75°C temperature range.

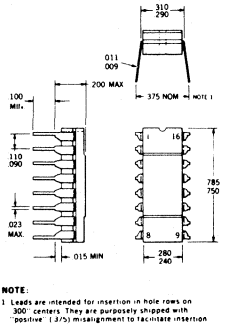
LOGIC DIAGRAM



V_{CC} = Pin 16
Gnd = Pin 8

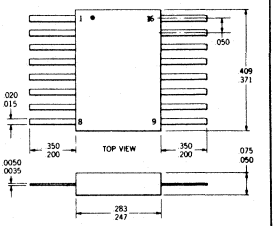
PHYSICAL DIMENSIONS

DUAL IN-LINE PACKAGE



NOTE:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.3/.5) misalignment to facilitate insertion.

FLAT PACKAGE



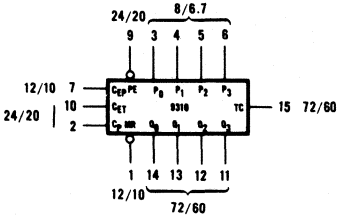
FAIRCHILD
SEMICONDUCTOR

FUNCTIONAL DESCRIPTION — A clock buffer and inverter drives the four clocked RS master-slave flip flops in parallel, so that synchronous operation is obtained. When the clock input (CP) is low, the slave is steady, but data can enter the master via the R and the S inputs. During the low to high transition of CP, first the data inputs (R and S) are inhibited, so that a later change in the input data will not affect the master; secondly, the now trapped information in the master is transferred to the slave and is reflected at the outputs. When the transfer is completed both the master and the slave are steady as long as the clock input remains high, and regardless of the logic state at any other input to the device. During the high to low transition of the clock input, first the transfer path from master to slave are inhibited, leaving the slave steady in its present state, secondly, the data inputs (R and S) are enabled so that new data can enter the master. As a result of this synchronous operation higher clock frequency is possible and much less external logic is required in most applications. Some restrictions are placed on the manner of selection. First, the transition of CEP or CET from high to low or of PE from low to high may only be done when CP is high. The remaining transitions may be made by following the setup and release times specified under "Switching Characteristics." The asynchronous MR clears the counter independent of any other input.

Note: CE (count enable) = CEP • CET
TC = CET • Q_0 • Q_1 • Q_2 • Q_3

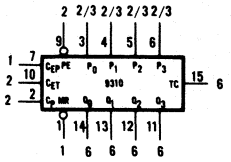
LOADING RULES

CCSL LOAD AND DRIVE FACTORS



V_{CC} = Pin 16
Gnd = Pin 8

TTμL LOAD AND DRIVE FACTORS



V_{CC} = Pin 16
Gnd = Pin 8

(1 U.L. = 1 TTμL input gate load)

ELECTRICAL CHARACTERISTICS (T_A = −55°C to +125°C, V_{CC} = 5.0 V ±10%)

SYMBOL	CHARACTERISTICS	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS & COMMENTS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	V_{CC} = 4.5 V, I_{OH} = −0.36 mA
V_{OL}	Output Low Voltage		0.4		0.2	0.4		0.4	Volts	V_{CC} = 5.5 V, I_{OL} = 9.6 mA V_{CC} = 4.5 V, I_{OL} = 7.44 mA
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current MR, CEP		−1.6		−1.0	−1.6		−1.6	mA	
2 I_F	Input Load Current CP, PE, CET		−3.2		−2.0	−3.2		−3.2	mA	V_{CC} = 5.5 V V_F = 0.4 V
⅔ I_F	Input Load Current P_0, P_1, P_2, P_3		−1.07		−0.7	−1.07		−1.07	mA	
I_R	Input Leakage Current MR, CEP		60		10	60		60	μA	
2 I_R	Input Leakage Current CP, PE, CET		120		20	120		120	μA	V_{CC} = 5.5 V V_R = 4.5 V
⅔ I_R	Input Leakage Current P_0, P_1, P_2, P_3		40		7.0	40		40	μA	

ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0\ V \pm 5\%$)

SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	CONDITIONS & COMMENTS
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	$V_{CC} = 4.75\ V$, $I_{OH} = -0.36\ mA$
V_{OL}	Output Low Voltage		0.45		0.2	0.45		0.45	Volts	$V_{CC} = 5.25\ V$, $I_{OL} = 9.6\ mA$ $V_{CC} = 4.75\ V$, $I_{OL} = 8.5\ mA$
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current MR, CEP		−1.6		−1.0	−1.6		−1.6	mA	
$2\ I_F$	Input Load Current CP, PE, CET		−3.2		−2.0	−3.2		−3.2	mA	$V_{CC} = 5.25\ V$ $V_F = 0.4\ V$
$^2/_3 I_F$	Input Load Current P_0, P_1, P_2, P_3		−1.07		−0.7	−1.07		−1.07	mA	
I_R	Input Leakage Current MR, CEP		60		10	60		60	μA	
$2\ I_R$	Input Leakage Current CP, PE, CET		120		20	120		120	μA	$V_{CC} = 5.25\ V$ $V_R = 4.5\ V$
$^2/_3 I_R$	Input Leakage Current P_0, P_1, P_2, P_3		40		7.0	40		40	μA	

SWITCHING CHARACTERISTICS ($T_A = 25°C$)

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	CONDITIONS & COMMENTS
t_{pd+} (Q)	Turn-Off Delay		20		ns	$V_{CC} = 5.0\ V$ $C_L = 15\ pF$ (Fig. 1)
t_{pd-} (Q)	Turn-On Delay		15		ns	
t_{pd+} (TC)	Turn-Off Delay for TC		35		ns	
t_{pd-} (TC)	Turn-On Delay for TC		20		ns	
t_s (SE)	Set-Up Time for CE		14		ns	$V_{CC} = 5.0\ V$ $C_L = 15\ pF$ (Fig.2)
t_r (CE)	Release Time for CE		12		ns	
t_s	Set-Up Time for Data		18		ns	$V_{CC} = 5.0\ V$ $C_L = 15\ pF$ (Fig. 3)
t_r	Release Time for Data		17		ns	
t_s (PE)	Set-Up Time for PE		30		ns	
t_r (PE)	Release Time for PE		28		ns	
t_{pd-} (MR)	Turn-On Delay for MR		33		ns	$V_{CC} = 5.0\ V$, $C_L = 15\ pF$ (Fig. 4)
$t_{P\pm}$	Propagation Delay for CET to TC		14		ns	$V_{CC} = 5.0\ V$, $C_L = 15\ pF$ (Fig. 5)

SET-UP TIME: t_s is defined as the minimum time required for the logic level to be present at the logic input prior to the clock transition from low to high in order for the flip-flop(s) to respond.

RELEASE TIME: t_r is defined as the maximum time allowed for the logic level to be present at the logic input prior to the clock transition from low to high in order for the flip-flop(s) not to respond.

SWITCHING TIME WAVEFORMS

Fig. 1

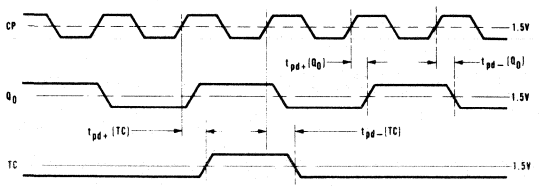


Fig. 2

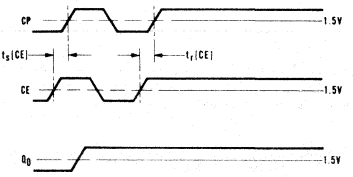


Fig. 3

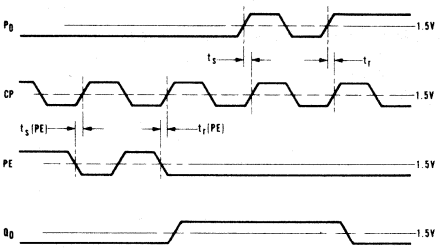


Fig. 4

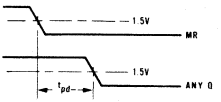
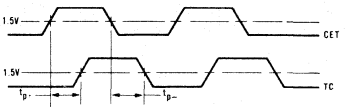
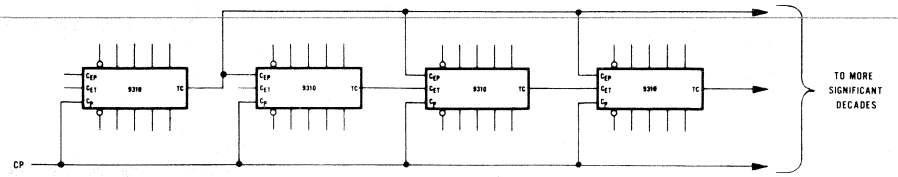


Fig. 5



APPLICATIONS



SYNCHRONOUS COUNTING SCHEME

9311

MSI ONE-OF-SIXTEEN DECODER

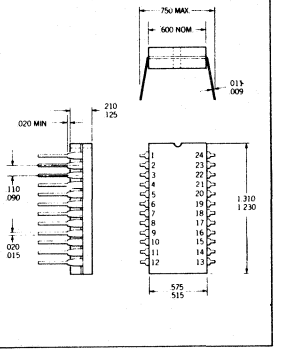
A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

GENERAL DESCRIPTION — The 9311 is a multi-purpose decoder designed to accept four inputs and provide 16 mutually exclusive outputs. The circuit uses TTμL for high speed and high fan-out capability, and is compatible with all members of the CCSL group of digital integrated circuits.

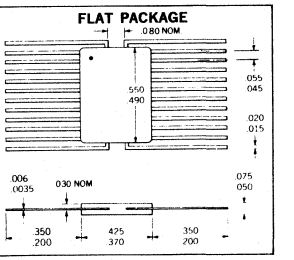
FEATURES:

- **MULTI-FUNCTION CAPABILITY**
- **MUTUALLY EXCLUSIVE OUTPUTS**
- **GUARANTEED FANOUT OF 10 TTμL LOADS OVER THE FULL TEMPERATURE RANGE AND SUPPLY VOLTAGE RANGES**
- **HIGH CAPACITIVE DRIVE CAPABILITY**
- **DEMULTIPLEXING CAPABILITY**
- **TYPICAL POWER DISSIPATION OF 175 mW**
- **THE INPUT/OUTPUT CHARACTERISTICS PROVIDE EASY INTERFACING WITH FAIRCHILD DTμL, LPDTμL AND TTμL FAMILIES (CCSL).**
- **ALL CERAMIC "HERMETIC" 24-PIN DUAL IN-LINE PACKAGE**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED LINE TERMINATION EFFECTS**
- **TWO INPUT ENABLE GATE**

DUAL IN-LINE PACKAGE



FLAT PACKAGE



ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7 V
Voltage Applied to Outputs for high output state	−0.5 V to +V_{CC} value
Input Voltage (D.C.)	−0.5 V to +5.5 V

ORDER INFORMATION

Specify U6N9311XXX for 24-pin Dual In-Line package or U3M9311XXX for 24-pin Flat Package where XXX is 51X for the −55°C to +125°C temperature range, or 59X for the 0°C to +75°C temperature range.

LOGIC SYMBOL

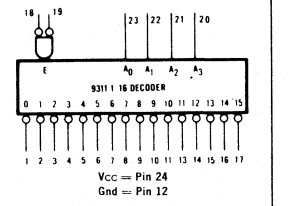


Fig. 1

FAIRCHILD SEMICONDUCTOR

FUNCTIONAL DESCRIPTION — The 9311 decoder accepts four active high BCD inputs and provides 16 mutually exclusive active low outputs, as shown by Figure 1. The active low outputs facilitate memory addressing when inverting drivers are used between decoder and memory elements such as the 9033.
The most significant A_3 input produces a useful inhibit function when the 9311 is used as a 1 out of 8 decoder.

The Truth Table and Loading Rules for the 9311 are shown in Table I and Table II.

TABLE I — TRUTH TABLE

Eo	EI	A_0	A_1	A_2	A_3	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L

H = High Voltage Level
L = Low Voltage Level
X = Level Does Not Affect Output

TABLE II
TTμL INPUT LOAD AND DRIVE FACTORS

INPUTS	LOADING
All Inputs	1 U.L.

OUTPUTS	DRIVE FACTOR
All Outputs	10 U.L.

(1 U.L. = TTμL Gate Input Load)

CCSL INPUT LOAD AND DRIVE FACTORS

GRADE	INPUTS	LOADING
59	All Inputs	12/11
51	All Inputs	12/10

GRADE	OUTPUTS	DRIVE FACTOR
59	All Outputs	120/94
51	All Outputs	120/78

TABLE III —
ELECTRICAL CHARACTERISTICS ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$) (Part #UXX931151X) See Note 1

SYMBOL	CHARACTERISTICS	LIMITS						UNITS	CONDITIONS
		−55°C		+25°C			+125°C		
		MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	$V_{CC} = 4.5\ V$, $I_{OH} = -0.6\ mA$
V_{OL}	Output Low Voltage		0.4		0.2	0.4		0.4	Volts	$V_{CC} = 4.5\ V$, $I_{OL} = 12.4\ mA$ $V_{CC} = 5.5\ V$, $I_{OL} = 16.0\ mA$
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		−1.6		−1.10	−1.6		−1.6	mA	$V_{CC} = 5.5\ V$, $V_F = 0.4\ V$
			−1.24		−0.97	−1.24		−1.24	mA	$V_{CC} = 4.5\ V$
I_R	Input Leakage Current				15	60		60	μA	$V_{CC} = 5.5\ V$, $V_R = 4.5\ V$
I_{PD}	V_{CC} Current				35	55			mA	$V_{CC} = 5.0\ V$
t_{pd+}	Turn Off Delay A Input to Output				23	35			ns	$V_{CC} = 5.0\ V$ $C_L = 15\ pF$ See Fig. 8
t_{pd-}	Turn On Delay A Input to Output				20	30			ns	
t_{pd+}	Turn Off Delay E Input to Output				17	26			ns	
t_{pd-}	Turn On Delay E Input to Output				16	21			ns	

Note 1: Units are pulse tested.

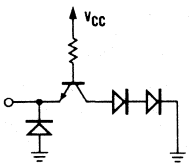
TABLE IV —
ELECTRICAL CHARACTERISTICS (T_A = 0°C to +75°C, V_{CC} = 5.0 V ±5%) (Part #UXX931159X) See Note 1

SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	0°C MAX.	+25°C MIN.	+25°C TYP.	+25°C MAX.	+75°C MIN.	+75°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	V_{CC} = 4.75 V, I_{OH} = −0.6 mA
V_{OL}	Output Low Voltage		0.45		0.2	0.45		0.45	Volts	V_{CC} = 4.75 V, I_{OL} = 14.1 mA
										V_{CC} = 5.25 V, I_{OL} = 16.0 mA
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		−1.6		−1.0	−1.6		−1.6	mA	V_{CC} = 5.25 V, V_F = 0.45 V
			−1.41		−0.9	−1.41		−1.41	mA	V_{CC} = 4.75 V
I_R	Input Leakage Current				15	60		60	μA	V_{CC} = 5.25 V, V_R = 4.5 V
I_{PD}	V_{CC} Current				35	60			mA	V_{CC} = 5.0 V
t_{pd+}	Turn Off Delay A Input to Output			10	23	40			ns	V_{CC} = 5.0 V, C_L = 15 pF, See Fig. 8
t_{pd-}	Turn On Delay A Input to Output			7.0	20	35			ns	
t_{pd+}	Turn Off Delay E Input to Output			10	17	31			ns	
t_{pd-}	Turn On Delay E Input to Output			7.0	17	26			ns	

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

INPUTS

EQUIVALENT CIRCUIT



INPUT CURRENT VERSUS INPUT VOLTAGE

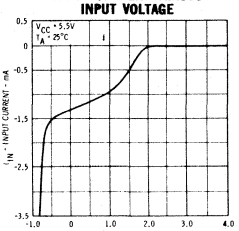
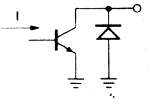


Fig. 3

OUTPUTS

EQUIVALENT CIRCUIT

OUTPUT LOW



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE OUTPUT LOW

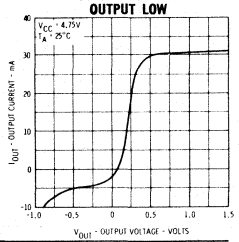
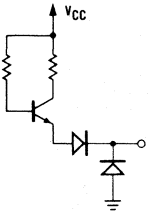


Fig. 4

OUTPUT HIGH



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE OUTPUT HIGH

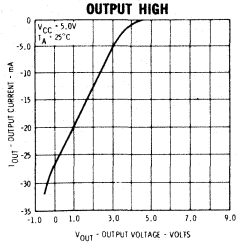


Fig. 5

SWITCHING PERFORMANCE

TYPICAL TURN ON DELAY VERSUS TEMPERATURE

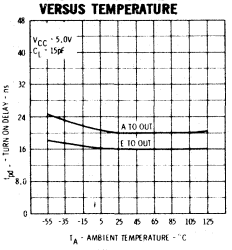


Fig. 6

TYPICAL TURN OFF DELAY VERSUS TEMPERATURE

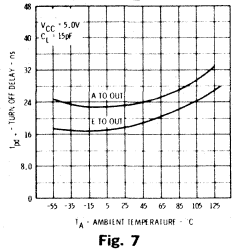
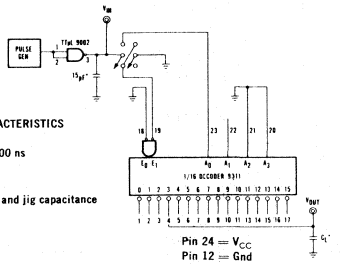
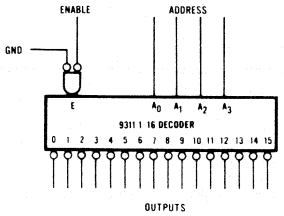


Fig. 7



PULSE GEN CHARACTERISTICS
Freq. ≈ 1 MHz
Pulse Width ≈ 100 ns
$t_r = t_f \leq 15$ ns
Amplitude ≈ 4 V
*Includes all probe and jig capacitance

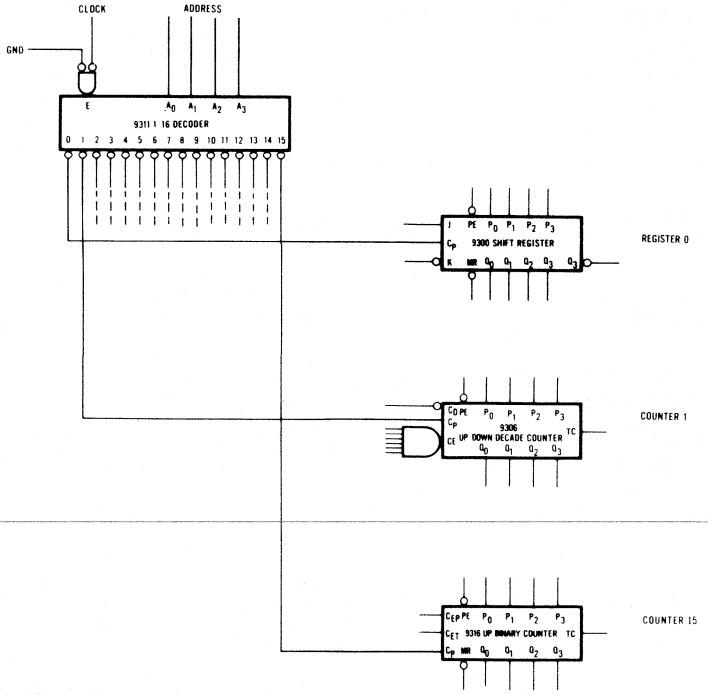
Fig. 8 — SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



DECIMAL DIGIT	OUTPUT SELECTION			
	BCD CODE			
	8421	5421	EXCESS 3	GRAY
0	0	0	3	0
1	1	1	4	1
2	2	2	5	3
3	3	3	6	2
4	4	4	7	6
5	5	8	8	7
6	6	9	9	5
7	7	10	10	4
8	8	11	11	12
9	9	12	12	13

DECODE ANY BCD CODE

Decode any BCD code using a 9311 element. Any 4 bit BCD code may be decoded by selecting outputs, examples are shown in the table.



CLOCK DEMULTIPLEXING

The 9311 can be used as a clock demultiplexer. The binary address designates to which register or counter the clock is sent. Up to 5 register counter stages can be driven by one decoder output allowing word lengths of 20 bits to be controlled. Any sequential circuit in the 9300 MSI family can be used in this configuration.

9312

MSI EIGHT-INPUT MULTIPLEXER

A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

GENERAL DESCRIPTION — The 9312 is a monolithic, high speed, eight input digital multiplexer circuit. It provides in one package the ability to select one bit of data from up to eight sources. The 9312 can be used as a universal function generator to generate any logic function of four variables. Both assertion and negation outputs are provided. TTμL circuitry with active pullups on the outputs provides high speed, high fanout operation and is compatible with all other members of the CCSL family of digital integrated circuits.

- **MULTIFUNCTION CAPABILITY**
- **25 ns THROUGH DELAY**
- **ON-CHIP SELECT LOGIC DECODING**
- **FULLY BUFFERED COMPLEMENTARY OUTPUTS**
- **THE INPUT/OUTPUT CHARACTERISTICS PROVIDE EASY INTERFACING WITH FAIRCHILD DTμL, LPDTμL, TTμL, AND MSI FAMILIES (CCSL).**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS.**

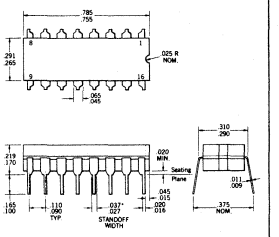
ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7 V
Voltage applied to output when output is high	0 V to +V_{CC} value
Input Voltage (DC) (See Note 1)	−0.5 V to +5.5 V
Input Current (DC) (See Note 1)	−30 mA to +5 mA
Current into output when output is low	+30 mA

Note 1: Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

ORDER INFORMATION — Specify U7B9312XXX for 16-pin Dual In-Line package or U4L9312XXX for 16-pin Flatpak, where XXX is 51X for the −55°C to +125°C temperature range, or 59X for the 0°C to +75°C temperature range.

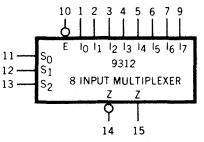
DUAL IN-LINE PACKAGE



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers.
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020" diameter lead
Leads are tin-plated kovar
Package weight is 2.2 grams
*The .027 dimension does not apply to the corner leads

Fig. 1

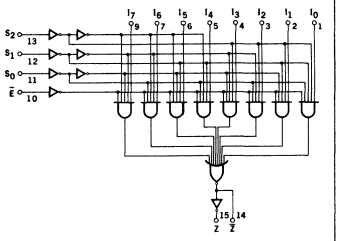
LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

Fig. 2

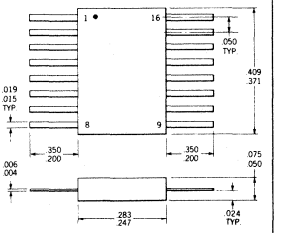
LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8

Fig. 3

FLAT PACKAGE



NOTES:
All dimensions in inches
Leads are gold-plated kovar
Package weight is 0.4 gram

Fig. 4

FAIRCHILD
SEMICONDUCTOR

FUNCTIONAL DESCRIPTION — The 9312 is a logical implementation of a single pole - 8 position switch with the switch position controlled by the state of three select inputs, S_0, S_1, S_2. Both assertion and negation outputs are provided. The enable input ($\overline{E}$) is active low. When it is not activated the negation output is high and the assertion output is low regardless of all other inputs. The logic function provided at the output is:

$Z = E \cdot (I_0 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot \overline{S}_2 + I_1 \cdot S_0 \cdot \overline{S}_1 \cdot \overline{S}_2 + I_2 \cdot \overline{S}_0 \cdot S_1 \cdot \overline{S}_2 + I_3 \cdot S_0 \cdot S_1 \cdot \overline{S}_2 + I_4 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot S_2 + I_5 \cdot S_0 \cdot \overline{S}_1 \cdot S_2 + I_6 \cdot \overline{S}_0 \cdot S_1 \cdot S_2 + I_7 \cdot S_0 \cdot S_1 \cdot S_2)$.

The 9312 provides the ability, in one package, to select from eight sources of data or control information. By proper manipulation of the inputs, the 9312 can provide any logic function of four variables and its negation. Thus any number of random logic elements used to generate unusual truth tables can be replaced by one 9312.

TRUTH TABLE

$\overline{E}$	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	$\overline{Z}$	Z
H	X	X	X	X	X	X	X	X	X	X	X	H	L
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

H = High voltage level
L = Low voltage level
X = Level does not affect output

Fig. 5

LOADING RULES

INPUTS	LOADING
All Inputs	1 U.L.

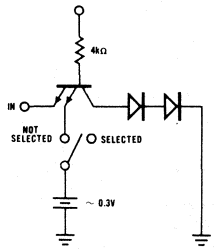
OUTPUTS	FAN-OUT	
	High State	Low State
$\overline{Z}$	18	9
Z	20	10

1 U.L. = 1 TTμL Unit Load
1 U.L. is defined by the entries I_R and I_F in the table on page 3.

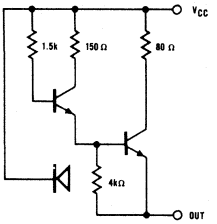
Fig. 6

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

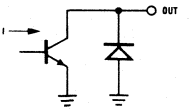
EQUIVALENT INPUT CIRCUIT



OUTPUT HIGH EQUIVALENT CIRCUIT



OUTPUT LOW EQUIVALENT CIRCUIT



INPUT CURRENT VERSUS INPUT VOLTAGE

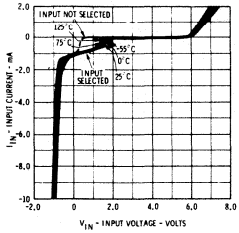


Fig. 7

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)

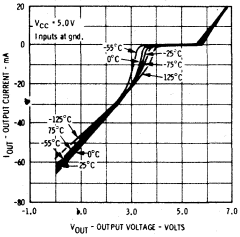


Fig. 8

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)

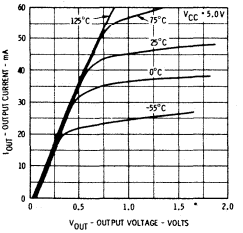


Fig. 9

ELECTRICAL CHARACTERISTICS* ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$) (Part No. UXX931251X)

SYMBOL	CHARACTERISTICS	LIMITS −55°C MIN.	MAX.	+25°C MIN.	TYP.	MAX.	+125°C MIN.	MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	$V_{CC} = 4.5\ V$ $I_{OH} = -1.2$ mA (Pin 15) $V_{CC} = 4.5\ V$ $I_{OH} = -1.08$ mA (Pin 14) Inputs at threshold voltages (V_{IL} or V_{IH}) as per truth table
V_{OL}	Output Low Voltage		0.4		0.21	0.4		0.4	Volts	$V_{CC} = 5.5\ V$ $I_{OL} = 16.0$ mA (Pin 15) $I_{OL} = 14.4$ mA (Pin 14) $V_{CC} = 4.5\ V$ $I_{OL} = 12.4$ mA (Pin 15) $I_{OL} = 11.2$ mA (Pin 14) Inputs at threshold voltages (V_{IL} or V_{IH}) as per truth table
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F (all inputs)	Input Load Current		−1.6		−1.1	−1.6		−1.6	mA	$V_{CC} = 5.5\ V$ $V_F = 0.4\ V$
			−1.24		−0.85	−1.24		−1.24	mA	$V_{CC} = 4.5\ V$ Input Selected
I_R (all inputs)	Input Leakage Current				15	60		60	μA	$V_{CC} = 5.5\ V$ $V_R = 4.5\ V$ Input not selected
I_{PDH}	V_{CC} Current	40			27	40		40	mA	$V_{CC} = 5.0\ V$
t_{pd+} (S_0 to Z)	Switching Speed				23	34			ns	$V_{CC} = 5.0\ V$, See Page 4
t_{pd-} (S_0 to Z)	Switching Speed				25	36			ns	$C_L = 15$ pF

*Pulse tested

ELECTRICAL CHARACTERISTICS* ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0\ V \pm 5\%$) (Part No. UXX931259X)

SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	MAX.	+25°C MIN.	TYP.	MAX.	+75°C MIN.	MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	$V_{CC} = 4.75\ V$ $I_{OH} = -1.2$ mA (Pin 15) $V_{CC} = 4.75\ V$ $I_{OH} = -1.08$ mA (Pin 14) Inputs at threshold voltages (V_{IL} or V_{IH}) as per truth table
V_{OL}	Output Low Voltage		0.45		0.21	0.45		0.45	Volts	$V_{CC} = 5.25\ V$ $I_{OL} = 16.0$ mA (Pin 15) $I_{OL} = 14.4$ mA (Pin 14) $V_{CC} = 4.75\ V$ $I_{OL} = 14.1$ mA (Pin 15) $I_{OL} = 12.7$ mA (Pin 14) Inputs at threshold voltages (V_{IL} or V_{IH}) as per truth table
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F (all inputs)	Input Load Current		−1.6		−1.0	−1.6		−1.6	mA	$V_{CC} = 5.25\ V$ $V_F = 0.45\ V$
			−1.41		−0.91	−1.41		−1.41	mA	$V_{CC} = 4.75\ V$ Input Selected
I_R (all inputs)	Input Leakage Current				15	60		60	μA	$V_{CC} = 5.25\ V$ $V_R = 4.5\ V$ Input not selected
I_{PDH}	V_{CC} Current	43			27	43		43	mA	$V_{CC} = 5.0\ V$
t_{pd+} (S_0 to Z)	Switching Speed				23	34			ns	$V_{CC} = 5.0\ V$, See Page 4
t_{pd-} (S_0 to Z)	Switching Speed				25	36			ns	$C_L = 15$ pF

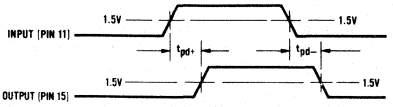
*Pulse tested

A.C. CHARACTERISTICS

A.C. CHARACTERISTICS

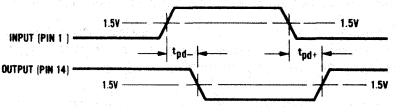
All measurements are made with $V_{CC} = 5.0$ V applied to pin 16 and with pin 8 grounded. The active input is driven by a 9002 TTμL gate with the output loaded with 15 pF. Both outputs of the 9312 are loaded with 15 pF.

t_{pd}: S_0 to Z



Other Conditions: Pins 1, 8, 10, 12, 13 = Gnd
Pin 2 = V_{CC} through 1.0 kΩ
Pin 16 = V_{CC}

t_{pd}: I_0 to $\overline{Z}$



Other Conditions: Pins 8, 10, 11, 12, 13 = Gnd
Pin 16 = V_{CC}

TURN OFF DELAY VERSUS AMBIENT TEMPERATURE; S_0 to Z

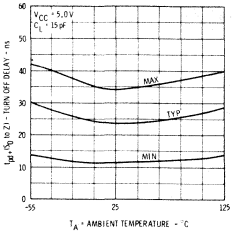


Fig. 10

TURN ON DELAY VERSUS AMBIENT TEMPERATURE; S_0 to Z

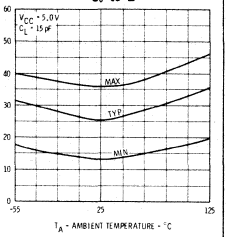


Fig. 11

TURN OFF DELAY VERSUS AMBIENT TEMPERATURE; I_0 to $\overline{Z}$

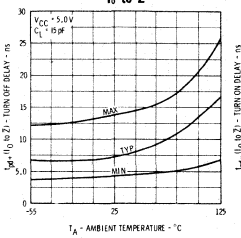


Fig. 12

TURN ON DELAY VERSUS AMBIENT TEMPERATURE; I_0 to $\overline{Z}$

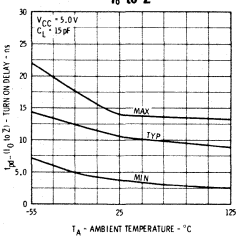
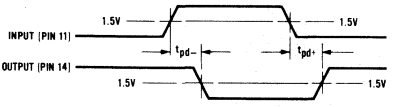


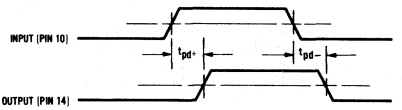
Fig. 13

t_{pd}: S_0 to $\overline{Z}$



Other Conditions: Pins 1, 8, 10, 12, 13 = Gnd
Pin 2 = V_{CC} through 1.0 kΩ
Pin 16 = V_{CC}

t_{pd}: $\overline{E}$ to $\overline{Z}$



Other Conditions: Pins 8, 11, 12, 13 = Gnd
Pin 1 = V_{CC} through 2.0 kΩ
Pin 16 = V_{CC}

TURN OFF DELAY VERSUS AMBIENT TEMPERATURE; S_0 to $\overline{Z}$

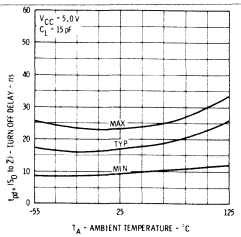


Fig. 14

TURN ON DELAY VERSUS AMBIENT TEMPERATURE; S_0 to $\overline{Z}$

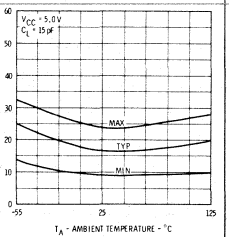


Fig. 15

TURN OFF DELAY VERSUS AMBIENT TEMPERATURE; E to $\overline{Z}$

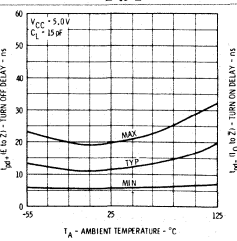


Fig. 16

TURN ON DELAY VERSUS AMBIENT TEMPERATURE; E to $\overline{Z}$

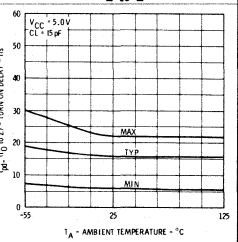


Fig. 17

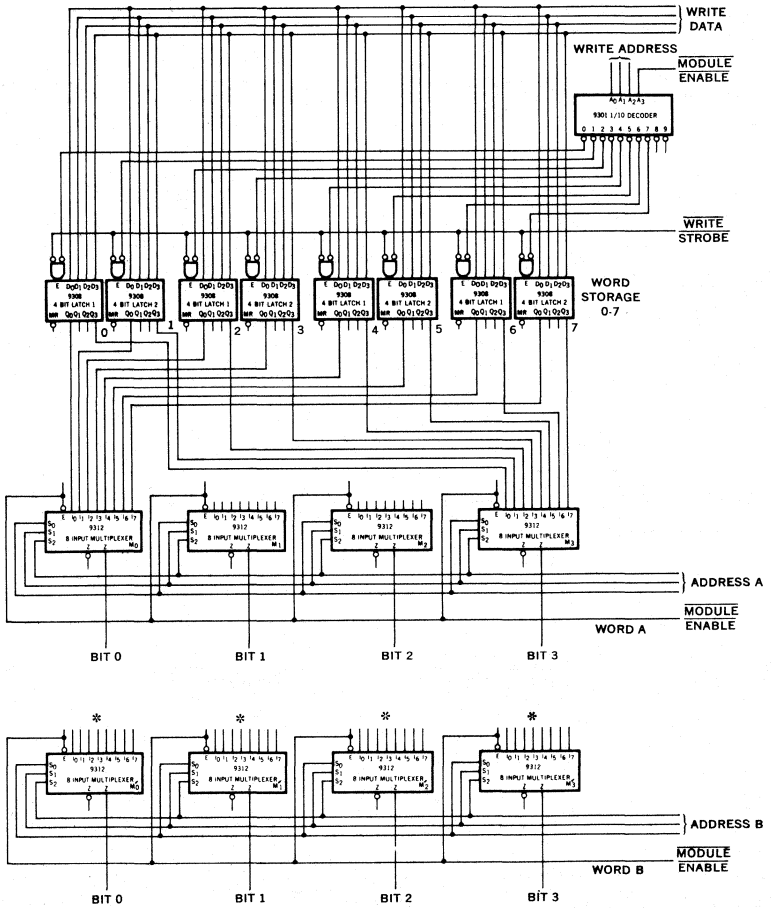
APPLICATIONS

A MULTI-PORT MEMORY MODULE

The four bit by eight word multi-port memory module shown in the below diagram uses only thirteen MSI packages; four 9308 24 pin dual four bit latches, eight 9312 eight input multiplexers, and one 9301 one-out-of-ten decoder.

The module as shown is capable of simultaneously reading from two independently specified locations and writing into a third independently selected location. The necessary enables are provided so that a number of these modules may be connected together to produce a larger memory. As an example a sixteen bit by sixty-four word memory would require thirty-two of the modules shown below.

By connecting this type of memory to a function generator unit, a processor could be constructed that would execute three address instructions at a very high speed on the data contained in this type of memory. In order to utilize the speed of the memory the instructions would also have to be contained in fast semiconductor memory.



* All Multiplexer connections are similar to M_0 and M_0' with inputs to M_0 and M_0' being the Q_0 outputs of the latches, M_1 and M_1' inputs being the Q_1 outputs of the latch, M_2 and M_2' inputs being Q_2 outputs of the latch, etc.

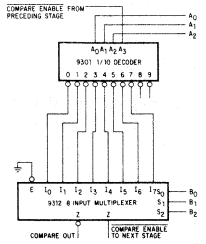
Fig. 18

APPLICATIONS

3 BIT COMPARATOR

Three bits of data to be compared are supplied to the address and select inputs of the 9301 and 9312 respectively. If A_0, A_1, A_2, and B_0, B_1, B_2 compare, the mutually exclusive active low output of the 9301 1/10 decoder and the selected input of the 9312 multiplexer will be coincidental and COMPARE OUT will be high. The COMPARE ENABLE must be low to permit compare operation.

3 BIT COMPARATOR



INTERCONNECTION DIAGRAM FOR 9 BITS

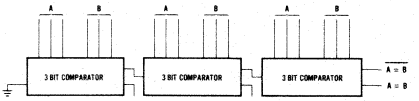


Fig. 18

IMPLEMENTING ANY FOUR-VARIABLE BOOLEAN FUNCTION

The 9312 eight input multiplexer can (in addition to performing its nominal function) produce any Boolean function of four variables without any additional elements if both the assertion and negation of one of the variables are present. If an assertion and negation are not present, one inverter may be required.

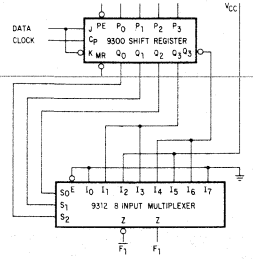
The procedure for implementing a four-variable function, along with an example, is shown in the attached diagram. First, consider the function in terms of a Karnaugh map. If the Q_0, Q_1 and Q_2 variable are connected to the S_0, S_1 and S_2 inputs of the 9312 then the Karnaugh map will be split, as shown, into eight sections, with each section corresponding to an input to the 9312. In order to implement the function each input of the 9312 is connected to one of the following four signals: ground, V_{CC}, the assertion, or negation of the fourth variable.

The contents of the two squares associated with an input, on the Karnaugh map, determine which connection is made to that input. If both squares contain a zero, ground should be connected to the input; if both squares contain a one, the input should be connected to V_{CC}. If the two squares contain a one and a zero then either the assertion or negation of the fourth variable will be required to implement the function. If the single one is located in the square associated with the assertion of the fourth variable then the assertion of the assertion of the fourth variable is connected to that input, and vice versa.

Shown in the illustration below is a 9312 decoding the condition of a 9300, producing a one output whenever the register contains two or more transitions. The truth table, Karnaugh map and the connection to the 9312 for this function are also shown in the illustration.

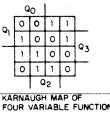
In many applications, using the 9312 to implement general logic functions of four variables will result in a sizeable reduction in package count. In many cases use of the 9312 with additional gates to produce functions of more than four variables will also reduce the package count.

The concept of using the 9312 eight input-multiplexer as a general logic function generator is described by S. S. Yau and C. K. Tang of Northwestern University in a paper presented at the 1968 Spring Joint Computer Conference in Atlantic City, New Jersey.

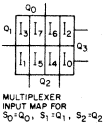


Q_0	Q_1	Q_2	Q_3	F_1
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	0

TRUTH TABLE



KARNAUGH MAP OF FOUR VARIABLE FUNCTION.



MULTIPLEXER INPUT MAP FOR $S_0=Q_0$, $S_1=Q_1$, $S_2=Q_2$

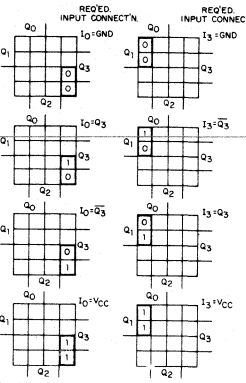


Fig. 19 FROM THE KARNAUGH MAP OF THE DESIRED FUNCTION I_0-I_7 CONNECTIONS CAN BE DETERMINED.

TTμL/MSI 9313
EIGHT-INPUT MULTIPLEXER WITH OPEN COLLECTOR OUTPUT
A FAIRCHILD TTμL IC PRODUCT

GENERAL DESCRIPTION – The TTμL/MSI 9313 is an eight-input multiplexer with open collector output. The 9313 has the same pinning and logic configuration as the 9312, but with an open collector $\overline{Z}$ output which allows for easy expansion of input terms. The device can select one bit of data from up to eight sources. It has an active low enable, and internal select decoding. The 9313 is fully compatible with all members of the Fairchild TTμL family.

FEATURES

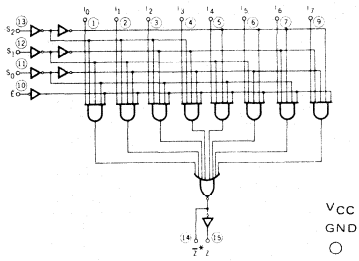
- **PIN FOR PIN REPLACEMENT FOR THE SIGNETICS 8231**
- **SAME PINNING AND LOGIC CONFIGURATION AS THE 9312 BUT WITH OPEN COLLECTOR OUTPUT**
- **OPEN COLLECTOR OUTPUT $\overline{Z}$ FOR EASY EXPANSION OF INPUT TERMS (WIRED-OR APPLICATIONS)**
- **MULTIFUNCTION CAPABILITY**
- **ON-CHIP SELECT LOGIC DECODING**
- **FULLY BUFFERED Z OUTPUT**
- **INPUT CLAMP DIODES**
- **TTμL COMPATIBLE**

PIN NAMES

S_0, S_1, S_2	Select Inputs
$\overline{E}$	Enable (Active Low) Input
I_0 to I_7	Multiplexer Inputs
Z	Multiplexer Output
$\overline{Z}$	Complementary Open Collector Multiplexer Output

ORDER INFORMATION – Specify U7B9313XXX for 16 pin Dual In-Line Package or U4L9313XXX for 16 pin Flatpak, where XXX is 51X for the -55°C to +125°C temperature range, or 59X for the 0°C to +75°C temperature range.

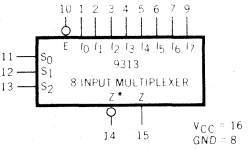
LOGIC DIAGRAM



V_{CC} = PIN 16
GND = PIN 8
○ = PIN NUMBERS
*Open Collector

Fig. 4

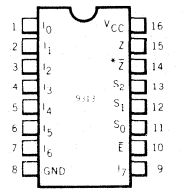
LOGIC SYMBOL



*Open Collector

Fig. 1

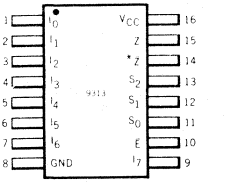
CONNECTION DIAGRAM
DIP (TOP VIEW)



*Open Collector

Fig. 2

FLATPAK (TOP VIEW)



*Open Collector

Fig. 3

FAIRCHILD SEMICONDUCTOR

FUNCTIONAL DESCRIPTION — The TTμL/MSI 9313 is a logical implementation of a single pole - 8 position switch with the switch position controlled by the state of three select inputs, S_0, S_1, S_2. An open collector output $\overline{Z}$ is provided for easy expansion of input terms. Also a fully buffered Z output is available. The enable input (E) is active low. When it is not activated the negation output is high and the assertion output is low regardless of all other inputs. The logic function provided at the output is:

$$Z = E \cdot (I_0 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot \overline{S}_2 + I_1 \cdot S_0 \cdot \overline{S}_1 \cdot \overline{S}_2 + I_2 \cdot \overline{S}_0 \cdot S_1 \cdot \overline{S}_2 + I_3 \cdot S_0 \cdot S_1 \cdot \overline{S}_2 + I_4 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot S_2 + I_5 \cdot S_0 \cdot \overline{S}_1 \cdot S_2 + I_6 \cdot \overline{S}_0 \cdot S_1 \cdot S_2 + I_7 \cdot S_0 \cdot S_1 \cdot S_2).$$

The 9313 provides the ability, in one package, to select from eight sources of data or control information. By proper manipulation of the inputs, the 9313 can provide any logic function of four variables and its negation.

TABLE I TRUTH TABLE

$\overline{E}$	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	$\overline{Z}$	Z
H	X	X	X	X	X	X	X	X	X	X	X	H	L
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

H = High voltage level
L = Low voltage level
X = Level does not affect output

TABLE II
TTμL LOADING RULES

INPUTS	LOADING	
	HIGH STATE	LOW STATE
All	1 U.L.	1 U.L.

OUTPUTS	DRIVE FACTOR	
	HIGH STATE	LOW STATE
Z	30 U.L.	10 U.L.
$\overline{Z}$	*	10 U.L.

1 Unit Load (U.L.) = 40 μA High/1.6 mA Low

*An external pull-up resistor is needed to provide high level drive capability. This output will source a maximum of 1.6 mA at V_{out} = 0.4 volts.

NOTE: See page 5 for details on Wired-OR applications.

TYPICAL INPUT AND OUTPUT CIRCUITS

INPUTS
EQUIVALENT CIRCUIT

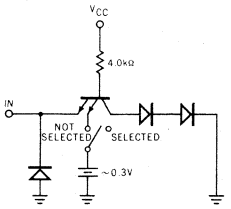


Fig. 5

Z Output (Pin 15)
EQUIVALENT CIRCUIT

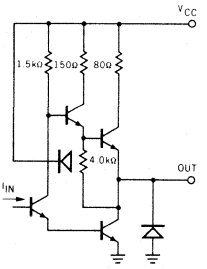


Fig. 6

$\overline{Z}$ Output (Pin 14)
EQUIVALENT CIRCUIT

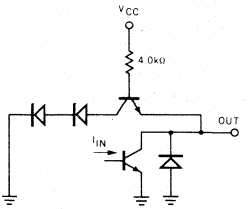


Fig. 7

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	-65°C to +150°C
Temperature (Ambient) Under Bias	-55°C to +125°C
V_{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
*Input Voltage (D.C.)	-0.5V to +5.5V
*Input Current (D.C.)	-30 mA to +5.0 mA
Voltage Applied to Outputs (Output High)	0.5V to +V_{CC} value
Output Current (D.C.) (Output Low)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC}) MIN.	TYP.	MAX.	TEMPERATURE
U7B/4L9313 51X	4.5V	5.0V	5.5V	-55°C to 125°C
U7B/4L9313 59X	4.75V	5.0V	5.25V	0°C to 75°C

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	CHARACTERISTIC	LIMITS MIN.	TYP. (Note 4)	MAX.	UNITS	CONDITIONS
V_{OH}	Output HIGH Voltage on Z (Pin 15)	2.4	3.6		Volts	V_{CC}= MIN., I_{OH} = -1.2 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.25	0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{IH}	Input HIGH Level	2.0			Volts	Guaranteed input logical HIGH voltage for all inputs
V_{IL}	Input LOW Level			0.8	Volts	Guaranteed input logical LOW voltage for all inputs
I_{IL}	Input LOW Current		-1.0	-1.6	mA	V_{CC} = MAX., V_{IN} = 0.4V
I_{IH}	Input HIGH Current		5.0	40	μA	V_{CC} = MAX., V_{IN} = 2.4V
			0.02	1.0	mA	V_{CC} = MAX., V_{IN} = 5.5V
I_{CEX}	Output High Leakage Current on $\overline{Z}$ (Pin 14)		5.0	150	μA	V_{CC} = 4.5V, V_{OUT} = 4.5V, V_{IN} = 0.6V on Data Input V_{IN} (E & S Inputs) = V_{IL} or V_{IH} per Truth Table
I_{SC}	Output Short Circuit Current on Z (Pin 15)	30	75	100	mA	V_{CC} = MAX., V_{OUT} = 0.0V
I_{CC}	Power Supply Current		28	40	mA	V_{CC} = MAX.

NOTES:
(1) The actual Testing Procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this Specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California (see page 1 for address and phone).
(2) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
(3) The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
(4) Typical limits are at V_{CC} = 5.0 V, 25°C, and max. loading.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	CHARACTERISTIC	LIMITS 51 GRADE TYP.	51 GRADE MAX.	59 GRADE TYP.	59 GRADE MAX.	UNITS	CONDITIONS
t_{pd+} (S_0 to Z)	Turn Off Delay Input to Output	25	32	25	36	ns	V_{CC} = 5.0 V
t_{pd-} (S_0 to Z)	Turn On Delay Input to Output	33	40	33	45	ns	C_T = C_L = 15 pF, R_X = 400 Ω

SWITCHING TIME TEST CIRCUIT

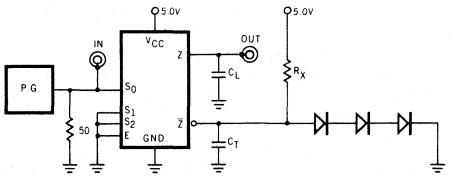


Fig. 8

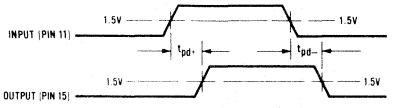
FREQ: 1 MHz
AMP: 4.0 V (referenced to ground)
PW: 500 ns
t_r = t_f = 2.5 ns (1 V to 2 V)

C_L = C_T = 15 pF which includes probe and jig capacitance.
All diodes 1N4376 or equivalent.
Rx = 400Ω

SWITCHING CHARACTERISTIC CURVES

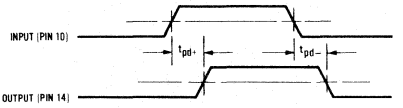
All measurements are made with V_{CC} = 5.0 V applied to pin 16 and with pin 8 grounded.

t_{pd}: S_0 to Z



Other Conditions: Pins 1, 8, 10, 12, 13 = GND
Pin 2 = V_{CC} through 1.0 kΩ
Pin 16 = V_{CC}

t_{pd}: I_0 to Z



Other Conditions: Pins 8, 10, 11, 12, 13 = GND
Pin 1 = V_{CC} through 2.0 kΩ
Pin 16 = V_{CC}

TURN OFF DELAY VERSUS AMBIENT TEMPERATURE; S_0 to Z

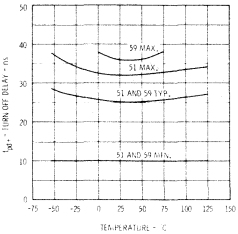


Fig. 9

TURN ON DELAY VERSUS AMBIENT TEMPERATURE; S_0 to Z

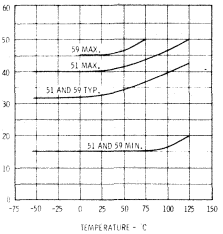


Fig. 10

TURN OFF DELAY VERSUS AMBIENT TEMPERATURE; I_0 to Z

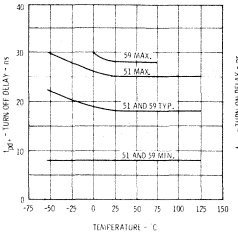


Fig. 11

TURN ON DELAY VERSUS AMBIENT TEMPERATURE; I_0 to Z

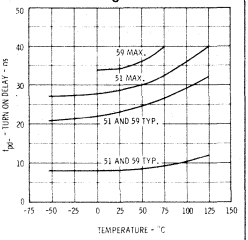
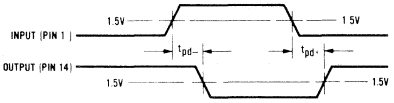


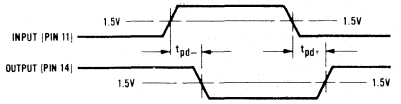
Fig. 12

t_{pd}: $\overline{E}$ to Z



Other Conditions: Pins 8, 10, 11, 12, 13 = GND
Pin 1 = V_{CC} through 2.0 kΩ
Pin 16 = V_{CC}

t_{pd}: S_0 to $\overline{Z}$



Other Conditions: Pins 1, 8, 10, 12, 13 = GND
Pin 2 = V_{CC} through 1.0 kΩ
Pin 16 = V_{CC}

TURN OFF DELAY VERSUS AMBIENT TEMPERATURE; $\overline{E}$ to Z

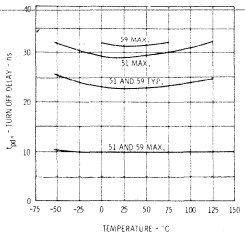


Fig. 13

TURN ON DELAY VERSUS AMBIENT TEMPERATURE; $\overline{E}$ to Z

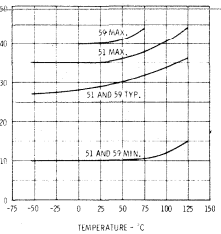


Fig. 14

TURN OFF DELAY VERSUS AMBIENT TEMPERATURE; S_0 to $\overline{Z}$

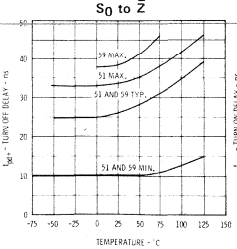


Fig. 15

TURN ON DELAY VERSUS AMBIENT TEMPERATURE; S_0 to $\overline{Z}$

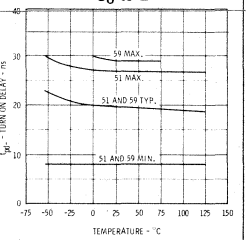


Fig. 16

SWITCHING CHARACTERISTICS CURVES

SWITCHING DELTA FOR TURN OFF DELAY (Δt_{pd+}), ANY INPUT TO Z OUTPUT, VERSUS LOAD CAPACITANCE (C_T)

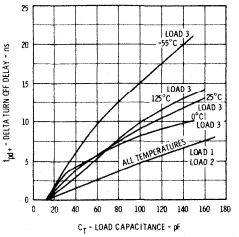


Fig. 17

SWITCHING DELTA FOR TURN ON DELAY (Δt_{pd-}), ANY INPUT TO Z OUTPUT, VERSUS LOAD CAPACITANCE (C_T)

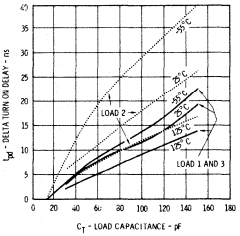


Fig. 18

WIRED OR APPLICATIONS

It is possible to perform the "Wired OR" function by connecting the open collector $\overline{Z}$ outputs together and adding an external pull up resistor.

The value of the pull up is determined by considering the fanout of the "OR Tie" and the number of devices in the "OR Tie". The pull up resistor value is chosen from a range between a maximum value (determined such that the required V_{OH} is maintained with all the OR tied outputs off) and a minimum value (determined such that with only one output on in the "OR-Tie", its fanout is not exceeded.

Minimum and Maximum Pull up Values

$$R_x\ (\text{Min.}) = \frac{V_{CC}\ (\text{max.}) - V_{OL}}{I_{OL} - N_2\, I_{IL} - (N_1 - 1)\, I_{IL}}$$

$$R_x\ (\text{Max.}) = \frac{V_{CC}\ (\text{min.}) - V_{OH}}{N_1\, I_{CEX} + N_2\, I_{IH}}$$

Where

- N_1 = Number of "Wired OR" Outputs
- N_2 = Fanout of "OR Tie'
- V_{CC} = Power Supply Voltage
- R_x = External Pull-up Resistor
- I_{CEX} = Output High Leakage Current on $\overline{Z}$ (150 μA)
- I_{IH} = Input High Current (40 μA)
- I_{IL} = Input Low Current (1.6 mA)
- V_{OL} = Output Low Level (0.4 V)
- V_{OH} = Output High Level (2.4 V)
- I_{OL} = Maximum Current Sinking Capability of Single Output (16 mA)

Example R_L (Min) and R_L (Max.) for four 9313's OR Tied and driving 1 TTμL gate. (Industrial V_{CC} tolerances used)

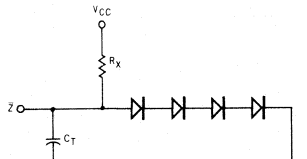
$$R_x\ (\text{Min.}) = \frac{5.25\ \text{V} - 0.4\ \text{V}}{16\ \text{mA} - 1\ (1.6\ \text{mA}) - (4-1)\ 1.6\ \text{mA}} = \frac{4.85\ \text{V}}{9.6\ \text{mA}} = 505\ \Omega$$

$$R_x\ (\text{Max.}) = \frac{4.75\text{V} - 2.4\text{V}}{4\ (150\ \mu\text{A}) + 1\ (40\ \mu\text{A})} = \frac{2.35\text{V}}{640\ \mu\text{A}} = 3.7\ \text{k}\Omega$$

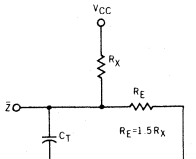
The pull up resistor value (± Resistor Tolerance) selected should be between these max. and min. values.

Minimum propagation delay results when the minimum value of external pull-up resistor is used in circuit 1. Diodes should be fast recovery 1N4376 or equivalent. External pull-up resistor circuits 2 and 3 give progressively slower propagation delays. (See Figures 17 and 18.)

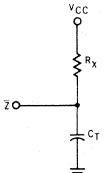
CIRCUIT 1



CIRCUIT 2



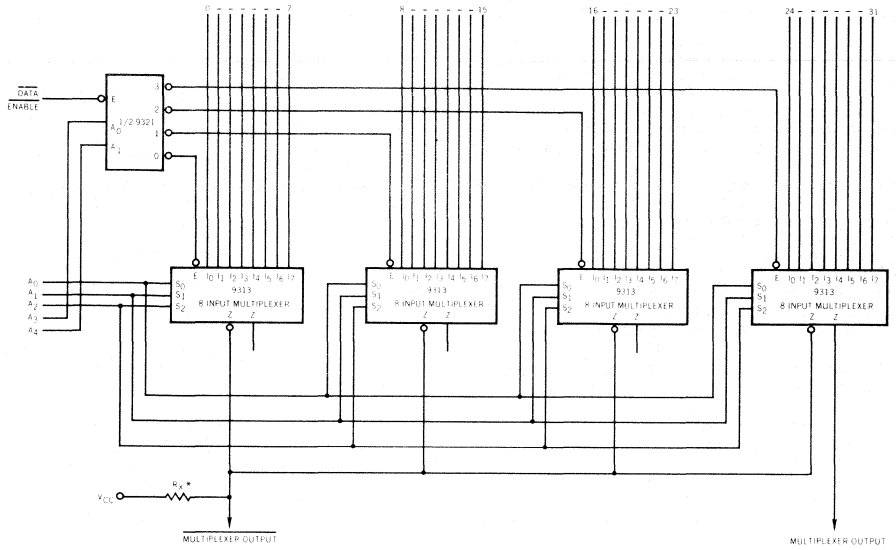
CIRCUIT 3



C_T = Total Capacitance at Output

APPLICATION (Cont'd)

THIRTY TWO INPUT DIGITAL MULTIPLEXER



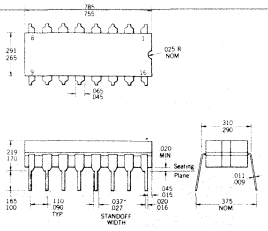
* The value of R_X determined according to the wiring rules specified on page 5.

The Figure above illustrates a 32 input multiplexer. The negation of the selected input is available from the OR Tie. The negation of the OR Tie and correspondingly the assertion of the selected input is available from each Z output. Each Z output can drive 10 UL, thus allowing this multiplexer to drive 40 TTL Loads.

Fig. 19

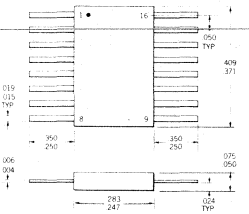
PACKAGE INFORMATION

7B — 16 LEAD DUAL IN-LINE PACKAGE



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers.
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.2 grams
*The .037/.027 dimension does not apply to the corner leads

4L — 16 LEAD FLATPAK



NOTES:
All dimensions in inches
Leads are gold-plated kovar
Package weight is 0.4 gram

9314
MSI QUAD LATCH
A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

GENERAL DESCRIPTION — The MSI 9314 is a multifunctional 4-Bit Latch. The latch is designed for general purpose storage applications in high speed digital systems. The 9314 uses TTμL technology and is CCSL compatible. All inputs feature diode clamping to reduce negative line transients. All outputs have active pull-up circuitry to provide high capacitance drive and to provide low impedance in both logic states for good A.C. noise immunity.

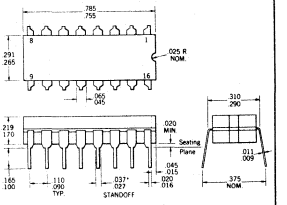
FEATURES
- **CAN BE USED AS SINGLE INPUT D LATCHES OR SET/RESET LATCHES**
- **ACTIVE LEVEL LOW ENABLE GATE INPUT**
- **OVERRIDING MASTER RESET**
- **25 ns THROUGH DELAY**
- **THE INPUT/OUTPUT CHARACTERISTICS PROVIDE DIRECT INTERFACING WITH FAIRCHILD DTμL, LPDTμL, TTμL, AND MSI FAMILIES (CCSL).**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
Input Voltage (D.C.) (See Note 1)	−0.5 V to +5.5 V
Input Current (D.C.) (See Note 1)	−30 mA to +5 mA
Voltage Applied to Outputs (Output High)	−0.5 V to +V_{CC} value
Output Current (D.C.) (Output Low)	+30 mA

NOTE 1: Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

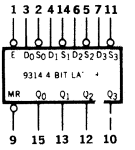
DUAL IN-LINE PACKAGE
16 Lead Dual In-Line



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" center
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for a conventional .020 inch diameter Lead
Package weight is 2.0 grams
Leads are tin-plated Kovar
*The .037 dimension does not apply .027 to the corner leads

Fig. 1

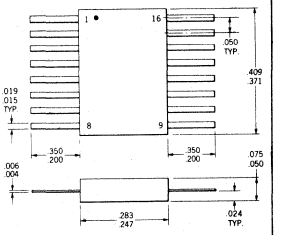
LOGIC DIAGRAM



V_{CC} = Pin 16
Gnd = Pin 8

Fig. 3

FLAT PAK
16 Lead BeO Cerpak



NOTES:
All dimensions in inches
Leads are gold-plated Kovar
Package weight is 0.4 gram

Fig. 2

ORDER INFORMATION — Specify U6B9314XXX for 16-pin Dual In-Line package or U4L9314XXX for 16-pin Flatpak, where XXX is 51X for the −55°C to +125°C temperature range, or 59X for the 0°C to +75°C temperature range.

Electrical Characteristics on Page 3
Notes on Page 3

FAIRCHILD
SEMICONDUCTOR

FUNCTIONAL DESCRIPTION

LATCH OPERATION — The 9314 consists of four latches with a common active low enable and active low master reset. When the common enable goes high, data present in the latches is stored and the state of a latch is no longer affected by the S and D inputs. The master reset when activated overrides all other input conditions forcing all latch outputs low.

Each of the four latches can be operated in one of two modes:

D TYPE LATCH — For D type operation the S input of a latch is held low. While the common enable is active the latch output follows the D input. Information present at the latch output is stored in the latch when the enable goes high.

SET/RESET LATCH — During set/reset operation when the common enable is low a latch is reset by a low on the D input, and can be set by a low on the S input if the D input is high. If both S and D inputs are low, the D input will dominate and the latch will be reset. When the enable goes high, the latch remains in the last state prior to disablement.

The two modes of operation of the 9314 latches are shown in the Truth Table below.

Fig. 4—TRUTH TABLE

MR	E	D	S	Q_N	OPERATION
H	L	L	L	L	D MODE
H	L	H	L	H	
H	H	X	X	Q_{N-1}	
H	L	L	L	L	R/S MODE
H	L	H	L	H	
H	L	L	H	L	
H	L	H	H	Q_{N-1}	
H	H	X	X	Q_{N-1}	
L	X	X	X	L	RESET

X = Don't Care
L = Low Voltage Level
H = High Voltage Level
Q_{N-1} = Previous Output State
Q_N = Present Output State

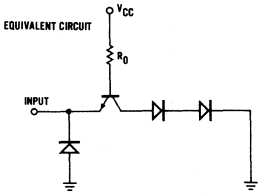
Fig. 5—LOADING RULES
(1 U.L. = 1 TTμL Gate Input Load)

INPUTS	LOADING
D_0, D_1, D_2, D_3	1.5 U.L.
MR, E, S_0, S_1, S_2, S_3	1.0 U.L.

OUTPUTS	FAN OUT
Q_0, Q_1, Q_2, Q_3	9 U.L.

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

Fig. 6—INPUTS



INPUT CURRENT VERSUS INPUT VOLTAGE

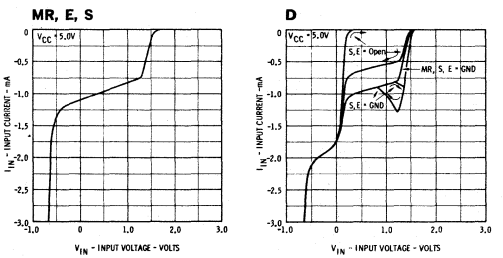
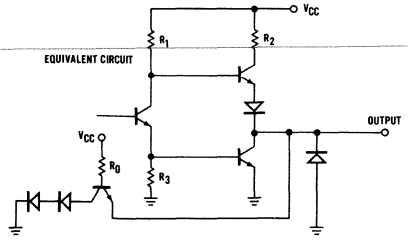


Fig. 7—OUTPUTS



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE

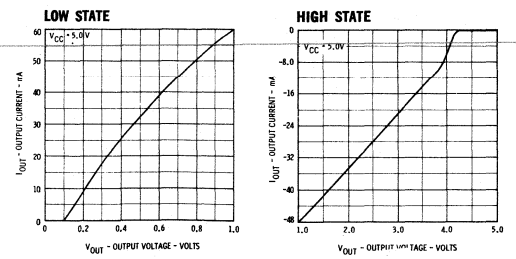


TABLE I —
ELECTRICAL CHARACTERISTICS ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0$ V $\pm 10\%$, See Note 1) (Part #U6B/4L931451X)

SYMBOL	CHARACTERISTICS	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	2.8		2.4		Volts	$V_{CC} = 4.5$ V, $I_{OH} = -0.6$ mA Inputs at threshold voltages (V_{IL} or V_{IH}) (See Note 2)
V_{OL}	Output Low Voltage		0.4		0.21	0.4		0.4	Volts	$V_{CC} = 5.5$ V, $I_{OL} = 14.4$ mA $V_{CC} = 4.5$ V, $I_{OL} = 11.2$ mA Inputs at threshold voltages (V_{IL} or V_{IH}) (See Note 2)
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current S, E, and MR Inputs		−1.6		−1.1	−1.6		−1.6	mA	$V_{CC} = 5.5$ V, $V_F = 0.4$ V
1.5 I_F	Input Load Current D Inputs		−2.7		−1.9	−2.7		−2.7		$V_F = 0.0$ V (See Note 3)
I_R	Input Leakage Current S, E, and MR Inputs				10	60		60	μA	$V_{CC} = 5.5$ V, $V_R = 4.5$ V
1.5 I_R	Input Leakage Current D Inputs				15	90		90		
I_{PD}	Power Supply Current		50		35	50		50	mA	$V_{CC} = 5.0$ V, all outputs low, inputs disabled

TABLE II —
ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0$ V $\pm 5\%$, See Note 1) (Part #U6B/4L931459X)

SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	3.1		2.4		Volts	$V_{CC} = 4.75$ V, $I_{OUT} = -0.6$ mA Inputs at threshold voltages (V_{IL} or V_{IH}) (See Note 2)
V_{OL}	Output Low Voltage		0.45		0.21	0.45		0.45	Volts	$V_{CC} = 5.25$ V, $I_{OUT} = 14.4$ mA $V_{CC} = 4.75$ V, $I_{OUT} = 12.7$ mA Inputs at threshold voltages (V_{IL} or V_{IH}) (See Note 2)
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current S, E, and MR Inputs		−1.6		−1.0	−1.6		−1.6	mA	$V_{CC} = 5.25$ V, $V_F = 0.45$ V
1.5 I_F	Input Load Current D Inputs		−2.7		−1.8	−2.6		−2.7		$V_F = 0.0$ V (See Note 3)
I_R	Input Leakage Current S, E, and MR Inputs				10	60		60	μA	$V_{CC} = 5.25$ V, $V_R = 4.5$ V
1.5 I_R	Input Leakage Current D Inputs				15	90		90		
I_{PD}	Power Supply Current		60		35	60		60	mA	$V_{CC} = 5.0$ V, all outputs low, inputs disabled

NOTES:
(1) Units are pulse tested.
(2) Output Voltages are guaranteed for either the input enabled or input disabled case.
(3) This current is measured at $V_{IN} = 0.0$ V to insure that no current is being absorbed by the device internally. The maximum value given guarantees that the maximum instantaneous current that can flow out of the input at $V_{IN} = 0.4$ V is 2.4 mA.

A.C. CHARACTERISTICS ($T_A = 25°C$, $V_{CC} = 5.0$ Volts, Pin 8 = Gnd)

CHARACTERISTIC	LIMITS				UNITS	CONDITIONS
	51 GRADE		59 GRADE			
	MIN.	MAX.	MIN.	MAX.		
t_{pd+} (Enable to Output)		25		28	ns	See Figure No. 8
t_{pd-}		26		28		
t_{pd+} (Data to Output)		16		18	ns	See Figure No. 9
t_{pd-}		30		32		
t_s "H" (High Data to Enable)	5		7		ns	See Figure No. 10
t_s "L" (Low Data to Enable)	20		22			
t_r "H" (High Data to Enable)	0		0		ns	See Figure No. 11
t_r "L" (Low Data to Enable)	5		7			
t_{PW} (Enable Pulse Width)	20		22		ns	See Figure No. 12
t_{PW} (Master Reset Pulse Width)	18		20		ns	See Figure No. 13
t_{pd-} (Master Reset to Output)		20		22	ns	See Figure No. 13
t_{rec} (Master Reset Recovery Time)	0		0		ns	See Figure No. 14
t_{pd+} (Set Input to Output)		25		28	ns	See Figure No. 15
t_{hold} (Set to Data)	8		10		ns	See Figure No. 15

SET UP TIME: t_s is defined as the minimum time required for the logic level to be present at the Data Input prior to the enable transition from Low to High in order for the latch to recognize and store the new data.

RELEASE TIME: t_r is defined as the minimum time that the logic level on the Data Input must remain constant after the Enable transition from Low to High in order for the latch to retain the correct data.

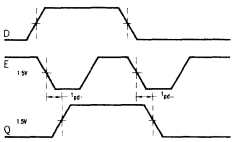
RECOVERY TIME: t_{rec} is defined as the minimum time that the Enable must remain Low after the Master Reset transition from Low to High in order for the latch to recognize and store High data.

HOLD TIME: t_{hold} is defined as the minimum time required for the Set Input to be High prior to the Data Input transition from Low to High in order to retain a Low output.

A.C. CHARACTERISTICS

All delays are measured with $V_{CC} = 5.0$ V applied to Pin 24 and Pin 12 grounded. The active input is driven by a 9002 TTμL or equivalent gate with the output loaded with 15 pF (includes jig and probe). Outputs under test are loaded with 15 pF (includes jig and probe). Pins not reference are not connected.

Fig. 8—t_{pd} (ENABLE TO OUTPUT)



Other Conditions: S = Gnd

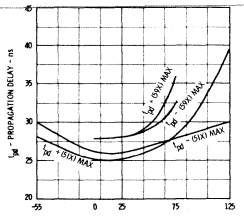
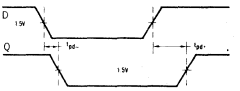
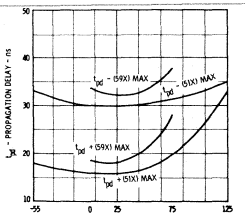


Fig. 9—t_{pd} (DATA TO OUTPUT)

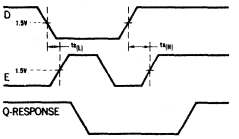


Other Conditions: E = Gnd, S = Gnd



A.C. CHARACTERISTICS

Fig. 10—t_s (DATA TO ENABLE)



Other Condition: S = Gnd

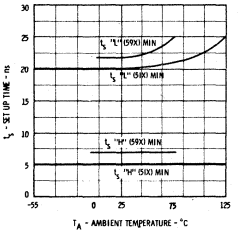
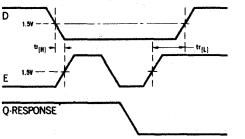


Fig. 11—t_r (DATA TO ENABLE)



Other Condition: S = Gnd

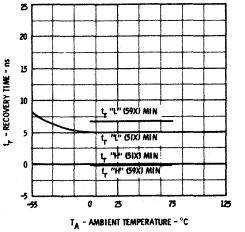
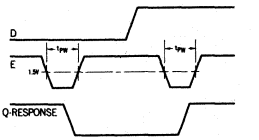


Fig. 12—t_{PW} (MIN. ENABLE PULSE WIDTH)



Other Condition: S = Gnd

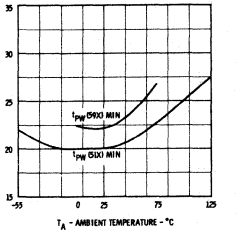
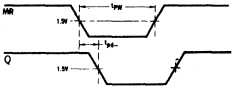


Fig. 13—t_{PW} (MIN. MASTER RESET PULSE WIDTH) t_{pd-} (MASTER RESET TO OUTPUT)



Other Conditions: S =Gnd
E = Gnd

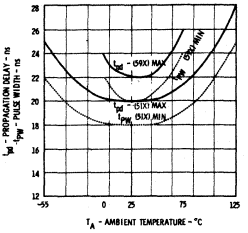
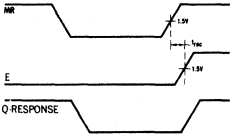


Fig. 14—t_{rec} (MASTER RESET RECOVERY TIME)



Other Conditions: S = Gnd, D = Open

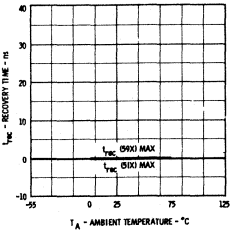
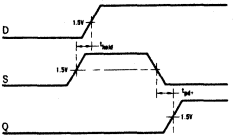
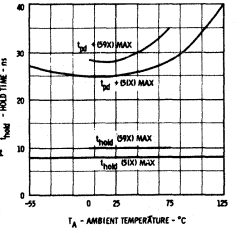


Fig. 15—t_{pd+} (SET TO OUTPUT) t_{hold} (SET TO DATA)



Other Conditions: E = Gnd



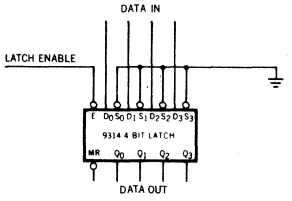


Fig. 16—4 BIT STORAGE LATCH

The figure illustrates the use of the 9314 as a D type storage latch. Data is stored in the latch when the enable line is high.

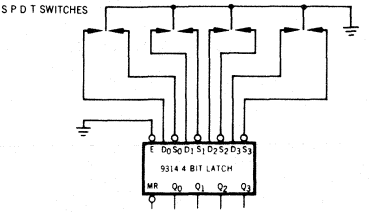


Fig. 17—CONTACT BOUNCE ELIMINATOR

The 9314 can be used to eliminate mechanical switch bounce for a single pole double throw switch. The latch operation is that of an active low input set/reset latch. The pole of the switch is low so that when in the S position, the output is high, in the D position the output is low.

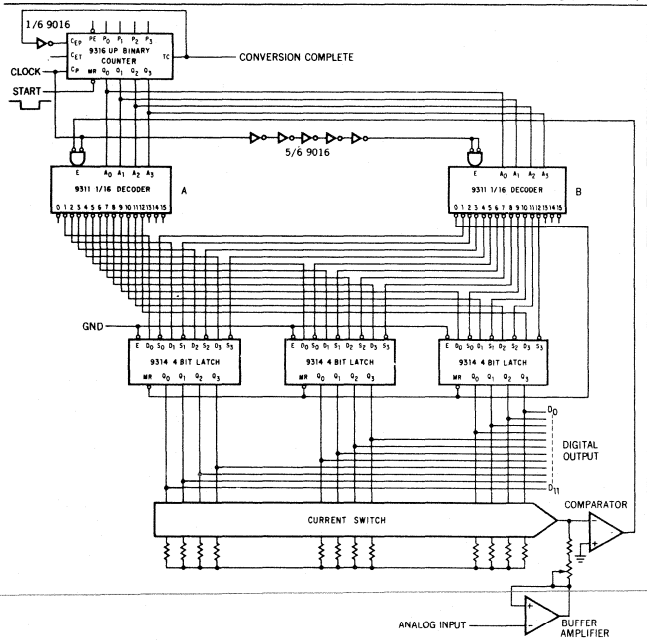


Fig. 18—ANALOG TO DIGITAL CONVERSION

The figure illustrates a 12 bit high speed successive approximation A/D Converter using the 9314 Quad Latch. Conversion is actually completed in 13 clock periods, but for convenience a 16-clock conversion is used.

At time period "0", decoder B (during the time the input clock is high) resets all stages of the 12-bit register that drive the current switches feeding to the resistance ladder network. At time period 1, output "1" from decoder B sets the first latch, which contains the most significant bit in the register. The comparator then decides whether this binary value is greater or less than its analog equivalent. If it is greater, the comparator resets that latch via decoder A when the clock is low. In this manner the various stages in the holding register are set and reset, or left set, until conversion is complete after 13 clock periods. The counter then continues until the terminal count is reached, whereupon an inverter in a feedback path inhibits further counting until another conversion is required.

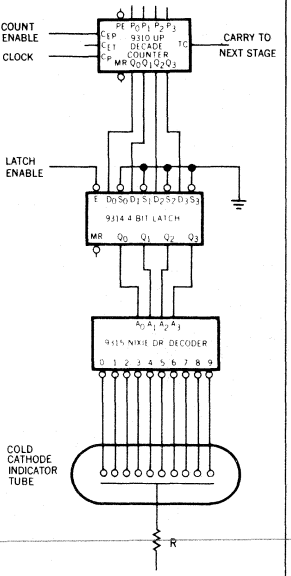


Fig. 19—COUNTING AND HOLDING DISPLAY SYSTEM

The figure illustrates the use of the 9314 as a D type storage latch used with the MSI 9310 (decade counter) and the MSI 9315 (one-of-ten decoder/driver). Data is stored when the enable line is high.

9315

MSI ONE-OF-TEN DECODER/DRIVER

A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

GENERAL DESCRIPTION — The MSI 9315 accepts 1-2-4-8 binary coded decimal inputs and provides ten mutually exclusive outputs, which can directly control the ionizing potentials of many gas filled cold cathode indicator tubes. The MSI 9315 is similar in operation to the CμL9960, but the MSI 9315 can be driven from any MSI, TTμL, DTμL or LPDTμL product.

- **STABLE HIGH-VOLTAGE OUTPUT CHARACTERISTICS**
- **DIRECT DISPLAY DRIVE CAPABILITY**
- **BCD ACTIVE-LEVEL HIGH INPUTS**
- **BLANKING TEST MODE**
- **—55°C TO +125°C TEMPERATURE CAPABILITY**

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

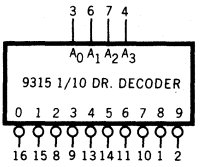
Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7 V
Input Voltage (DC) (See Note 1)	−1.5 V to +5.5 V
Input Current (DC) (See Note 1)	−10 mA to +1.0 mA
Current into output when output is low	+10 mA
Current into each output when output is high (See Note 2)	+1.5 mA

Note 1: Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

2: Total current through all 10 outputs in the high state shall not exceed 2.0 mA.

ORDER INFORMATION — Specify U6B9315XXX for 16-pin Dual In-Line package or U4L9315XXX for 16-pin Flatpak, where XXX is 51X for the −55°C to +125°C temperature range, or 59X for the 0°C to +75°C temperature range.

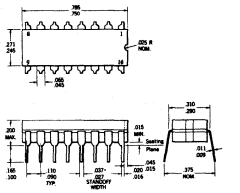
LOGIC SYMBOL



V_{CC} = PIN 5
GND = PIN 12

Fig. 1

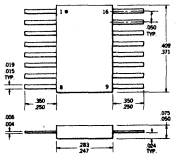
DUAL IN-LINE PACKAGE



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020" diameter lead
Leads are tin-plated kovar
Package weight is 2.0 grams
Hermetically sealed Alumina ceramic package
*The .027/.037 dimension does not apply to the corner leads

Fig. 2

FLAT PACKAGE



NOTES:
All dimensions in inches
Leads are gold-plated Kovar
Package weight is 0.4 gram

Fig. 3

FAIRCHILD
SEMICONDUCTOR

FUNCTIONAL DESCRIPTION — The one-of-ten decoder/driver accepts BCD inputs from all CCSL circuits and produces the correct output selection to directly drive gas filled cold cathode indicator tubes. The outputs are selected as shown in the Truth Table. It is capable of driving all known available cold cathode indicator tubes having 7 mA or less cathode current.

Unused input codes 12 and 13 cause all the outputs to remain high, no cathode will be selected. This results in the indicator tube being blanked. Using this feature for blanking may cause a slight glow to appear in the tube.

TRUTH TABLE

	A_0	A_1	A_2	A_3	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$	$\overline{8}$	$\overline{9}$
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	H	L	L	L	H	L	H	H	H	H	H	H	H	H
2	L	H	L	L	H	H	L	H	H	H	H	H	H	H
3	H	H	L	L	H	H	H	L	H	H	H	H	H	H
4	L	L	H	L	H	H	H	H	L	H	H	H	H	H
5	H	L	H	L	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	H	H	H	L	H	H	H	H	H	H	H	L	H	H
8	L	L	L	H	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
10	L	H	L	H	H	H	L	H	H	H	H	H	L	H
11	H	H	L	H	H	H	H	L	H	H	H	H	H	L
12	L	L	H	H	H	H	H	H	H	H	H	H	H	H
13	H	L	H	H	H	H	H	H	H	H	H	H	H	H
14	L	H	H	H	H	H	H	H	H	H	L	H	H	H
15	H	H	H	H	H	H	H	H	H	H	H	L	H	H

H = High voltage level
L = Low voltage level

Fig. 5

LOADING RULES

INPUTS	LOADING
All Inputs	1 U.L.

CCSL INPUT LOAD

GRADE	INPUTS	LOADING
59	All Inputs	1/9.4
51	All Inputs	2/9.4

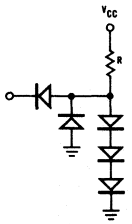
OUTPUTS are designed to drive gas filled cold Cathode indicator tubes

1 U.L. = 1 DTμL Unit Load
1 U.L. is defined by the entries I_R and I_F in the table on page 3.

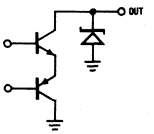
Fig. 4

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

EQUIVALENT INPUT CIRCUIT



EQUIVALENT OUTPUT CIRCUIT



INPUT CURRENT VERSUS INPUT VOLTAGE A_0, A_1, A_2, A_3 INPUTS

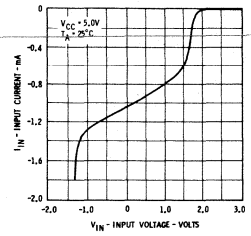


Fig. 6

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)

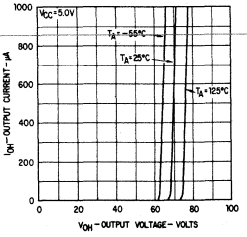


Fig. 7

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)

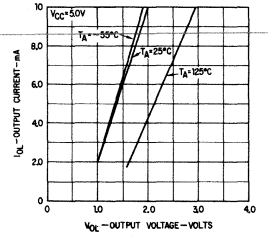


Fig. 8

ELECTRICAL CHARACTERISTICS ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$)

SYMBOL	CHARACTERISTIC	LIMITS						UNITS	CONDITIONS
		−55°C		+25°C			+125°C		
		MIN.	MAX.	MIN.	TYP.	MAX.	MIN. MAX.		
V_{OH}	Output High Voltage	61		70	75		70	Volts	$V_{CC} = 5.5\ V$, Force 2.0 mA into high output
I_{OH}	Output High Leakage Current					20	50	μA	$V_{CC} = 5.5\ V$, $V_{OUT} = 55\ V$ Inputs at threshold voltages (V_{IL} = Gnd, $V_{IH} = 4.5\ V$) as per truth table
V_{OL}	Output Low Voltage		3.0			2.5	3.7	Volts	$V_{CC} = 4.5\ V$, $I_{OL} = 7.0$ mA Inputs at threshold voltages (V_{IL} or V_{IH}) as per truth table
V_{IH}	Input High Voltage	2.1		1.9			1.7	Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		1.4			1.1	0.8	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		−1.5		−1.3	−1.5	−1.5	μA	$V_{CC} = 5.5\ V$, $V_F = 0.4\ V$ Other inputs open
I_R	Input Leakage Current				0.02	2.0	5.0	μA	$V_{CC} = 5.5\ V$, $V_R = 4.5\ V$ Other inputs open
I_{PD}	V_{CC} Current		29			29	29	mA	$V_{CC} = 5.0\ V$, No connection to input or output pins

ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0\ V \pm 5\%$)

SYMBOL	CHARACTERISTIC	LIMITS						UNITS	CONDITIONS
		0°C		+25°C			+75°C		
		MIN.	MAX.	MIN.	TYP.	MAX.	MIN. MAX.		
V_{OH}	Output High Voltage	67		70	75		70	Volts	$V_{CC} = 5.25\ V$, Force 2.0 mA into high output
I_{OH}	Output High Leakage Current					40	50	μA	$V_{CC} = 5.25\ V$, $V_{OUT} = 55\ V$ Inputs at threshold voltages (V_{IL} = Gnd, $V_{IH} = 4.5\ V$) as per truth table
V_{OL}	Output Low Voltage		3.2			3.0	3.6	Volts	$V_{CC} = 4.75\ V$, $I_{OL} = 7.0$ mA Inputs at threshold voltages (V_{IL} or V_{IH}) as per truth table
V_{IH}	Input High Voltage	2.0		2.0			2.0	Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85	0.85	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		−1.5			−1.5	−1.5	μA	$V_{CC} = 5.25\ V$, $V_F = 0.45\ V$ Other inputs open
I_R	Input Leakage Current					5.0	10	μA	$V_{CC} = 5.25\ V$, $V_R = 4.5\ V$ Other inputs open
I_{PD}	V_{CC} Current		31			31	31	mA	$V_{CC} = 5.0\ V$, No connection to input or output pins

TYPICAL APPLICATIONS

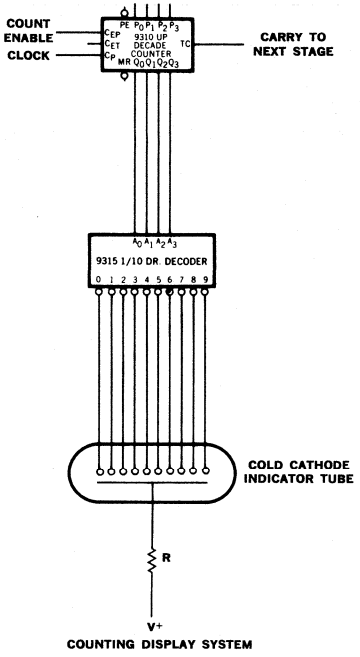


Fig. 9

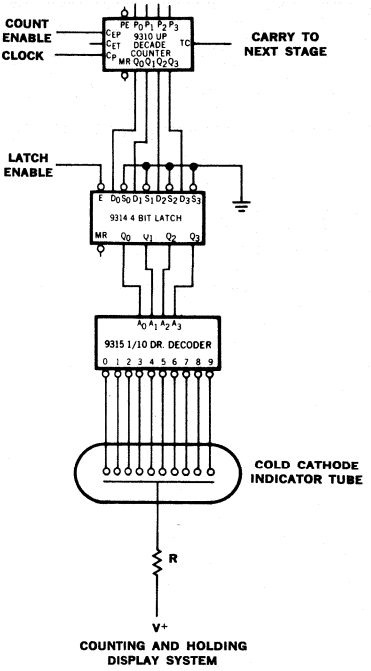


Fig. 10

The MSI 9315 is suitable for driving all commercially available numeric gas filled cold cathode indicator tubes in which ON Cathode current does not exceed 7.0 mA, and total OFF Cathode leakage current does not exceed 2.0 mA. The values of V^+ and R may be chosen following the readout tube manufacturers specifications.

9316

MSI 4-BIT BINARY COUNTER

A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

GENERAL DESCRIPTION — The 9316 is a high speed synchronous 4-bit binary decade counter. It is a synchronously presetable, multifunctional MSI building block useful in a large number of counting, digital integration, and conversion applications. Several stages of synchronous operation are obtainable with no external gating packages required through an internal carry look-ahead counting technique.

FEATURES:

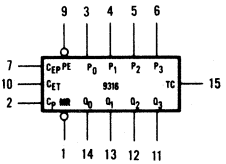
- **SYNCHRONOUS COUNTING AND PARALLEL ENTRY**
- **DECODED TERMINAL COUNT**
- **BUILT-IN CARRY CIRCUITRY**
- **TYPICAL POWER DISSIPATION OF 300 mW**
- **THE INPUT/OUTPUT CHARACTERISTICS PROVIDE EASY INTERFACING WITH FAIRCHILD DTμL, LPDTμL, AND TTμL FAMILIES (CCSL).**
- **ALL CERAMIC HERMETIC 16 PIN DUAL IN-LINE PACKAGE AND FLAT PACKAGE**
- **INPUT DIODE CLAMPING**

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7 V
Voltage Applied to Outputs for high output state	−0.5 V to V_{CC} value
Input Voltage (D.C.)	−0.5 V to +5.5 V

ORDER INFORMATION — Specify U6B9316XXX for 16-pin Dual In-Line Package, U3L9316XXX for 16-pin Flat Package where XXX is 51X for the −55°C to +125°C temperature range, or 59X for the 0°C to 75°C temperature range.

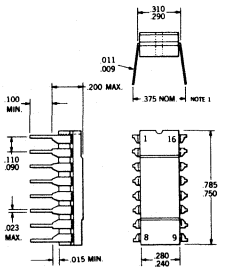
LOGIC DIAGRAM



V_{CC} = Pin 16
Gnd = Pin 8

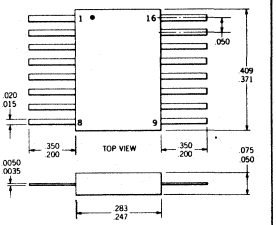
PHYSICAL DIMENSIONS

DUAL IN-LINE PACKAGE



NOTE:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.375) misalignment to facilitate insertion.

FLAT PACKAGE



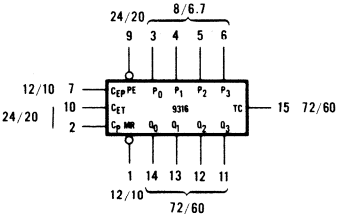
FAIRCHILD
SEMICONDUCTOR

FUNCTIONAL DESCRIPTION — A clock buffer and inverter drives the four clocked RS master-slave flip flops in parallel, so that synchronous operation is obtained. When the clock input (CP) is low, the slave is steady, but data can enter the master via the R and the S inputs. During the low to high transition of CP, first the data inputs (R and S) are inhibited, so that a later change in the input data will not affect the master; secondly, the now trapped information in the master is transferred to the slave and is reflected at the outputs. When the transfer is completed both the master and the slave are steady as long as the clock input remains high, and regardless of the logic state at any other input to the device. During the high to low transition of the clock input, first the transfer path from master to slave are inhibited, leaving the slave steady in its present state, secondly, the data inputs (R and S) are enabled so that new data can enter the master. As a result of this synchronous operation higher clock frequency is possible and much less external logic is required in most applications. Some restrictions are placed on the manner of selection. First, the transition of CEP or CET from high to low or of PE from low to high may only be done when CP is high. The remaining transitions may be made by following the setup and release times specified under "Switching Characteristics." The asynchronous MR clears the counter independent of any other input.

Note: CE (count enable) = CEP • CET
TC = CET • Q_0 • Q_1 • Q_2 • Q_3

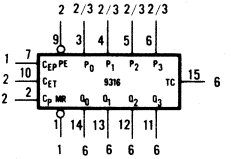
LOADING RULES

CCSL LOAD AND DRIVE FACTORS



V_{CC} = Pin 16
Gnd = Pin 8

TTμL LOAD AND DRIVE FACTORS



V_{CC} = Pin 16
Gnd = Pin 8

(1 U.L. = 1 TTμL input gate load)

ELECTRICAL CHARACTERISTICS (T_A = −55°C to +125°C, V_{CC} = 5.0 V ±10%)

SYMBOL	CHARACTERISTICS	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS & COMMENTS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	V_{CC} = 4.5 V, I_{OH} = −0.36 mA
V_{OL}	Output Low Voltage		0.4		0.2	0.4		0.4	Volts	V_{CC} = 5.5 V, I_{OL} = 9.6 mA V_{CC} = 4.5 V, I_{OL} = 7.44 mA
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current MR, CEP		−1.6		−1.0	−1.6		−1.6	mA	
$2\ I_F$	Input Load Current CP, PE, CET		−3.2		−2.0	−3.2		−3.2	mA	V_{CC} = 5.5 V V_F = 0.4 V
$^2/_3 I_F$	Input Load Current P_0, P_1, P_2, P_3		−1.07		−0.7	−1.07		−1.07	mA	
I_R	Input Leakage Current MR, CEP		60		10	60		60	μA	
$2\ I_R$	Input Leakage Current CP, PE, CET		120		20	120		120	μA	V_{CC} = 5.5 V V_R = 4.5 V
$^2/_3 I_R$	Input Leakage Current P_0, P_1, P_2, P_3		40		7.0	40		40	μA	

ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0\ V \pm 5\%$)

SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	CONDITIONS & COMMENTS
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	$V_{CC} = 4.75\ V$, $I_{OH} = -0.36\ mA$
V_{OL}	Output Low Voltage		0.45		0.2	0.45		0.45	Volts	$V_{CC} = 5.25\ V$, $I_{OL} = 9.6\ mA$ $V_{CC} = 4.75\ V$, $I_{OL} = 8.5\ mA$
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current MR, CEP		−1.6		−1.0	−1.6		−1.6	mA	
$2\ I_F$	Input Load Current CP, PE, CET		−3.2		−2.0	−3.2		−3.2	mA	$V_{CC} = 5.25\ V$ $V_F = 0.4\ V$
$⅔ I_F$	Input Load Current P_0, P_1, P_2, P_3		−1.07		−0.7	−1.07		−1.07	mA	
I_R	Input Leakage Current MR, CEP		60		10	60		60	μA	
$2\ I_R$	Input Leakage Current CP, PE, CET		120		20	120		120	μA	$V_{CC} = 5.25\ V$ $V_R = 4.5\ V$
$⅔ I_R$	Input Leakage Current P_0, P_1, P_2, P_3		40		7.0	40		40	μA	

SWITCHING CHARACTERISTICS ($T_A = 25°C$)

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	CONDITIONS & COMMENTS
t_{pd+} (Q)	Turn-Off Delay		20		ns	$V_{CC} = 5.0\ V$ $C_L = 15\ pF$ (Fig. 1)
t_{pd-} (Q)	Turn-On Delay		15		ns	
t_{pd+} (TC)	Turn-Off Delay for TC		35		ns	
t_{pd-} (TC)	Turn-On Delay for TC		20		ns	
t_s (SE)	Set-Up Time for CE		14		ns	$V_{CC} = 5.0\ V$ $C_L = 15\ pF$ (Fig.2)
t_r (CE)	Release Time for CE		12		ns	
t_s	Set-Up Time for Data		18		ns	$V_{CC} = 5.0\ V$ $C_L = 15\ pF$ (Fig. 3)
t_r	Release Time for Data		17		ns	
t_s (PE)	Set-Up Time for PE		30		ns	
t_r (PE)	Release Time for PE		28		ns	
t_{pd-} (MR)	Turn-On Delay for MR		33		ns	$V_{CC} = 5.0\ V$, $C_L = 15\ pF$ (Fig. 4)
$t_{P\pm}$	Propagation Delay for CET to TC		14		ns	$V_{CC} = 5.0\ V$, $C_L = 15\ pF$ (Fig. 5)

SET-UP TIME: t_s is defined as the minimum time required for the logic level to be present at the logic input prior to the clock transition from low to high in order for the flip-flop(s) to respond.

RELEASE TIME: t_r is defined as the maximum time allowed for the logic level to be present at the logic input prior to the clock transition from low to high in order for the flip-flop(s) not to respond.

SWITCHING TIME WAVEFORMS

Fig. 1

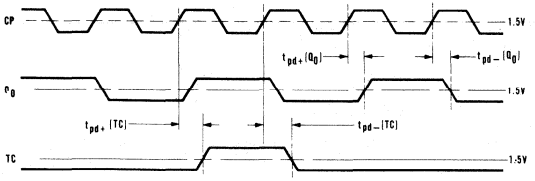


Fig. 2

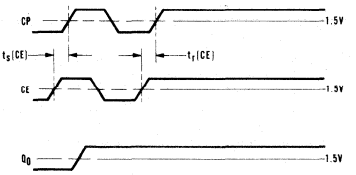


Fig. 3

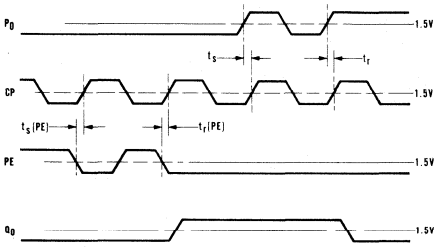


Fig. 4

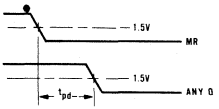
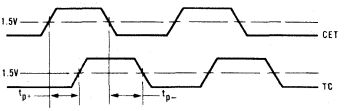
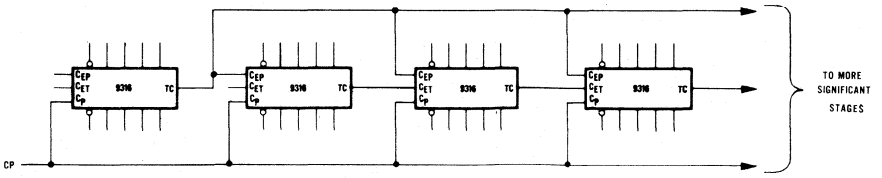


Fig. 5



APPLICATIONS



SYNCHRONOUS COUNTING SCHEME

9317A . 9317B . 9317C . 9317D

MSI SEVEN SEGMENT DECODER/DRIVER

A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

GENERAL DESCRIPTION — The MSI 9317 is a Seven Segment Decoder/Driver designed to accept four inputs in 8421 BCD code and provide the appropriate outputs to drive a seven segment numerical display. The decoder can be used to directly drive seven-segment incandescent lamp displays and light emitting diode indicators (or indirectly drive neon, electro-luminescent, or CRT numeric displays). The MSI 9317 is compatible with all other Fairchild CCSL devices.

- **CCSL COMPATIBLE**
- **AUTOMATIC RIPPLE BLANKING FOR SUPPRESSION OF LEADING EDGE ZEROES**
- **LAMP INTENSITY MODULATION CAPABILITY**
- **LAMP TEST FACILITY**
- **BLANKING INPUT**
- **ACTIVE LOW OUTPUTS**
- **ALL CERAMIC "HERMETIC" 16 PIN DUAL IN-LINE* PACKAGE**
- **DRIVE LAMPS DIRECTLY**
- **CODES IN EXCESS-OF BINARY 9 DISABLE OUTPUTS**
- **ENHANCED RELIABILITY WITH UNIQUE NUMERIC ONE DISPLAY POSITION**

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
Voltage Applied to Outputs for high output state	−0.5 V to +30 V
Input Voltage (D.C.)	−0.5 V to +5.5 V
Current Into Outputs	80 mA
Power Dissipation per Output	50 mW

OPTIONS

PARAMETER	9317A	9317B	9317C	9317D
Latch Voltage	30 Volts	20 Volts	30 Volts	20 Volts
Output Current (Pins 9 through 15)	40 mA	40 mA	20 mA	20 mA

LOGIC SYMBOL

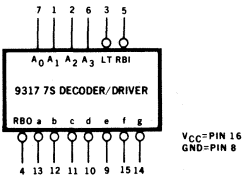


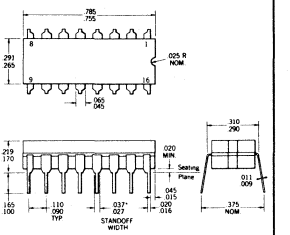
Fig. 3

ORDER INFORMATION

Specify U7B9317XXZ for 16-pin Dual In-Line Package or U4L9317XXZ for 16-pin Flatpak, where XXZ is 51Z for the −55°C to +125°C temperature range, or 59Z for the 0°C to +75°C temperature range. Z is used to identify the operating characteristics shown in table above. The following codes should be used when ordering the options: Z = 1 for 9317A; Z = 2 for 9317B; Z = 3 for 9317C; Z = 4 for 9317D.

PHYSICAL DIMENSIONS

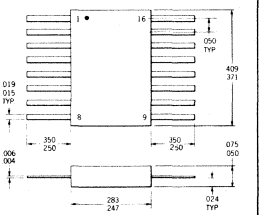
16 Lead Dual-In-Line



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for a conventional .020 inch diameter Lead
Leads are tin plated Kovar
Package weight is 2.2 grams
*The .037 / .027 dimension does not apply to the corner leads

Fig. 1

FLAT PACKAGE



NOTES:
All dimensions in inches
Leads are gold-plated Kovar
Package weight is 0.4 gram

Fig. 2

FAIRCHILD SEMICONDUCTOR

The 9317 seven segment decoder/driver accepts a 4 Bit BCD 8421 code input and produces the appropriate outputs for selection of segments in a seven segment matrix display used for representing the decimal numbers 0 - 9. The seven outputs (a, b, c, d, e, f, g) of the decoder select the corresponding segments in the matrix shown in Figure 3. The numeric designations chosen to represent the decimal numbers are shown in Figure 5. Code configurations in excess of binary nine disable the outputs.

The decoder has active low outputs so that it may be used directly to drive incandescent displays, or light emitting diode indicators.

The device has provision for automatic blanking of the leading and/or trailing edge zeroes in a multidigit decimal number, resulting in an easily readable decimal display, conforming to normal writing practice. In an eight digit mixed integer fraction decimal representation, using the automatic blanking capability, (0060.0300) would be displayed as (60.03). Leading edge zero suppression is obtained by connecting the Ripple Blanking Output ($\overline{RBO}$) of a decoder to the Ripple Blanking Input ($\overline{RBI}$) of the next lower stage device. The most significant decoder stage should have the $\overline{RBI}$ input grounded; and, since suppression of the least significant integer zero in a number is not usually desired, the $\overline{RBI}$ input of this decoder stage should be left open. A similar procedure for the fractional part of a display will provide automatic suppression of trailing edge zeroes.

The decoder has an active low input Lamp Test which overrides all other input combinations and enables a check to be made on possible display malfunctions. The $\overline{RBO}$ terminal of the decoder can be OR - tied with a modulating signal via an isolating buffer to achieve pulse duration intensity modulation. A suitable signal can be generated for this purpose by forming a variable frequency multivibrator with a cross coupled pair of DTμL gates.

Fig. 4
SEGMENT DESIGNATION

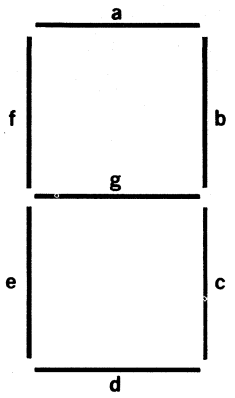


Fig. 5
TRUTH TABLE

$\overline{LT}$	$\overline{RBI}$	A_0	A_1	A_2	A_3	$\bar{a}$	$\bar{b}$	$\bar{c}$	$\bar{d}$	$\bar{e}$	$\bar{f}$	$\bar{g}$	$\overline{RBO}$	DECIMAL OR FUNCTION
L	X	X	X	X	X	L	L	L	L	L	L	L	H	
H	L	L	L	L	L	H	H	H	H	H	H	H	L	0
H	H	L	L	L	L	L	L	L	L	L	L	H	H	0
	X	H	L	L	L	H	H	H	H	L	L	H	H	1
		L	H	L	L	L	L	H	L	L	H	L	H	2
		H	H	L	L	L	L	L	L	H	H	L	H	3
		L	L	H	L	H	L	L	H	H	L	L	H	4
		H	L	H	L	L	H	L	L	H	L	L	H	5
		L	H	H	L	H	H	L	L	L	L	L	H	6
		H	H	H	L	L	L	L	H	H	H	H	H	7
		L	L	L	H	L	L	L	L	L	L	L	H	8
		H	L	L	H	L	L	L	H	H	L	L	H	9
		L	H	L	H	H	H	H	H	H	H	H	L	10
		H	H	L	H	H	H	H	H	H	H	H	L	11
		L	L	H	H	H	H	H	H	H	H	H	L	12
		H	L	H	H	H	H	H	H	H	H	H	L	13
		L	H	H	H	H	H	H	H	H	H	H	L	14
H	X	H	H	H	H	H	H	H	H	H	H	H	L	15

H = High Voltage Level
L = Low Voltage Level
X = Don't Care Condition

Fig. 6
NUMERICAL DESIGNATIONS

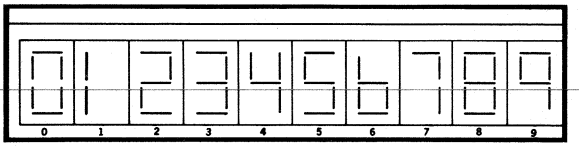


Table 1 — Loading Rules (1 U.L. = 1 DTμL Gate Input Load)

Inputs	Loading (51 & 59)	
	High State	Low State
A_0, A_1, A_2, A_3	1	1
$\overline{RBI}$	1	½
$\overline{LT}$	5	4.3

Outputs	Fan Out	
	51	59
$\overline{RBO}$	2.0	1.5

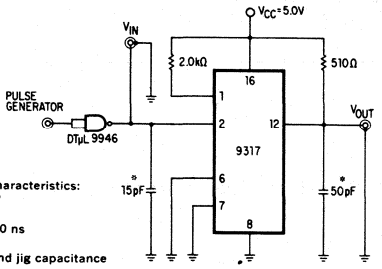
TABLE II —
ELECTRICAL CHARACTERISTICS ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$) (Part = U7B/4L931751Ƶ)

SYMBOL	CHARACTERISTIC	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage on $\overline{RBO}$ Only	3.0		3.0	4.0		3.0		Volts	$V_{CC} = 4.5\ V$, $I_{OH} = -70\ \mu A$ Pin 6 = V_{IL}, Pin 5 = V_{IH}
I_{CEX}	Output High Leakage Current				100	200		250	μA	$V_{CC} = 5.5\ V$, $V_{CEX} = 30\ V$ Inputs at V_{IH} or V_{IL} per Truth Table
V_{OL}	Output Low Voltage on $\overline{RBO}$ Only		0.4		0.21	0.4		0.4	Volts	$V_{CC} = 5.5\ V$, $I_{OL} = 3.1\ mA$
			0.4		0.21	0.4		0.4	Volts	$V_{CC} = 4.5\ V$, $I_{OL} = 2.4\ mA$
V_{OL}	Output Low Voltage Options A & B		0.8		0.50	0.8		0.8	Volts	$V_{CC} = 4.5\ V$, $I_{OL} = 40\ mA$
V_{OL}	Output Low Voltage Options C & D		0.4		0.21	0.4		0.4	Volts	$V_{CC} = 4.5\ V$, $I_{OL} = 20\ mA$
										Inputs at V_{IH} or V_{IL} per Truth Table
V_{LATCH}	Output Latch Voltage Option A & C	30		30			30		Volts	V_{CC} = Open, $I_{OUT} = 10\ mA$
V_{LATCH}	Output Latch Voltage Option B & D	20		20			20		Volts	Inputs = Open
V_{IH}	Input High Voltage	2.1		1.9			1.7		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		1.4			1.1		0.8	Volts	Guaranteed input low threshold for all inputs
I_F (Pin 3)	Input Load Current		−6.4			−6.4		−6.4	mA	$V_{CC} = 5.5\ V$, $V_F = 0.4\ V$
I_F (Pins 1, 2, 6, 7)	Input Load Current		−1.5			−1.5		−1.5	mA	$V_R = 5.5\ V$ on other inputs
I_F (Pin 5)	Input Load Current		−0.75			−0.75		−0.75	mA	
5 I_R (Pin 3)	Input Leakage Current					10		25	μA	$V_{CC} = 5.5\ V$, $V_R = 4.5\ V$
I_R (Pins 1, 2, 5, 6, 7)	Input Leakage Current					2.0		5.0	μA	Ground on other inputs
t_{pd+}	Switching Speed					500			ns	$V_{CC} = 5.0\ V$, See Figure 6
t_{pd-}	Switching Speed					500			ns	

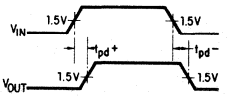
TABLE III —
ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0\ V \pm 5\%$) (Part = U7B/4L931759Ƶ)

SYMBOL	CHARACTERISTIC	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage on $\overline{RBO}$ Only	3.0		3.0	4.0		3.0		Volts	$V_{CC} = 4.75\ V$, $I_{OH} = -70\ \mu A$ Pin 6 = V_{IL}, Pin 5 = V_{IH}
I_{CEX}	Output High Leakage Current				100	200		250	μA	$V_{CC} = 5.25\ V$, $V_{CEX} = 30\ V$ Inputs at V_{IH} or V_{IL} per Truth Table
V_{OL}	Output Low Voltage on $\overline{RBO}$		0.45		0.25	0.45		0.45	Volts	$V_{CC} = 5.25\ V$, $I_{OL} = 2.75\ mA$
			0.45		0.25	0.45		0.45	Volts	$V_{CC} = 4.75\ V$, $I_{OL} = 2.4\ mA$
V_{OL}	Output Low Voltage Options A & B		0.9		0.65	0.9		0.9	Volts	$V_{CC} = 4.75\ V$, $I_{OL} = 40\ mA$
V_{OL}	Output Low Voltage Options C & D		0.45		0.25	0.45		0.45	Volts	$V_{CC} = 4.75\ V$, $I_{OL} = 20\ mA$
										Inputs at V_{IH} or V_{IL} per Truth Table
V_{LATCH}	Output Latch Voltage Option A & C	30		30			30		Volts	V_{CC} = Open, $I_{OUT} = 10\ mA$
V_{LATCH}	Output Latch Voltage Option B & D	20		20			20		Volts	Inputs = Open
V_{IH}	Input High Voltage	2.0		2.0			2.0		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F (Pin 3)	Input Load Current		−6.4			−6.4		−6.4	mA	$V_{CC} = 5.25\ V$, $V_F = 0.45\ V$
I_F (Pins 1, 2, 6, 7)	Input Load Current		−1.5			−1.5		−1.5	mA	$V_R = 5.25\ V$ on other inputs
I_F (Pin 5)	Input Load Current		−0.75			−0.75		−0.75	mA	
5 I_R (Pin 3)	Input Leakage Current					25		50	μA	$V_{CC} = 5.25\ V$, $V_R = 4.5\ V$
I_R (Pins 1, 2, 5, 6, 7)	Input Leakage Current					5.0		10	μA	Ground on other inputs
t_{pd+}	Switching Speed					500			ns	$V_{CC} = 5.0\ V$, See Figure 6
t_{pd-}	Switching Speed					500			ns	

Fig. 7—SWITCHING CIRCUIT AND WAVEFORMS

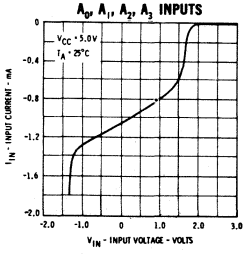


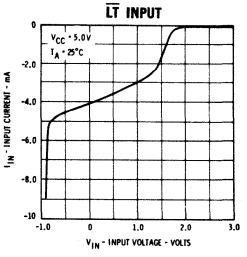
Pulse generator characteristics:
Amplitude = 3.0 V
Freq. = 500 kHz
Pulse width = 1000 ns
$t_r = t_f \leq 15$ ns
*Includes probe and jig capacitance

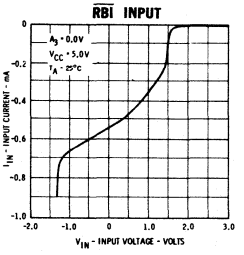


TYPICAL INPUT CHARACTERISTICS

INPUT CURRENT VERSUS INPUT VOLTAGE

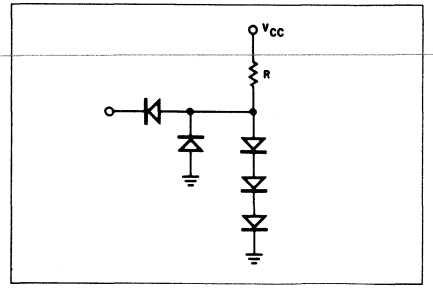






INPUTS

Equivalent Circuit

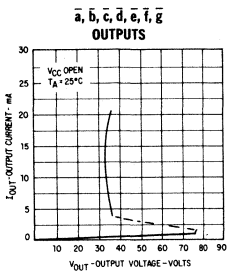


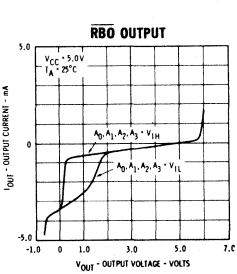
OUTPUT CHARACTERISTICS

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE

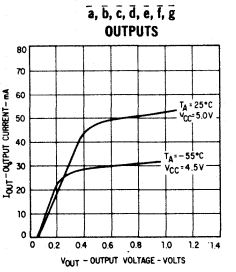
U7B/4L931751Z (−55°C to +125°C)

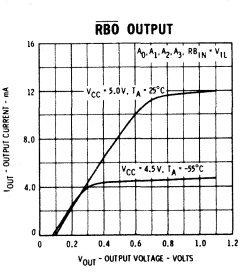
TYPICAL OUTPUT IN HIGH STATE





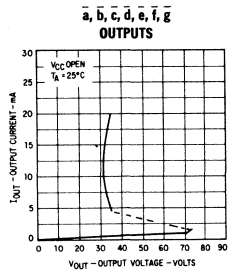
TYPICAL OUTPUT IN LOW STATE

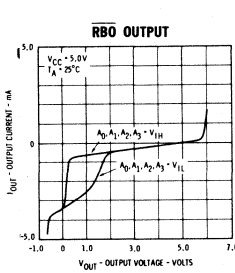




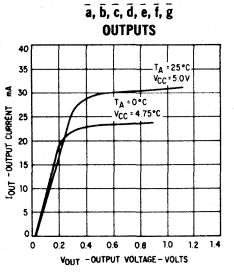
U7B/4L931759Z (0°C to +75°C)

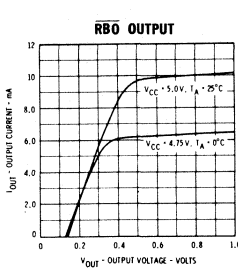
TYPICAL OUTPUT IN HIGH STATE





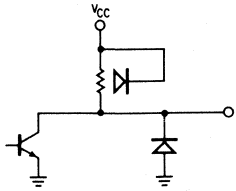
TYPICAL OUTPUT IN LOW STATE



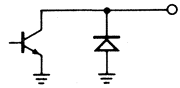


OUTPUTS

Equivalent Circuit (Pin 4)



Equivalent Circuit (Pins 9 thru 15)



APPLICATIONS

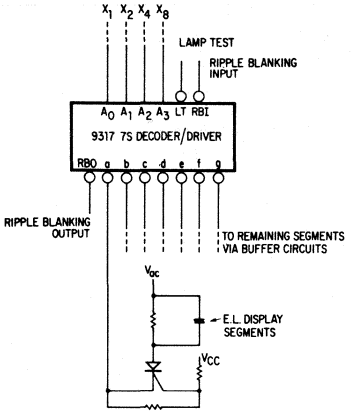


Fig. 8
9317 Seven Segment Decoder Driving Electro-Luminescent Display

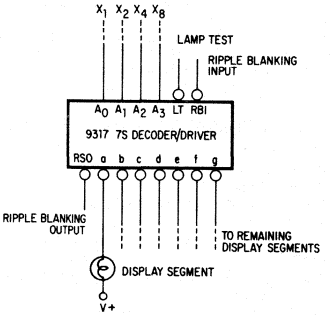


Fig. 9
9317 Seven Segment Decoder Driving Incandescent Lamp Display

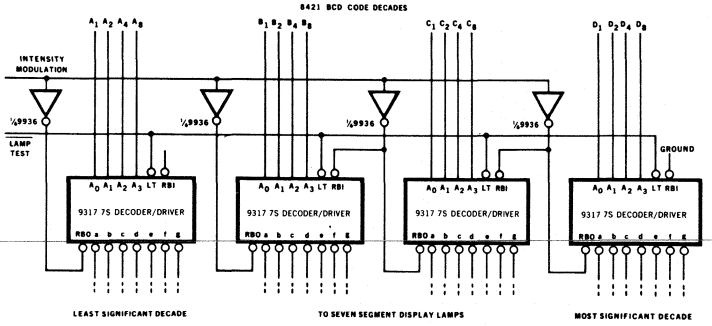


Fig. 10—FOUR DECADE SEVEN SEGMENT INTEGER DISPLAY SCHEME
This scheme incorporates automatic blanking of leading edge zeroes and intensity modulation using an external variable duty cycle signal.

9318

MSI EIGHT INPUT PRIORITY ENCODER

A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

GENERAL DESCRIPTION — The MSI 9318 is a multipurpose encoder designed to accept 8 inputs and produce a binary weighted code of the highest order input. The circuit uses TTμL for high speed and high fanout capability, and is compatible with all members of the CCSL group of digital integrated circuits.

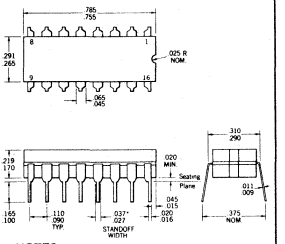
FEATURES:

- **MULTI-FUNCTION CAPABILITY**
  - **—CODE CONVERSIONS**
  - **—MULTI-CHANNEL D/A CONVERTER**
  - **—DECIMAL TO BCD CONVERTER**
  - **—CASCADING FOR PRIORITY ENCODING OF N BITS**
- **INPUT ENABLE CAPABILITY**
- **PRIORITY ENCODING . . . . AUTOMATIC SELECTION OF HIGHEST PRIORITY INPUT LINE**
- **OUTPUT ENABLE . . . . . ACTIVE LOW WHEN ALL INPUTS HIGH**
- **GROUP SIGNAL OUTPUT . . . ACTIVE WHEN ANY INPUT IS LOW**
- **TYPICAL POWER DISSIPATION OF 250 mW**
- **INPUT/OUTPUT CHARACTERISTICS PROVIDE EASY INTERFACING WITH FAIRCHILD DTμL, LPDTμL, TTμL, AND MSI FAMILIES (CCSL)**
- **ALL CERAMIC HERMETIC 16 PIN DUAL IN-LINE PACKAGE**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**

ABSOLUTE MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to GND	−0.5 V to +7 V
Voltages Applied to Outputs for High Output State	−0.5 V to V_{CC} Value
Input Voltage (D.C.)	−0.5 V to +5.5 V
Output Current, into Low Outputs	50 mA

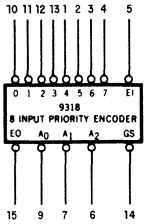
PHYSICAL DIMENSIONS
16 Lead Dual In-Line



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for a conventional .020 inch diameter Lead
Leads are tin plated Kovar
Package weight is 2.2 grams
*The .037 dimension does not apply to the corner leads

Fig. 1

LOGIC SYMBOL



V_{CC} = Pin 16
Gnd = Pin 8

FLAT PACKAGE

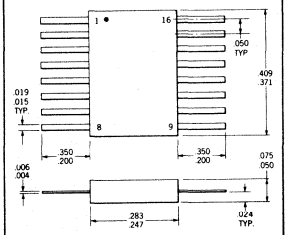


Fig. 2

ORDER INFORMATION:

Specify U6B9318XXX for 16 pin Dual In-Line package or U4L9318XXX for 16 pin Flatpak where XXX is 51X −55°C to +125°C temperature or 59X for 0°C to 75°C temperature.

FAIRCHILD
SEMICONDUCTOR

FUNCTIONAL DESCRIPTION: The MSI 9318 8 Input Priority Encoder accepts data from 8 active low inputs and provides a binary representation on the 3 active low outputs. A priority is assigned to each input so that when two or more inputs are simultaneously active, the input with the highest priority is represented on the output, with input line 7 having the highest priority.

A high on the input enable (EI) will force all outputs to the inactive (high) state and allow new data to settle without producing erroneous information at the outputs.

Provided with the 3 data outputs are a group signal output (GS) and an enable output (EO). The GS is active level low when any input is low; this indicates when any input is active. The EO is active level low when all inputs are high. Using the output enable along with the input enable allows priority encoding of N input signals. Both EO and GS are inactive high when the input enable is high.

The Truth Table and Loading Rules are shown in Figures 3 and 4 respectively.

Fig. 3 — TRUTH TABLE

EI	0	1	2	3	4	5	6	7	GS	A_0	A_1	A_2	EO
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	H	L	L	H
L	X	X	X	X	X	L	H	H	L	L	H	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	L	L	L	H	H
L	X	X	L	H	H	H	H	H	L	H	L	H	H
L	X	L	H	H	H	H	H	H	L	L	H	H	H
L	L	H	H	H	H	H	H	H	L	H	H	H	H

H = High Voltage Level
L = Low Voltage Level
X = Don't Care

Fig. 4 — LOADING RULES

INPUTS	LOADING
0	1 U.L.
EI, 1, 2, 3, 4, 5, 6, 7	2 U.L.
OUTPUTS	**FANOUT**
EO	5 U.L.
GS	6 U.L.
A_0, A_1, A_2	10 U.L.

(1 U.L. = TTμL Gate Input Load)

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

EQUIVALENT INPUT CIRCUIT

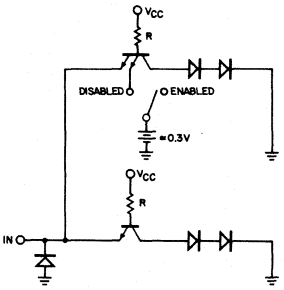


Fig. 5

OUTPUT HIGH EQUIVALENT CIRCUIT

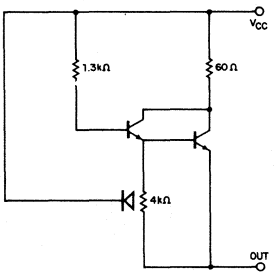


Fig. 6

OUTPUT LOW EQUIVALENT CIRCUIT

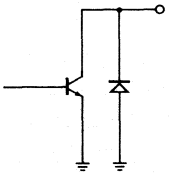
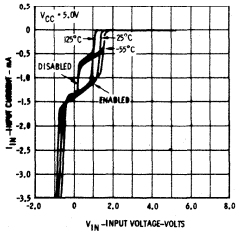
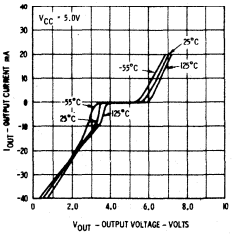


Fig. 7

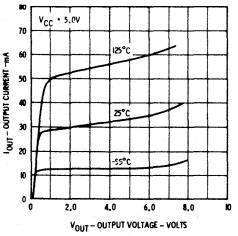
INPUT CURRENT VERSUS INPUT VOLTAGE



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE OUTPUT HIGH STATE



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE OUTPUT LOW STATE



FAIRCHILD MEDIUM SCALE INTEGRATION 9318

ELECTRICAL CHARACTERISTICS ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$) (Part #U6B/4L931851X)

SYMBOL	CHARACTERISTIC	LIMITS −55°C MIN.	−55°C MAX.	+25°C MIN.	+25°C TYP.	+25°C MAX.	+125°C MIN.	+125°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	$V_{CC} = 4.5\ V$, $I_{OH} = -1.2\ mA$ (Pins 6, 7, 9) $V_{CC} = 4.5\ V$, $I_{OH} = -0.72\ mA$ (Pin 14) $V_{CC} = 4.5\ V$, $I_{OH} = -0.60\ mA$ (Pin 15)
V_{OL}	Output Low Voltage		0.4		0.21	0.4		0.4	Volts	$V_{CC} = 5.5\ V$, $I_{OL} = 16\ mA$ (Pins 6, 7, 9) $V_{CC} = 5.5\ V$, $I_{OL} = 9.6\ mA$ (Pin 14) $V_{CC} = 5.5\ V$, $I_{OL} = 8.0\ mA$ (Pin 15) $V_{CC} = 4.5\ V$, $I_{OL} = 12.4\ mA$ (Pins 6, 7, 9) $V_{CC} = 4.5\ V$, $I_{OL} = 7.5\ mA$ (Pin 14) $V_{CC} = 4.5\ V$, $I_{OL} = 6.2\ mA$ (Pin 15)
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed High Input Threshold
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed Low Input Threshold
I_F (Pin 10)	Input Load Current		−1.6		−1.1	−1.6		−1.6	mA	$V_{CC} = 5.5\ V$, $V_F = 0.4\ V$, $V_R = 5.5\ V$ on other inputs
$2\ I_F$	Input Load Current		−3.2		−2.2	−3.2		−3.2		
I_F (Pin 10)	Input Load Current		−1.24		−0.97	−1.24		−1.24	mA	$V_{CC} = 4.5\ V$, $V_F = 0.4\ V$, $V_R = 5.5\ V$ on other inputs
$2\ I_F$	Input Load Current		−2.48		−1.94	−2.48		−2.48		
I_R (Pin 10)	Input Leakage				15	60		60	μA	$V_{CC} = 5.5\ V$, $V_R = 4.5\ V$
$2\ I_R$	Input Leakage				30	120		120		Ground on other inputs
I_{PDH}	Power Dissipation				50	70		70	mA	$V_{CC} = 5.0\ V$ (Gnd Pins 4, 5) All other pins high

ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0V \pm 5\%$) (Part #U6B/4L931859X)

SYMBOL	CHARACTERISTIC	LIMITS 0°C MIN.	0°C MAX.	+25°C MIN.	+25°C TYP.	+25°C MAX.	+75°C MIN.	+75°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	$V_{CC} = 4.75\ V$, $I_{OH} = -1.2\ mA$ (Pins 6, 7, 9) $V_{CC} = 4.75\ V$, $I_{OH} = -0.72\ mA$ (Pin 14) $V_{CC} = 4.75\ V$, $I_{OH} = -0.60\ mA$ (Pin 15)
V_{OL}	Output Low Voltage		0.45		0.21	0.45		0.45	Volts	$V_{CC} = 5.25\ V$, $I_{OL} = 16\ mA$ (Pins 6, 7, 9) $V_{CC} = 5.25\ V$, $I_{OL} = 9.6\ mA$ (Pin 14) $V_{CC} = 5.25\ V$, $I_{OL} = 8.0\ mA$ (Pin 15) $V_{CC} = 4.75\ V$, $I_{OL} = 14.1\ mA$ (Pins 6, 7, 9) $V_{CC} = 4.75\ V$, $I_{OL} = 8.5\ mA$ (Pin 14) $V_{CC} = 4.75\ V$, $I_{OL} = 7.1\ mA$ (Pin 15)
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed High Input Threshold
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed Low Input Threshold
I_F (Pin 10)	Input Load Current		−1.6		−1.0	−1.6		−1.6	mA	$V_{CC} = 5.5\ V$, $V_F = 0.4\ V$, $V_R = 5.5\ V$ on other inputs
$2\ I_F$	Input Load Current		−3.2		−2.0	−3.2		−3.2		
I_F (Pin 10)	Input Load Current		−1.41		−0.9	−1.41		−1.41	mA	$V_{CC} = 4.5\ V$, $V_F = 0.4\ V$, $V_R = 5.5\ V$ on other inputs
$2\ I_F$	Input Load Current		−2.82		−1.8	−2.82		−2.82		
I_R (Pin 10)	Input Leakage				15	60		60	μA	$V_{CC} = 5.25\ V$, $V_R = 4.5\ V$
$2\ I_R$	Input Leakage				30	120		120		Ground on other inputs
I_{PDH}	Power Dissipation				55	80		80	mA	$V_{CC} = 5.0\ V$, (Gnd Pins 4, 5) All other pins high

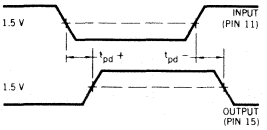
A.C. CHARACTERISTICS ($T_A = 25°C$, $V_{CC} = 5.0\ V$, Pin 8 = GND)

SYMBOL	CHARACTERISTIC	LIMITS (51X) MIN.	(51X) MAX.	(59X) MIN.	(59X) MAX.	UNITS	CONDITIONS
t_{pd+}	(Data Input to Enable Output)	2.0	10	2.0	15	ns	See Figure 8
t_{pd-}	(Data Input to Enable Output)	5.0	30	5.0	40	ns	
t_{pd+}	(Enable Input to Group Signal)	8.0	16	8.0	20	ns	See Figure 9
t_{pd-}	(Enable Input to Group Signal)	14	25	14	31	ns	
t_{pd+}	(Enable Input to Enable Output)	7.0	15	7.0	21	ns	See Figure 10
t_{pd-}	(Enable Input to Enable Output)	18	40	18	45	ns	
t_{pd+}	(Enable Input to Data Output)	8.0	20	8.0	25	ns	See Figure 11
t_{pd-}	(Enable Input to Data Output)	10	25	10	30	ns	
t_{pd+}	(Data Input to Group Signal)	12	40	12	45	ns	See Figure 12
t_{pd-}	(Data Input to Group Signal)	12	25	12	30	ns	
t_{pd+}	(Data Input to Data Output)	14	30	14	38	ns	See Figure 13
t_{pd-}	(Data Input to Data Output)	15	30	15	38	ns	

AC CHARACTERISTICS

All measurements are made with $V_{CC} = 5.0$ V applied to Pin 16 and Pin 8 grounded. The active input is driven by a 9002 TTμL gate. The input and output pins under test are loaded with 15 pF of capacitance. (This includes probe & jig capacitance).

Fig. 8
DATA INPUT TO ENABLE OUTPUT



Other Conditions: Pin 5 = Gnd
Pins 1, 2, 3, 4, 10, 12, 13 = V_{CC} through 750 Ω

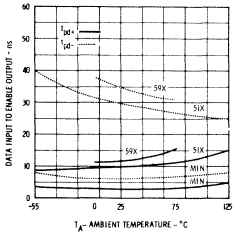
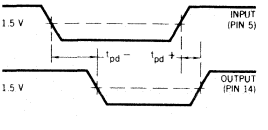


Fig. 9
ENABLE INPUT TO GROUP SIGNAL



Other Conditions: Pin 10 = Gnd
Pins 1, 2, 3, 4, 11, 12, 13 = V_{CC} through 750 Ω

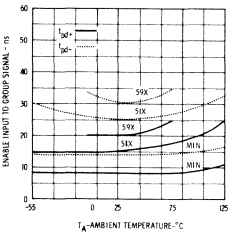
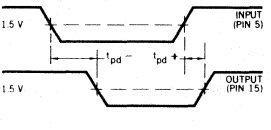


Fig. 10
ENABLE INPUT TO ENABLE OUTPUT



Other Conditions:
Pins 1, 2, 3, 4, 10, 11, 12, 13 = V_{CC} through 750 Ω

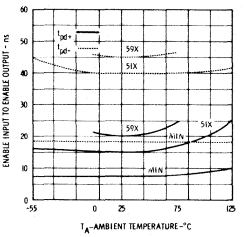
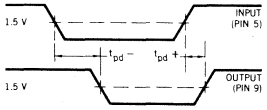


Fig. 11
ENABLE INPUT TO DATA OUTPUT



Other Conditions: Pin 4 = Gnd
Pins 1, 2, 3, 10, 11, 12, 13 = V_{CC} through 750 Ω

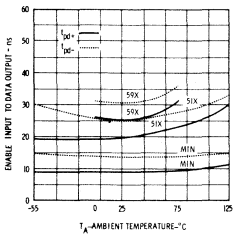
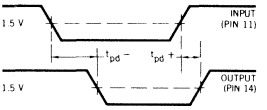


Fig. 12
DATA INPUT TO GROUP SIGNAL



Other Conditions: Pin 5 = Gnd
Pins 1, 2, 3, 4, 10, 12, 13 = V_{CC} through 750 Ω

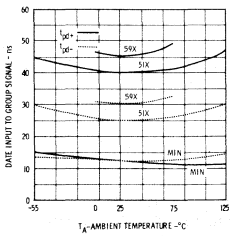
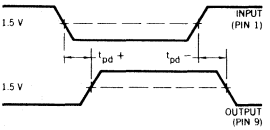
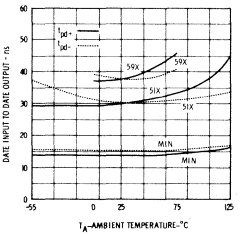


Fig. 13
DATA INPUT TO DATA OUTPUT



Other Conditions: Pins 5, 11 = Gnd
Pins 2, 3, 4, 10, 12, 13 = V_{CC} through 750 Ω



APPLICATIONS

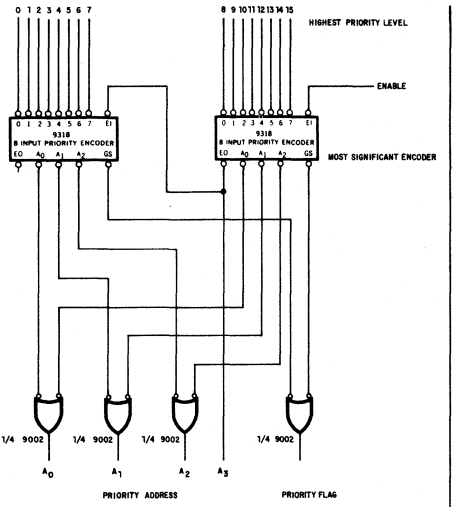


Fig. 14

16 INPUT PRIORITY ENCODER

The number of priority levels can be increased by cascading 9318 encoders. This may be accomplished by connecting the most significant encoder's enable output (EO) to the next most significant encoder's enable input (EI).

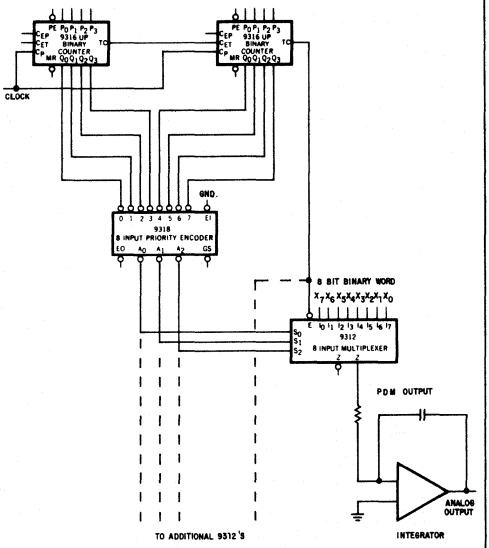


Fig. 15

MULTIPLE CHANNEL D/A CONVERTER

The 9318 supplies a code sequence to the multiplexer, such that the most significant binary input is sampled for 50% of the count cycle, the next most significant input is sampled for 25% of the cycle, and so on. This sampling produces a PDM Output which can be integrated or in many cases, such as panel meters, motors, or audio speakers, fed directly to the analog output device. For each additional channel, a multiplexer and integrator are required.

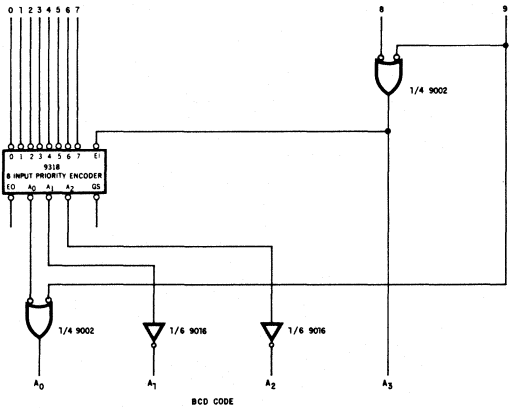


Fig. 16

DECIMAL TO BCD CONVERTER

The converter produces a BCD code corresponding to the most significant active low decimal input.

APPLICATIONS

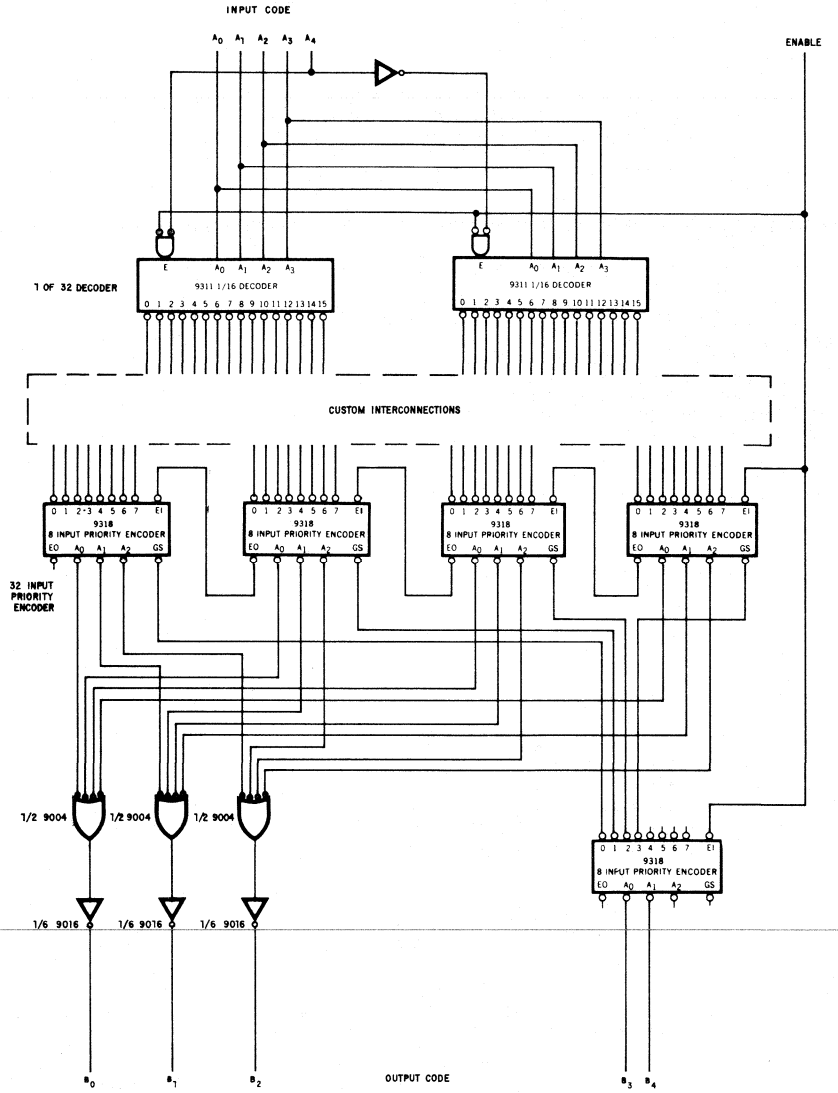


Fig. 17
5 BIT CODE CONVERTER

The 5 bit input code applied to the one of thirty-two decoder produces one low output. This low decoder output can be arbitrarily connected to any encoder input to produce any desired 5 bit output code. To cover all combinations of input codes, wiring connections are made between every possible decoder output and appropriate encoder inputs.

9321

MSI DUAL ONE-OF-FOUR DECODER

A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

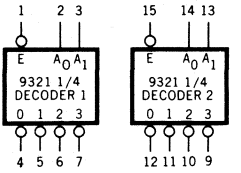
GENERAL DESCRIPTION — The 9321 consists of two independent multipurpose decoders, each designed to accept 2 inputs and provide 4 mutually exclusive outputs. In addition an active low enable input is provided for each decoder which gives demultiplexing capability. The circuit uses TTμL for high speed and high fanout capability, and is compatible with all members of the CCSL group of digital integrated circuits.

- **MULTI-FUNCTION CAPABILITY**
- **MUTUALLY EXCLUSIVE OUTPUTS**
- **GUARANTEED FANOUT OF 10 TTμL LOADS OVER THE FULL TEMPERATURE RANGE AND SUPPLY VOLTAGE RANGES**
- **HIGH CAPACITIVE DRIVE CAPABILITY**
- **DEMULTIPLEXING CAPABILITY**
- **TYPICAL POWER DISSIPATION OF 150 mW**
- **THE INPUT/OUTPUT CHARACTERISTICS PROVIDE EASY INTERFACING WITH FAIRCHILD MSI, DTμL, LPDTμL AND TTμL FAMILIES (CCSL).**
- **ALL CERAMIC "HERMETIC" 16-PIN DUAL IN-LINE PACKAGE**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED LINE TERMINATION EFFECTS**
- **ACTIVE LOW ENABLE FOR EACH DECODER**

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7 V
Voltage Applied to Outputs for high output state	−0.5 V to +V_{CC} value
Input Voltage (D.C.)	−0.5 V to +5.5 V

LOGIC SYMBOL

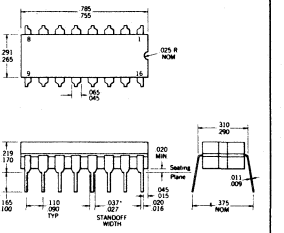


V_{CC} = PIN 16
GND = PIN 8

ORDER INFORMATION

Specify U7B9321XXX for 16-pin Dual In-Line package or U4L9321XXX for 16-pin Flat Package where XXX is 51X for the −55°C to +125°C temperature range, or 59X for the 0°C to +75°C temperature range.

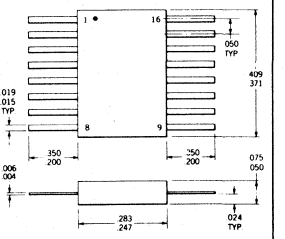
PHYSICAL DIMENSIONS
16 Lead Large Cavity (MSI) Dual In-Line



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020" diameter lead
Leads are tin-plated kovar
Package weight is 2.2 grams
*The .037/.027 dimension does not apply to the corner leads

Fig. 1

PHYSICAL DIMENSIONS
16 Lead BeO Cerpak



NOTES:
All dimensions in inches
Leads are gold-plated kovar
Package weight is 0.4 gram

Fig. 2

FAIRCHILD
SEMICONDUCTOR

FUNCTIONAL DESCRIPTION — The 9321 consists of two separate decoders each designed to accept two binary weighted inputs and provide four mutually exclusive active low outputs as shown in Figure 1. Each decoder can be used as a four output demultiplexer by using the enable as a data input.

The active low outputs facilitate memory addressing for units such as the 4102 associative memory. The active low outputs are also compatible with the active low enables of other MSI elements making the 9321 useful in logic selection schemes.

The Truth Table and Loading Rules for the 9321 are shown in Tables I & II.

TABLE I — TRUTH TABLE

DECODER I & II

$\overline{E}$	A_0	A_1	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L
H	X	X	H	H	H	H

H = High Voltage Level
L = Low Voltage Level
X = Level Does Not Affect Output

TABLE II — LOADING RULES

TTμL INPUT LOAD AND DRIVE FACTORS

INPUTS	LOADING
All Inputs	1 U.L.

OUTPUTS	DRIVE FACTOR
All Outputs	10 U.L.

(1 U.L. = TTμL Gate Input Load)

CCSL INPUT LOAD AND DRIVE FACTORS

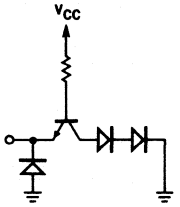
GRADE	INPUTS	LOADING
59	All Inputs	12/11
51	All Inputs	12/10

GRADE	OUTPUTS	DRIVE FACTOR
59	All Outputs	120/94
51	All Outputs	120/78

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

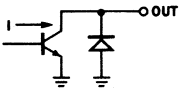
INPUTS

EQUIVALENT CIRCUIT

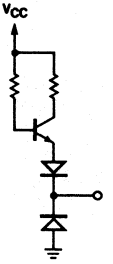


OUTPUTS

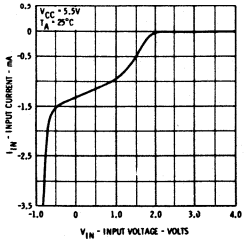
EQUIVALENT CIRCUIT
OUTPUT LOW



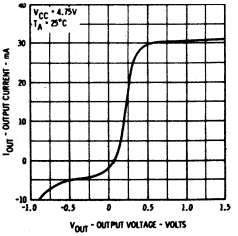
EQUIVALENT CIRCUIT
OUTPUT HIGH



INPUT CURRENT VERSUS INPUT VOLTAGE



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE OUTPUT LOW



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE OUTPUT HIGH

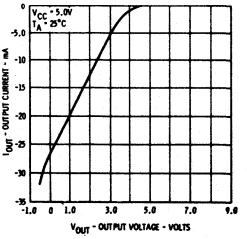


TABLE III — ELECTRICAL CHARACTERISTICS ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$) (Part #U7B/4L932151X) Units are pulse tested

SYMBOL	CHARACTERISTIC	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	$V_{CC} = 4.5\ V$, $I_{OH} = -0.6\ mA$
V_{OL}	Output Low Voltage		0.4		0.2	0.4		0.4	Volts	$V_{CC} = 4.5\ V$, $I_{OL} = 12.4\ mA$ $V_{CC} = 5.5\ V$, $I_{OL} = 16.0\ mA$
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		−1.24		−0.97	−1.24		−1.24	mA	$V_{CC} = 4.5\ V$, $V_F = 0.4\ V$
			−1.6		−1.10	−1.6		−1.6	mA	$V_{CC} = 5.5\ V$
I_R	Input Leakage Current				6.0	60		60	μA	$V_{CC} = 5.5\ V$, $V_R = 4.5\ V$
I_{PD}	V_{CC} Current				30	45			mA	$V_{CC} = 5.0\ V$ All inputs = GND
t_{pd+}	Turn Off Delay A Input to Output			15	22	30			ns	$V_{CC} = 5.0\ V$
t_{pd-}	Turn On Delay A Input to Output			13	19	25			ns	$C_L = 15\ pF$, See Fig. 6
t_{pd+}	Turn Off Delay $\overline{E}$ Input to Output			8.0	15	20			ns	$V_{CC} = 5.0\ V$
t_{pd-}	Turn On Delay $\overline{E}$ Input to Output			7.0	14	19			ns	$C_L = 15\ pF$, See Fig. 7

TABLE IV — ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0\ V \pm 5\%$) (Part #U7B/4L932159X) Units are pulse tested

SYMBOL	CHARACTERISTIC	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	$V_{CC} = 4.75\ V$, $I_{OH} = -0.6\ mA$
V_{OL}	Output Low Voltage		0.45		0.2	0.45		0.45	Volts	$V_{CC} = 4.75\ V$, $I_{OL} = 14.1\ mA$ $V_{CC} = 5.25\ V$, $I_{OL} = 16.0\ mA$
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		−1.41		−0.9	−1.41		−1.41	mA	$V_{CC} = 4.75\ V$, $V_F = 0.45\ V$
			−1.6		−1.0	−1.6		−1.6	mA	$V_{CC} = 5.25\ V$
I_R	Input Leakage Current				6.0	60		60	μA	$V_{CC} = 5.25\ V$, $V_R = 4.5\ V$
I_{PD}	V_{CC} Current				30	50			mA	$V_{CC} = 5.0\ V$ All Inputs = GND
t_{pd+}	Turn Off Delay A Input to Output			15	22	35			ns	$V_{CC} = 5.0\ V$
t_{pd-}	Turn On Delay A Input to Output			13	19	30			ns	$C_L = 15\ pF$, See Fig. 6
t_{pd+}	Turn Off Delay $\overline{E}$ Input to Output			8.0	15	25			ns	$V_{CC} = 5.0\ V$
t_{pd-}	Turn On Delay $\overline{E}$ Input to Output			7.0	14	23			ns	$C_L = 15\ pF$, See Fig. 7

AC CHARACTERISTICS

All measurements are made with $V_{CC} = 5.0\ V$ applied to Pin 16 and Pin 8 grounded. The active input is driven by a 9002 TTμL gate. The input and output pins under test are loaded with 15pF of capacitance (this includes probe and jig capacitance).

DATA INPUT TO DATA OUTPUT

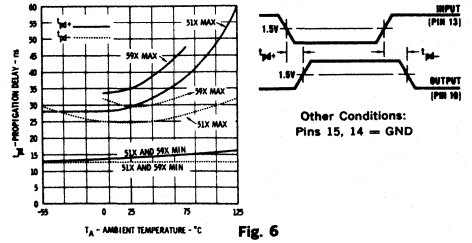


Fig. 6

ENABLE INPUT TO DATA OUTPUT

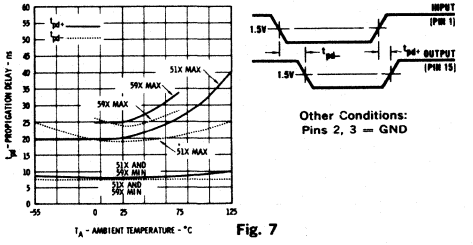


Fig. 7

APPLICATIONS

DUAL 1 OUT OF 10 DECODER WITH ENABLES (ACCEPTS BCD INPUTS)

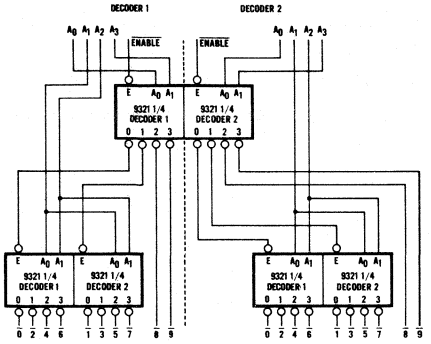
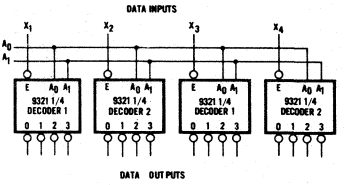


Fig. 8

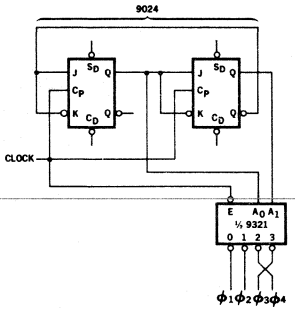
4 BIT DIGITAL DEMULTIPLEXER



Data may be routed from a source to any of four outputs by addressing that output. All non-addressed outputs remain high.

Fig. 9

4-PHASE CLOCK GENERATOR



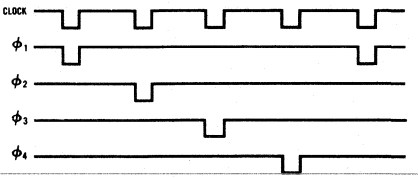


Fig. 10

9322

MSI QUAD TWO-INPUT MULTIPLEXER

A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

GENERAL DESCRIPTION — The 9322 is a monolithic, high speed, quad two-input digital multiplexer circuit, constructed with the Fairchild Planar* epitaxial process. It consists of four multiplexing circuits with common select and enable logic, each circuit contains two inputs and one output. The circuit uses TTμL for high speed, high fanout operation and is compatible with all other members of the CCSL family of digital integrated circuits.

- **MULTIFUNCTION CAPABILITY**
- **20 ns THROUGH DELAY**
- **ON-CHIP SELECT LOGIC DECODING**
- **FULLY BUFFERED OUTPUTS**
- **THE INPUT/OUTPUT CHARACTERISTICS PROVIDE EASY INTERFACING WITH FAIRCHILD DTμL, LPDTμL, TTμL, AND MSI FAMILIES (CCSL).**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS.**

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	0.5 V to +7.0 V
Voltage Applied to Output when output is high	0 V to +V_{CC} value
Input Voltage (DC) (See Note 1)	−0.5 V to +5.5 V
Input Current (DC) (See Note 1)	−30 mA to +5 mA
Current into Output when output is low	+30 mA

Note 1—either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

LOGIC DIAGRAM

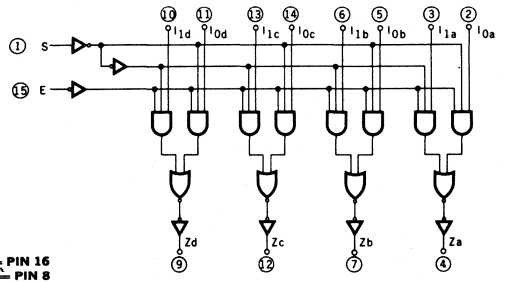
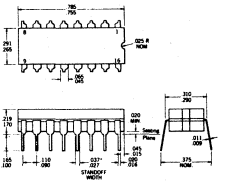


Fig. 4

ORDER INFORMATION — Specify U7B9322XXX for 16-pin Dual In-Line package or U4L9322XXX for 16-pin Flatpak, where XXX is 51X for the −55°C to +125°C temperature range, or 59X for the 0°C to +75°C temperature range.

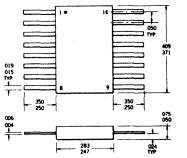
DUAL IN-LINE PACKAGE



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020" diameter lead
Leads are tin-plated Kovar
Package weight is 2.2 grams
*The .027/.037 dimension does not apply to the corner leads

Fig. 1

FLAT PACKAGE



NOTES:
All dimensions in inches
Leads are gold-plated kovar
Package weight is 0.4 gram

Fig. 2

LOGIC SYMBOL

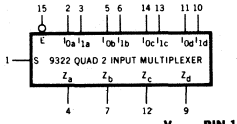


Fig. 3

*Planar is a patented Fairchild process.

FAIRCHILD
SEMICONDUCTOR

FUNCTIONAL DESCRIPTION

The 9322 quad two input multiplexer is a member of the Fairchild family of compatible Medium Scale Integrated (MSI) digital building blocks. It provides this family with the ability to select four bits of either data or control from two sources, in one package. The enable input ($\bar{E}$) is active low. When not activated all outputs (Z) are low regardless of all other inputs.

The 9322 quad two input multiplexer is the logical implementation of a four-pole two-position switch, with the position of the switch being set by the logic levels supplied to the one select input. The logic equations for the outputs are shown below:

$Z_a = E \cdot (I_{1a} \cdot S + I_{0a} \cdot \bar{S})$ $\quad Z_b = E \cdot (I_{1b} \cdot S + I_{0b} \cdot \bar{S})$

$Z_c = E \cdot (I_{1c} \cdot S + I_{0c} \cdot \bar{S})$ $\quad Z_d = E \cdot (I_{1d} \cdot S + I_{0d} \cdot \bar{S})$

A common use of the 9322 would be the moving of data from a group of registers to four common output busses. The particular register from which the data came would be determined by the state of the select input. A less obvious use is as a function generator. The 9322 can generate four functions of two variables with one variable common. This is useful for implementing gating functions.

TRUTH TABLE

ENABLE	SELECT INPUT	INPUTS		OUTPUT
$\bar{E}$	S	I_{0X}	I_{1X}	Z_X
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

Identical for Each Multiplexer

L = low voltage level
H = high voltage level
X = either high or low logic level

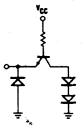
LOADING RULES

(1 U.L. = 1 TTμL gate input load)

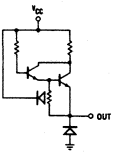
INPUTS	LOADING	
I_{0a}, I_{1a}, I_{0b}, I_{1b}, I_{0c}, I_{1c}, I_{0d}, I_{1d} S, $\bar{E}$	1 U.L.	
OUTPUTS	FANOUT AT LOGIC LEVEL	
	HIGH	LOW
Z_a, Z_b, Z_c, Z_d	20 U.L.	10 U.L.

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

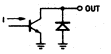
INPUT EQUIVALENT CIRCUIT



OUTPUT EQUIVALENT CIRCUIT (Output High)



OUTPUT EQUIVALENT CIRCUIT (Output Low)



INPUT CURRENT VERSUS INPUT VOLTAGE

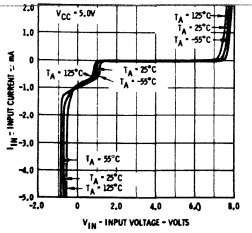


Fig. 5

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)

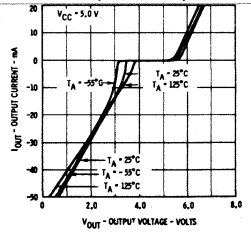


Fig. 6

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)

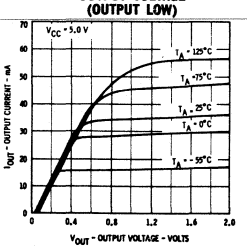


Fig. 7

ELECTRICAL CHARACTERISTICS* ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$) (Part No. U7B/4L932251X)

SYMBOL	CHARACTERISTICS	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	$V_{CC} = 4.5\ V$ $I_{OH} = -1.2\ mA$ Inputs at threshold voltages (V_{IL} or V_{IH}) as per truth table
V_{OL}	Output Low Voltage		0.4		0.21	0.4		0.4	Volts	$V_{CC} = 5.5\ V$ $I_{OL} = 16.0\ mA$ $V_{CC} = 4.5\ V$ $I_{OL} = 12.4\ mA$ Inputs at threshold voltages (V_{IL} or V_{IH}) as per truth table
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F (all inputs)	Input Load Current		−1.6		−1.1	−1.6		−1.6	mA	$V_{CC} = 5.5\ V$ $V_F = 0.4\ V$
			−1.24		−0.85	−1.24		−1.24	mA	$V_{CC} = 4.5\ V$ Input selected
I_R (all inputs)	Input Leakage Current				8.0	60		60	μA	$V_{CC} = 5.5\ V$ $V_R = 4.5\ V$
I_{PDH}	V_{CC} Current		43		30	43		43	mA	$V_{CC} = 5.0\ V$ All inputs high
t_{pd+} (S to Z_a)	Switching Speed				17	25			ns	$V_{CC} = 5.0\ V$, $C_L = 15\ pF$, See Figure 8
t_{pd-} (S to Z_a)	Switching Speed				20	27			ns	

*Pulse Tested

ELECTRICAL CHARACTERISTICS* ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0\ V \pm 5\%$) (Part No. U7B/4L932259X)

SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	$V_{CC} = 4.75\ V$ $I_{OH} = -1.2\ mA$ Inputs at threshold voltages (V_{IL} or V_{IH}) as per truth table
V_{OL}	Output Low Voltage		0.45		0.21	0.45		0.45	Volts	$V_{CC} = 5.25\ V$ $I_{OL} = 16.0\ mA$ $V_{CC} = 4.75\ V$ $I_{OL} = 14.1\ mA$ Inputs at threshold voltages (V_{IL} or V_{IH}) as per truth table
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F (all inputs)	Input Load Current		−1.6		−1.0	−1.6		−1.6	mA	$V_{CC} = 5.25\ V$ $V_F = 0.45\ V$
			−1.41		−0.91	−1.41		−1.41	mA	$V_{CC} = 4.75\ V$ Input selected
I_R (all inputs)	Input Leakage Current				8.0	60		60	μA	$V_{CC} = 5.25\ V$ $V_R = 4.5\ V$
I_{PDH}	V_{CC} Current		45		30	45		45	mA	$V_{CC} = 5.0\ V$ All inputs high
t_{pd+} (S to Z_a)	Switching Speed				17	30			ns	$V_{CC} = 5.0\ V$, $C_L = 15\ pF$, See Figure 8
t_{pd-} (S to Z_a)	Switching Speed				20	31			ns	

*Pulse Tested

A.C. CHARACTERISTICS

SWITCHING WAVEFORMS

All inputs are outputs of TTμL 9000 series gates loaded with 15 pF. All outputs are loaded with the same capacitance (referred to as C_L) and only with capacitance.

t_{pd}; S to Z_a
CONDITIONS
Pins 2, 15 = GND.
Pin 3 = V_{CC}

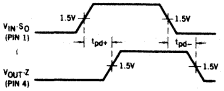


Fig. 8

t_{pd}; $\overline{E}$ to Z_a
CONDITIONS
All Other Inputs High

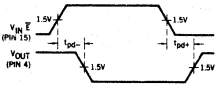


Fig. 9

t_{pd}; I_{0a} to Z_a
CONDITIONS
Pins 1, 15 = GND.

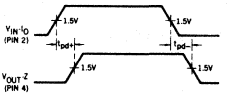


Fig. 10

SWITCHING CHARACTERISTICS

TURN OFF DELAY TIME VERSUS AMBIENT TEMPERATURE (S to Z_a)

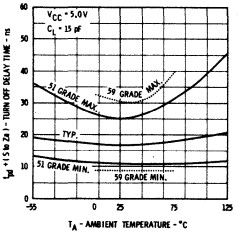


Fig. 11

TURN ON DELAY TIME VERSUS AMBIENT TEMPERATURE (S to Z_a)

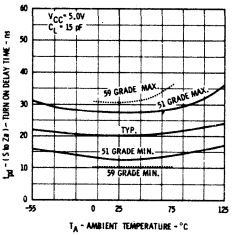


Fig. 12

TURN OFF DELAY TIME VERSUS AMBIENT TEMPERATURE ($\overline{E}$ to Z_a)

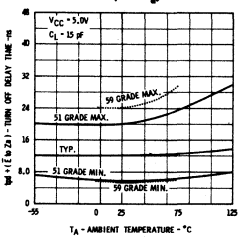


Fig. 13

TURN ON DELAY TIME VERSUS AMBIENT TEMPERATURE ($\overline{E}$ to Z_a)

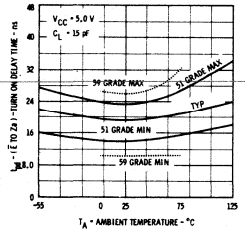


Fig. 14

TURN OFF DELAY TIME VERSUS AMBIENT TEMPERATURE (I_{1a} to Z_a)

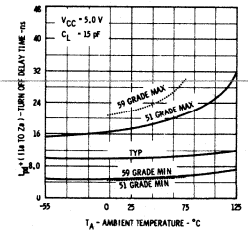


Fig. 15

TURN ON DELAY TIME VERSUS AMBIENT TEMPERATURE (I_{1a} to Z_a)

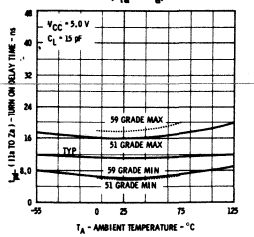


Fig. 16

I

APPLICATIONS

DUAL 10 INPUT MULTIPLEXER

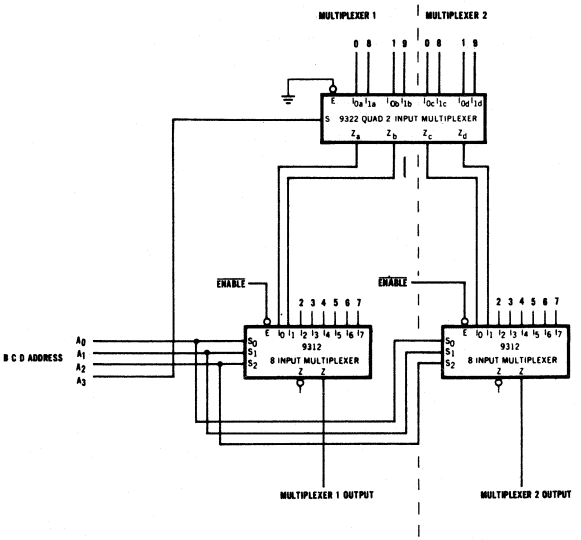
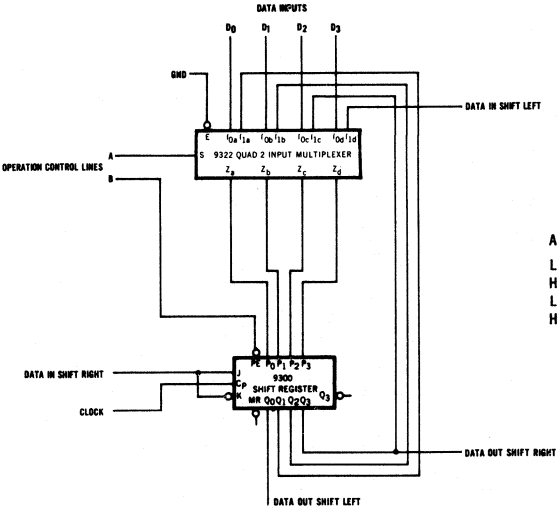


Fig. 17

SHIFT LEFT, SHIFT RIGHT, PARALLEL LOAD REGISTER



OPERATION CODE LIST

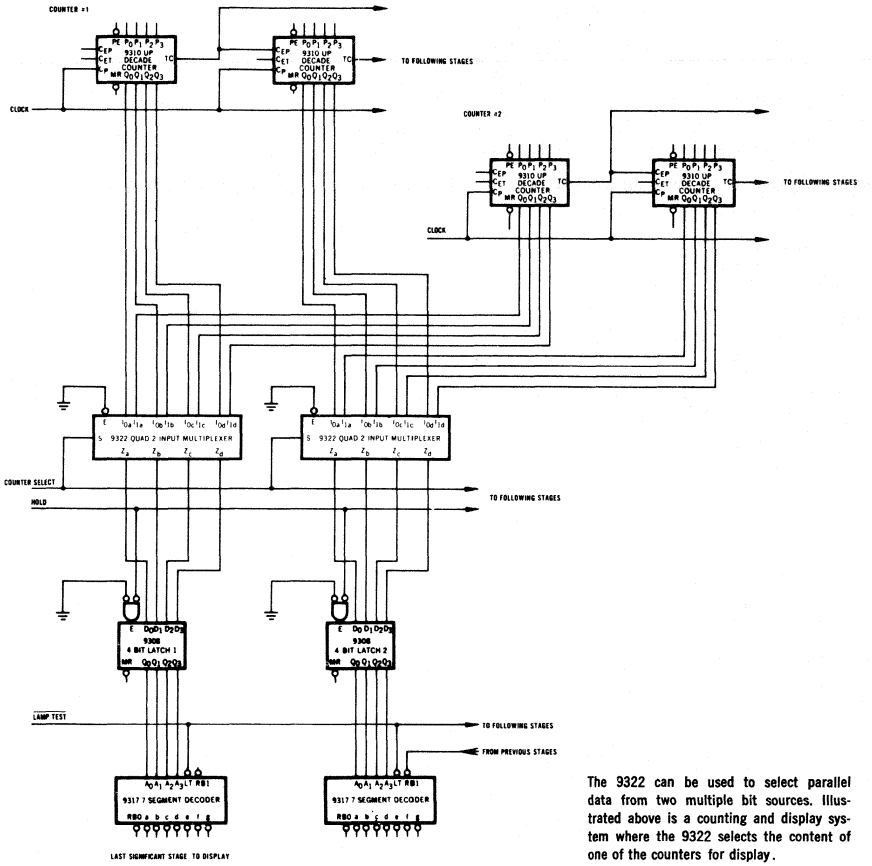
A	B	Operation
L	L	Parallel Load
H	L	Shift Left
L	H	Shift Right
H	H	Shift Right

This register will shift left, shift right, and load 4 bits of parallel data according to the operation code applied to A and B.

Fig. 18

APPLICATIONS

REGISTER SELECTION



The 9322 can be used to select parallel data from two multiple bit sources. Illustrated above is a counting and display system where the 9322 selects the content of one of the counters for display.

Fig. 19

9327A . 9327B

MSI SEVEN SEGMENT DECODER/DRIVER

A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

GENERAL DESCRIPTION — The MSI 9327 is a Seven Segment Decoder/Driver designed to accept four inputs in 8421 BCD code and provide the appropriate outputs to drive a seven segment vacuum fluorescent numerical display. The MSI 9327 will drive up to 12 seven segment vacuum fluorescent numerical displays with the use of the device's time sharing capability and the appropriate external pull-up resistors.

The 9327A part has the higher output voltage breakdown for use in the time share systems. The 9327B part with a lower breakdown voltage should be used for driving single tubes.

The inputs of the MSI 9327 are compatible with all other Fairchild CCSL devices.

- **CCSL COMPATIBLE**
- **AUTOMATIC RIPPLE BLANKING FOR SUPPRESSION OF LEADING EDGE ZEROES**
- **LAMP INTENSITY MODULATION CAPABILITY**
- **LAMP TEST FACILITY**
- **BLANKING INPUT**
- **ACTIVE HIGH OUTPUTS**
- **ALL CERAMIC "HERMETIC" 16 PIN DUAL IN-LINE* PACKAGE**
- **DRIVE TUBES DIRECTLY WITH EXTERNAL RESISTORS**
- **CODES IN EXCESS OF BINARY 9 DISABLE OUTPUTS**
- **ENHANCED RELIABILITY WITH UNIQUE NUMERIC ONE DISPLAY POSITION**
- **HIGH VOLTAGE OUTPUT FOR TIME SHARE**
- **UP TO 12 TUBE TIME SHARE CAPABILITY**

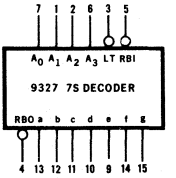
ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	0°C to +75°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
Voltage Applied to Outputs for high output state	−0.5 V to +30 V
Input Voltage (D.C.)	−0.5 V to +5.5 V
Current Into Outputs	30 mA
Power Dissipation per Output	30 mW

OPTIONS

PARAMETER	9327A	9327B
Min Output High Breakdown Voltage	64 Volts	30 Volts
Output Current	7.0 mA	5.0 mA

LOGIC SYMBOL



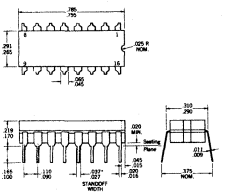
V_{CC} = PIN 16
GND = PIN 8

ORDER INFORMATION

Specify U7B9317XXZ for 16-pin Dual In-Line package or U4L9317XXZ for 16-pin Flatpak, where XXX is 59Z for the 0°C to 75°C temperature range. Z is used to identify the operating characteristics shown in the table above. The following codes should be used when ordering options: Z = 1 for 9327A; Z = 2 for 9327B.

PHYSICAL DIMENSIONS

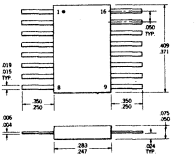
16 Lead Dual In-Line



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020" diameter lead
Leads are tin-plated Kovar
Package weight is 2.2 grams
*The .037/.027 dimension does not apply to the corner leads

Fig. 1

FLAT PACKAGE



NOTES:
All dimensions in inches
Leads are gold-plated Kovar
Package weight is 0.4 gram

Fig. 2

*Fairchild patent pending.

FAIRCHILD
SEMICONDUCTOR

The 9327 seven segment decoder/driver accepts a 4 Bit BCD 8421 code input and produces the appropriate outputs for selection of segments in a seven segment matrix display used for representing the decimal numbers 0 - 9. The seven outputs (a, b, c, d, e, f, g) of the decoder select the corresponding segments in the matrix shown in Figure 3. The numeric designations chosen to represent the decimal numbers are shown in Figure 5. Code configurations in excess of binary nine disable the outputs.

The decoder has active high outputs so that it may be used to drive vacuum fluorescent displays, using external pull-up resistors.

The device has provision for automatic blanking of the leading and/or trailing edge zeroes in a multidigit decimal number, resulting in an easily readable decimal display, conforming to normal writing practice. In an eight digit mixed integer fraction decimal representation, using the automatic blanking capability, (0060.0300) would be displayed as (60.03). Leading edge zero suppression is obtained by connecting the Ripple Blanking Output ($\overline{RBO}$) of a decoder to the Ripple Blanking Input ($\overline{RBI}$) of the next lower stage device. The most significant decoder stage should have the $\overline{RBI}$ input grounded; and, since suppression of the least significant integer zero in a number is not usually desired, the $\overline{RBI}$ input of this decoder stage should be left open. A similar procedure for the fractional part of a display will provide automatic suppression of trailing edge zeroes.

The decoder has an active low input Lamp Test which overrides all other input combinations and enables a check to be made on possible display malfunctions. The $\overline{RBO}$ terminal of the decoder can be OR - tied with a modulating signal via an isolating buffer to achieve pulse duration intensity modulation. A suitable signal can be generated for this purpose by forming a variable frequency multivibrator with a cross coupled pair of DTμL gates. The high output breakdown voltage allows up to 12 tubes to be driven from one 9327 in a time share mode of operation. The high voltage of the system can be higher than the breakdown voltage of the 9327 as long as the voltage at the anode is less than the breakdown voltage.

Fig. 3
SEGMENT DESIGNATION

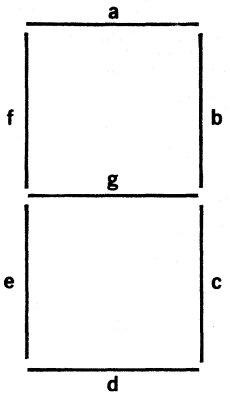


Fig. 4
TRUTH TABLE

$\overline{LT}$	$\overline{RBI}$	A	B	C	D	a	b	c	d	e	f	g	$\overline{RBO}$	DECIMAL OR FUNCTION
L	X	X	X	X	X	H	H	H	H	H	H	H	H	
H	L	L	L	L	L	L	L	L	L	L	L	L	L	0
H	H	L	L	L	L	H	H	H	H	H	H	L	H	0
|	X	H	L	L	L	L	L	L	L	H	H	L	H	1
|	|	L	H	L	L	H	H	L	H	H	L	H	H	2
|	|	H	H	L	L	H	H	H	H	L	L	H	H	3
|	|	L	L	H	L	L	H	H	L	L	H	H	H	4
|	|	H	L	H	L	H	L	H	H	L	H	H	H	5
|	|	L	H	H	L	L	L	H	H	H	H	H	H	6
|	|	H	H	H	L	H	H	H	L	L	L	L	H	7
|	|	L	L	L	H	H	H	H	H	H	H	H	H	8
|	|	H	L	L	H	H	H	H	L	L	H	H	H	9
|	|	L	H	L	H	L	L	L	L	L	L	L	L	10
|	|	H	H	L	H	L	L	L	L	L	L	L	L	11
|	|	L	L	H	H	L	L	L	L	L	L	L	L	12
|	|	H	L	H	H	L	L	L	L	L	L	L	L	13
|	|	L	H	H	H	L	L	L	L	L	L	L	L	14
H	X	H	H	H	H	L	L	L	L	L	L	L	L	15

H = High Voltage Level
L = Low Voltage Level
X = Don't Care Condition

Fig. 5
NUMERICAL DESIGNATIONS

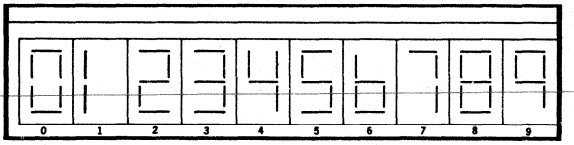


TABLE I — Loading Rules (1 U.L. = 1 DTμL Gate Input Load)

Inputs	Loading	
	High State	Low State
A_0, A_1, A_2, A_3	1	1
$\overline{RBI}$	1	½
$\overline{LT}$	5	4.0

Outputs	Fan Out
$\overline{RBO}$	1.5

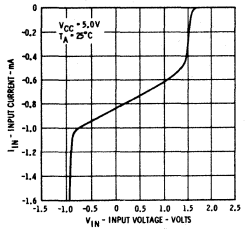
TABLE II —
ELECTRICAL CHARACTERISTICS (T_A = 0°C to +75°C, V_{CC} = 5.0 V ±5%) (Part = U7B/4L932759Z)

SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	0°C MAX.	+25°C MIN.	+25°C TYP.	+25°C MAX.	+75°C MIN.	+75°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage on $R_{B(OUT)}$ Only	3.0		3.0	4.0		3.0		Volts	V_{CC} = 4.75 V, I_{OH} = −70 μA Pin 6 = V_{IL}, Pin 5 = V_{IH}
V_{BD2}	Output High Breakdown Voltage, Option "A"	64		67	70		67		Volts	V_{CC} = 5.25 V, I_{OUT} = 7.0 mA
V_{BD2}	Output High Breakdown Voltage, Option "B"	30		33	65		33		Volts	V_{CC} = 5.25 V, I_{OUT} = 5.0 mA
V_{OL}	Output Low Voltage on $R_{B(OUT)}$ Only		0.45		0.25	0.45		0.45	Volts	V_{CC} = 5.25 V, I_{OL} = 2.4 mA
			0.45		0.25	0.45		0.45	Volts	V_{CC} = 4.75 V, I_{OL} = 2.12 mA
V_{OL}	Output Low Voltage		0.45		0.25	0.45		0.45	Volts	V_{CC} = 4.75 V, I_{OL} = 0 mA
V_{BD1}	Output High Breakdown Voltage, Option "A"			55			55		Volts	V_{CC} = 5.25 V, I_{OUT} = 50 μA @ 25°C, I_{OUT} = 70 μA @ 75°C
V_{BD1}	Output High Breakdown Voltage, Option "B"			25			25		Volts	V_{CC} = 5.25 V, I_{OUT} = 35 μA @ 25°C, I_{OUT} = 50 μA @ 75°C
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F (Pin 3)	Input Load Current		−6.4			−6.4		−6.4	mA	V_{CC} = 5.25 V, V_F = 0.45 V
I_F (Pins 1, 2, 6, 7)	Input Load Current		−1.6			−1.6		−1.6	mA	V_R = 5.25 V on other inputs
I_F (Pin 5)	Input Load Current		−0.8			−0.8		−0.8	mA	
5 I_R (Pin 3)	Input Leakage Current					300		300	μA	V_{CC} = 5.25 V, V_R = 4.5 V
I_R (Pins 1, 2, 5, 6, 7)	Input Leakage Current					60		60	μA	Ground on other inputs
I_{PD}	V_{CC} Current		36		22	36		36	mA	V_{CC} = 5.0 V, All inputs and outputs open

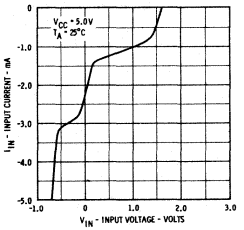
TYPICAL INPUT AND OUTPUT CHARACTERISTICS

INPUT CURRENT VERSUS INPUT VOLTAGE

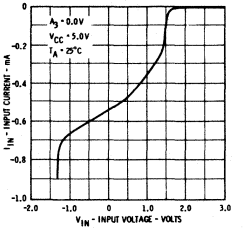
A_0, A_1, A_2, A_3 INPUTS



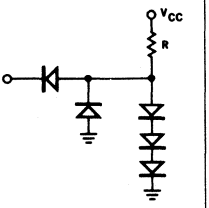
$\overline{LT}$ INPUT



$\overline{RBI}$ INPUT

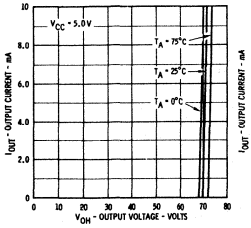


INPUTS
Equivalent Circuit

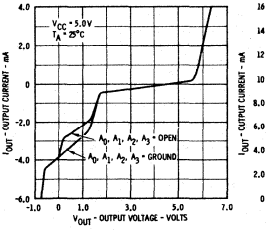


OUTPUT CURRENT VERSUS OUTPUT VOLTAGE

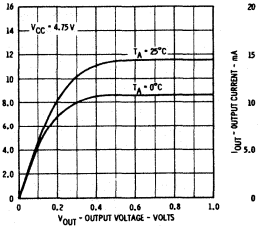
OUTPUT IN HIGH STATE
a, b, c, d, e, f, g OUTPUTS



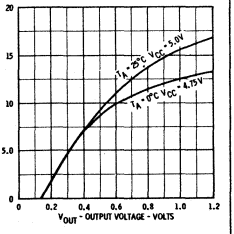
$\overline{RBO}$ OUTPUT



OUTPUT IN LOW STATE
a, b, c, d, e, f, g OUTPUTS

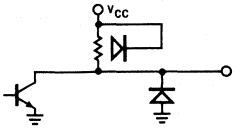


$\overline{RBO}$ OUTPUT

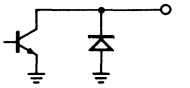


OUTPUTS

Equivalent Circuit (Pin 4)



Equivalent Circuit (Pins 9 thru 15)



APPLICATIONS

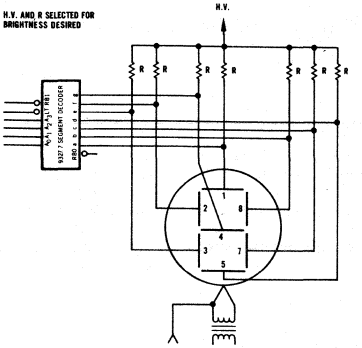


Fig. 7
9327 Seven Segment Decoder Driving Vacuum Fluorescent Readout

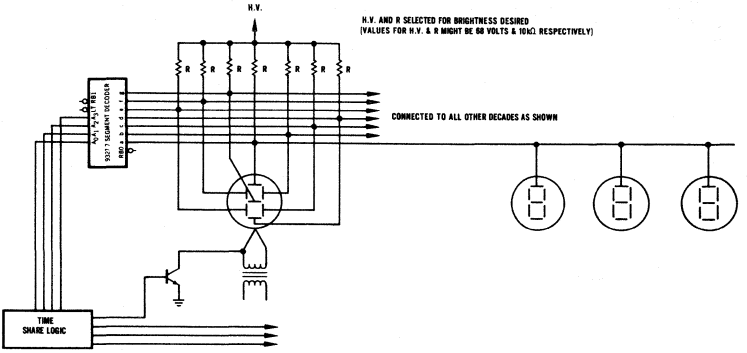


Fig. 8
9327 Seven Segment Decoder driving fluorescent tubes in time share mode

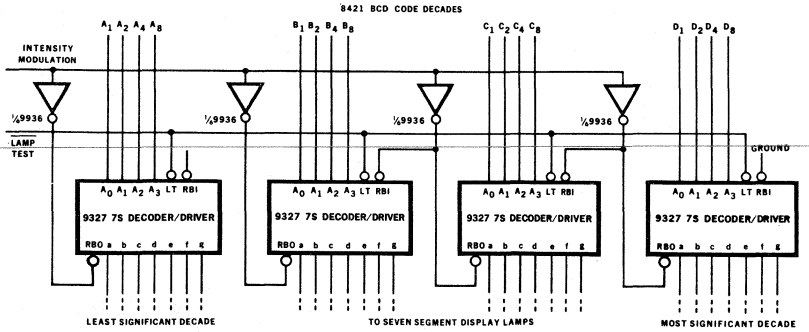


Fig. 9 — FOUR DECADE SEVEN SEGMENT INTEGER DISPLAY SCHEME
This scheme incorporates automatic blanking of leading edge zeroes and intensity modulation using an external variable duty cycle signal.

9328

MSI DUAL 8-BIT SHIFT REGISTER

A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

GENERAL DESCRIPTION — The 9328 is a high speed serial storage element providing sixteen bits of storage in the form of two eight bit registers that will shift at greater than 20 MHz rates. The multi-functional capability of this device is provided by several features: 1) Additional gating is provided at the input to both shift registers so that the input is easily multiplexed between two sources. 2) The clock of each register may be provided separately or together. 3) Both the true and complementary outputs are provided from each eight bit register, and both registers may be master cleared from a common input.

FEATURES:

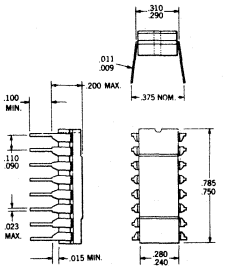
- **20 MHz SHIFT FREQUENCY**
- **TWO INPUT MULTIPLEXER PROVIDED AT DATA INPUT OF EACH REGISTER**
- **GATED CLOCK INPUT CIRCUITRY**
- **BOTH TRUE AND COMPLEMENTARY OUTPUTS PROVIDED FROM LAST BIT OF EACH REGISTER**
- **ASYNCHRONOUS MASTER RESET COMMON TO BOTH REGISTERS**
- **TYPICAL POWER DISSIPATION OF 300 mW**
- **CCSL COMPATIBLE**
- **INPUT DIODE CLAMPING**

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7 V
Voltage Applied to Outputs for high output state	−0.5 V to +V_{CC} value
Input Voltage (D.C.)	−0.5 V to +5.5 V

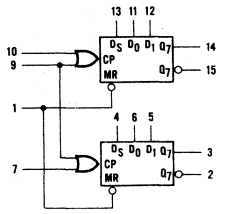
ORDER INFORMATION — Specify U6B9328XXX for 16-pin Dual In-Line package where XXX is 51X for the −55°C to +125°C temperature range, or 59X for the 0°C to +75°C temperature range.

PHYSICAL DIMENSIONS



NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.375) misalignment to facilitate insertion.
2. Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

LOGIC DIAGRAM



V_{CC} = Pin 16
Gnd = Pin 8

FAIRCHILD
SEMICONDUCTOR

FUNCTIONAL DESCRIPTION — The two 8 bit shift registers have a common clock input (pin 9) and separate clock inputs (pins 10 & 7). The clocking of each register is controlled by the OR function of the separate and the common clock input. Each register is composed of eight clocked RS master-slave flip-flops and a number of gates. The clock OR gate drives the eight clock inputs of the flip-flop in parallel. When the two clock inputs (the separate and the common) to the OR gate are low, the slave latches are steady, but data can enter the master latches via the R and S input. During the first low to high transition of either, or both simultaneously, of the two clock inputs, the data inputs (R and S) are inhibited so that a later change in input data will not affect the master; then the now trapped information in the master is transferred to the slave. When the transfer is complete, both the master and the slave are steady as long as either or both clock inputs remain high. During the high to low transition of the last remaining high clock input, the transfer path from master to slave is inhibited first, leaving the slave steady in its present state; second the data inputs (R and S) are enabled so that new data can enter the master. Either of the clock inputs can be used as clock inhibit inputs by applying a logic high signal. Each 8 bit shift register has a two input multiplexer in front of the serial data input. The two data inputs D_0 and D_1 are controlled by the data select input D_S following the Boolean expression:

Serial data in: $S_D = \overline{D}_S D_0 + D_S D_1$

An asynchronous master reset is provided which, when activated by a low logic level, will clear all sixteen stages independently of any other input signal.

LOADING RULES
(1 U.L. = 1 TTμL input gate load)

INPUT	FAN IN
MR, D_0, D_1	1 Unit Load
Separate CP (pins 7 & 10)	1.5 Unit Loads
D_S	2 Unit Loads
Common CP (pin 9)	3 Unit Loads
OUTPUT	**FAN OUT**
Q_7, $\overline{Q}_7$	6 Unit Loads

ELECTRICAL CHARACTERISTICS ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0$ V $\pm 10\%$)

SYMBOL	CHARACTERISTICS	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS & COMMENTS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	$V_{CC} = 4.5$ V, $I_{OH} = -0.36$ mA
V_{OL}	Output Low Voltage		0.4		0.2	0.4		0.4	Volts	$V_{CC} = 5.5$ V, $I_{OL} = 9.6$ mA $V_{CC} = 4.5$ V, $I_{OL} = 7.44$ mA
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current (MR, D_0, D_1)		−1.6		−1.0	−1.6		−1.6	mA	$V_{CC} = 5.5$ V $V_F = 0.4$ V
1.5 I_F	Input Load Current (separate CP pins 7 & 10)		−2.4		−1.5	−2.4		−2.4	mA	
2 I_F	Input Load Current (D_S)		−3.2		−2.0	−3.2		−3.2	mA	
3 I_F	Input Load Current (common CP pin 9)		−4.8		−3.0	−4.8		−4.8	mA	
I_R	Input Leakage Current (MR, D_0, D_1)		60		10	60		60	μA	$V_{CC} = 5.5$ V $V_R = 4.5$ V
1.5 I_R	Input Leakage Current (separate CP pins 7 & 10)		90		15	90		90	μA	
2 I_R	Input Leakage Current (D_S)		120		20	120		120	μA	
3 I_R	Input Leakage Current (common CP pin 9)		180		30	180		180	μA	
I_{PD}	Power Dissipation		365		300	365		365	mW	$V_{CC} = 5.0$ V

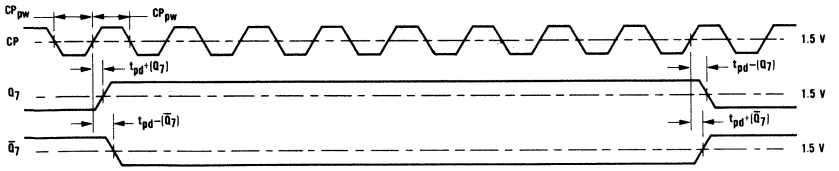
ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0\ V \pm 5\%$)

SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	0°C MAX.	+25°C MIN.	+25°C TYP.	+25°C MAX.	+75°C MIN.	+75°C MAX.	UNITS	CONDITIONS & COMMENTS
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	$V_{CC} = 4.75\ V$, $I_{OH} = -0.36\ mA$
V_{OL}	Output Low Voltage		0.45		0.2	0.45		0.45	Volts	$V_{CC} = 5.25\ V$, $I_{OL} = 9.6\ mA$ $V_{CC} = 4.75\ V$, $I_{OL} = 8.5\ mA$
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current (MR, D_0, D_1)		−1.6		−1.0	−1.6		−1.6	mA	
1.5 I_F	Input Load Current (separate CP pins 7 & 10)		−2.4		−1.5	−2.4		−2.4	mA	$V_{CC} = 5.25\ V$
2 I_F	Input Load Current (D_S)		−3.2		−2.0	−3.2		−3.2	mA	$V_F = 0.4\ V$
3 I_F	Input Load Current (common CP pin 9)		−4.8		−3.0	−4.8		−4.8	mA	
I_R	Input Leakage Current (MR, D_0, D_1)		60		10	60		60	μA	
1.5 I_R	Input Leakage Current (separate CP pins 7 & 10)		90		15	90		90	μA	$V_{CC} = 5.25\ V$
2 I_R	Input Leakage Current (D_S)		120		20	120		120	μA	$V_R = 4.5\ V$
3 I_R	Input Leakage Current (common CP pin 9)		180		30	180		180	μA	
I_{PD}	Power Dissipation		365		300	365		365	mW	$V_{CC} = 5.0\ V$

SWITCHING CHARACTERISTICS ($T_A = 25°C$)

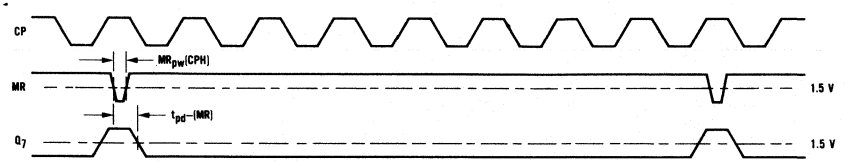
SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	CONDITIONS & COMMENTS
t_{pd+} (Q_7 & $\overline{Q}_7$)	Turn-Off Delay (clock to output)		13		ns	$V_{CC} = 5.0\ V$, $C_L = 15\ pF$ Fig. 1
t_{pd-} (Q_7 & $\overline{Q}_7$)	Turn-On Delay (clock to output)		22		ns	
t_{pd-} (MR)	Turn-On Delay (Master reset to output)		35		ns	$V_{CC} = 5.0\ V$, $C_L = 15\ pF$ Fig. 2 & 3
CP_{pw}	Min. Clock Pulse Width		14		ns	$V_{CC} = 5.0\ V$, $C_L = 15\ pF$ Fig. 1
MR_{pw} (CPH)	Min. Master Reset pulse width with clock high		15		ns	$V_{CC} = 5.0\ V$, $C_L = 15\ pF$ Fig. 2
MR_{pw} (CPL)	Min. Master Reset pulse width with clock low		28		ns	$V_{CC} = 5.0\ V$, $C_L = 15\ pF$ Fig. 3

SWITCHING WAVEFORMS



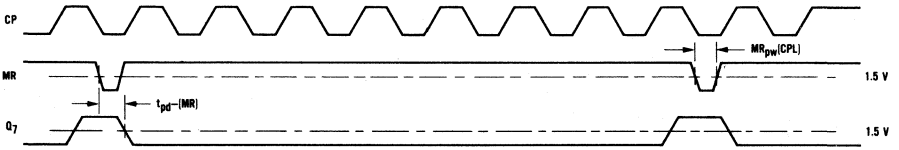
Note: $\overline{Q}_7$ is connected to D_1. Other clock is grounded.

Fig. 1



Note: D_S, D_1, D_0 are high. Other clock input is grounded.

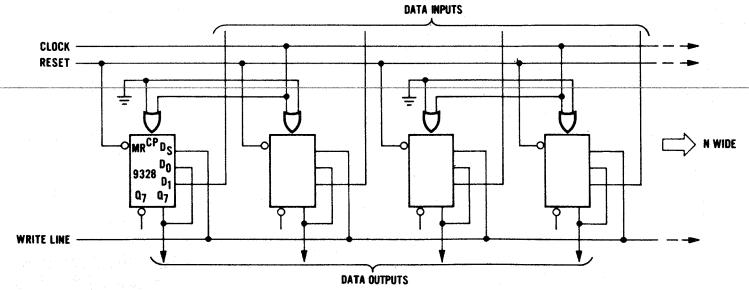
Fig. 2



Note: D_S, D_1, D_0 are high. Other clock input is grounded.

Fig. 3

APPLICATION:



N-BIT BY 8-WORD HIGH-SPEED MEMORY

TTμL/LMSI 9334

8-BIT ADDRESSABLE LATCH

A FAIRCHILD TTμL® IC PRODUCT

GENERAL DESCRIPTION – The TTμL/MSI 9334 is a high speed 8-bit addressable latch designed for general purpose storage applications in digital systems. It is a multifunctional device capable of storing single line data in eight addressable latches, and being a one-of-eight decoder and demultiplexer with active level high outputs. The device also incorporates an active level low common clear for resetting all latches, as well as, an active level low enable. The 9334 is compatible with all members of Fairchild's TTμL family.

FEATURES

- **SERIAL TO PARALLEL CAPABILITY**
- **8-BITS OF STORAGE WITH OUTPUT OF EACH BIT AVAILABLE**
- **RANDOM (ADDRESSABLE) DATA ENTRY**
- **ACTIVE HIGH DEMULTIPLEXING OR DECODING CAPABILITY**
- **EASILY EXPANDABLE**
- **COMMON CLEAR**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **TTμL COMPATIBLE**

PIN NAMES		LOADING
A_0, A_1, A_2	Address Inputs	1 U.L.
D	Data Input	1 U.L.
$\overline{E}$	Enable (Active Low) Input	1.5 U.L.
$\overline{C}$	Clear (Active Low) Input	1 U.L.
0 to 7	Parallel Latch Outputs	6 U.L.

NOTE: 1 UNIT LOAD (U.L.) = 40 μA HIGH/1.6 mA LOW

ORDER INFORMATION

Specify U7B9334XXX for 16 pin Dual In-Line package or U4L9334XXX for 16 pin Flat Package where XXX is 51X for the -55°C to + 125°C temperature range, or 59X for the 0°C to + 75°C temperature range.

LOGIC DIAGRAM

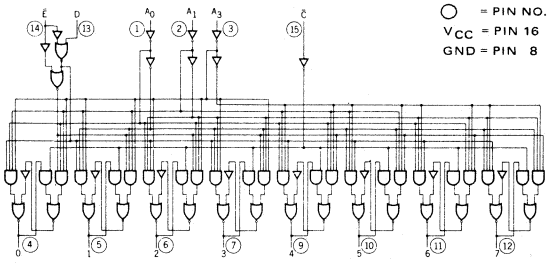


Fig. 4

LOGIC SYMBOL

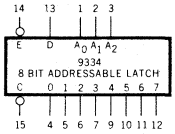


Fig. 1

CONNECTION DIAGRAM
DIP (TOP VIEW)

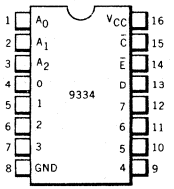


Fig. 2

FLATPAK
(TOP VIEW)

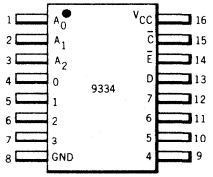


Fig. 3

*Planar is a patented Fairchild process.

FAIRCHILD
SEMICONDUCTOR

FUNCTIONAL DESCRIPTION – The TTμL/MSI 9334 has four modes of operation which are shown in the mode selection table. When in the addressable latch mode data on the data line (D) is written into the addressed latch. The addressed latch will follow the data input with all non-addressed latches remaining in their previous states. In the memory mode, all latches remain in their previous state and are unaffected by the data or address inputs.

In the one-of-eight decoding or demultiplexing mode the addressed output will follow the state of the D input with all other inputs in the low state. In the clear mode all outputs are low and unaffected by the address and data inputs.

When operating the 9334 as an addressable latch, changing more than one bit of the address could impose a transient wrong address and therefore should only be done while in the memory mode.

The truth table below summarizes the operations of the 9334.

MODE SELECTION

$\bar{E}$	C	MODE
L	H	Addressable Latch
H	H	Memory
L	L	Active High 8 Channel Demultiplexer
H	L	Clear

TTμL LOADING RULES

INPUTS	LOADING	
	HIGH	LOW
$A_0, A_1, A_2, D, \bar{C}$	1 U.L.	1 U.L.
$\bar{E}$	1.5 U.L.	1.5 U.L.

OUTPUTS	DRIVE FACTOR	
	HIGH	LOW
$Q_0, Q_1, Q_2, Q_3, Q_4, Q_5, Q_6, Q_7$	18 U.L.	6 U.L.

1 UNIT LOAD (U.L.) = 40 μA HIGH/1.6 mA LOW

TRUTH TABLE

						PRESENT OUTPUT STATES								
$\bar{C}$	$\bar{E}$	D	A_0	A_1	A_2	0	1	2	3	4	5	6	7	MODE
L	H	X	X	X	X	L	L	L	L	L	L	L	L	CLEAR
L	L	L	L	L	L	L	L	L	L	L	L	L	L	DEMULTIPLEX
L	L	H	L	L	L	H	L	L	L	L	L	L	L	
L	L	L	H	L	L	L	L	L	L	L	L	L	L	
L	L	H	H	L	L	L	H	L	L	L	L	L	L	
L	L	H	H	H	H	L	L	L	L	L	L	L	H	
H	H	X	X	X	X	Q_{N-1}								MEMORY
H	H	L	L	L	L	L	Q_{N-1}	Q_{N-1}	Q_{N-1}					ADDRESSABLE
H	L	H	L	L	L	H	Q_{N-1}	Q_{N-1}						LATCH
H	L	L	H	L	L	Q_{N-1}	L	Q_{N-1}						
H	L	H	H	L	L	Q_{N-1}	H	Q_{N-1}						
H	L	L	H	H	H	Q_{N-1}						Q_{N-1}	L	
H	L	H	H	H	H	Q_{N-1}						Q_{N-1}	H	

X = Don't Care Condition
L = Low Voltage Level
H = High Voltage Level
Q_{N-1} = Previous Output State

TYPICAL INPUT AND OUTPUT CIRCUITS

INPUTS EQUIVALENT CIRCUIT

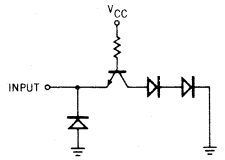


Fig. 5

OUTPUTS EQUIVALENT CIRCUIT

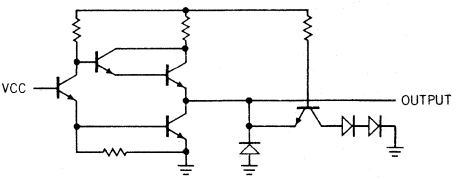
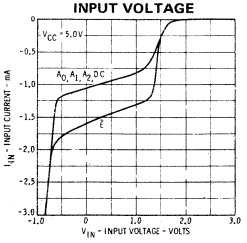
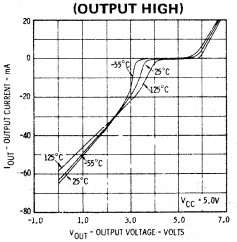


Fig. 6

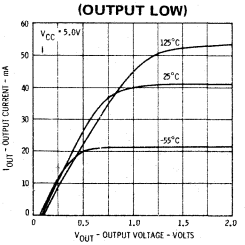
INPUT CURRENT VERSUS INPUT VOLTAGE



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)



ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	-65°C to + 150°C
Temperature (Ambient) Under Bias	-55°C to + 125°C
V_{CC} Pin Potential to Ground Pin	-0.5 V to + 7.0 V
*Input Voltage (D.C.)	-0.5 V to + 5.5 V
*Input Current (D.C.)	-30 mA to + 5.0 mA
Voltage Applied to Outputs (Output High)	0.5 V to + V_{CC} value
Output Current (D.C.) (Output Low)	+ 30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

	SUPPLY VOLTAGE (V_{CC})			
PART NUMBER	MIN.	TYP.	MAX.	TEMPERATURE
U7B/4L9334 51X	4.5 V	5.0 V	5.5 V	-55°C to 125°C
U7B/4L9334 59X	4.75 V	5.0 V	5.25 V	0°C to 75°C

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		MIN	TYP. (Note 4)	MAX.		
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = -720 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.2	0.4	Volts	V_{CC} = MIN., I_{OL} = 9.6 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{IH}	Input HIGH Level	2.0			Volts	Guaranteed input logical HIGH voltage for all inputs
V_{IL}	Input LOW Level			0.8	Volts	Guaranteed input logical LOW voltage for all inputs
I_{IL}	Input LOW Current $A_0, A_1, A_2, D, \overline{C}$ $\overline{E}$		-0.96 -1.44	-1.6 -2.4	mA	V_{CC} = MAX., V_{IN} = 0.4 V
I_{IH}	Input HIGH Current $A_0, A_1, A_2, D, \overline{C}$ $\overline{E}$			40 60	μA	V_{CC} = MAX., V_{IN} = 2.4 V
	Input HIGH Current			1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{SC}	Output Short Circuit Current	30		100	mA	V_{CC} = MAX., V_{OUT} = 0.0 V
I_{CC}	Power Supply Current		56	86	mA	V_{CC} = MAX.

NOTES:

(1) The actual Testing Procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this Specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California (see page 1 for address and phone).

(2) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.

(3) The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

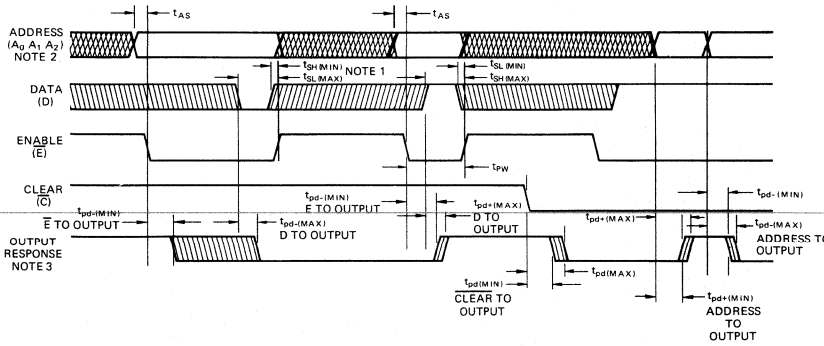
(4) Typical limits are at V_{CC} = 5.0 V, 25°C, and max. loading.

PRELIMINARY SWITCHING CHARACTERISTICS (T_A = 25°C) See Fig. 7

SYMBOL	CHARACTERISTIC	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	CONDITIONS
t_s "H"	Data set up time. The time required for a high or low logic to be present before the low to high enable transition in order to be recognized and stored. See Note 1.	10	32	50	ns	V_{CC} = 5 V, C_L = 15 pF
t_s "L"		6.0	18	25	ns	
t_{AS}	Address set up time. The time required for the address to be present before the high to low enable transition so that the correct latch is addressed and other latches are not disturbed.			10	ns	V_{CC} = 5 V, C_L = 15 pF
t_{PW}	Shortest enable pulse width. The shortest time required for the enable to be low in order to store data.	6.0	29	38	ns	V_{CC} = 5 V, C_L = 15 pF
t_{pd+} t_{pd-}	Enable to output. The delay between the enable transition and output response.	15 11	19 16	28 24	ns	V_{CC} = 5 V, C_L = 15 pF
t_{pd+} t_{pd-}	Data to output. The delay between the data transition and output response.	22 11	28 16	35 24	ns	V_{CC} = 5 V, C_L = 15 pF
t_{pd-}	Clear to output. The delay between the clear transition (high to low) and output response.	17	21	25	ns	V_{CC} = 5 V, C_L = 15 pF
t_{pd+} t_{pd-}	Address to output. The delay between address changes and the output response.	13 11		35 35	ns	V_{CC} = 5 V, C_L = 15 pF

NOTES:
(1) For one particular device and operating condition $t_{smin} \approx t_{smax}$. The published limits of t_{smin} and t_{smax} cover the production spread of the parameter. For predictable system performance input data must be stable between these limits.
(2) In the addressable latch mode the address inputs should be stable from t_{asmax}, before the High to Low transition on the $\overline{E}$ input, and while the $\overline{E}$ input is low, but may change simultaneously with the Low to High transition on the $\overline{E}$ input.
(3) The cross hatched areas of the output response curve show the effect of input changes while $\overline{E}$ is Low and of minimum and maximum propagation delays between inputs (D, $\overline{E}$, A) and outputs.

Fig. 7 PRELIMINARY SWITCHING TIME WAVEFORM



APPLICATIONS

Fig. 8 4096 BIT, 12 MHz SERIAL MEMORY

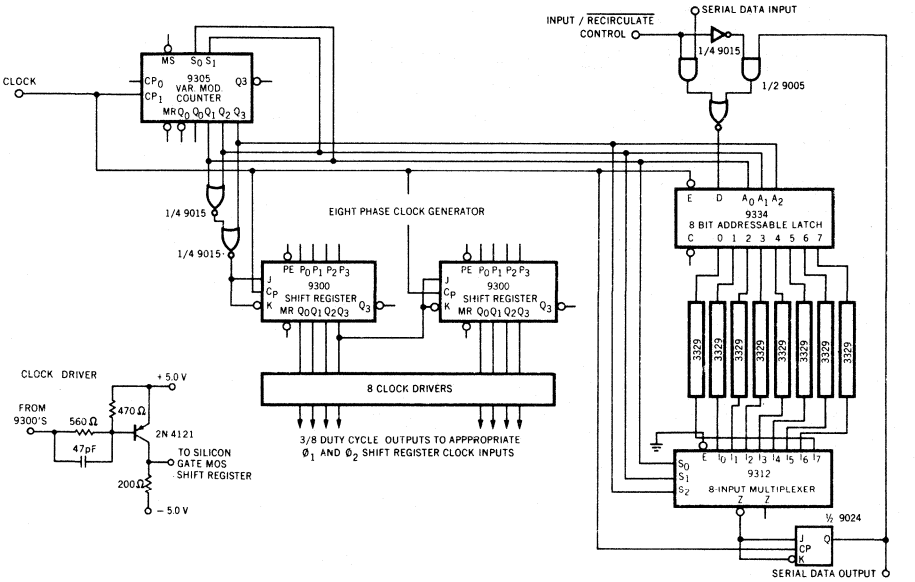
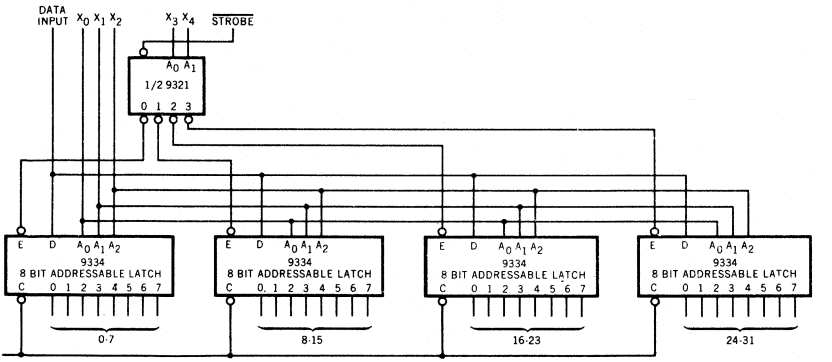
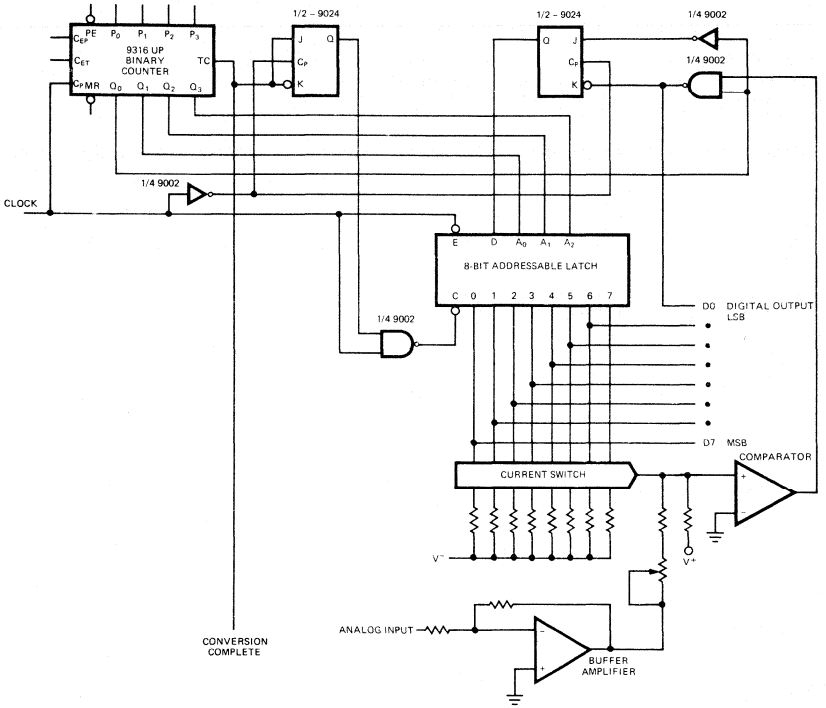


Fig. 9 32 BIT ADDRESSABLE LATCH AND 1 OF 32 DECODER/DEMULTIPLEXER



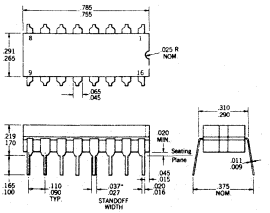
APPLICATIONS (Cont'd)

Fig. 10 8-BIT A TO D CONVERTER



PACKAGE INFORMATION

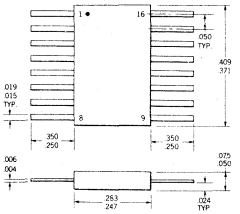
7B – 16 LEAD DUAL IN-LINE PACKAGE



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers.
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Hermetically sealed alumina ceramic package
Leads are tin-plated kovar
Package weight is 2.2 grams
* The .037/.027 dimension does not apply to the corner leads

Fig. 11

4L – 16 LEAD FLATPAK



NOTES:
All dimensions in inches
Leads are gold-plated kovar
Package weight is 0.4 gram

Fig. 12

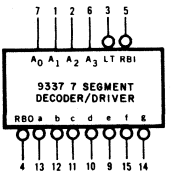
TTμL/MSI 9337
SEVEN SEGMENT DECODER/DRIVER
A FAIRCHILD TTμL® IC PRODUCT

GENERAL DESCRIPTION — The MSI 9337 is a Seven Segment Decoder/Driver designed to accept four inputs in 8421 BCD code and provide the appropriate outputs to drive a seven segment gas filled cold cathode indicator tube. The MSI 9337 also has time sharing capability. The inputs of the MSI 9337 are compatible with all other Fairchild TTμL families.

FEATURES

- **AUTOMATIC RIPPLE BLANKING FOR SUPPRESSION OF LEADING EDGE ZEROES**
- **LAMP INTENSITY MODULATION CAPABILITY**
- **LAMP TEST FACILITY**
- **BLANKING INPUT**
- **ACTIVE LOW OUTPUTS**
- **ALL CERAMIC "HERMETIC" 16 PIN DUAL IN-LINE AND FLAT PACKAGES**
- **DRIVE TUBES DIRECTLY WITH SERIES CATHODE RESISTORS**
- **CODES IN EXCESS OF BINARY 9 DISABLE OUTPUTS**
- **HIGH CURRENT OUTPUT FOR TIME SHARE**
- **TTμL COMPATIBLE**

LOGIC SYMBOL



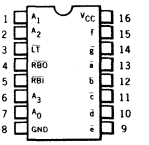
V_{CC} = PIN 16
GND = PIN 8

Fig. 1

PIN NAMES		LOADING
A_0, A_1, A_2, A_3	Address Inputs	1.0 U.L.
$\overline{LT}$	Lamp Test (Active Low) Input	4.0 U.L.
$\overline{RBI}$	Ripple Blanking (Active Low)Input	0.5 U.L.
$\overline{RBO}$	Ripple Blanking (Active Low) Output	1.5 U.L.
$\overline{a}$, $\overline{b}$, $\overline{c}$, $\overline{d}$, $\overline{e}$, $\overline{f}$, $\overline{g}$	(Active Low) Outputs	

1 Unit Load (U.L.) = 60 μA High/1.6 mA Low

CONNECTION DIAGRAMS
DIP (Top View)



FLATPAK (Top View)

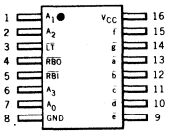


Fig. 2

ORDER INFORMATION
Specify U7B933759X for 16-pin Dual In-Line package or U4L933759X for 16-pin Flatpak for 0°C to 75°C temperature.

LOGIC DIAGRAM

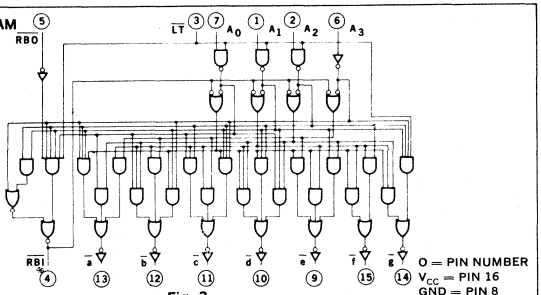


Fig. 3

FAIRCHILD SEMICONDUCTOR

The 9337 seven segment decoder/driver accepts a 4 Bit BCD 8421 code input and produces the appropriate outputs for selection of segments in a seven segment matrix display used for representing the decimal numbers 0 - 9. The seven outputs (a, b, c, d, e, f, g) of the decoder select the corresponding segments in the matrix shown in Figure 4. The numeric designations chosen to represent the decimal numbers are shown in Figure 6. Code configurations in excess of binary nine disable the outputs.

The decoder has active low outputs so that it may be used to drive gas filled cold cathode indicator tubes.

The device has provision for automatic blanking of the leading and/or trailing edge zeroes in a multidigit decimal number, resulting in an easily readable decimal display, conforming to normal writing practice. In an eight digit mixed integer fraction decimal representation, using the automatic blanking capability, (0060.0300) would be displayed as (60.03). Leading edge zero suppression is obtained by connecting the Ripple Blanking Output ($\overline{RBO}$) of a decoder to the Ripple Blanking Input ($\overline{RBI}$) of the next lower stage device. The most significant decoder stage should have the RBI input grounded; and, since suppression of the least significant integer zero in a number is not usually desired, the $\overline{RBI}$ input of this decoder stage should be left open. A similar procedure for the fractional part of a display will provide automatic suppression of trailing edge zeroes.

The decoder has an active low input Lamp Test which overrides all other input combinations and enables a check to be made on possible display malfunctions.

The $\overline{RBO}$ terminal of the decoder can be OR-tied with a modulating signal via an isolating buffer for pulse duration intensity modulation or complete display blanking. Isolating buffer should be either a DTμL unit or a transistor (Fig. 9). Using a TTμL unit could result in damage to both units. The high current sinking ability allows time share operation.

Fig. 4
SEGMENT DESIGNATION

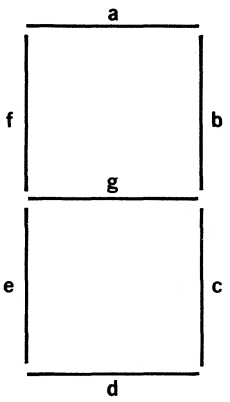
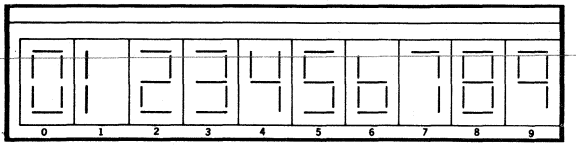


Fig. 5
TRUTH TABLE

$\overline{LT}$	$\overline{RBI}$	A_0	A_1	A_2	A_3	$\overline{a}$	$\overline{b}$	$\overline{c}$	$\overline{d}$	$\overline{e}$	$\overline{f}$	$\overline{g}$	$\overline{RBO}$	DECIMAL OR FUNCTION
L	X	X	X	X	X	L	L	L	L	L	L	L	H	TEST
H	L	L	L	L	L	H	H	H	H	H	H	H	L	BLANK
H	H	L	L	L	L	L	L	L	L	L	L	H	H	0
|	X	H	L	L	L	H	H	H	H	L	L	H	H	1
|	|	L	H	L	L	L	L	H	L	L	H	L	H	2
|	|	H	H	L	L	L	L	L	L	H	H	L	H	3
|	|	L	L	H	L	H	L	L	H	H	L	L	H	4
|	|	H	L	H	L	L	H	L	L	H	L	L	H	5
|	|	L	H	H	L	H	H	L	L	L	L	L	H	6
|	|	H	H	H	L	L	L	L	H	H	H	H	H	7
|	|	L	L	L	H	L	L	L	L	L	L	L	H	8
|	|	H	L	L	H	L	L	L	H	H	L	L	H	9
|	|	L	H	L	H	H	H	H	H	H	H	H	L	10
|	|	H	H	L	H	H	H	H	H	H	H	H	L	11
|	|	L	L	H	H	H	H	H	H	H	H	L	L	12
|	|	H	L	H	H	H	H	H	H	H	H	H	L	13
|	|	L	H	H	H	H	H	H	H	H	H	H	L	14
H	X	H	H	H	H	H	H	H	H	H	H	H	L	15

H = High Voltage Level
L = Low Voltage Level
X = Don't Care Condition

Fig. 6
NUMERICAL DESIGNATIONS



ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	0°C to +75°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
Voltage Applied to Outputs for high output state	−0.5 V to +70 V
Input Voltage (D.C.)	−0.5 V to +5.5 V
Current Into Outputs	40 mA
Power Dissipation per Output	30 mW

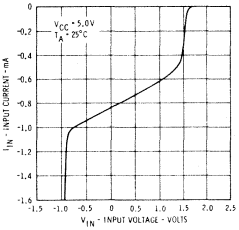
TABLE II —
ELECTRICAL CHARACTERISTICS (T_A = 0°C to +75°C, V_{CC} = 5.0 V ±5%) (Part # U7B/4L933759X)

SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	0°C MAX.	+25°C MIN.	+25°C TYP.	+25°C MAX.	+75°C MIN.	+75°C MAX.	UNITS	CONDITIONS	
V_{OH}	Output High Voltage on $R_{B(OUT)}$ Only	3.0		3.0	4.0		3.0		Volts	V_{CC} = 4.75 V, I_{OH} = −70 μA Pin 6 = V_{IL}, Pin 5 = V_{IH}	
V_{BD2}	Output High Breakdown Voltage	60		63	70		63		Volts	V_{CC} = 5.0 V, I_{OUT} = 2.0 mA	
V_{OL}	Output Low Voltage		0.45		0.25	0.45		0.45	Volts	V_{CC} = 5.25 V, I_{OL} = 2.4 mA	Inputs at V_{IH} or V_{IL} per Truth Table
	on $R_{B(OUT)}$ Only		0.45		0.25	0.45		0.45	Volts	V_{CC} = 4.75 V, I_{OL} = 2.12 mA	
V_{OL}	Output Low Voltage		0.45		0.25	0.45		0.45	Volts	V_{CC} = 4.75 V, I_{OL} = 10 mA	
V_{BD1}	Output High Breakdown Voltage			60			60		Volts	V_{CC} = 5.25 V, I_{OUT} = 6.0 μA @ 25°C; I_{OUT} = 10.0 μA @ 75°C	
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs	
V_{IL}	Inut Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs	
I_F(Pin 3)	Input Load Current		−6.4			−6.4		−6.4	mA	V_{CC} = 5.25 V, V_F = 0.45 V	
I_F(Pins 1,2,6,7)	Input Load Current		−1.6			−1.6		−1.6	mA	V_R = 5.25 V on other inputs	
I_F(Pin 5)	Input Load Current		−0.8			−0.8		−0.8	mA		
5 I_R(Pin 3)	Input Leakage Current					300		300	μA	V_{CC} = 5.25 V, V_R = 4.5 V	
I_R(Pins 1,2,5,6,7)	Input Leakage Current					60		60	μA	Ground on other inputs	
I_{PD}	V_{CC} Current	68			45	68		68	mA	V_{CC} = 5.0 V, All inputs and outputs open	

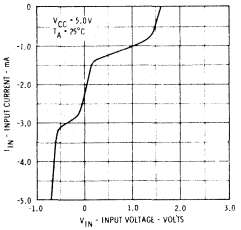
TYPICAL INPUT AND OUTPUT CHARACTERISTICS

INPUT CURRENT VERSUS INPUT VOLTAGE

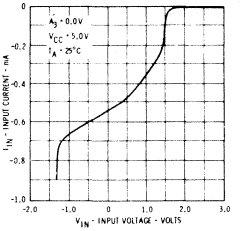
A_0, A_1, A_2, A_3 INPUTS



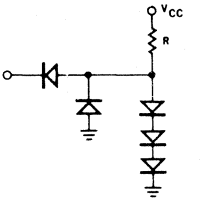
$\overline{LT}$ INPUT



$\overline{RBI}$ INPUT

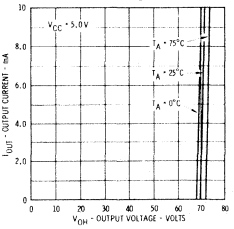


INPUTS
Equivalent Circuit

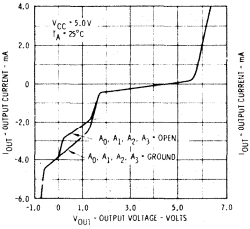


OUTPUT CURRENT VERSUS OUTPUT VOLTAGE

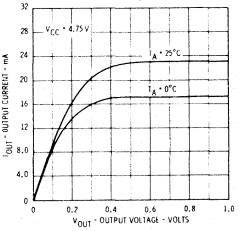
OUTPUT IN HIGH STATE
a, b, c, d, e, f, g OUTPUTS



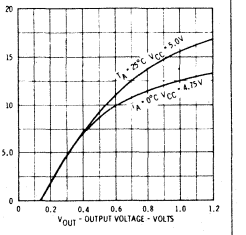
$\overline{RBO}$ OUTPUT



OUTPUT IN LOW STATE
a, b, c, d, e, f, g OUTPUTS

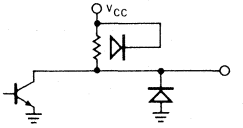


$\overline{RBO}$ OUTPUT

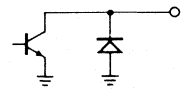


OUTPUTS

Equivalent Circuit (Pin 4)



Equivalent Circuit (Pins 9 thru 15)



APPLICATIONS

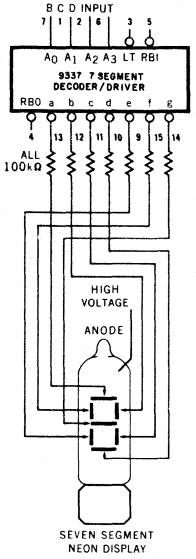
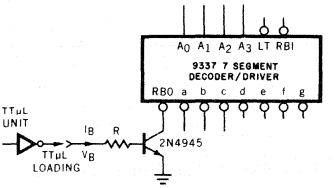


Fig. 8 — SEVEN SEGMENT NEON DISPLAY



TRANSISTOR BASE RESISTOR	TTL U.L. (High Level)	WORST CASE TRANSISTOR BASE CURRENT
1.5 kΩ	20 U.L.	1.2 mA
3 kΩ	10 U.L.	600 μA
15 kΩ	2 U.L.	120 μA
30 kΩ	1 U.L.	60 μA

NOTE: When V_B is high complete display blanking occurs. Almost any high beta NPN Transistor can be used.

Fig. 9 — COMPLETE DISPLAY BLANKING

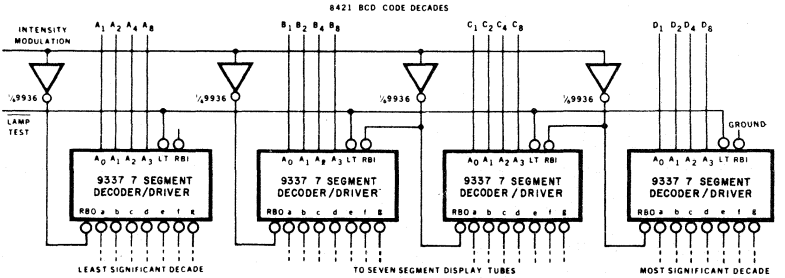


Fig. 10 — FOUR DECADE SEVEN SEGMENT INTEGER DISPLAY SCHEME

This scheme incorporates automatic blanking of leading edge zeroes and intensity modulation using an external variable duty cycle signal.

PACKAGE INFORMATION

7B — 16 LEAD DUAL IN-LINE PACKAGE

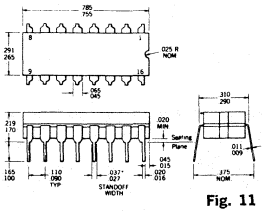


Fig. 11

NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.2 grams
*The .037/.027 dimension does not apply to the corner leads

4L — 16 LEAD (BeO) FLATPAK

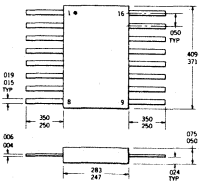


Fig. 12

NOTES:
All dimensions in inches
Leads are gold-plated kovar
Package weight is 0.4 gram

TTL/MSI 9338
8-BIT MULTIPLE PORT REGISTER

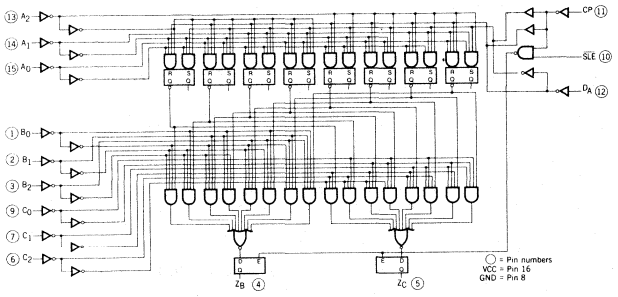
GENERAL DESCRIPTION – The TTL/MSI 9338 is an 8-bit multiple port register designed for high speed random access memory applications where the ability to simultaneously read and write is desirable. A common use would be as a register bank in a three address computer. Data can be written into any one of the 8-bits, and read from any two of the 8-bits simultaneously. The circuit uses TTL technology and is compatible with all members of Fairchild's TTL family.

- MASTER-SLAVE OPERATION PERMITTING SIMULTANEOUS WRITE/READ WITHOUT RACE PROBLEMS
- SIMULTANEOUSLY READ 2-BITS AND WRITE 1-BIT IN ANY ONE OF 8-BIT POSITIONS
- READILY EXPANDABLE TO ALLOW FOR LARGER WORD SIZES
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- ALL CERAMIC "HERMETIC" 16 PIN DUAL IN-LINE AND FLAT PACKAGES
- TTL COMPATIBLE

PIN NAMES		LOADING
A_0, A_1, A_2	Write Address Inputs	2/3 U.L.
D_A	Data Input	2/3 U.L.
B_0, B_1, B_2	B Read Address Inputs	2/3 U.L.
Z_B	B Output	10 U.L.
C_0, C_1, C_2	C Read Address Inputs	2/3 U.L.
Z_C	C Output	10 U.L.
CP	Clock Pulse Input	2/3 U.L.
$\overline{SLE}$	Slave Enable (Active Low) Input	2/3 U.L.

1 Unit Load (U.L.) = 40 μA High/1.6 mA Low

LOGIC DIAGRAM



LOGIC SYMBOL

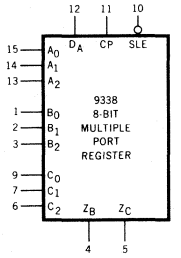


Fig. 1

CONNECTION DIAGRAM
DIP (TOP VIEW)

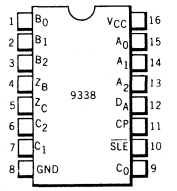


Fig. 2

FLATPAK (TOP VIEW)

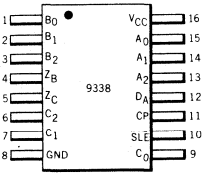


Fig. 3

Order Information on last page. See Notes on page 3.

FAIRCHILD
SEMICONDUCTOR

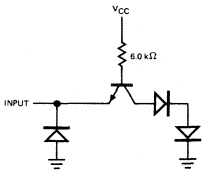
FUNCTIONAL DESCRIPTION – The 9338 8-bit multiple port register may be considered as a 1-bit slice of eight high speed working registers. Data may be written into any one of eight storage locations and read out from any two of the eight storage locations simultaneously. Master-slave operation eliminates all race problems associated with simultaneous writing in and reading from the same location.

The timing of this data transfer is similar to that of a standard master-slave flip-flop. While the clock is low the slaves are held steady, but the information on the D (data) input is permitted to enter the selected master. The next clock transition from low to high locks the masters in their present states making them insensitive to the D input and write address inputs. This rising clock edge also connects each of the two slaves to the selected masters causing their contents to be reflected on the outputs. Outputs change, therefore, following the low to high transition of the clock as on almost all Fairchild TTL/MSI devices and TTL flip-flops.

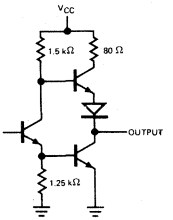
The slave enable ($\overline{SLE}$) input may be used to defeat the master-slave operation. If the slave enable ($\overline{SLE}$) line is held low, the slaves are continuously enabled allowing immediate transfer of information from the selected masters to the outputs.

TYPICAL INPUT AND OUTPUT CIRCUITS

INPUT EQUIVALENT CIRCUIT



OUTPUT EQUIVALENT CIRCUIT



TYPICAL INPUT AND OUTPUT CHARACTERISTICS

INPUT CURRENT VERSUS INPUT VOLTAGE
D_A A_2 A_1 A_0 C_2 C_1 C_0 B_2 B_1 B_0 CP

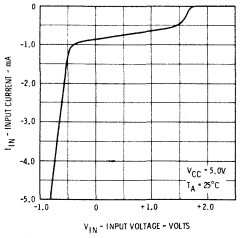


Fig. 5

INPUT CURRENT VERSUS INPUT VOLTAGE $\overline{SLE}$

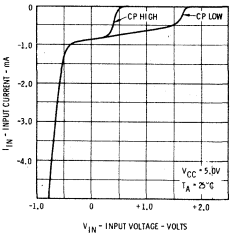


Fig. 6

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE Z_B AND Z_C (LOW STATE)

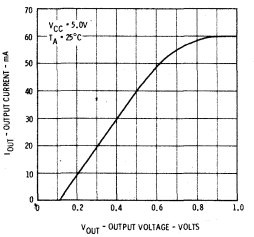


Fig. 7

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (D.C.)	−0.5 V to +5.5 V
*Input Current (D.C.)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output High)	0.5 V to +V_{CC}
Output Current (D.C.) (Output Low)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
U7B/U4L933851X	4.50 V	5.0 V	5.50 V	−55°C to +125°C
U7B/U4L933859X	4.75 V	5.0 V	5.25 V	0°C to 75°C

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

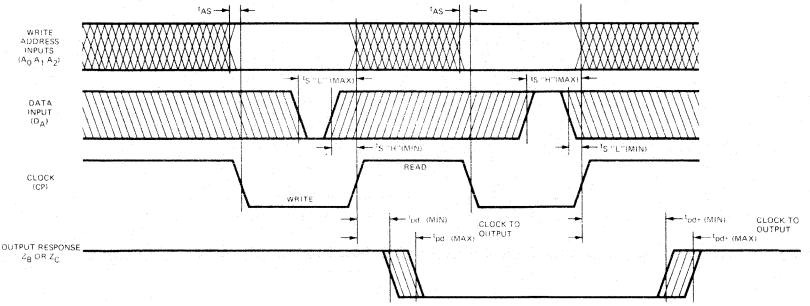
SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		MIN.	TYP. (Note 4)	MAX.		
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = −0.8 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.2	0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{IH}	Input HIGH Level	2.0			Volts	Guaranteed input logical HIGH voltage for all inputs
V_{IL}	Input LOW Level			0.8	Volts	Guaranteed input logical LOW voltage for all inputs
I_{IL}	Input LOW Current		−0.64	−1.1	mA	V_{CC} = MAX., V_{IN} = 0.4 V
				27	μA	V_{CC} = MAX., V_{IN} = 2.4 V
I_{IH}	Input HIGH Current			1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{SC}	Output Short Circuit Current	−10	−50	−70	mA	V_{CC} = MAX., V_{OUT} = 0 V
I_{CC}	Power Supply Current		85	135	mA	V_{CC} = MAX.

NOTES:
(1) The actual Testing Procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this Specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California (see page 1 for address and phone).
(2) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
(3) The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
(4) Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.

SWITCHING CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

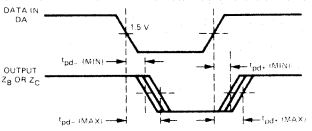
SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		MIN.	TYP.	MAX.		
t_S "H" t_S "L"	HIGH Data Setup Time LOW Data Setup Time	8.0 0	14 7.0	20 12	ns ns	C_L = 15 pF (See Fig. 8)
t_{AS}	Write Address Setup Time		5.0	10	ns	C_L = 15 pF (See Fig. 8)
t_{pd-} t_{pd+}	Read Time (Clock to Output)	15 20	21 30	35 40	ns ns	C_L = 15 pF (See Fig. 8)
t_{pd-} t_{pd+}	Delay Time (D_A to Z_B or Z_C)	35 30	40 35	50 50	ns ns	C_L = 15 pF (See Fig. 9)
t_{pd++} t_{pd+-} t_{pd-+} t_{pd--}	Read Time B or C Address to Output	15 20 20 20	22 27 30 27	30 35 40 35	ns ns ns ns	C_L = 15 pF (See Fig. 10)
t_{cp} "L"	Clock LOW Time Required to Write	2.0	7.0	20	ns	C_L = 15 pF (See Fig. 11)
t_{cp} "H"	Clock HIGH Time Required to Read	8.0	15	23	ns	C_L = 15 pF (See Fig. 12)

SWITCHING WAVEFORMS



The crosshatched areas of the input waveforms indicate when inputs are permitted to change. The crosshatched areas on the output response waveforms indicate minimum and maximum propagation delays.

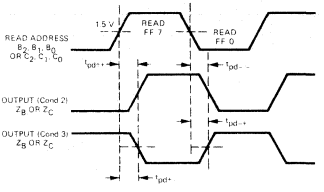
Fig. 8 DATA AND WRITE ADDRESS SETUP TIMES; READ TIME (CLOCK PULSE TO OUTPUT)



OTHER CONDITIONS

1. CP = LOW
2. $\overline{SLE}$ = LOW
3. $A_2, A_1, A_0 = B_2, B_1, B_0 = C_2, C_1, C_0$

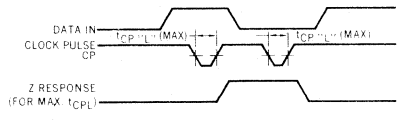
Fig. 9 $-t_{pd}$ (DATA INPUT TO OUTPUT)



OTHER CONDITIONS

1. CP = HIGH
2. Master FF 7 = H
3. Master FF 7 = L
   Master FF 0 = H

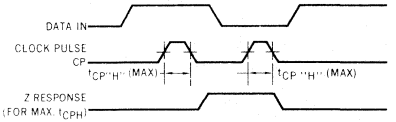
Fig. 10 $-t_{pd}$ (READ ADDRESS TO OUTPUT)



OTHER CONDITIONS

1. $\overline{SLE}$ = LOW
2. $A_2, A_1, A_0 = B_2, B_1, B_0 = C_2, C_1, C_0$

Fig. 11 t_{CP}"L" (CLOCK LOW TIME REQUIRED TO WRITE)



OTHER CONDITIONS

1. $\overline{SLE}$ = HIGH
2. $A_2, A_1, A_0 = B_2, B_1, B_0 = C_0, C_1, C_2$

Fig. 12 t_{CP}"H" (CLOCK HIGH TIME REQUIRED TO READ)

DEFINITION OF TERMS

READ TIME (CLOCK TO OUTPUT) – Is defined as the time elapsed between the rising edge of the clock pulse and data readout when $\overline{SLE}$=H.

READ TIME (READ ADDRESS TO OUTPUT) – Is defined as the time elapsed between a change in the read address and the corresponding data readout when CP=H.

THROUGH DELAY (D_A TO Z_B OR Z_C) – Is defined as the through delay between input and the output when the read (B or C) and write (A) addresses are identical, and $\overline{SLE}$=L, and CP=L.

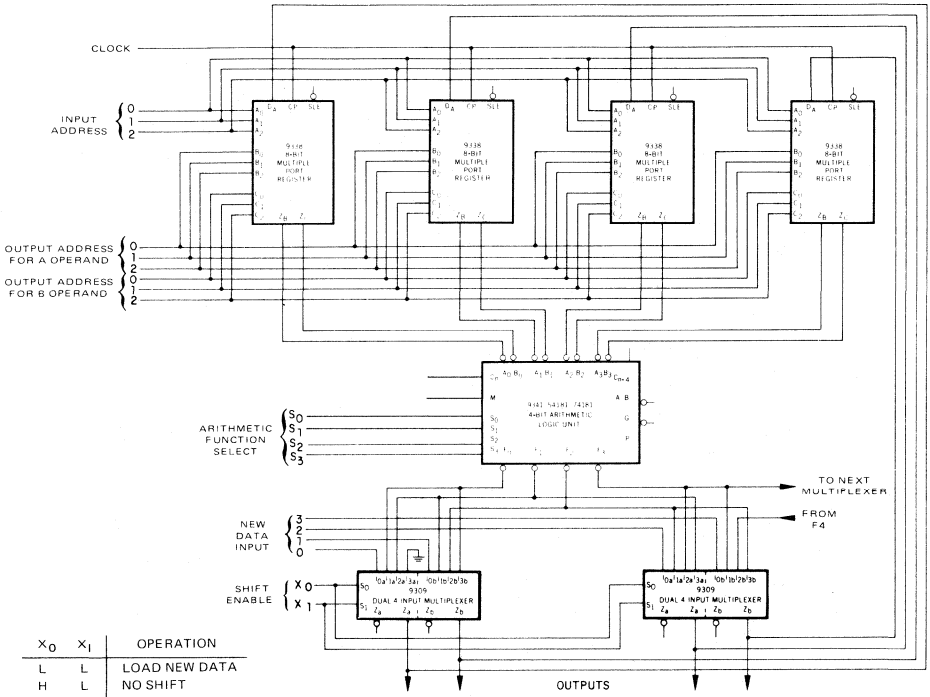
DATA SET UP TIME (t_s) – Is defined as the time required for a high (t_s "H") or a low (t_s "L") logic level to be present at the data input prior to the clock transition from low to high, in order for the master to recognize and store the new data. For one particular device and operating condition $t_{smin} = t_{smax}$ (neglecting minor differences between different masters). The published limit of t_s(min) and t_s(max) cover the production spread of the parameters. For predicable system performance, input data must be stable between these limits.

t_{CP} "L" (CLOCK LOW TIME REQUIRED TO WRITE) – This parameter is defined as the minimum Low clock pulse width required to write information into the master.

t_{CP} "H" (CLOCK HIGH TIME REQUIRED TO READ) – This parameter is defined as the minimum High clock pulse width required to store information in the slaves.

WRITE ADDRESS SET UP TIME (t_{AS}) – Is the time required for the write address to be present before the high to low clock transition so that the correct master is addressed and other masters are not disturbed. When writing data into the 9338, the write address inputs should be stable from t_{AS} (max) before the high to low transition of the clock and while the clock is low but they may change simultaneously with the low to high clock transition.

APPLICATIONS



X_0	X_1	OPERATION
L	L	LOAD NEW DATA
H	L	NO SHIFT
L	H	SHIFT LEFT
H	H	SHIFT RIGHT

The primary intended usage for the 9338 is as a 1-bit slice of eight registers/accumulators to be used with an arithmetic logic unit either the 9341/74181 or 9340. Shown above is a 4-bit section of such a system. This is easily expandable to a larger word length. The system provides eight storage registers any of which may be used as accumulators, data registers, or scratch pad memory.

One or two words can be written into the 9341/74181 and operated on according to the two select lines. The output can be fed back to the registers into the same or a new location and it may be shifted left or right by the multiplexers before being reloaded. New data is also entered through the multiplexers. Two words may be operated on by the 9341/74181 at the same time new data is being loaded for increased speed.

This configuration results in an arithmetic unit capable of operating by itself, without additional access to the main memory. The unit can execute short subroutines extremely rapidly by using the eight registers provided by the 9338. The shifting capability provided by the multiplexers permits multiplication and division to be performed.

With additional gating, this section could be part of a BCD arithmetic unit instead of the hexadecimal (binary) mode described here.

Fig. 14 THREE ADDRESS ARITHMETIC UNIT WITH EIGHT REGISTERS

APPLICATIONS

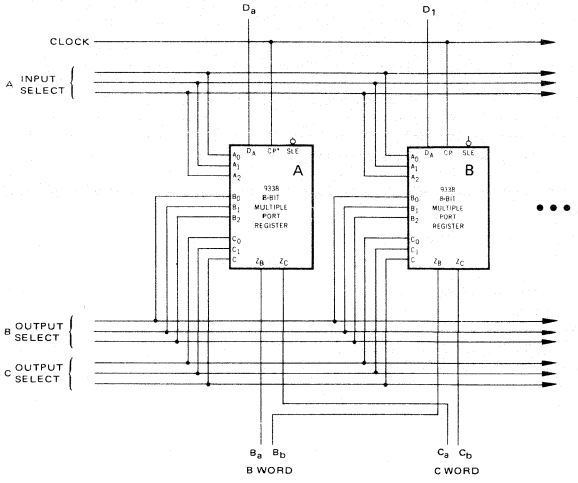


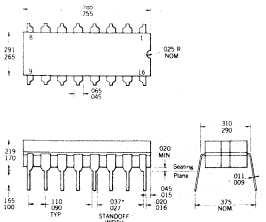
Fig. 15 PARALLEL EXPANSION

One 9338 is needed for each bit of the required word length. The read and write and write input lines should be connected in common on all of the devices. This register configuration provides 2 words of n-bits each at one time as is illustrated above, where n devices are connected in parallel.

ORDER INFORMATION – Specify U7B9338XXX for 16 pin Dual In-Line package or U4L9338XXX for 16 pin Flat package, where XXX is 51X for the –55°C to +125°C temperature range, or 59X for the 0°C to +75°C temperature range.

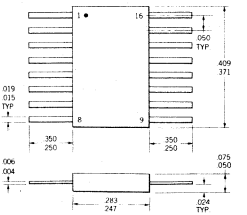
PACKAGE INFORMATION

7B – 16 LEAD DUAL IN-LINE PACKAGE



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers.
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Hermetically sealed alumina ceramic package
Leads are tin plated kovar
Package weight is 2.2 grams
The .037/.027 dimension does not apply to the corner leads

4L – 16 LEAD FLATPAK



NOTES:
All dimensions in inches
Leads are gold plated kovar
Package weight is 0.4 gram

9340

MSI 4-BIT ARITHMETIC LOGIC UNIT

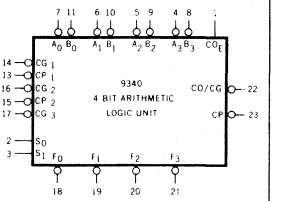
A FAIRCHILD TRANSISTOR-TRANSISTOR MICROLOGIC IC PRODUCT

GENERAL DESCRIPTION — The 9340 is a high speed arithmetic logic unit which can perform in parallel the arithmetic operations add or subtract, or either of six logic functions on two four-bit binary words. The device incorporates full carry-lookahead internally, and provides either a ripple carry output or carry lookahead outputs. An internal carry input network accepts carry lookahead outputs from up to three other packages producing a 16 bit full carry lookahead ALU without additional gates. Ripple carries can be used between additional blocks of 12 bits to further expand the word length.

FEATURES:

- **MULTIFUNCTION CAPABILITY**
  Two Arithmetic Operations — Add, Subtract
  Six Logic Functions — A Ex OR B, A AND B, Plus Four Others
- **ADD TWO 4-BIT WORDS IN 28 ns**
- **SUBTRACT TWO 4-BIT WORDS IN 33 ns**
- **LOOK-AHEAD CARRY INPUT AND OUTPUT NETWORKS ON CHIP**
- **EXPANSION FROM 4 BITS TO 16 BITS WITH ONLY 14 ns ADDITIONAL DELAY**
- **HIGH DRIVE OUTPUT CIRCUITRY**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **INPUT/OUTPUT CHARACTERISTICS PROVIDE EASY INTERFACING WITH FAIRCHILD DTμL, LPDTμL, TTμL, AND MSI FAMILIES**

LOGIC SYMBOL



V_{CC} = Pin 24
Gnd = Pin 12

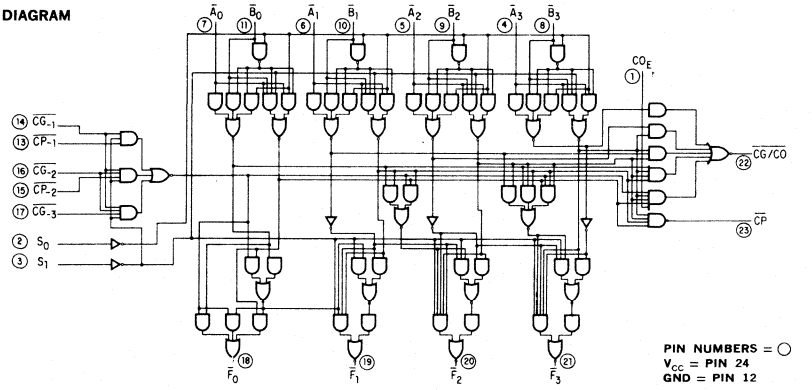
Fig. 1

ABSOLUTE MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to GND	−0.5 V to +7.0 V
Voltages Applied to Outputs for High Output State	−0.5 V to V_{CC} Value
Input Voltage (D.C.)	−0.5 V to +5.5 V
Output Current into Low Outputs	50 mA

ORDER INFORMATION — Specify U6N9340XXX for 24 pin Dual In-Line Package or U4M9340XXX for 24 pin Flatpak, where XXX is 51X for the −55°C to +125°C temperature range, or 59X for the 0°C to +75°C temperature range.

LOGIC DIAGRAM



PIN NUMBERS = ○
V_{CC} = PIN 24
GND = PIN 12

Fig. 2

FAIRCHILD SEMICONDUCTOR

FUNCTIONAL DESCRIPTION — The 9340 accepts two four-bit words, A_0, A_1, A_2, A_3 (A_{0-3}) and B_0, B_1, B_2, B_3 (B_{0-3}), and produces a four-bit output, F_0, F_1, F_2, F_3 (F_{0-3}). The output function is determined by the states on the control lines S_0 and S_1. The inputs and outputs of the 9340 may be considered to be active level low or active level high. Logic equivalents for four representations of the 9340 are shown in Figure 3a, b, c, and d.

The add and subtract operations are performed on the entire word, with carries or borrows propagated between bits of different weight. The arithmetic may be performed in 1's complement, 2's complement, or sign-magnitude notation. In the logic modes, carries are inhibited and the device acts like four gates of the type shown in Figure 3.

To achieve high speed operation, the 9340 is designed to be used in a carry lookahead system. Full carry lookahead is used inside the device to propagate carries between bits. Carry lookahead functions over the four bit block are available as outputs. These outputs are labeled $\overline{CO/CG}$ (Carry Out/Carry Generate) and $\overline{CP}$ (Carry Propagate) on the logic symbol. The carry in to the device is formed from a set of Carry Generate and Carry Propagate inputs (equation 1) so that three 9340's can be interconnected without any additional gates to form a 12 bit full carry lookahead ALU with a carry in. The pin labeled CO_E (Carry Out Enable) controls the $\overline{CO/CG}$ output according to equation 2. When CO_E is high, $\overline{CO/CG}$ becomes a Carry Out which can be used to ripple carries between blocks of 12 bits. The $\overline{CG_{-1}}$ input can be used for a ripple carry input, since this signal is sufficient to produce a carry in.

Both ripple carry and carry lookahead are illustrated in Figure 4 in the applications section which shows a 16 bit ALU and indicates how it can be expanded.

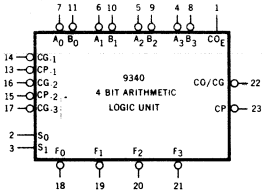
(1) $(\overline{CG_{-1}}) + (\overline{CP_{-1}})(\overline{CG_{-2}}) + (\overline{CP_{-1}})(\overline{CP_{-2}})(\overline{CG_{-3}}) = C_{in}$ (internal)

(2) $\overline{CO/CG} = (\overline{CG}) + (\overline{CP})(C_{in})(CO_E)$

Fig. 3 — FUNCTION TABLES FOR LOGIC EQUIVALENTS OF THE 9340

Note that when the input operants are defined as active high, the carry lookahead inputs and outputs are not formally carry generate and carry propagate. Consequently, these pins have been relabeled CX and CY in the active high cases. However, the signals are connected in the same manner as $\overline{CG}$ and $\overline{CP}$.

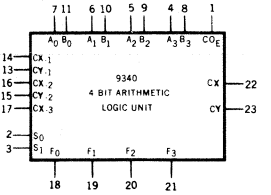
3a — ACTIVE LOW OPERANDS



V_{CC} = Pin 24
Gnd = Pin 12

CONTROL INPUTS S_0	CONTROL INPUTS S_1	OPERATION	EQUIVALENT LOGIC
L	L	A SUBTRACT B	
H	L	A ADD B	
L	H	A EX OR B	
H	H	A AND B	

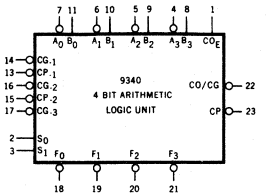
3b — ACTIVE HIGH OPERANDS



V_{CC} = Pin 24
Gnd = Pin 12

CONTROL INPUTS S_0	CONTROL INPUTS S_1	OPERATION	EQUIVALENT LOGIC
L	L	A SUBTRACT B	
H	L	A ADD B	
L	H	A EQUIV B	
H	H	A OR B	

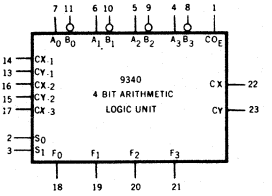
3c — ACTIVE LOW OPERANDS WITH INVERTED B



V_{CC} = Pin 24
Gnd = Pin 12

CONTROL INPUTS S_0	S_1	OPERATION	EQUIVALENT LOGIC
L	L	A ADD B	
H	L	A SUBTRACT B	
L	H	A EQUIV B	
H	H	A AND $\overline{B}$	

3d — ACTIVE HIGH OPERANDS WITH INVERTED B



V_{CC} = Pin 24
Gnd = Pin 12

CONTROL INPUTS S_0	S_1	OPERATION	EQUIVALENT LOGIC
L	L	A ADD B	
H	L	A SUBTRACT B	
L	H	A EX OR B	
H	H	A OR $\overline{B}$	

PIN NAMES

$\overline{A_0}$ to $\overline{A_3}$, $\overline{B_0}$ to $\overline{B_3}$	Operand Active Low Inputs
S_0, S_1	Mode Select Inputs
$\overline{CG_{-1}}$	Active Low Carry Generate Input from immediately preceding stage
$\overline{CP_{-1}}$	Active Low Carry Propagate Input from immediately preceding stage
$\overline{CG_{-2}}$	Active Low Carry Generate Input from second preceding stage
$\overline{CP_{-2}}$	Active Low Carry Propagate Input from second preceding stage
$\overline{CG_{-3}}$	Active Low Carry Generate Input from third preceding stage
CO_E	Carry Out Enable Input
$\overline{F_0}$, $\overline{F_1}$, $\overline{F_2}$, $\overline{F_3}$	Function (Active Low) Outputs
$\overline{CO/CG}$	Carry Out/Carry Generate (Active Low) Output
$\overline{CP}$	Carry Propagate (Active Low) Output

LOADING RULES

INPUTS	LOADING
S_0, S_1, $\overline{CP_{-1}}$, $\overline{CP_{-2}}$, $\overline{CG_{-3}}$	1 U.L.
CO_E	1.5 U.L.
$\overline{CG_{-2}}$	2 U.L.
$\overline{A_0}$ - $\overline{A_3}$, $\overline{B_0}$ - $\overline{B_3}$, $\overline{CG_{-1}}$	3 U.L.

OUTPUTS	FAN OUT
$\overline{F_0}$, $\overline{F_1}$, $\overline{F_2}$, $\overline{F_3}$, $\overline{CP}$, $\overline{CG/CO}$	10 U.L.

(1 U.L. = 1 TTμL Gate Input Load)

ELECTRICAL CHARACTERISTICS ($T_A = -55°C$ to $+125°C$; $V_{CC} = 5.0\ V \pm 10\%$) (Part No. U6N/4M934051X) — Pulse Tested

SYMBOL	CHARACTERISTIC	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	$V_{CC} = 4.5\ V$, $I_{OH} = -1.2\ mA$
V_{OL}	Output Low Voltage		0.4		0.21	0.4		0.4	Volts	$V_{CC} = 5.5\ V$, $I_{OL} = 16\ mA$ $V_{CC} = 4.5\ V$, $I_{OL} = 12.4\ mA$
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed High Input Threshold
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed Low Input Threshold
I_F	Input Load Current									
	$S_0, S_1, \overline{CP_{-1}}, \overline{CP_{-2}}, \overline{CG_{-3}}$		−1.6		−1.1	−1.6		−1.6	mA	$V_{CC} = 5.5\ V$
	$\overline{COE}$		−2.4		−1.65	−2.4		−2.4	mA	$V_F = 0.4\ V$ on Pin Under Test
	$\overline{CG_{-2}}$		−3.2		−2.2	−3.2		−3.2	mA	
	$\overline{A's}, \overline{B's}, \overline{CG_{-1}}$		−4.8		−3.3	−4.8		−4.8	mA	
I_F	Input Load Current									
	$S_0, S_1, \overline{CP_{-1}}, \overline{CP_{-2}}, \overline{CG_{-3}}$		−1.24		−0.97	−1.24		−1.24	mA	$V_{CC} = 4.5\ V$
	$\overline{COE}$		−1.86		−1.46	−1.86		−1.86	mA	$V_F = 0.4\ V$ on Pin Under Test
	$\overline{CG_{-2}}$		−2.48		−1.94	−2.48		−2.48	mA	
	$\overline{A's}, \overline{B's}, \overline{CG_{-1}}$		−3.72		−2.91	−3.72		−3.72	mA	
I_R	Input Leakage Current									
	$\overline{COE}, S_0, S_1, \overline{CP_{-1}}, \overline{CP_{-2}}, \overline{CG_{-3}}$				15	60		60	μA	$V_{CC} = 5.5\ V$, $V_R = 4.5\ V$
	$\overline{CG_{-2}}$				30	120		120	μA	Ground on other Inputs
	$\overline{A's}, \overline{B's}, \overline{CG_{-1}}$				45	180		180	μA	
I_{PD}	V_{CC} Current				85				mA	$V_{CC} = 5.0\ V$

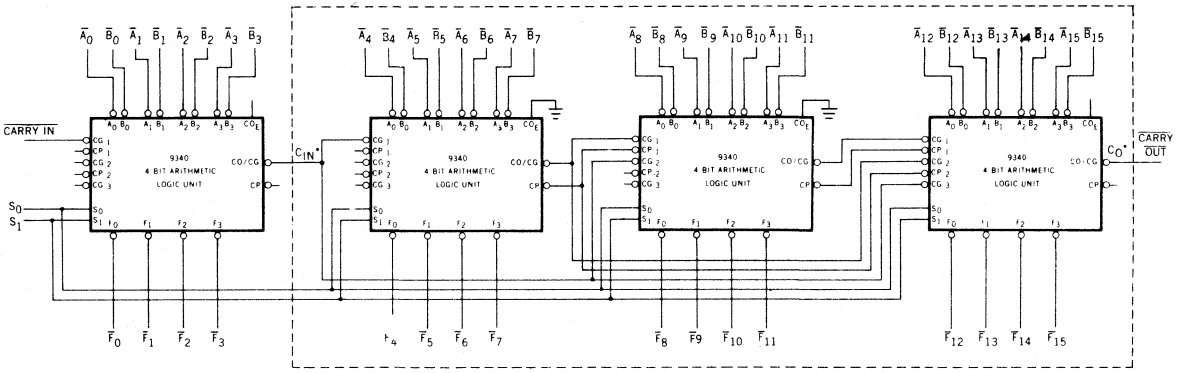
ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0\ V \pm 5\%$) (Part No. U6N/4M934059X) — Pulse Tested

SYMBOL	CHARACTERISTIC	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	$V_{CC} = 4.75\ V$, $I_{OH} = -1.2\ mA$
V_{OL}	Output Low Voltage		0.45		0.21	0.45		0.45	Volts	$V_{CC} = 5.25\ V$, $I_{OL} = 16\ mA$
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed High Input Threshold
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed Low Input Threshold
I_F	Input Load Current									
	$S_0, S_1, \overline{CP_{-1}}, \overline{CP_{-2}}, \overline{CG_{-3}}$		−1.6		−1.0	−1.6		−1.6	mA	$V_{CC} = 5.25\ V$
	$\overline{COE}$		−2.4		−1.5	−2.4		−2.4	mA	$V_F = 0.4\ V$ on Pin Under Test
	$\overline{CG_{-2}}$		−3.2		−2.0	−3.2		−3.2	mA	
	$\overline{A's}, \overline{B's}, \overline{CG_{-1}}$		−4.8		−3.0	−4.8		−4.8	mA	
I_F	Input Load Current									
	$S_0, S_1, \overline{CP_{-1}}, \overline{CP_{-2}}, \overline{CG_{-3}}$		−1.41		−0.9	−1.41		−1.41	mA	$V_{CC} = 4.75\ V$
	$\overline{COE}$		−2.12		−1.35	−2.12		−2.12	mA	$V_F = 0.4\ V$ on Pin Under Test
	$\overline{CG_{-2}}$		−2.82		−1.8	−2.82		−2.82	mA	
	$\overline{A's}, \overline{B's}, \overline{CG_{-1}}$		−4.23		−2.7	−4.23		−4.23	mA	
I_R	Input Leakage Current									
	$\overline{COE}, S_0, S_1, \overline{CP_{-1}}, \overline{CP_{-2}}, \overline{CG_{-3}}$				15	60		60	μA	$V_{CC} = 5.25\ V$, $V_R = 4.5\ V$
	$\overline{CG_{-2}}$				30	120		120	μA	Ground on other Inputs
	$\overline{A's}, \overline{B's}, \overline{CG_{-1}}$				45	180		180	μA	
I_{PD}	V_{CC} Current				85				mA	$V_{CC} = 5.0\ V$

A.C. CHARACTERISTICS ($T_A = 25°C$, $V_{CC} = 5.0\ V$)

SYMBOL	CHARACTERISTIC	TYPICAL LIMITS ADD	TYPICAL LIMITS SUBTRACT	UNITS	CONDITIONS
t_{pd+}	Data Input to Data	28	33	ns	
t_{pd-}	Output ($\overline{B_0}$ to $\overline{F_3}$)	28	32	ns	
t_{pd+}	Data Input to Carry	15	20	ns	
t_{pd-}	Output ($\overline{B_0}$ to $\overline{CO/CG}$)	17	21	ns	$C_L = 15\ pF$
t_{pd+}	Carry Input to Carry	16	16	ns	$V_{CC} = 5.0\ V$
t_{pd-}	Output ($\overline{CG_{-3}}$ to $\overline{CO/CG}$)	18	18	ns	
t_{pd+}	Carry Input to Data	28	28	ns	
t_{pd-}	Output ($\overline{CG_{-3}}$ to $\overline{F_3}$)	30	30	ns	

APPLICATIONS



For 1's complement arithmetic, connect $\overline{\text{Carry In}}$ to $\overline{\text{Carry Out}}$
For 2's complement arithmetic, connect $\overline{\text{Carry In}}$ to S_0

FUNCTION TABLE

S_0	S_1	FUNCTION
L	L	A SUBTRACT B
H	L	A ADD B
L	H	A EX OR B
H	H	A AND B

H = High Voltage Level
L = Low Voltage Level

DELAY TABLE

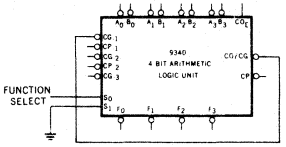
WORD LENGTH (in bits)	ADD (in ns)	SUBTRACT (in ns)
1-4	28	35
5-16	42	49
17-28	56	63
29-40	70	77
41-52	84	91
53-64	98	105
65-76	112	119
77-88	126	133
89-100	140	147

Fig. 4 — 9340 16-BIT FULL LOOKAHEAD CARRY ALU

Shown above is a 16 bit ALU with full carry lookahead. For 2's complement arithmetic a carry-in must be forced in subtraction; this may be done by connecting the $\overline{\text{carry in}}$ to the S_0 control line. For 1's complement arithmetic, an "end around carry" is required, so the $\overline{\text{carry out}}$ should be connected to the $\overline{\text{carry in}}$. Care must be exercised in 1's complement mode due to problems associated with logic oscillations between the two possible representations of zero.

The portion shown within the dashed lines is a 12 bit full lookahead ALU with a carry in $\overline{C_{in}}^*$ and carry out $\overline{C_0}^*$. If an ALU longer than 16 bits is required, then additional 12 bit blocks like the one shown may be added with a ripple carry between the blocks, $\overline{C_0}^*$ of one block goes to $\overline{C_{in}}^*$ of the next. In the 16 bit ALU, the very first 9340 does not add any delay, even though it is used in a ripple carry mode, because the $\overline{\text{carry in}}$ appears at $\overline{CO/CG}$ just as fast as the input operands appear. Note that this is true only for the first 9340, because only at this point are the inputs and the carry in available simultaneously.

APPLICATIONS (CONT'D)



S_0	FUNCTION
L	A SUBTRACT B
H	A ADD B

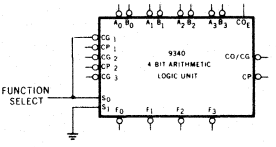


Fig. 5a — FOUR BIT ADDER/SUBTRACTOR USING 1's COMPLEMENT ARITHMETIC

This figure illustrates a 1's complement Adder/Subtractor with active low inputs and outputs. Connection from $\overline{CO/CG}$ to $\overline{CG_{-1}}$ represents end around carry from the most significant to the least significant unit. Care must be exercised in this mode due to problems associated with logic oscillations between the two possible representations of zero.

Fig. 5b — FOUR BIT ADDER/SUBTRACTOR USING 2's COMPLEMENT ARITHMETIC

This figure shows a 2's complement Adder/Subtractor with low inputs and outputs. The S_0 terminal is connected to the $\overline{CG_{-1}}$ so as to provide an addition of one to the least significant bit during subtraction.

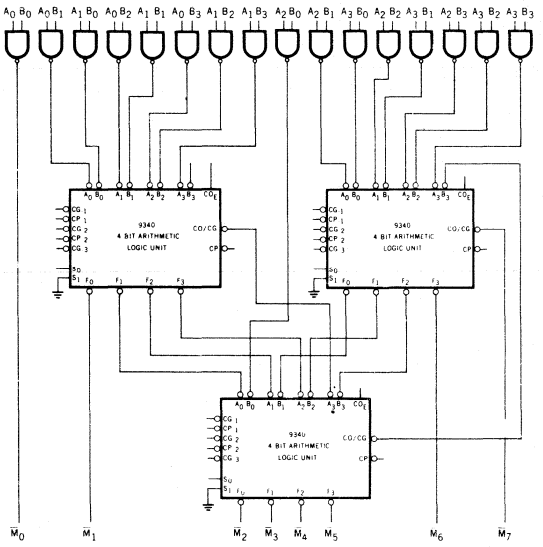
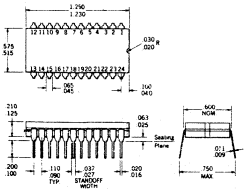


Fig. 6 — 4x4 MULTIPLICATION

This figure illustrates a 4x4 multiplier which uses four 9002 gate packages preceding a network of 9340 arithmetic logic units connected as adders. This scheme can be extended to provide multiplication over larger word lengths.

PACKAGE INFORMATION

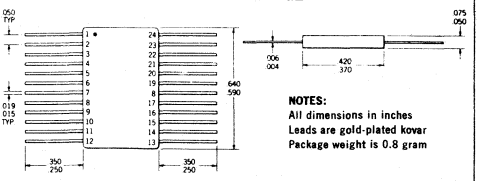
6N — DUAL IN-LINE PACKAGE



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .600" centers. They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 6.5 grams

Fig. 7

4M — FLAT PACKAGE



NOTES:
All dimensions in inches
Leads are gold-plated kovar
Package weight is 0.8 gram

Fig. 8

TTμL/MSI 9341/54181, 74181
4-BIT ARITHMETIC LOGIC UNIT
A FAIRCHILD TTμL® IC PRODUCT

GENERAL DESCRIPTION – The TTμL/MSI 9341/54181, 74181 is a 4-bit high speed Arithmetic Logic Unit (ALU) which can perform all the possible 16 logic operations on two variables and a variety of arithmetic operations; the Add and Subtract modes are the most important. The ALU is fully compatible with all members of the Fairchild TTμL family.

- **PROVIDES 16 ARITHMETIC OPERATIONS**
  ADD, SUBTRACT, COMPARE, DOUBLE,
  PLUS TWELVE OTHER ARITHMETIC OPERATIONS
- **PROVIDES ALL 16 LOGIC OPERATIONS OF TWO VARIABLES**
  EXCLUSIVE–OR, COMPARE, AND, NAND, OR, NOR, PLUS
  TEN OTHER LOGIC OPERATIONS
- **FULL LOOKAHEAD FOR HIGH SPEED ARITHMETIC OPERATION ON LONG WORDS**
- **INPUT CLAMP DIODES**
- **TTμL COMPATIBLE**

PIN NAMES		LOADING
$\overline{A_0}$ to $\overline{A_3}$, $\overline{B_0}$ to $\overline{B_3}$	Operand (Active Low) Inputs	3
S_0, S_1, S_2, S_3	Function - Select Inputs	4
M	Mode Control Input	1
C_n	Carry Input	5
$\overline{F_0}$, $\overline{F_1}$, $\overline{F_2}$, $\overline{F_3}$	Function (Active Low) Outputs	10*
A = B	Comparator Output	O.C/10
$\overline{G}$	Carry Generate (Active Low) Output	10*
$\overline{P}$	Carry Propagate (Active Low) Output	10*
$C_n + 4$	Carry Output	10*

1 Unit Load (U.L.) = 40 μA High/1.6 mA Low O.C. = Open Collector Output
*Note: 10 U.L. is the output Low drive factor and 20 U.L. is the output High drive factor.

LOGIC SYMBOL

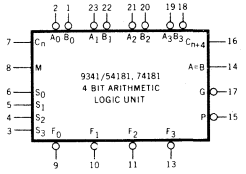


Fig. 1

CONNECTION DIAGRAM
DIP (TOP VIEW)

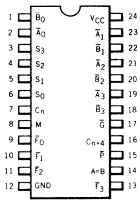


Fig. 2

FLATPAK (TOP VIEW)

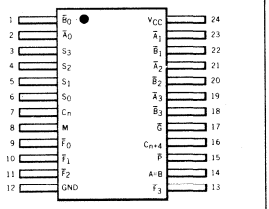


Fig. 3

LOGIC DIAGRAM

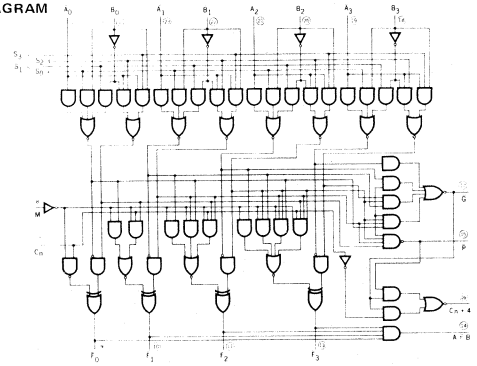


Fig. 4

Order Information on Last Page.

FAIRCHILD SEMICONDUCTOR

FUNCTIONAL DESCRIPTION – The TTL/MSI 9341/54181, 74181 is a 4-bit, high speed parallel Arithmetic Logic Unit (ALU). Controlled by the four Function Select Inputs ($S_0 \ldots S_3$) and the Mode Control Input (M), it can perform all the 16 possible logic operations or 16 different arithmetic operations on active HIGH or active LOW operands. The Function Table below lists these operations.

When the Mode Control Input (M) is HIGH, all internal carries are inhibited and the device performs Logic operations on the individual bits as listed. When the Mode Control Input is LOW, the carries are enabled and the device performs Arithmetic operations on the two, 4-bit words. The device incorporates full internal look-ahead carry and provides for either ripple carry between devices using the C_{n+4} output, or for carry look-ahead between packages using the signals P (carry propagate) and G (carry generate). P and G are not affected by carry in. When speed requirements are not stringent, the 9341/54181, 74181 can be used in a simple ripple carry mode by connecting the carry out (C_{n+4}) signal to the carry input (C_n) of the next unit. For high speed operation the 9341/54181, 74181 is used in conjunction with the 9342/54182, 74182 carry look-ahead circuit. One carry look-ahead package is required for each group of four 9341/54181, 74181 devices. Carry look-ahead can be provided at various levels and offers high speed capability over extremely long word lengths.

The A = B output from the 9341/54181, 74181 goes HIGH when all four F outputs are HIGH and can be used to indicate logic equivalence over 4-bits when the unit is in the subtract mode. The A = B output is open collector and can be wire ANDed with other A = B outputs to give a comparison for more than 4-bits. The A = B signal can also be used with the carry out signal to indicate A > B and A < B.

The Function Table lists the Arithmetic operations that are performed without a carry in. An incoming carry adds a one to each operation. Thus Select Code LHHL generates A minus B minus 1 (2's complement notation) without a carry in and generates A minus B when a carry is applied. Because subtraction is actually performed by complementary addition (1's complement), a CARRY OUT means BORROW; thus a carry is generated when there is no underflow and no carry is generated when there is underflow.

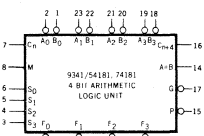
As indicated the 9341/54181, 74181 can be used with either active LOW inputs producing active LOW outputs or with active HIGH inputs producing active HIGH outputs. For either case the table lists the operations that are performed to the operands labeled inside the logic symbol.

FUNCTION TABLE

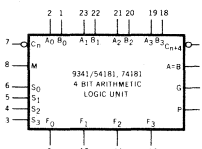
MODE SELECT INPUTS $S_3\ S_2\ S_1\ S_0$	ACTIVE LOW INPUTS & OUTPUTS		ACTIVE HIGH INPUTS & OUTPUTS	
	LOGIC (M = H)	ARITHMETIC ** (M = L) (C_n = H)	LOGIC (M = H)	ARITHMETIC ** (M = L) (C_n = L)
L L L L	$\overline{A}$	A minus 1	$\overline{A}$	A
L L L H	$\overline{AB}$	AB minus 1	$\overline{A+B}$	A + B
L L H L	$\overline{A}+B$	$A\overline{B}$ minus 1	$\overline{A\overline{B}}$	$A+\overline{B}$
L L H H	Logical 1	minus 1	Logical 0	minus 1
L H L L	$\overline{A+B}$	A plus [A + $\overline{B}$]	$\overline{AB}$	A plus $A\overline{B}$
L H L H	$\overline{B}$	AB plus [A + $\overline{B}$]	$\overline{B}$	[A + B] plus $A\overline{B}$
L H H L	$\overline{A \oplus B}$	A minus B minus 1	A ⊕ B	A minus B minus 1
L H H H	$A+\overline{B}$	$A+\overline{B}$	$A\overline{B}$	$A\overline{B}$ minus 1
H L L L	$A\overline{B}$	A plus [A + B]	$\overline{A+B}$	A plus AB
H L L H	A ⊕ B	A plus B	A ⊕ B	A plus B
H L H L	B	AB plus [A + B]	B	[A + $\overline{B}$] plus AB
H L H H	A + B	A + B	AB	AB minus 1
H H L L	Logical 0	A plus A*	Logical 1	A plus A*
H H L H	$A\overline{B}$	AB plus A	$A+\overline{B}$	[A + B] plus A
H H H L	AB	AB plus A	A + B	[A + $\overline{B}$] plus A
H H H H	A	A	A	A minus 1

LOGIC SYMBOLS

ACTIVE LOW OPERANDS



ACTIVE HIGH OPERANDS

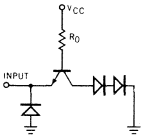


V_{CC} = Pin 24
GND = Pin 12

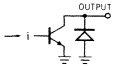
H = High Voltage Level
L = Low Voltage Level
*Each bit is shifted to the next more significant position
**Arithmetic operations expressed in 2's complement notation

TYPICAL INPUT AND OUTPUT CIRCUITS

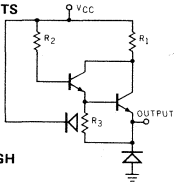
INPUTS EQUIVALENT CIRCUIT



OUTPUTS EQUIVALENT CIRCUITS



LOW



HIGH

Fig. 5 INPUT CURRENT VERSUS INPUT VOLTAGE

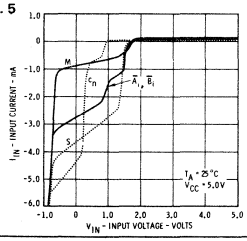


Fig. 6 OUTPUT CURRENT VERSUS OUTPUT VOLTAGE LOW STATE

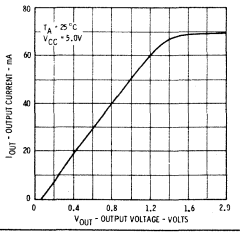
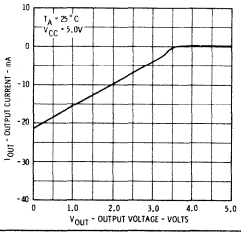


Fig. 7 OUTPUT CURRENT VERSUS OUTPUT VOLTAGE HIGH STATE



ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (D.C.)	−0.5 V to +5.5 V
*Input Current (D.C.)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output High)	0.5 V to +V_{CC} value
Output Current (D.C.) (Output Low)	+30 mA

*Either Input Voltage Limit or Input Current is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC}) MIN.	TYP.	MAX.	TEMPERATURE
U6N/U4M 934151X or 54181	4.5 V	5.0 V	5.5 V	−55°C to 125°C
U6N/U4M 934159X or 74181	4.75 V	5.0 V	5.25 V	0°C to 75°C

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted) See Notes on Page 4.

SYMBOL	CHARACTERISTIC	LIMITS MIN.	LIMITS MAX.	UNITS	CONDITIONS
V_{OH}	Output HIGH Voltage	2.4		Volts	V_{CC} = MIN., I_{OH} = −800 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{IH}	Input HIGH Level	2.0		Volts	Guaranteed input logical HIGH voltage for all inputs
V_{IL}	Input LOW Level		0.8	Volts	Guaranteed input logical LOW voltage for all inputs
I_{IL}	Input LOW Current			mA	V_{CC} = MAX., V_{IN} = 0.4 V
	M		−1.6		
	$\overline{A}_0$ $\overline{A}_1$ $\overline{A}_2$ $\overline{A}_3$ $\overline{B}_0$ $\overline{B}_1$ $\overline{B}_2$ $\overline{B}_3$		−4.8		
	S_0 S_1 S_2 S_3		−6.4		
	C_n		−8.0		
I_{IH}	Input HIGH Current			μA	V_{CC} = MAX., V_{IN} = 2.4 V
	M		40		
	$\overline{A}_0$ $\overline{A}_1$ $\overline{A}_2$ $\overline{A}_3$ $\overline{B}_0$ $\overline{B}_1$ $\overline{B}_2$ $\overline{B}_3$		120		
	S_0 S_1 S_2 S_3		160		
	C_n		200		
	Input HIGH Current all inputs		1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{SC} (I_{OS})	Output Short Circuit Current	−20	−55	mA	51 Grade, V_{CC} = MAX. V_{OUT} = 0.0 V
		−18	−57	mA	59 Grade
I_{CC}	Power Supply Current		127	mA	51 Grade, V_{CC} = MAX. C_n = B_0 = B_1 = B_2 = B_3 = GND, all other inputs = 4.5 V
			140	mA	59 Grade
			135	mA	51 Grade, V_{CC} = MAX. M = S_0 = S_1 = S_2 = S_3 = 4.5 V, all other inputs = GND
			150	mA	59 Grade

SWITCHING CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V, Pin 12 = GND)

CHARACTERISTICS		LIMITS TYP.	LIMITS MAX.	UNITS	CONDITIONS
t_{PLH}	(C_n to C_n + 4)	12	16	ns	M = OV, (Sum or Diff Mode)
t_{PHL}		13	17		See Fig. 8 and Tables I & II
t_{PLH}	(C_n to $\overline{F}$ outputs)	13	16	ns	M = OV, (Sum Mode)
t_{PHL}		14	17		See Fig. 8 and Table I
t_{PLH}	($\overline{A}$ or $\overline{B}$ inputs to $\overline{G}$ output)	16	19	ns	M = S_1 = S_2 = OV, S_0 = S_3 = 4.5 V
t_{PHL}		9	12		(Sum Mode) See Fig. 8 and Table I
t_{PLH}	($\overline{A}$ or $\overline{B}$ inputs to $\overline{G}$ output)	18	22	ns	M = S_0 = S_3 = OV, S_1 = S_2 = 4.5 V
t_{PHL}		13	17		(Diff Mode) See Fig. 9 and Table II
t_{PLH}	($\overline{A}$ or $\overline{B}$ inputs to $\overline{P}$ output)	16	19	ns	M = S_1 = S_2 = OV, S_0 = S_3 = 4.5 V
t_{PHL}		11	15		(Sum Mode) See Fig. 8 and Table I
t_{PLH}	($\overline{A}$ or $\overline{B}$ inputs to $\overline{P}$ output)	17	21	ns	M = S_0 = S_3 = OV, S_1 = S_2 = 4.5 V
t_{PHL}		14	19		(Diff Mode) See Fig. 9 and Table II
t_{PLH}	($\overline{A_i}$ or $\overline{B_i}$ inputs to $\overline{F_i}$ outputs)	19	26	ns	M = S_1 = S_2 = OV, S_0 = S_3 = 4.5 V
t_{PHL}		24	32		(Sum Mode) See Fig. 8 and Table I
t_{PLH}	($\overline{A_i}$ or $\overline{B_i}$ inputs to $\overline{F_i}$ outputs)	20	26	ns	M = S_0 = S_3 = OV, S_1 = S_2 = 4.5 V
t_{PHL}		28	32		(Diff Mode) See Fig. 9 and Table II
t_{PLH}	($\overline{A_i}$ or $\overline{B_i}$ inputs to $\overline{F_i}$ + 1 outputs)	23	29	ns	M = OV, S_0 = S_3 = 4.5 V, S_1 = S_2 = OV
t_{PHL}		19	25		(Sum Mode) See Fig. 8 and Table I
t_{PLH}	($\overline{A_i}$ or $\overline{B_i}$ inputs to $\overline{F_i}$ + 1 outputs)	23	29	ns	M = OV, S_0 = S_3 = OV, S_1 = S_2 = 4.5 V
t_{PHL}		24	30		(Diff Mode) See Fig. 9 and Table II
t_{PLH}	($\overline{A}$ or $\overline{B}$ inputs to $\overline{F}$ outputs)	18	22	ns	M = 4.5 V (Logic Mode)
t_{PHL}		21	26		See Fig. 8 and Table III
t_{PLH}	($\overline{A}$ or $\overline{B}$ inputs to C_n + 4 output)	16	21	ns	M = OV, S_0 = S_3 = 4.5 V, S_1 = S_2 = OV
t_{PHL}		26	30		(Sum Mode) See Fig. 10 and Table I
t_{PLH}	($\overline{A}$ or $\overline{B}$ inputs to C_n + 4 output)	19	25	ns	M = OV, S_0 = S_3 = OV, S_1 = S_2 = 4.5 V
t_{PHL}		26	30		(Diff Mode)
t_{PLH}	($\overline{A}$ or $\overline{B}$ inputs to A = B output)	33	37	ns	M = S_0 = S_3 = OV, S_1 = S_2 = 4.5 V, R_O = 400 Ω to 5.0 V
t_{PHL}		30	32		(Diff Mode) See Fig. 9 and Table II

NOTES:

(1) The actual Testing Procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this Specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California (see page 1 for address and phone).

(2) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.

(3) The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

SWITCHING TIME WAVEFORMS

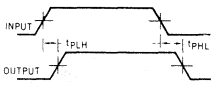


Fig. 8

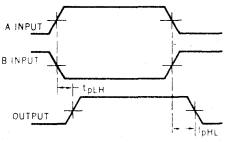


Fig. 9

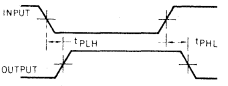


Fig. 10

SUM MODE TEST TABLE I

FUNCTION INPUTS: $S_0 = S_3 = 4.5$ V, $S_1 = S_2 = M = 0$ V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND	
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	C_n	Remaining $\overline{A}$ and $\overline{B}$	$\overline{F}_{i+1}$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	C_n	Remaining $\overline{A}$ and $\overline{B}$	$\overline{F}_{i+1}$
t_{PLH} t_{PHL}	$\overline{A}$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$	All $\overline{B}$	Any $\overline{F}$ or C_{n+4}

DIFF MODE TEST TABLE II

FUNCTION INPUTS: $S_1 = S_2 = 4.5$ V, $S_0 = S_3 = M = 0$ V

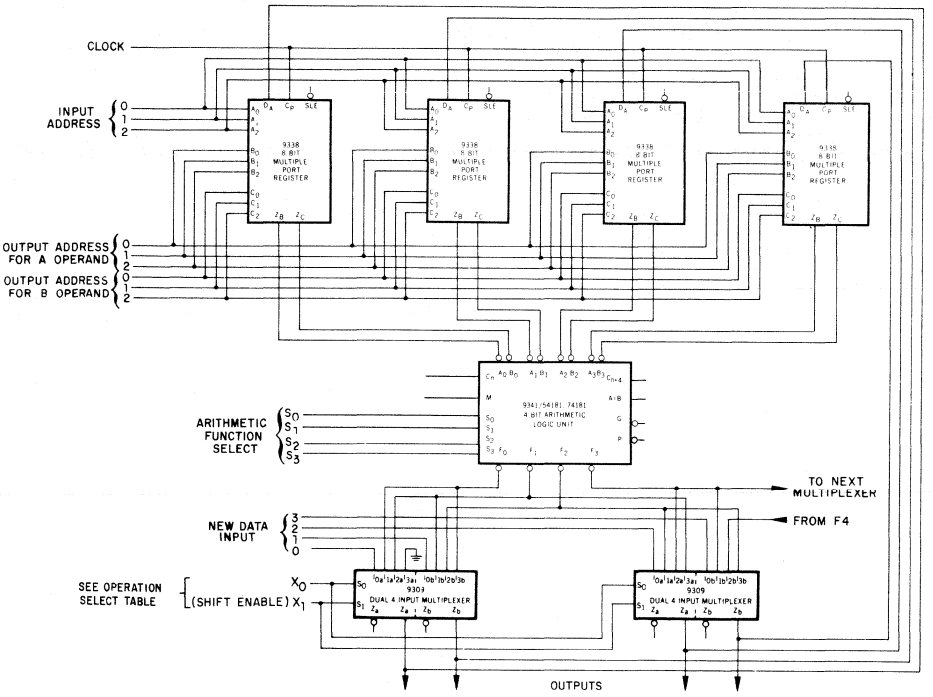
PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND	
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	Any $\overline{F}$
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	Any $\overline{F}$
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$, C_n	Remaining $\overline{A}$	$\overline{F}_{i+1}$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{B}$, C_n	Remaining $\overline{A}$	$\overline{F}_{i+1}$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{A}$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B
t_{PLH} t_{PHL}	$\overline{A}$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$ and $\overline{B}$	None	C_{n+4}

LOGIC MODE TEST TABLE III

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	FUNCTION INPUTS
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	Any $\overline{F}$	$S_1 = S_3 = M = 4.5$ V $S_0 = S_2 = 4.5$ V
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	Any $\overline{F}$	$S_1 = S_3 = M = 4.5$ V $S_0 = S_2 = 0$ V

APPLICATIONS

SECTION OF 3 ADDRESS ARITHMETIC LOGIC UNIT WITH 8 REGISTERS



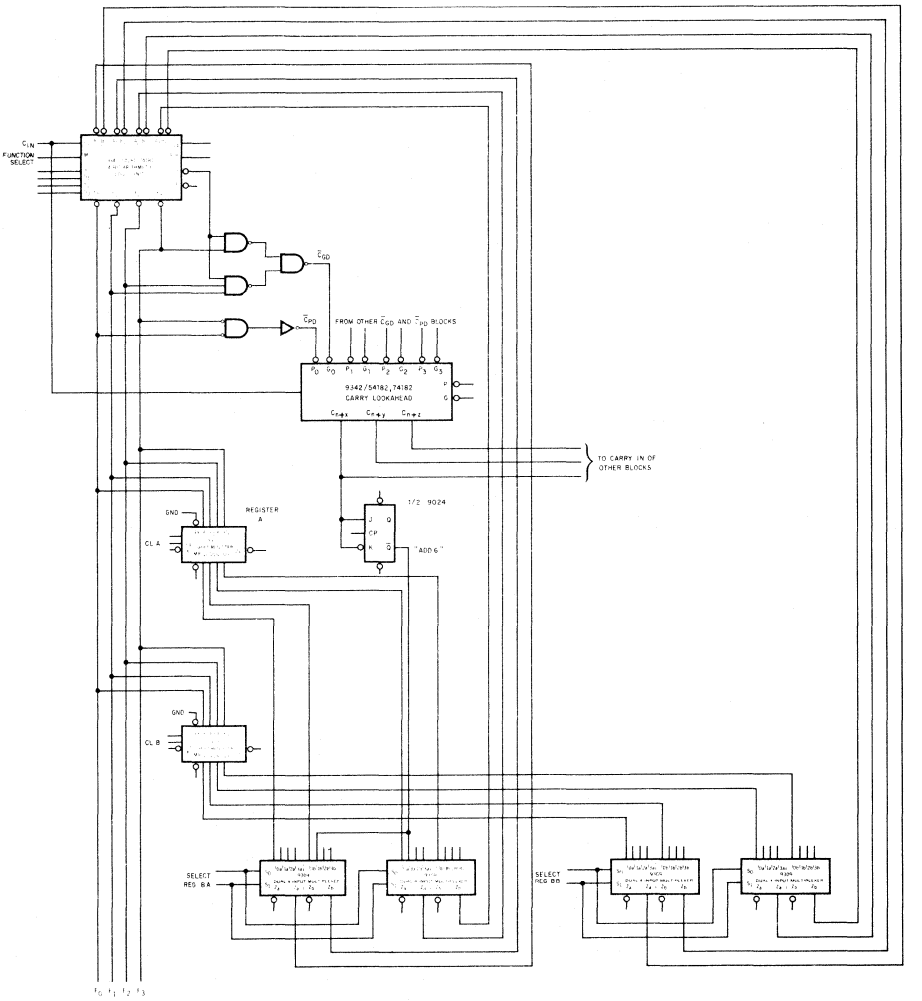
X_0	X_1	OPERATION
L	L	LOAD NEW DATA
H	L	NO SHIFT
L	H	SHIFT LEFT
H	H	SHIFT RIGHT

This figure indicates a section of three address arithmetic unit with eight registers. It uses a TTμL/MSI 9341/54181, 74181 ALU, and four 9338 8-bit multiple port registers, and two 9309 multiplexers to give shifting capability.

Fig. 11

APPLICATIONS (Cont'd)

TWO CYCLE BCD ARITHMETIC LOGIC UNIT

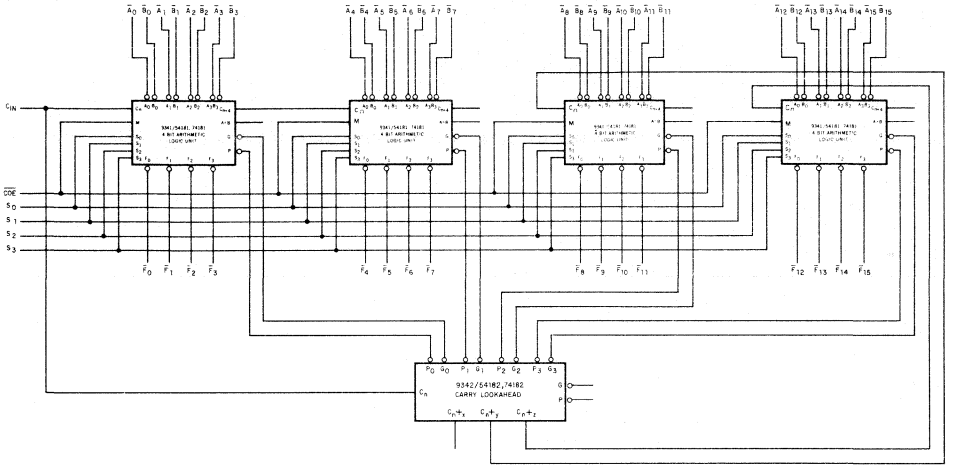


This figure illustrates a two cycle BCD Arithmetic Logic Unit using the 9341/54181, 74181 ALU and the 9342/54182, 74182 Look-ahead Carry Generator with several TTμL/MSI shift registers and multiplexers.

Fig. 12

APPLICATIONS (Cont'd)

16-BIT FULL LOOK-AHEAD CARRY ARITHMETIC LOGIC UNIT



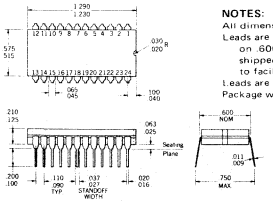
This figure illustrates use of the 9341/54181, 74181 ALU and the 9342/54182, 74182 Look-ahead Carry Generator

Fig. 13

ORDER INFORMATION – Specify UXX934159X or UXX74181 for the 0°C to +75°C temperature range, or UXX934151X or UXX54181 for the −55°C to +125°C temperature range, where XX is 6N for the 24 pin Dual In-Line package or 4M for the 24 pin Flat package.

PACKAGE INFORMATION

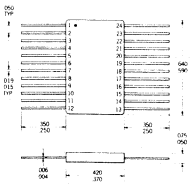
6N–24 LEAD DUAL IN-LINE PACKAGE



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .600" centers. They are purposely shipped with "positive" misalignment to facilitate insertion
Leads are tin plated kovar
Package weight is 6.5 grams

Fig. 14

4M–24 LEAD (BeO) FLATPAK



NOTES:
All dimensions in inches
Leads are gold plated kovar
Package weight is 0.8 gram

Fig. 15

TTμL/MSI 9342/54182, 74182
LOOK-AHEAD CARRY GENERATOR
A FAIRCHILD TTμL® IC PRODUCT

GENERAL DESCRIPTION – The TTμL/MSI 9342/54182, 74182 is a high speed Look-Ahead Carry Generator. It is generally used with the 9341/54181, 74181 4-Bit Arithmetic Logic Unit to provide high speed look-ahead over word lengths of more than four-bits. The Look-Ahead Carry Generator is fully compatible with all members of the Fairchild TTμL Family.

FEATURES

- **PROVIDES LOOK-AHEAD CARRIES ACROSS A GROUP OF FOUR ALU'S**
- **MULTI-LEVEL LOOK-AHEAD FOR HIGH SPEED ARITHMETIC OPERATION OVER LONG WORD LENGTHS**
- **INPUT CLAMP DIODES**
- **TTμL COMPATIBLE**

PIN NAMES

C_N	Carry Input
$\overline{G}_0, \overline{G}_1, \overline{G}_2, \overline{G}_3$	Carry Generate (Active Low) Inputs
$\overline{P}_0, \overline{P}_1, \overline{P}_2, \overline{P}_3$	Carry Propagate (Active Low) Inputs
$C_{n+x}, C_{n+y}, C_{n+z}$	Carry Outputs
$\overline{G}$	Carry Generate (Active Low) Output
$\overline{P}$	Carry Propagate (Active Low) Output

ORDER INFORMATION – Specify UXX934259X or UXX74182 for the 0°C to +75°C temperature range, or UXX934251X or UXX54182 for the -55°C to +125°C temperature range, where XX is 6B for the 16 pin Dual In-Line package or 4L for the 16 pin Flat package.

LOGIC DIAGRAM

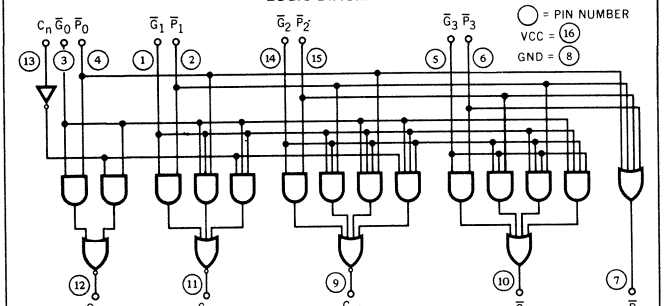


Fig. 4

LOGIC SYMBOL

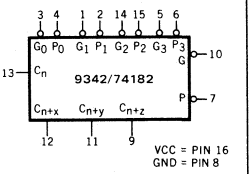


Fig. 1

CONNECTION DIAGRAM DIP (TOP VIEW)

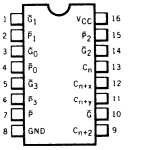


Fig. 2

FLATPAK (TOP VIEW)

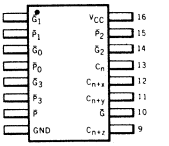


Fig. 3

FAIRCHILD SEMICONDUCTOR

FUNCTIONAL DESCRIPTION – The TTμL/MSI 9342/54182, 74182 Look-Ahead Carry Generator accepts up to four pairs of active low carry propagate ($\overline{P}_0$, $\overline{P}_1$, $\overline{P}_2$, $\overline{P}_3$) and carry generate ($\overline{G}_0$, $\overline{G}_1$, $\overline{G}_2$, $\overline{G}_3$) signals and an active High carry input (C_n) and provides anticipated active high carries (C_{n+x}, C_{n+y}, C_{n+z}) across four groups of binary adders. The 9342/54182, 74182 also has active low carry propagate ($\overline{P}$) and carry generate ($\overline{G}$) outputs which may be used for further levels of look-ahead.

The logic equations provided at the outputs are:

$$C_{n+x} = G_0 + P_0C_n$$

$$C_{n+y} = G_1 + P_1G_0 + P_1P_0C_n$$

$$C_{n+z} = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_n$$

$$G = G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0$$

$$P = P_3P_2P_1P_0$$

Also the Look-Ahead Carry Generator can be used with binary ALU's in an active Low or active High input operand mode. The connections to and from the ALU to the Look-Ahead Carry Generator are identical in both cases.

TRUTH TABLE

INPUTS								OUTPUTS				
C_n	$\overline{G}_0$	$\overline{P}_0$	$\overline{G}_1$	$\overline{P}_1$	$\overline{G}_2$	$\overline{P}_2$	$\overline{G}_3$	$\overline{P}_3$	C_{n+x}	C_{n+y}	C_{n+z}	G P
X	H	H							L			
L	H	X							L			
X	L	X							H			
H	X	L							H			
X	X	X	H	H						L		
X	H	H	H	X						L		
L	H	X	H	X						L		
X	X	X	L	X						H		
X	L	X	X	L						H		
H	X	L	X	L						H		
X	X	X	X	X	H	H					L	
X	X	X	H	H	H	X					L	
X	H	H	H	X	H	X					L	
L	H	X	H	X	H	X					L	
X	X	X	X	X	L	X					H	
X	X	X	X	L	X	L					H	
X	L	X	L	X	L	L					H	
H	X	L	X	L	X	L					H	
X	X	X	X	X	H	H	H					H
X	X	X	H	H	H	X	H					H
X	H	H	H	X	H	X	H					H
X	H	X	H	X	H	X	H					H
X	X	X	X	X	L	X	L					L
X	X	X	X	L	X	X	L					L
X	L	X	X	L	X	L	L					L
L	X	L	X	L	X	L	L					L
*	H	X	X	X	X							H
	X	H	X	X	X							H
	X	X	H	X	X							H
	X	X	X	H	X							H
	L	L	L	L	L							L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

TTμL LOADING RULES

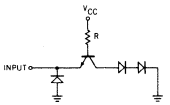
INPUTS	LOADING
C_n	1 U.L.
$\overline{P}_3$	2 U.L.
$\overline{P}_2$	3 U.L.
$\overline{P}_0$, $\overline{P}_1$, $\overline{G}_3$	4 U.L.
$\overline{G}_0$, $\overline{G}_2$	7 U.L.
$\overline{G}_1$	8 U.L.

OUTPUTS	DRIVE FACTOR	
	HIGH	LOW
$\overline{P}$, $\overline{G}$	20 U.L.	10 U.L.
C_{n+x}, C_{n+y}, C_{n+z}	20 U.L.	10 U.L.

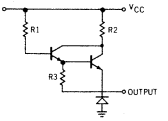
1 Unit Load (U.L.) = 40 μA High/1.6 mA Low

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

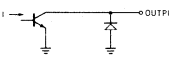
EQUIVALENT INPUT CIRCUIT



OUTPUT HIGH EQUIVALENT CIRCUIT

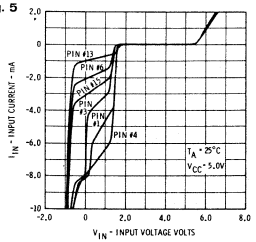


OUTPUT LOW EQUIVALENT CIRCUIT



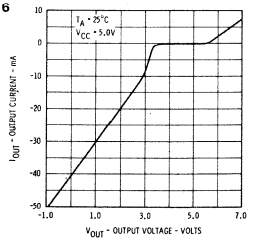
INPUT CURRENT VERSUS INPUT VOLTAGE

Fig. 5



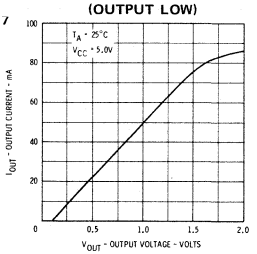
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)

Fig. 6



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)

Fig. 7



ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (D.C.)	−0.5 V to +5.5 V
*Input Current (D.C.)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output High)	0.5 V to +V_{CC} value
Output Current (D.C.) (Output Low)	+30 mA

*Entire Input Voltage Limit or Input Current is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
U6B/U4L 934251X or 54182	4.5 V	5.0 V	5.5 V	−55°C to 125°C
U6B/U4L 934259X or 74182	4.75 V	5.0 V	5.25 V	0°C to 75°C

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	CHARACTERISTIC	LIMITS		UNITS	CONDITIONS
		MIN.	MAX.		
V_{OH}	Output HIGH Voltage	2.4		Volts	V_{CC} = MIN., I_{OH} = −800 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{IH}	Input HIGH Level	2.0		Volts	Guaranteed input logical HIGH voltage for all inputs
V_{IL}	Input LOW Level		0.8	Volts	Guaranteed input logical LOW voltage for all inputs
I_{IL}	Input LOW Current $\overline{C_n}$ $\overline{P_3}$ $\overline{P_2}$ $\overline{P_0}$, $\overline{P_1}$ or $\overline{G_3}$ $\overline{G_0}$ or $\overline{G_2}$ $\overline{G_1}$		 −1.6 −3.2 −4.8 −6.4 −11.2 −12.8	mA	V_{CC} = MAX., V_{IN} = 0.4 V
I_{IH}	Input HIGH Current $\overline{C_n}$ $\overline{P_3}$ $\overline{P_2}$ $\overline{P_0}$, $\overline{P_1}$ or $\overline{G_3}$ $\overline{G_0}$ or $\overline{G_2}$ $\overline{G_1}$		 40 80 120 160 280 320	μA	V_{CC} = MAX., V_{IN} = 2.4 V
	Input HIGH Current all inputs		1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{SC}	Output Short Circuit Current	−40	−100	mA	V_{CC} = MAX., V_{OUT} = 0.0 V
I_{CC1}	Power Supply Current 934251X or 54182 934259X or 74182		 35 39	 mA mA	V_{CC} = MAX.
I_{CC2}	Power Supply Current 934251X or 54182 934259X or 74182		 65 72	 mA mA	V_{CC} = MAX.

NOTES:

(1) The actual Testing Procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this Specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California (see page 1 for address and phone).

(2) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.

(3) The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

SWITCHING CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0V, Pin 8 = Gnd)

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		MIN.	TYP.	MAX.		
t_{PLH} t_{PHL}	(C_n to C_{n+x}, C_{n+y}, C_{n+z})		12 15	16 19	ns	$\overline{P}_0 = \overline{P}_1 = \overline{P}_2$ = Gnd, $\overline{G}_0 = \overline{G}_1 = \overline{G}_2$ = 4.5V See Fig. 8 & 10
t_{PLH} t_{PHL}	($\overline{P}_0$, $\overline{P}_1$, or $\overline{P}_2$ to C_{n+x}, C_{n+y}, or C_{n+z})		8 9	10 11	ns	$\overline{P}_x$ = Gnd (If not under test), $C_n = \overline{G}_0 = \overline{G}_1 = \overline{G}_2$ = 4.5V, Fig. 9 & 10
t_{PLH} t_{PHL}	(G_0, G_1 or G_2 to C_{n+x}, C_{n+y}, or C_{n+z})		8 9	10 11	ns	$\overline{G}_x$ = 4.5V (If not under test), $C_n = \overline{P}_0 = \overline{P}_1 = \overline{P}_2$ = Gnd, Fig. 9 & 10
t_{PLH} t_{PHL}	($\overline{P}_1$, $\overline{P}_2$ or $\overline{P}_3$ to $\overline{G}$ or $\overline{P}$)		12 15	16 19	ns	$\overline{P}_x$ = Gnd (If not under test), $\overline{G}_0 = \overline{G}_1 = \overline{G}_2 = \overline{G}_3$ = 9.5V, Fig. 8 & 10
t_{PLH} t_{PHL}	($\overline{G}_0$, $\overline{G}_1$, $\overline{G}_2$ or $\overline{G}_3$ to $\overline{G}$)		12 15	16 19	ns	$\overline{G}_x$ = 4.5V (If not under test), $\overline{P}_1 = \overline{P}_2 = \overline{P}_3$ = Gnd, Fig. 8 & 10
t_{PLH} t_{PHL}	($\overline{P}_0$, $\overline{P}_1$, $\overline{P}_2$ or $\overline{P}_3$ to $\overline{P}$)		12 15	16 19	ns	$\overline{P}_x$ = Gnd (If not under test), Fig. 8 & 10

SWITCHING TIME WAVEFORMS

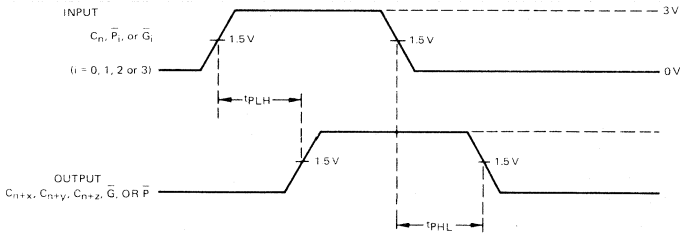


Fig. 8

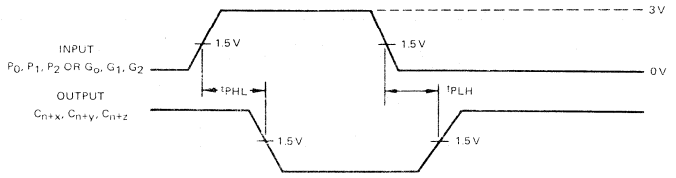


Fig. 9

SWITCHING TIME TEST CIRCUIT

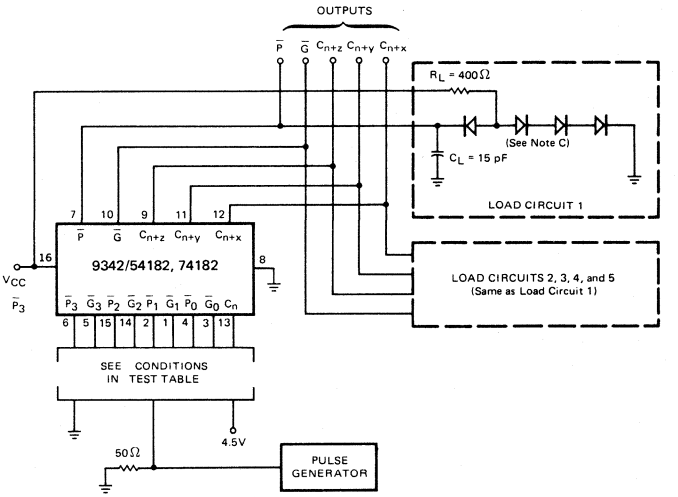


Fig. 10

APPLICATIONS

9341/74181, 54181 ALU

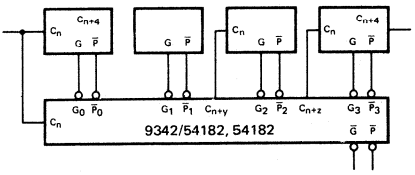


Fig. 11 16 bit ALU with full carry look-ahead

APPLICATIONS (cont'd)

9341/74181, 54181 ALU

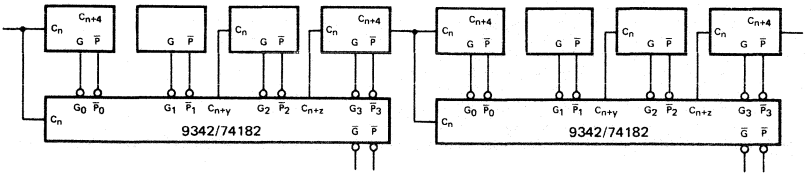
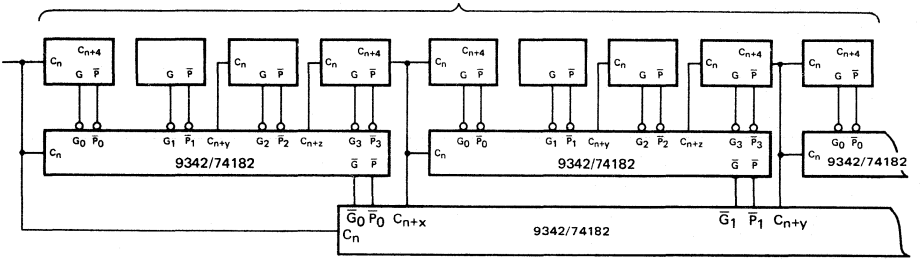


Fig. 12 32 bit ALU with ripple carry between 16 bit look-ahead ALUs

9341/74181, 54181 ALU



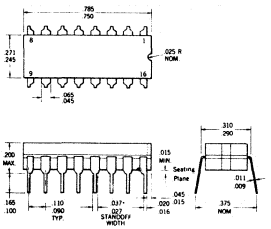
Note: $\overline{A}$ and $\overline{B}$ inputs and $\overline{F}$ outputs for the 9341/74181 are not shown.

In the 16-bit look-ahead blocks the C_n (Carry In Signal) for the second 9341/74181 can be obtained from either the C_{n+y} output of the first 9341/74181 or the C_{n+x} output of the 9342/74182.

Fig. 13 64 bit ALU full carry look-ahead

PACKAGE INFORMATION

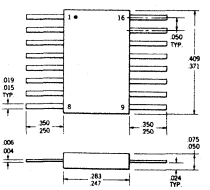
6B – 16 LEAD DUAL IN-LINE PACKAGE



NOTES:
All dimensions are in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Broad-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.2 grams
*The .027/.037 dimension does not apply to the corner leads

Fig. 14

4L – 16 LEAD (BeO) FLATPAK



NOTES:
All dimensions in inches
Leads are gold plated kovar
Package weight is 0.4 gram

Fig. 15

TTμL/MSI 9348

12-INPUT PARITY CHECKER/GENERATOR

A FAIRCHILD TTμL® IC PRODUCT

GENERAL DESCRIPTION – The TTμL/MSI 9348 is a 12-input parity checker/generator generating odd and even parity outputs. It can be used in high speed error detection applications. The 9348 uses TTμL technology for high capacitive drive capability, and provides low impedance in both logic states for good A.C. noise immunity. All inputs feature diode clamping to reduce negative line transients. This device is compatible with all members of the TTμL family of digital integrated circuits.

FEATURES

- **BOTH ODD AND EVEN PARITY OUTPUTS PROVIDED**
- **GENERATES A PARITY BIT FOR UP TO 12 BITS**
- **CHECKS FOR PARITY ON UP TO 12 BITS**
- **EASILY EXPANDABLE**
- **HIGH DRIVE OUTPUT CIRCUITRY**
- **INPUT CLAMP DIODE LIMITS HIGH SPEED TERMINATION EFFECTS**
- **TTμL COMPATIBLE**

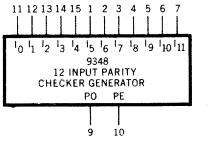
ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to + 150°C
Temperature (Ambient) Under Bias	−55°C to + 125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to + 7.0 V
Voltage applied to output when output is high	−0.5 V to + V_{CC} Value
Input Voltage (DC) (See Note 1)	−0.5 V to + 5.5 V
Input Current (DC) (See Note 1)	−30 mA to + 5 mA
Current into output when output is low	+ 30 mA

Note 1: Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

ORDER INFORMATION – Specify U7B9348XXX for 16-pin Dual In-Line Package or U4L9348XXX for 16-pin Flatpak, where XXX is 51X for the −55°C to + 125°C temperature range, or 59X for the 0°C to + 75°C temperature range.

LOGIC SYMBOL



V_{CC} = Pin 16
Gnd = Pin 8

Fig. 1

CONNECTION DIAGRAM
DIP (TOP VIEW)

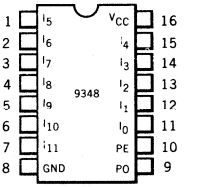


Fig. 2

FLATPAK (TOP VIEW)

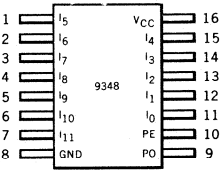
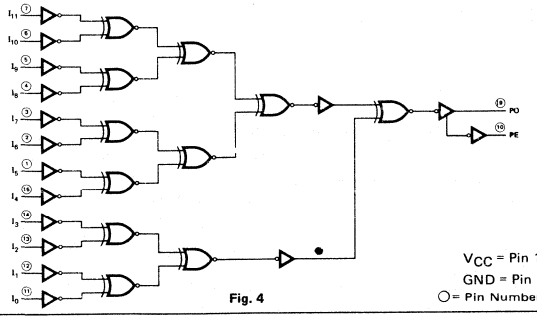


Fig. 3

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

Fig. 4

FAIRCHILD SEMICONDUCTOR

FUNCTIONAL DESCRIPTION – The MSI 9348 is a 12-input Parity Generator. It provides odd and even parity for up to 12 data bits. The even parity output (PE) will be high if an even number of logic ones are present on the inputs. The odd parity output (PO) will be high if an odd number of logic ones are present on the inputs. The logic equations for the outputs are shown below.

$$PO = I_0 \oplus I_1 \oplus I_2 \oplus I_3 \oplus I_4 \oplus I_5 \oplus I_6 \oplus I_7 \oplus I_8 \oplus I_9 \oplus I_{10} \oplus I_{11}$$

$$PE = \overline{I_0 \oplus I_1 \oplus I_2 \oplus I_3 \oplus I_4 \oplus I_5 \oplus I_6 \oplus I_7 \oplus I_8 \oplus I_9 \oplus I_{10} \oplus I_{11}}$$

NOTE: Less through delay is encountered from the I_0, I_1, I_2, and I_3 inputs than I_4 thru I_{11} inputs. Therefore, if some signals are slower than others, the slower signals should be applied to these four inputs for maximum speed.

TRUTH TABLE

INPUTS		OUTPUTS	
$I_0, I_1, I_2, I_3, I_4, I_5, I_6, I_7, I_8, I_9, I_{10}, I_{11}$		P_O	P_E
All Twelve	Inputs Low	0	1
Any One	Input High	1	0
Any Two	Inputs High	0	1
Any Three	Inputs High	1	0
Any Four	Inputs High	0	1
Any Five	Inputs High	1	0
Any Six	Inputs High	0	1
Any Seven	Inputs High	1	0
Any Eight	Inputs High	0	1
Any Nine	Inputs High	1	0
Any Ten	Inputs High	0	1
Any Eleven	Inputs High	1	0
All Twelve	Inputs High	0	1

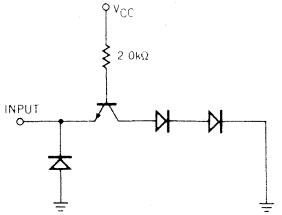
TTμL LOADING RULES

INPUTS	LOADING	
All Inputs	2 U.L.	
OUTPUTS	DRIVING FACTOR	
	HIGH	LOW
All Outputs	20 U.L.	10 U.L.

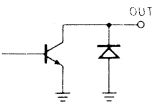
1 Unit Load (U.L.) = 60 μA High / 1.6 mA low

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

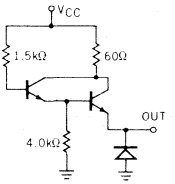
INPUT EQUIVALENT CIRCUIT



OUTPUT EQUIVALENT CIRCUIT (Output Low)



OUTPUT EQUIVALENT CIRCUIT (Output High)



INPUT CURRENT VERSUS INPUT VOLTAGE

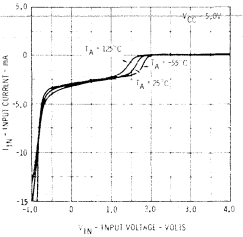


Fig. 5

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)

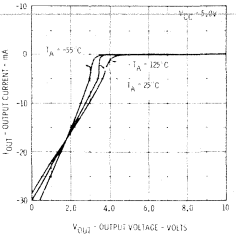


Fig. 6

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)

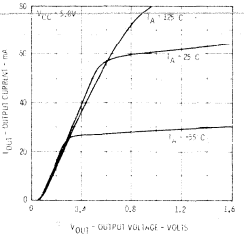


Fig. 7

ELECTRICAL CHARACTERISTICS (T_A = -55°C to + 125°C, V_{CC} = 5.0 V ± 10%) (Part #U7B/4L934851X) Units are pulse tested

SYMBOL	CHARACTERISTIC	LIMITS -55°C MIN.	LIMITS -55°C MAX.	LIMITS + 25°C MIN.	LIMITS + 25°C TYP.	LIMITS + 25°C MAX.	LIMITS + 125°C MIN.	LIMITS + 125°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	V_{CC} = 4.5 V, I_{OH} = -1.2 mA
V_{OL}	Output Low Voltage		0.4		0.2	0.4		0.4	Volts	V_{CC} = 4.5 V, I_{OL} = 12.4 mA V_{CC} = 5.5 V, I_{OL} = 16.0 mA
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current	-2.48			-1.65	-2.48		-2.48	mA	V_{CC} = 4.5 V, V_F = 0.4 V
		-3.2			-2.15	-3.2		-3.2	mA	V_{CC} = 5.5 V, V_F = 0.4 V
I_R	Input Leakage Current				13	90		90	μA	V_{CC} = 5.5 V, V_R = 4.5 V
I_{PD}	V_{CC} Current		75		47	75		75	mA	V_{CC} = 5.0 V Pins 4, 11 & 15 = GND

ELECTRICAL CHARACTERISTICS (T_A = 0°C to + 75°C, V_{CC} = 5.0 V ± 5%) (Part #U7B/4L934859X) Units are pulse tested

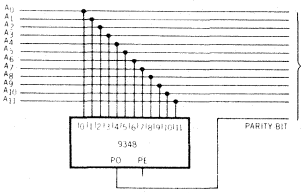
SYMBOL	CHARACTERISTIC	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS + 25°C MIN.	LIMITS + 25°C TYP.	LIMITS + 25°C MAX.	LIMITS + 75°C MIN.	LIMITS + 75°C MAX	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	V_{CC} = 4.75 V, I_{OH} = -1.2 mA
V_{OL}	Output Low Voltage		0.45		0.2	0.45		0.45	Volts	V_{CC} = 4.75 V, I_{OL} = 14.1 mA V_{CC} = 5.25 V, I_{OL} = 16.0 mA
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current	-2.82			-1.75	-2.82		-2.82	mA	V_{CC} = 4.75 V, V_F = 0.45 V
		-3.2			-2.0	-3.2		-3.2	mA	V_{CC} = 5.25 V, V_F = 0.45 V
I_R	Input Leakage Current				13	120		120	μA	V_{CC} = 5.25 V, V_R = 4.5 V
I_{PD}	V_{CC} Current		80		47	80		80	mA	V_{CC} = 5.0 V Pins 4, 11 & 15 = GND

9348 SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	CHARACTERISTIC	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	CONDITIONS
t_{pd+} (I_4 to PO) Pin 15 to Pin 9	Switching Speed		40		ns	V_{CC} = 5.0 V, C_L = 15 pF PINS 3, 4, 13 & 14 = GND OTHERS HIGH
t_{pd-} (I_4 to PO) Pin 15 to Pin 9	Switching Speed		36		ns	
t_{pd+} (I_4 to PE) Pin 15 to Pin 10	Switching Speed		47		ns	V_{CC} = 5.0 V, C_L = 15 pF PINS 3, 4, 13 & 14 = GND OTHERS HIGH
t_{pd-} (I_4 to PE) Pin 15 to Pin 10	Switching Speed		41		ns	
t_{pd+} (I_3 to PO) Pin 14 to Pin 9	Switching Speed		20		ns	V_{CC} = 5.0 V, C_L = 15 pF PINS 1, 2, 4, 5, 6, 7, 11, 12, 13, & 15 = GND OTHERS HIGH
t_{pd-} (I_4 to PO) Pin 15 to Pin 9	Switching Speed		19		ns	V_{CC} = 5.0 V, C_L = 15 pF PINS 1, 2, 3, 4, 5, 6, 7, 11, 12, 13, 14 = GND

APPLICATIONS

PARITY GENERATION



PARITY CHECKING

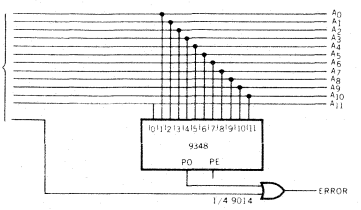


Fig. 8 – 12 BIT PARITY GENERATION/CHECKING SCHEME

Odd parity as shown. For even parity scheme PE rather than PO should be used from both 9348s.

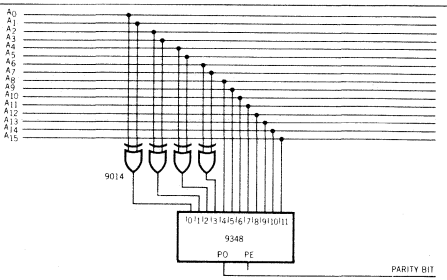


Fig. 9 – 16 BIT PARITY GENERATOR

The 9348 may easily be expanded to 16 inputs with little sacrifice in speed by adding a 9014 quad exclusive OR gate. The through delay from I_0, I_1, I_2 and I_3 is less than from the other inputs, so it is important to connect the exclusive OR gates to these inputs for maximum speed. For over 16 inputs, an additional 9348 should be used.

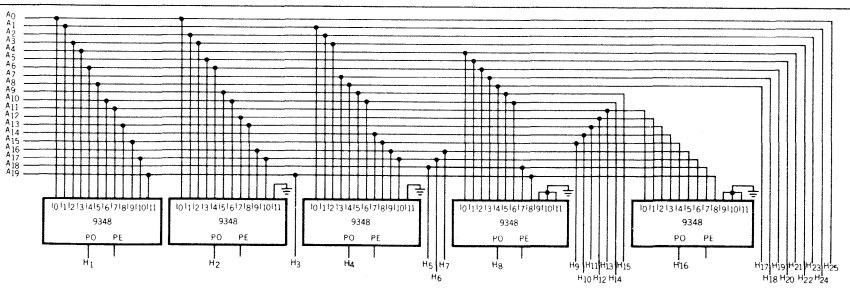


Fig. 10 – SINGLE ERROR CORRECTION HAMMING CODE GENERATION FOR 20 BITS

PACKAGE INFORMATION

7B – 16 LEAD DUAL IN-LINE PACKAGE

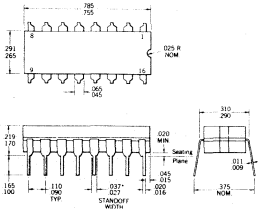


Fig. 11

NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.2 grams
* The .027/.037 dimension does not apply to the corner leads

4L – 16 LEAD (BeO) FLATPAK

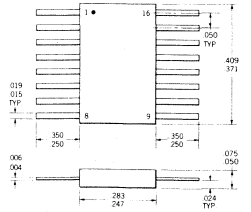


Fig. 12

NOTES:
All dimensions in inches
Leads are gold-plated kovar
Package weight is 0.4 gram

TTμL/MSI 9350
DECADE COUNTER
A FAIRCHILD TTμL® IC PRODUCT

GENERAL DESCRIPTION — The TTμL/MSI 9350 is a monolithic decade counter. This multifunctional MSI building block is capable of being used as a divide-by-two, divide-by-five counter or as a divide-by-ten counter. It is useful in a large number of counting applications in digital computer systems, data handling systems and control systems.

FEATURES

- **FUNCTIONALLY EQUIVALENT TO THE 7490**
- **STANDARD CORNER POWER PINS FOR EASY USE**
- **HIGH SPEED, 18 MHz TYPICAL**
- **TYPICAL POWER DISSIPATION OF 160 mW**
- **TTμL COMPATIBLE**
- **ALL CERAMIC, HERMETIC 14 PIN DUAL IN-LINE PACKAGE**
- **INPUT DIODE CLAMPING**

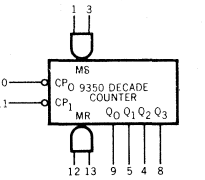
ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	0°C to +75°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
Voltage Applied to Outputs in High Output State	−0.5 V to +V_{CC} Value
Input Voltage (DC)	−0.5 V to +5.5 V

ORDER INFORMATION

Specify U7A935059X for 14 pin Dual In-Line package and 0°C to +75°C temperature range.

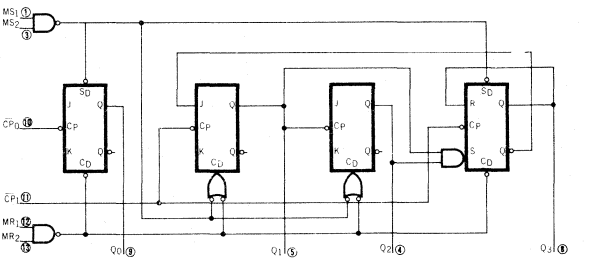
LOGIC SYMBOL



V_{CC} = Pin 14
GND = Pin 7
N.C. = Pins 2,6

Fig. 1

LOGIC DIAGRAM



V_{CC} = Pin 14
GND = Pin 7

Fig. 2

FAIRCHILD
SEMICONDUCTOR

FUNCTIONAL DESCRIPTION

The 9350 is an up decade counter. It consists of four dual-rank, master-slave flip-flops internally interconnected to provide a divide-by-two counter and a divide-by-five counter. A gated "AND" Master Reset is provided to inhibit counting and return all outputs to a LOW state. A gated "AND" Master Set is provided which will set the counter to a binary coded decimal count of nine (9), overriding all other count or Reset conditions. Since the output from the first flip-flop is not internally connected to the succeeding stages, the device may be operated in three independent count modes:

A. BCD Decade Counter — The $\overline{CP}_1$ input must be externally connected to the Q_0 output. The $\overline{CP}_0$ input receives the incoming count and a BCD count sequence is produced.

B. Symmetrical Divide-By-Ten Counter — The Q_3 output must be externally connected to the $\overline{CP}_0$ input. The input count is then applied to the $\overline{CP}_1$ input and a divide-by-ten square wave is obtained at output Q_0.

C. Divide-By-Two & Divide-By-Five Counter — No external interconnections are required. The first flip-flop is used as a binary element for the divide-by-two function. (CP_0 as the input and Q_0 as the output). The $\overline{CP}_1$ input is used to obtain binary divide by five operation at the Q_1, Q_2, and Q_3 outputs.

NOTE: The 9350 flip-flops change state after the high to low transition of the clock.

PIN FUNCTIONS

$\overline{CP}_0$	Clock First Stage Negative Edge Input
$\overline{CP}_1$	Clock Second, Third, and Fourth Stage Negative Edge Input
MR	"AND" Master Reset to Binary Zero (Asynchronous) Input
MS	"AND" Master Set to Binary Nine (Asynchronous) Input
Q_0, Q_1, Q_2, Q_3	Counter Outputs
N.C.	No Internal Connection

LOADING RULES

	PIN	LOADING
INPUTS	$\overline{CP}_0$	2 U.L.
	$\overline{CP}_1$	4 U.L.
	MR	1 U.L.
	MS	1 U.L.
OUTPUTS	All Outputs	10 U.L.

(1 U.L. = TTμL Gate Input Load)

MODE SELECTION

RESET/SET INPUTS				OUTPUTS			
MR_1	MR_2	MS_1	MS_2	Q_0	Q_1	Q_2	Q_3
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
L	X	L	X	COUNT			
X	L	X	L	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

H = High Voltage Level
L = Low Voltage Level
X = Don't Care Condition

BCD COUNT SEQUENCE

COUNT	OUTPUT			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

Note: Output Q_0 is connected to Input $\overline{CP}_1$ for BCD count.

ELECTRICAL CHARACTERISTICS (T_A = 0°C to +75°C, V_{CC} = 5.0 V ±5%) (Part # U7A935059X)

SYMBOL	CHARACTERISTIC	LIMITS 0°C MIN.	0°C MAX.	+25°C MIN.	+25°C TYP.	+25°C MAX.	+75°C MIN.	+75°C MAX.	UNITS	CONDITIONS & COMMENTS
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	V_{CC} = 4.75 V, I_{OH} = −600 μA
V_{OL}	Output Low Voltage		0.45		0.2	0.45		0.45	Volts	V_{CC} = 4.75 V, I_{OL} = 16 mA
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed Input High Threshold For All Inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed Input Low Threshold For All Inputs
I_F	Input Load Current MS, MR		−1.6		−1.0	−1.6		−1.6	mA	V_{CC} = 5.25 V, V_F = 0.45 V
2 I_F	Input Load Current CP_0		−3.2		−2.0	−3.2		−3.2	mA	
4 I_F	Input Load Current CP_1		−6.4		−4.0	−6.4		−6.4	mA	
I_R	Input Leakage Current MS, MR		60		10	60		60	μA	V_{CC} = 5.25 V, V_R = 4.5 V
2 I_R	Input Leakage Current CP_0		120		20	120		120	μA	
4 I_R	Input Leakage Current CP_1		240		40	240		240	μA	
I_{PD}	Power Supply Current				30	50			mA	V_{CC} = 5.0 V

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS & COMMENTS
t_{pd+}	Turn-Off Delay CP_0 to Output Q_2		60	100	ns	V_{CC} = 5.0 V, C_L = 15 pF, Q_0 Output Connected To $\overline{CP}_1$ Input
t_{pd-}	Turn-On Delay CP_0 to Output Q_2		60	100	ns	
f_{max}	Maximum Frequency of Input Count Pulses	10	18		MHz	

SWITCHING TIME WAVEFORMS

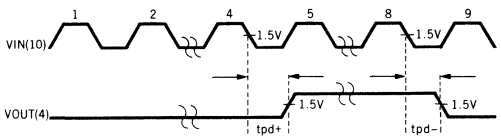


Fig. 3

APPLICATIONS

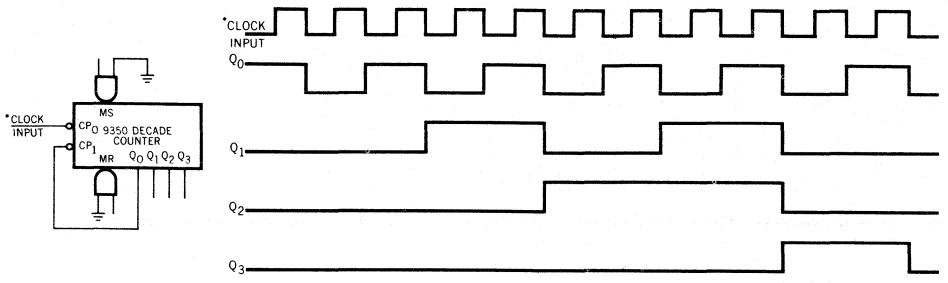


Fig. 4. WAVEFORMS OF A SINGLE DECADE COUNTER

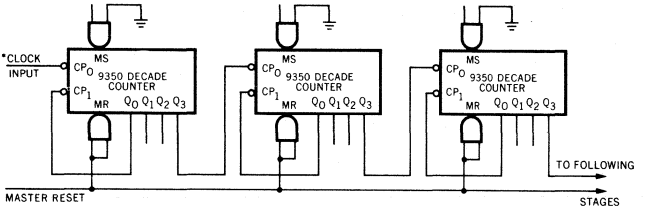


Fig. 5. MULTISTAGE DECADE COUNTING SCHEME

The interconnections required for a multistage ripple decade counter are shown above.

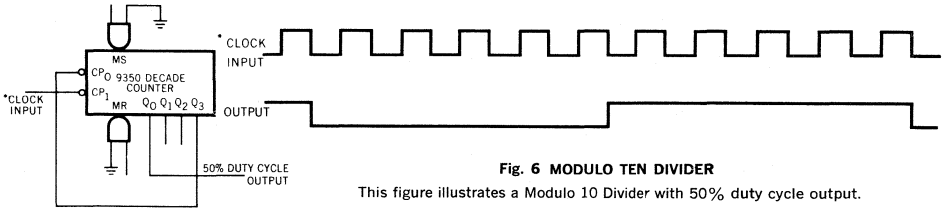


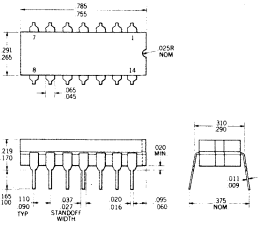
Fig. 6 MODULO TEN DIVIDER

This figure illustrates a Modulo 10 Divider with 50% duty cycle output.

*Note: The 9350 Decade Counter Flip Flops change state on the HIGH TO LOW transition of the clock.

PACKAGE INFORMATION

7A - 14 LEAD MSI DUAL IN-LINE PACKAGE



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020" diameter lead
Leads are tin plated kovar
Package weight is 2.2 grams

TTμL/MSI 9356
4-BIT BINARY COUNTER
A FAIRCHILD TTμL® IC PRODUCT

GENERAL DESCRIPTION — The TTμL/MSI 9356 is a monolithic 4-bit binary counter. This device is capable of being used as a divided-by-two, divided-by-eight, or a divided-by-sixteen counter. It is useful in a large number of counting applications in digital computer systems, data handling systems and control systems.

FEATURES
- **FUNCTIONALLY EQUIVALENT TO THE 7493**
- **STANDARD CORNER POWER PINS FOR EASY USE**
- **HIGH SPEED, 18 MHz TYPICAL**
- **TYPICAL POWER DISSIPATION OF 160 mW**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **TTμL COMPATIBLE**
- **ALL CERAMIC, HERMETIC 14 PIN DUAL IN-LINE PACKAGE.**

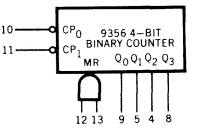
ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} Value
Input Voltage (DC)	−0.5 V to +5.5 V

ORDER INFORMATION

Specify U7A935659X for 14 pin Dual In-Line package and 0°C to +75°C temperature range.

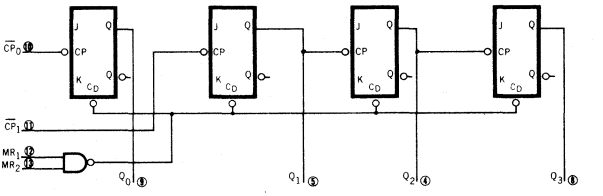
LOGIC SYMBOL



V_{CC} = Pin 14
GND = Pin 7
N.C. = Pins 1,2,3,6

Fig. 1

LOGIC DIAGRAM



V_{CC} = Pin 14
GND = Pin 7

Fig. 2

FAIRCHILD SEMICONDUCTOR

FUNCTIONAL DESCRIPTION

The MSI 9356 is an 4-bit up binary counter. It consists of four master-slave flip-flops which are internally interconnected to provide a divide-by-two counter and a divide-by-eight counter. A gated "AND" master reset is provided to inhibit the counting and return all outputs to a low state.* Since the output from the first flip-flop is not internally connected to the succeeding flip-flops, the device may be operated in two independent modes:

A. Four-Bit Ripple-Counter — The output Q_0 must be externally connected to input $\overline{CP}_1$. The input count pulses are applied to input $\overline{CP}_0$. Simultaneous divisions of 2, 4, 8, and 16 are performed at the Q_0, Q_1, Q_2, and Q_3 outputs as shown in the truth table.

B. Three-Bit Ripple-Counter — The input count pulses are applied to input $\overline{CP}_1$. Simultaneous frequency divisions of 2, 4, and 8 are available at the Q_1, Q_2, and Q_3 outputs. Independent use of the first flip-flop is available if the reset function coincides with reset of the 3-bit ripple-through counter.

*(i.e., When both inputs of the "AND" master reset are high outputs Q_{0-3} will be forced low, resetting the flip-flops, regardless of all other input conditions.)

NOTE: The 9356 flip-flops change state after the high to low transition of the clock.

PIN FUNCTIONS

$\overline{CP}_0$	Clock First Stage Negative Edge Input
$\overline{CP}_1$	Clock Second, Third, and Fourth Stage Negative Edge Input
MR	"AND" Master Reset to Binary Zero (Asynchronous) Input
Q_0, Q_1, Q_2, Q_3	Counter Outputs
N.C.	No Internal Connection

LOADING RULES

	PIN	LOADING
INPUTS	$\overline{CP}_0$	2 U.L.
	$\overline{CP}_1$	2 U.L.
	MR	1 U.L.
OUTPUTS	All Outputs	10 U.L.

(1 U.L. = TTμL Gate Input Load)

MODE SELECTION

Reset	Inputs	Outputs			
MR_1	MR_2	Q_0	Q_1	Q_2	Q_3
H	H	L	L	L	L
L	H	Count			
H	L	Count			
L	L	Count			

H = High Voltage Level
L = Low Voltage Level
X = Don't Care Condition

TRUTH TABLE

COUNT	OUTPUT			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

Note: Output Q_0 connected to input Q_1.

ELECTRICAL CHARACTERISTICS (T_A = 0°C to +75°C, V_{CC} = 5.0 V ±5%) (Part # U7A935659X)

SYMBOL	CHARACTERISTIC	LIMITS 0°C MIN.	0°C MAX.	+25°C MIN.	+25°C TYP.	+25°C MAX.	+75°C MIN.	+75°C MAX.	UNITS	CONDITIONS & COMMENTS
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	V_{CC} = 4.75 V, I_{OH} = −600 μA
V_{OL}	Output Low Voltage		0.45		0.2	0.45		0.45	Volts	V_{CC} = 4.75 V, I_{OL} = 16 mA
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed Input High Threshold For All Inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed Input Low Threshold For All Inputs
I_F	Input Load Current MR		−1.6		−1.0	−1.6		−1.6	mA	V_{CC} = 5.25 V, V_F = 0.45 V
2 I_F	Input Load Current $\overline{CP}_0$ $\overline{CP}_1$		−3.2		−2.0	−3.2		−3.2	mA	
4 I_F	Input Load Current		−6.4		−4.0	−6.4		−6.4	mA	
I_R	Input Leakage Current MR		60		10	60		60	μA	V_{CC} = 5.25 V, V_R = 4.5 V
2 I_R	Input Leakage Current $\overline{CP}_0$ $\overline{CP}_1$		120		20	120		120	μA	
4 I_R	Input Leakage Current		240		40	240		240	μA	
I_{PD}	Power Supply Current				30	50			mA	V_{CC} = 5.0 V

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS & COMMENTS
t_{pd+}	Turn-Off Delay $\overline{CP}_0$ to Output Q_3		75	135	ns	V_{CC} = 5.0 V, C_L = 15 pF Q_0 Output Connected To $\overline{CP}_1$ Input
t_{pd-}	Turn-On Delay $\overline{CP}_0$ to Output Q_3		75	135	ns	
f_{max}	Maximum Frequency of Input Count Pulses	10	18		MHz	

SWITCHING TIME WAVEFORMS

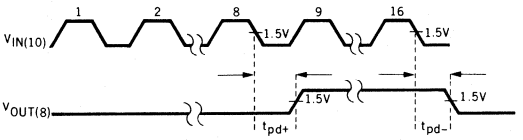
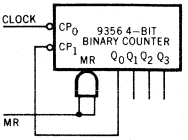


Fig. 3

APPLICATIONS



WAVEFORMS

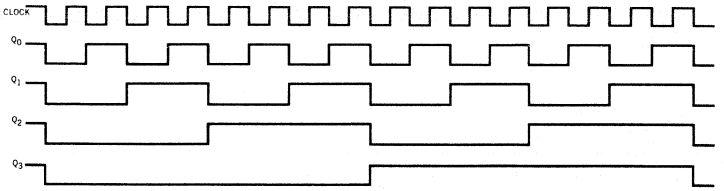


Fig. 4 — 4-BIT BINARY COUNTER

This Figure illustrates the external connection required to make the 9356 a four-bit counter and the resulting waveforms.

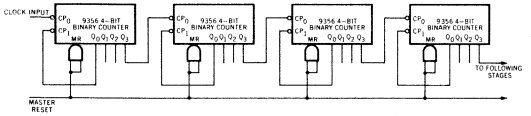


Fig. 5 — MULTISTAGE COUNTING USING THE 9356

The interconnections required for a multistage binary ripple type counter are shown above.

NOTE: The 9356 flip-flops change state on the high to low transition of the clock.

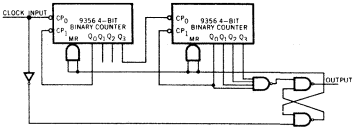
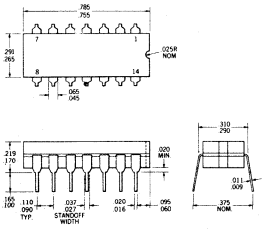


Fig. 6 — MODULO 240 DIVIDER

This modulo 240 divider is an example of a modulo N divider that can be formed using the 9356 4-bit binary counter. The two 9356 counters form an 8-bit binary counter where a gate is used to decode the state which will give the desired modulo. The gate sets a latch that assures that the counters are reset. On the positive edge of the clock the latch is reset and on the negative edge of the same pulse, the counter starts on a new cycle.

PACKAGE INFORMATION

7A - 14 LEAD MSI DUAL IN-LINE PACKAGE



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.2 grams

TTμL/MSI 9360/74192 . 9366/74193

UP/DOWN DECADE AND BINARY COUNTERS

FAIRCHILD TTμL® IC PRODUCTS

GENERAL DESCRIPTION – The TTμL/MSI 9360/74192 is a synchronous up/down BCD decade counter, and the TTμL/MSI 9366/74193 is a synchronous up/down 4-bit binary counter. Both counters have separate up/down clocks, parallel load facility, terminal count outputs for multidecade operation, and an asynchronous overriding master reset. The circuits use TTμL technology for high speed, and are compatible with the entire Fairchild TTμL family.

FEATURES

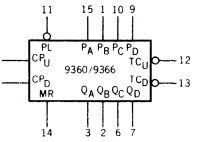
- **SYNCHRONOUS OPERATION**
- **CASCADING CIRCUITRY INTERNALLY PROVIDED**
- **PARALLEL LOAD FACILITY**
- **ASYNCHRONOUS MASTER RESET**
- **30MHz TYPICAL COUNT FREQUENCY**
- **TYPICAL POWER DISSIPATION OF 300mW**
- **INPUT CLAMP DIODES**
- **ALL CERAMIC "HERMETIC" 16 PIN DUAL-IN-LINE PACKAGE**
- **TTμL COMPATIBLE**

PIN NAMES

$\overline{PL}$	Parallel Load (Active Low) Input
P_A, P_B, P_C, P_D	Parallel Data Inputs
CP_U	Count Up Clock Pulse Input
CP_D	Count Down Clock Pulse Input
MR	Master Reset (Clear) Input (Asynchronous)
Q_A, Q_B, Q_C, Q_D	Counter Outputs
$\overline{TC_U}$	Terminal Count Up (Carry) Output
$\overline{TC_D}$	Terminal Count Down (Borrow) Output

ORDER INFORMATION – Specify U7B936059X or U7B74192 for the up/down decade counter and U7B936659X or U7B74193 for the 4-Bit binary counter in a 16-pin Dual In-line package, 0°C to 75°C temperature range.

LOGIC SYMBOL



9360/74192 & 9366/74193

V_{CC} = Pin 16
GND = Pin 8

Fig. 1

CONNECTION DIAGRAM
DIP (TOP VIEW)

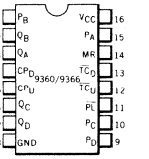


Fig. 2

LOGIC DIAGRAMS

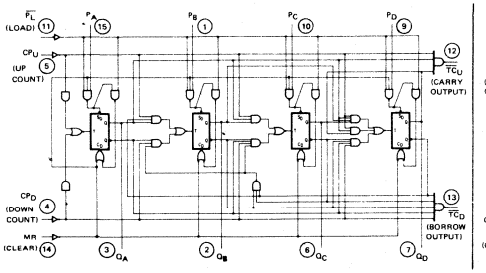
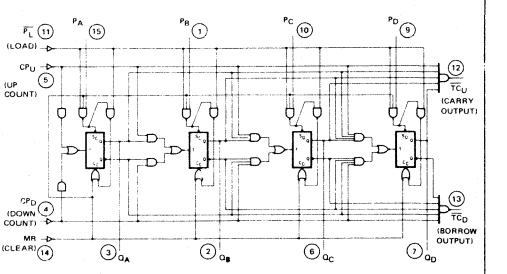


Fig. 3 9360/74192



V_{CC} = PIN 16 GND = PIN 8 ◯ = PIN NUMBER

Fig. 4 9366/74193

FAIRCHILD SEMICONDUCTOR

FUNCTIONAL DESCRIPTION — The 9360/74192 and 9366/74193 can be reset, preset and count up or down. These operating modes of the 9360/74192 and 9366/74193 are tabulated in figure 7. The operating modes of the 9360/74192 and 9366/74193 are identical, the only difference between the devices is the count sequences.

Counting is synchronous, with the outputs changing state after the low to high transition of either the count-up clock (CP_U) or count-down clock (CP_D). The direction of counting is determined by which clock input is pulsed while the other clock input is high. (Incorrect counting will occur if both the count-up clock and count-down clock inputs are low simultaneously.) Both counters will respond to a clock pulse on either input by changing to the next appropriate state of the count sequence. (The state diagram for the 9360/74192 shows the regular sequence and in addition shows the sequence of states if a code greater than nine is present in the counter.)

Both the 9360/74192 and the 9366/74193 have a parallel load (asynchronous) facility which permits the counter to be preset. Whenever the parallel load ($\overline{PL}$) input is low, and master reset is low, the information present on the parallel data inputs (P_A, P_B, P_C, P_D) will be loaded into the counters and appear on the outputs independent of the conditions of the clock inputs. When the parallel load input goes high this information is stored in the counters and when the counters are clocked they change to the next appropriate state in the count sequence. The parallel data inputs are inhibited when the parallel load is high and have no effect on the counters.

The terminal count-up ($\overline{TC_U}$) and terminal count-down ($\overline{TC_D}$) outputs (carry and borrow respectively) allow multidecade counter operations without additional logic. The counters are cascaded by feeding the terminal count-up output to the count-up clock input and terminal count-down clock input of the following counter.

The terminal count-up outputs for the 9360/74192 and 9366/74193 are low when their count-up clock inputs are low and the counters are in state nine and state fifteen respectively. Similarly, the terminal count-down outputs are low when their count-down clock inputs are low and both counters are in state zero. Thus, when the 9360/74192 counter is in state nine and the 9366/74193 counter is in state fifteen and both are counting up, or both counters are in state zero and counting down, a clock pulse will change the counter's state on the rising edge and simultaneously clock the following counter through the appropriate active low terminal count output. There are two gate delays per state when these counters are cascaded.

The asynchronous master reset input (MR), when high, overrides all input and clears the counters. Master reset overrides parallel load so that when both are activated the counters will be reset. (Obviously, both parallel load and master reset must not be deactivated simultaneously for predictable operation.

9360/74192 LOGIC EQUATIONS FOR TERMINAL COUNT

$$TC_U = Q_0 \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot Q_3 \cdot \overline{CP_U}$$
$$TC_D = \overline{Q_0} \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot \overline{Q_3} \cdot \overline{CP_D}$$

9366/74193 LOGIC EQUATIONS FOR TERMINAL COUNT

$$TC_U = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot \overline{CP_U}$$
$$TC_D = \overline{Q_0} \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot \overline{Q_3} \cdot \overline{CP_D}$$

Fig. 5 **9360/74192 STATE DIAGRAM**

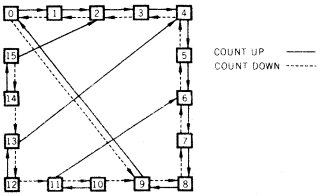


Fig. 6 **9366/74193 STATE DIAGRAM**

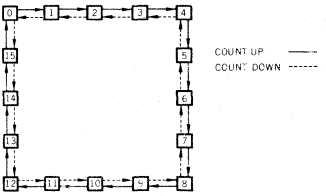


Fig. 7 **MODE SELECTION (Both Counters)**

MR	PL	CP_U	CP_D	MODE
H	X	X	X	Preset (Asyn.)
L	L	X	X	Preset (Asyn.)
L	H	H	H	No Change
L	H	CP	H	Count Up
L	H	H	CP	Count Down

H = High Voltage Level
L = Low Voltage Level
X = Don't Care Condition
CP = Clock Pulse

TTμL LOADING RULES

INPUTS	LOADING
All Inputs	1 UL

OUTPUTS	DRIVE FACTOR
All Outputs	10 UL

NOTE: 1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to + 150°C
Temperature (Ambient) Under Bias	0°C to + 75°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to + 7.0 V
Input Voltage (D.C.)	−0.5 V to + 5.5 V

RECOMMENDED OPERATING CONDITIONS

PART NUMBER	SUPPLY VOLTAGE (V_{CC}) MIN.	TYP.	MAX.	TEMPERATURE
U7B936059X(74192)	4.75 V	5.0 V	5.25 V	0°C to 75°C
U7B936659X(74193)	4.75 V	5.0 V	5.25 V	0°C to 75°C

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS MIN.	TYP. (Note 2)	MAX.	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Level	2.0			Volts	Guaranteed input logical HIGH voltage for all inputs
V_{IL}	Input LOW Level			0.8	Volts	Guaranteed input logical LOW voltage for all inputs
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = −400μA, V_{IH} = 2.0 V, V_{IL} = 0.8V
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 16mA, V_{IH} = 2.0V, V_{IL} = 0.8V
I_{IH}	Input HIGH Current			40	μA	V_{CC} = MAX., V_{IN} = 2.4V
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5V
I_{IL}	Input LOW Current			−1.6	mA	V_{CC} = MAX., V_{IN} = 0.4V
I_{SC} (I_{OS})	Output Short Circuit Current (Note 3)	−18		−65	mA	V_{CC} = MAX.
I_{CC}	Power Supply Current		65	102	mA	V_{CC} = MAX.

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0V, 25°C.
(3) Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
f_{max}	Maximum Input Count Frequency		30		MHz	V_{CC} = 5.0V, C_L = 15pF, R_L = 400Ω
t_{PLH}	Turn Off Delay, Count-Up Input (CP_U) to Carry Output ($\overline{TC_U}$)		22		ns	V_{CC} = 5.0 V, C_L = 15 pF, R_L = 400 Ω
t_{PHL}	Turn On Delay, Count-Up Input (CP_U) to Carry Output ($\overline{TC_U}$)		18		ns	
t_{PLH}	Turn Off Delay, Count-Down Input (CP_D) to Borrow Output ($\overline{TC_D}$)		22		ns	V_{CC} = 5.0 V, C_L = 15 pF, R_L = 400 Ω
t_{PHL}	Turn On Delay, Count-Down Input (CP_D) to Borrow Output ($\overline{TC_D}$)		18		ns	
t_{PLH}	Turn Off Delay, Either Count Input to Q Output		27		ns	V_{CC} = 5.0 V, C_L = 15 pF, R_L = 400 Ω
t_{PHL}	Turn On Delay, Either Count Input to Q Output		37		ns	

APPLICATIONS

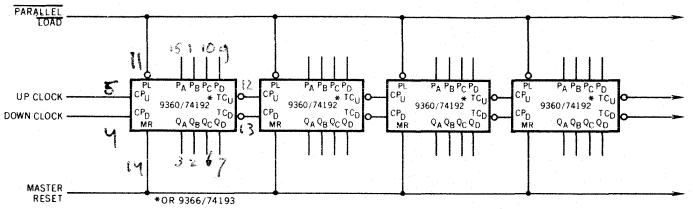


Fig. 8 MULTISTAGE UP/DOWN COUNTER

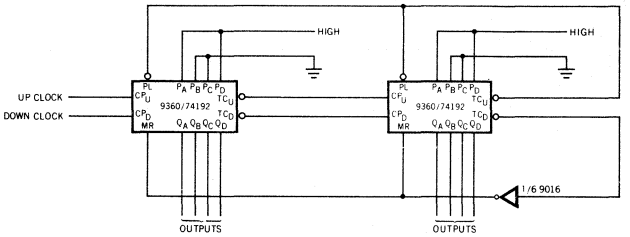


Fig. 9 DEAD ENDED COUNTER

Some systems employing up/down counters require that underflow or overflow be inhibited. A change from the maximum count to zero in the count up mode or the change from zero to the maximum count value in the count down mode has to be prevented.

This limited range operation is implemented by the feedback connections illustrated above for the case of two 9360/74192 decade counters. The same feedback can be used with more or less than two stages and also used with the 9366/74193 binary counter. However, fifteen must be loaded into the 9366/74193 to prevent overflow.

PACKAGE INFORMATION

7B — 16 LEAD DUAL IN-LINE PACKAGE

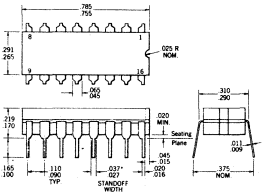


Fig. 10

NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.2 grams
*The .037/.027 dimension does not apply to the corner leads

LPTTμL/MSI 93L00
LOW POWER 4-BIT SHIFT REGISTER
A FAIRCHILD TTμL® IC PRODUCT

GENERAL DESCRIPTION — The LPTTμL/MSI 93L00 Four-Bit Shift Register is a medium speed multi-functional sequential logic block which is useful in a wide variety of register and counter applications. As a register it may be used in serial-serial, shift left, shift right, serial-parallel, parallel-serial, and parallel-parallel data transfers. The circuit uses TTμL technology for high speed and high fanout capability, and is compatible with the Fairchild TTμL family.

FEATURES

- **10 MHz TYPICAL SHIFT FREQUENCY**
- **ASYNCHRONOUS COMMON RESET**
- **J, $\overline{K}$ INPUTS TO FIRST STAGE**
- **SYNCHRONOUS PARALLEL ENTRY**
- **TYPICAL POWER DISSIPATION OF 75 mW**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **ALL CERAMIC "HERMETIC" 16 PIN DUAL IN-LINE AND FLAT PACKAGES**
- **TTμL COMPATIBLE**

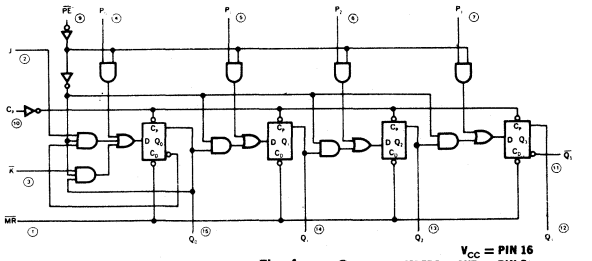
PIN NAMES

$\overline{PE}$	Parallel Enable (Active Low) Input
P_0, P_1, P_2, P_3	Parallel Inputs
J	First Stage J (Active High) Input
$\overline{K}$	First Stage K (Active Low) Input
C_P	Clock (Active High) Going Edge Input
$\overline{MR}$	Master Reset (Active Low) Input
Q_0, Q_1, Q_2, Q_3	Parallel Outputs
$\overline{Q}_3$	Complementary Last Stage Output

ORDER INFORMATION

Specify U7B93L00XXX for 16 pin Dual In-Line Package or U4L93L00XXX for 16 pin Flat Package where XXX is 51X for the −55°C to +125°C temperature range, or 59X for the 0°C to +75°C temperature range.

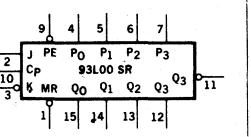
LOGIC DIAGRAM



V_{CC} = PIN 16
GND = PIN 8

Fig. 4 ○ = PIN NUMBERS

LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

Fig. 1

CONNECTION DIAGRAM
DIP (TOP VIEW)

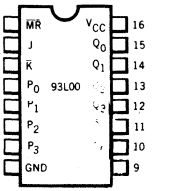


Fig. 2

FLATPAK (TOP VIEW)

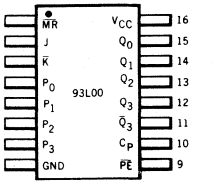


Fig. 3

FAIRCHILD
SEMICONDUCTOR

FUNCTIONAL DESCRIPTION — The logic symbol of Figure 2 provides an indication of the functional characteristics of the 93L00 four bit shift register. Several special logical features of the 93L00 design which provide a high degree of general usefulness are described below:

1. A $\overline{JK}$ input is provided to the first flip flop in the register. This type of input is the same as the more common JK input except that the low voltage level activates the $\overline{K}$ input. This provides the greater power of the JK type input for more general applications and at the same time the simple D type input that is most appropriate for a shift register can be easily obtained by simply tying the two inputs together.
2. There is no restriction on the activity of the J or $\overline{K}$ inputs for logical operation — except for the set up and release time requirements.
3. Parallel inputs for all four stages are provided. These will determine the next condition of the shift register synchronous with the clock input, whenever the Parallel Enable input is low. With the Parallel Enable input low the element appears as four common clocked D flip flops. When the Parallel Enable is high, or not connected, the shift register performs a one bit shift for each clock input. In both cases the next state of the flip flops occurs after the low to high transition of the clock input.
4. An internal clock buffer provides both reduced clock input loading, and the ability to gate the clock with only a single NAND gate.
5. The active high output is provided for all four stages and an active low output is provided for the last stage.
6. A master asynchronous reset input allows the setting to zero of all stages, independent of the condition of any other inputs.

TRUTH TABLES

TABLE I — SERIAL ENTRY
($\overline{PE}$ = High, $\overline{MR}$ = High)

J	$\overline{K}$	Q_0 at t_{n+1}
L	L	L
L	H	Q_0 at t_n (no change)
H	L	$\overline{Q}_0$ at t_n (toggles)
H	H	H

TABLE II — SERIAL ENTRY
($\overline{PE}$ = High, $\overline{MR}$ = High)

J&$\overline{K}$ Connected	Q_0 at t_{n+1}
L	L
H	H

TABLE III — PARALLEL ENTRY
($\overline{PE}$ = Low, $\overline{MR}$ = High)

D-Input (P_0, P_1, P_2 or P_3)	Output Q at t_{n+1} (Q_0, Q_1, Q_2 or Q_3)
L	L
H	H

(n+1) = Indicates state after next clock

TABLE IV — MODE SELECTION

	$\overline{PE}$	P_0 P_1 P_2 P_3	J $\overline{K}$	$\overline{MR}$
Serial Entry	H	X X X X	Refer to Table I & II	H
Parallel Entry	L	Refer to Table III	X X	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

TABLE V — TTμL LOADING RULES

INPUTS	LOADING	
	HIGH	LOW
J, $\overline{K}$, $\overline{MR}$, P_0, P_1, P_2 & P_3	0.5 U.L.	0.25 U.L.
$\overline{PE}$	1.15 U.L.	0.575 U.L.
CP	1.0 U.L.	0.5 U.L.

OUTPUTS	DRIVE FACTORS	
	HIGH	LOW
Q_0, Q_1, Q_2, Q_3 & $\overline{Q}_3$	8.0 U.L.	2.0 U.L.

Note: 1 Unit Load (U.L.) = 40 μA High/1.6 mA Low

TYPICAL INPUT AND OUTPUT CIRCUITS

INPUTS EQUIVALENT CIRCUIT

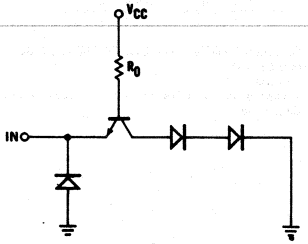


Fig. 5

TYPICAL RESISTORS

R_0 = 16 kΩ R_2 = 240 Ω
R_1 = 6 kΩ R_3 = 5 kΩ

OUTPUTS EQUIVALENT CIRCUIT

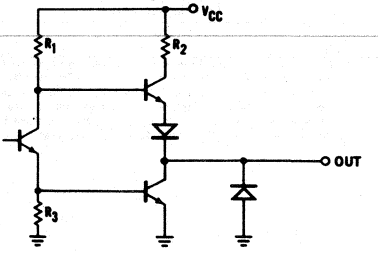


Fig. 6

L

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (D.C.)	−0.5 V to +5.5 V
*Input Current (D.C.)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output High)	0.5 V to +V_{CC} value
Output Current (D.C.) (Output Low)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC}) MIN.	TYP.	MAX.	TEMPERATURE
U7B/4L93L0051X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
U7B/4L93L0059X	4.75 V	5.0 V	5.25 V	0°C to 75°C

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	CHARACTERISTIC	LIMITS MIN.	TYP. (Note 4)	MAX.	UNITS	CONDITIONS
V_{OH}	Output HIGH Voltage	2.4	0.15		Volts	V_{CC} = MIN., I_{OH} = −0.32 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.1	0.3	Volts	V_{CC} = MIN., I_{OL} = 3.2 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{IH}	Input HIGH Level	2.0			Volts	Guaranteed input logical HIGH voltage for all inputs
V_{IL}	Input LOW Level			0.7	Volts	Guaranteed input logical LOW voltage for all inputs
I_{IL}	Input LOW Current J, $\overline{K}$, $\overline{MR}$, P_0, P_1, P_2 & P_3 CP $\overline{PE}$		 −0.25 −0.50 −0.58	 −0.40 −0.80 −0.92	mA	V_{CC} = MAX., V_{IN} = 0.3 V
I_{IH}	Input HIGH Current J, $\overline{K}$, $\overline{MR}$, P_0, P_1, P_2 & P_3 CP $\overline{PE}$		 2.0 4.0 5.0	 20 40 46	μA	V_{CC} = MAX., V_{IN} = 2.4 V
	Input HIGH Current			1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{SC}	Output Short Circuit Current	−2.5	−16	−25	mA	V_{CC} = MAX., V_{OUT} = 0.0 V
I_{CC}	Power Supply Current		15	23	mA	V_{CC} = MAX.

NOTES:

(1) The actual Testing Procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this Specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California (see page 1 for address and phone).

(2) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.

(3) The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

(4) Typical limits are at V_{CC} = 5.0 V, 25°C, and max. loading.

SWITCHING CHARACTERISTICS ($T_A = 25°C$)

SYMBOL	CHARACTERISTIC	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	CONDITIONS
t_{pd+}	Turn Off Delay		55		ns	$V_{CC} = 5.0$ V, $C_L = 15$ pF (See Fig. 7)
t_{pd-}	Turn On Delay		65		ns	
f_{sr}	Shift Right Frequency		10		MHz	$V_{CC} = 5.0$ V, $C_L = 15$ pF (See Fig. 7)
CP_{pw}	Clock Pulse Width		50		ns	$V_{CC} = 5.0$ V, $C_L = 15$ pF (See Figs. 7a & 7b)
t_s	Set-up Time		65		ns	
t_r	Release Time		35		ns	
$t_s(\overline{PE})$	Set-up Time for $\overline{PE}$		90		ns	
$t_r(\overline{PE})$	Release Time for $\overline{PE}$		55		ns	
$t_{pd-}(\overline{MR})$	Reset Time for $\overline{MR}$		80		ns	
$t_{rec}(\overline{MR})$	Recovery Time for $\overline{MR}$		55		ns	
$\overline{MR}_{pw}$	Min Reset Pulse Width		50		ns	

SET-UP TIME: t_s is defined as the minimum time required for the logic level to be present at the logic input prior to the clock transition from low to high in order for the flip-flop(s) to respond.

RELEASE TIME: t_r is defined as the maximum time allowed for the logic level to be present at the logic input prior to the clock transition from low to high in order for the flip-flop(s) not to respond.

RECOVERY TIME FOR MR: $t_{rec}(MR)$ is defined as the minimum time required between the end of the reset pulse and the clock transition from low to high in order for the flip-flop(s) to respond to the clock.

Fig. 7a

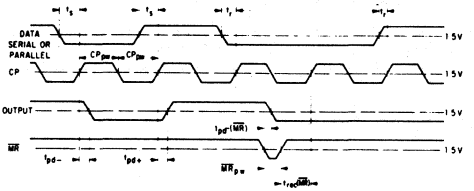


Fig. 7b

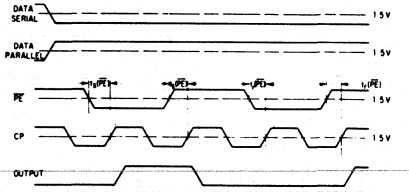


Fig. 7c

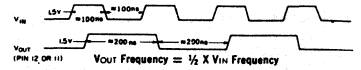


Fig. 7 — SWITCHING TIME & SHIFT RIGHT FREQUENCY WAVEFORMS

APPLICATIONS

APPLICATIONS — The 93L00 has been designed to be useful in a wide variety of applications. The multifunctional capability of the Fairchild 93L00 is illustrated by the applications shown below.

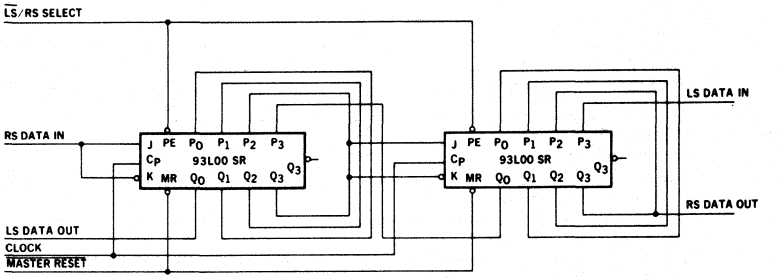


Fig. 8 — EIGHT BIT LEFT/RIGHT SHIFT REGISTER

This register shifts Left or Right on each shift clock, depending upon the condition of the $\overline{LS}$/RS SELECT input. If this input is high, Right Shift occurs and if low, Left Shift occurs.

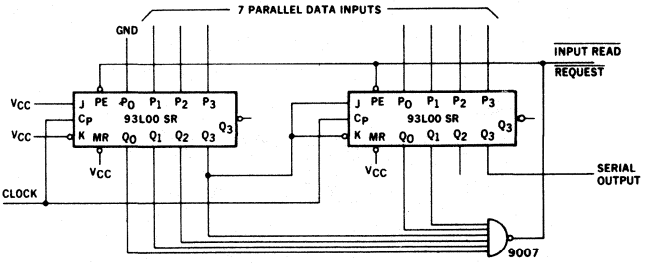
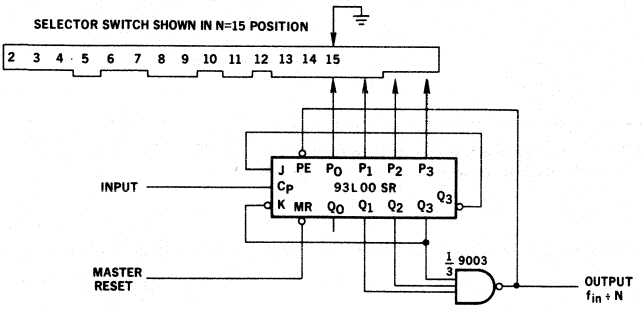


Fig. 9 — SEVEN BIT PARALLEL TO SERIAL CONVERTER

This parallel to serial converter uses a marker bit, to count the data bits shifted out, so that a parallel load enable is generated to load the next parallel word for conversion at the correct time.

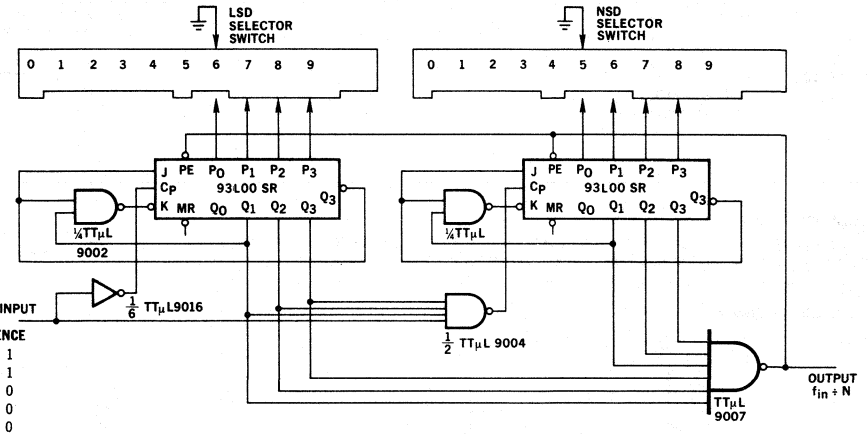
APPLICATIONS (Cont'd)



COUNT SEQUENCE	
0111	
0011	
0001	
0000	
1000	
0100	
1010	
0101	
0010	
1001	
1100	
0110	
1011	
1101	
1110	LOAD STATE

Fig. 10 — DIVIDE BY N COUNTER FOR N = 2 to 15

This counter produces an output pulse for every N input pulses, where the number N is determined by the setting of the slide selector switch as shown or by logic inputs to the parallel data lines from an external source.



COUNT	SEQUENCE
9	0 0 1 1
8	0 0 0 1
7	0 0 0 0
6	1 0 0 0
5	1 1 0 0
4	0 1 1 0
3	1 0 1 1
2	1 1 0 1
1	1 1 1 0
0	0 1 1 1

Fig. 11 — TWO DECADE PROGRAMMABLE DIVIDER

This circuit divides by any number "N" from 1 to 100. The selected N is one greater than is shown on the slide switches. As an example the switches are showing 56, therefore the circuit will divide by 57 with this setting.

PACKAGE INFORMATION

7B — 16 LEAD DUAL IN-LINE PACKAGE

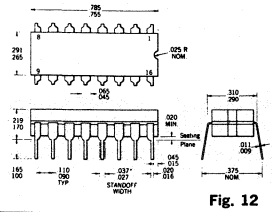


Fig. 12

NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.2 grams
*The .027/.037 dimension does not apply to the corner leads

4L — 16 LEAD (BeO) FLATPAK

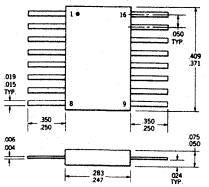


Fig. 13

NOTES:
All dimensions in inches
Leads are gold-plated kovar
Package weight is 0.4 gram

LPTTμL/MSI 93L01

LOW POWER ONE-OF-TEN DECODER

A FAIRCHILD TTμL® IC PRODUCT

GENERAL DESCRIPTION — The LPTTμL/MSI 93L01 is a multipurpose decoder designed to accept four inputs and provide 10 mutually exclusive outputs. The circuit uses TTμL technology and is compatible with the Fairchild TTμL family.

FEATURES

- **MULTI-FUNCTION CAPABILITY**
- **MUTUALLY EXCLUSIVE OUTPUTS**
- **DEMULTIPLEXING CAPABILITY**
- **TYPICAL PROPAGATION DELAY OF 63 ns**
- **TYPICAL POWER DISSIPATION OF 45 mW**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **ALL CERAMIC "HERMETIC" 16 PIN DUAL IN-LINE AND FLAT PACKAGES**
- **TTμL COMPATIBLE**

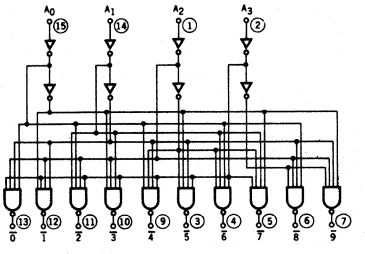
PIN NAMES

A_0, A_1, A_2, A_3	Address Inputs
$\overline{0}$ to $\overline{9}$	Outputs (Active Low)

ORDER INFORMATION

Specify U7B93L01XXX for 16 pin Dual In-Line package or U4L93L01XXX for 16 pin Flat Package where XXX is 51X for the −55°C to +125°C temperature range, or 59X for the 0°C to +75°C temperature range.

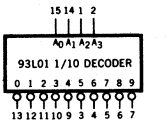
LOGIC DIAGRAM



V_{CC} = PIN 16
GND = PIN 8
○ = PIN NUMBERS

Fig. 4

LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

Fig. 1

CONNECTION DIAGRAM
DIP (TOP VIEW)

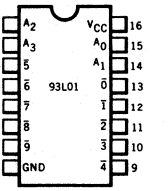


Fig. 2

FLATPAK (TOP VIEW)

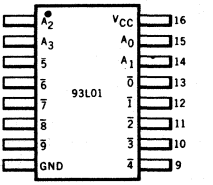


Fig. 3

FAIRCHILD
SEMICONDUCTOR

FUNCTIONAL DESCRIPTION

The 93L01 Decoder accepts four active high BCD inputs and provides ten mutually exclusive active low outputs, as shown by Figure 1 or 4. The active low outputs facilitate memory addressing when inverting drivers are used between decoder and memory elements such as the 9033.

The logic design of the 93L01 ensures that all outputs are high when binary codes greater than nine are applied to the inputs.

The most significant A_3 input produces a useful inhibit function when the 93L01 is used as a 1 out of 8 decoder. This is illustrated in the 1 out of 32 decoder shown in Figure 9.

The Truth Table and Loading Rules for the 93L01 are shown in Table I and Table II.

TABLE I — TRUTH TABLE

A_0	A_1	A_2	A_3	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$	$\overline{8}$	$\overline{9}$
L	L	L	L	L	H	H	H	H	H	H	H	H	H
H	L	L	L	H	L	H	H	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H	H	H
H	H	L	L	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	H	H	H	L	H	H	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
H	H	H	L	H	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = High Voltage Level
L = Low Voltage Level

TABLE II — TTμL LOADING RULES

INPUTS	LOADING	
	High	Low
All Inputs	0.5 U.L.	0.25 U.L.

OUTPUTS	DRIVE FACTOR	
	High	Low
All Outputs	10 U.L.	2.5 U.L.

Note: 1 Unit Load (U.L.) = 40 μA High/1.6 mA Low

TYPICAL INPUT AND OUTPUT CIRCUITS

INPUTS
EQUIVALENT CIRCUIT

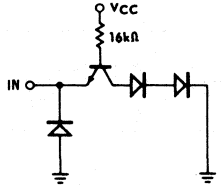


Fig. 5

OUTPUTS
EQUIVALENT CIRCUITS

OUTPUT LOW

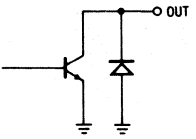


Fig. 6

OUTPUT HIGH

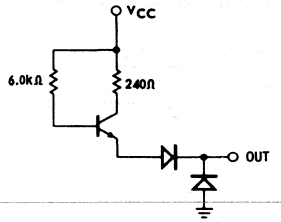


Fig. 7

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (D.C.)	−0.5 V to +5.5 V
*Input Current (D.C.)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output High)	0.5 V to +V_{CC} value
Output Current (D.C.) (Output Low)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC}) MIN.	TYP.	MAX.	TEMPERATURE
U7B/4L93L0151X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
U7B/4L93L0159X	4.75 V	5.0 V	5.25 V	0°C to 75°C

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	CHARACTERISTIC	LIMITS MIN.	TYP. (Note 4)	MAX.	UNITS	CONDITIONS
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = − 0.4 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.15	0.3	Volts	V_{CC} = MIN., I_{OL} = 4.0 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{IH}	Input HIGH Level	2.0			Volts	Guaranteed input logical HIGH voltage for all inputs
V_{IL}	Input LOW Level			0.7	Volts	Guaranteed input logical LOW voltage for all inputs
I_{IL}	Input LOW Current		−0.25	−0.4	mA	V_{CC} = MAX., V_{IN} = 0.3 V
I_{IH}	Input HIGH Current		2.0	20	μA	V_{CC} = MAX., V_{IN} = 2.4 V
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{SC}	Output Short Circuit Current	−2.5	−16	−25	mA	V_{CC} = MAX., V_{OUT} = 0.0 V
I_{CC}	Power Supply Current		9.0	13	mA	V_{CC} = MAX., inputs at GND.

NOTES:
(1) The actual Testing Procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this Specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California (see page 1 for address and phone).
(2) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
(3) The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
(4) Typical limits are at V_{CC} = 5.0 V, 25°C, and max. loading.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	CHARACTERISTIC	LIMITS MIN.	TYP.	MAX.	UNITS	CONDITIONS
t_{pd+}	Turn Off Delay Input to Output		60		ns	V_{CC} = 5.0 V See Fig. 8
t_{pd-}	Turn On Delay Input to Output		65		ns	C_L = 15 pF

SWITCHING TIME WAVEFORMS

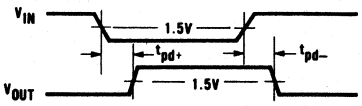


Fig. 8

APPLICATIONS

APPLICATIONS — The 93L01 decoder may be used for BCD to Decimal or 3 bit binary to octal conversion as well as many other applications. The general purpose nature of the 93L01 is indicated by its use in the following applications.

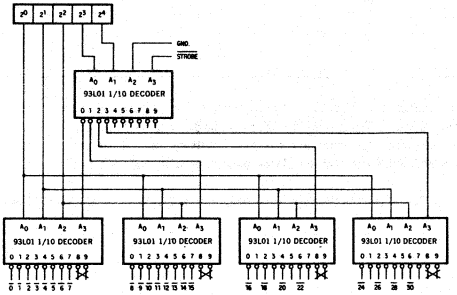
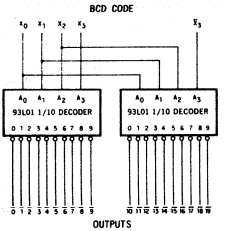


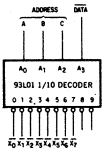
Fig. 9 — ONE-OUT-OF-THIRTY-TWO DECODING



DECIMAL DIGIT	OUTPUT SELECTION BCD CODE 8421	5421	EXCESS 3	4221
0	0, 18	0, 18	3	0, 18
1	1, 19	1, 19	4	1, 19
2	2	2	5	2
3	3	3	6	3
4	4	4	7	6
5	5	8, 10	8, 10	9, 11
6	6	9, 11	9, 11	14
7	7	12	12	15
8	8, 10	13	13	16
9	9, 11	14	14	17

Decode any BCD code using two 93L01 elements. Any 4 bit BCD code may be decoded by selecting outputs as shown in the table.

Fig. 10 — DECODE ANY BCD CODE



ADDRESS A	B	C	OUTPUT LINE
0	0	0	0
1	0	0	1
0	1	0	2
1	1	0	3
0	0	1	4
1	0	1	5
0	1	1	6
1	1	1	7

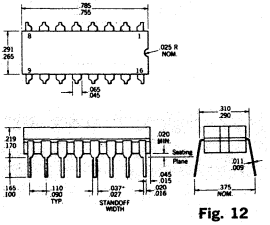
Data may be routed from a source to any of 8 outputs by addressing that output. All non-addressed outputs remain high.

Complements of outputs 0 and 1 are available at outputs 8 and 9 respectively.

Fig. 11 — DIGITAL DEMULTIPLEXER

PACKAGE INFORMATION

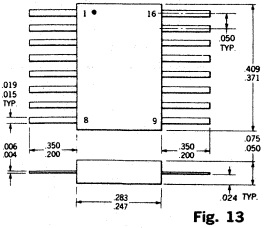
7B — 16 LEAD MSI DUAL IN-LINE PACKAGE



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.2 grams
*The .027/.037 dimension does not apply to the corner leads

Fig. 12

4M — 24 LEAD (BeO) FLATPAK



NOTES:
All dimensions in inches
Leads are gold-plated kovar
Package weight is 0.4 gram

Fig. 13

LPTTμL/MSI 93L08

LOW POWER DUAL FOUR-BIT LATCH

A FAIRCHILD TTμL® IC PRODUCT

GENERAL DESCRIPTION — The LPTTμL/MSI 93L08 is a Dual 4-Bit Latch designed for general purpose storage applications in medium speed digital systems. The 93L08 uses TTμL technology and is TTμL compatible. All inputs incorporate diode clamps to ground to reduce negative line transients. All outputs have active pull-up circuitry to provide high capacitive drive and low impedance outputs in both logic states to provide good A.C. noise immunity.

FEATURES

- **ACTIVE LEVEL LOW ENABLE GATE INPUTS**
- **OVERRIDING MASTER RESET**
- **TYPICAL PROPAGATION DELAY OF 53 ns**
- **TYPICAL POWER DISSIPATION OF 100 mW**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS.**
- **ALL CERAMIC "HERMETIC" 24 PIN DUAL IN-LINE AND FLAT PACKAGES**
- **TTμL COMPATIBLE**

PIN NAMES

D_0, D_1, D_2, D_3	Parallel Latch Inputs
$\overline{E}$	AND Enable (Active Low) Inputs
$\overline{MR}$	Master Reset (Active Low) Input
Q_0, Q_1, Q_2, Q_3	Parallel Latch Outputs

ORDER INFORMATION — Specify U6N93L08XXX for 24-pin Dual In-Line Package or U4M93L08XXX for 24-pin Flat Package, where XXX is 51X for the −55°C to +125°C temperature range, or 59X for the 0°C to +75°C temperature range.

Electrical Characteristics on Page 2.

LOGIC SYMBOL

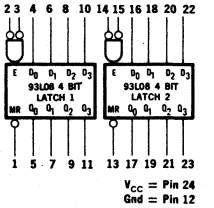


Fig. 1

CONNECTION DIAGRAM

DIP (TOP VIEW)

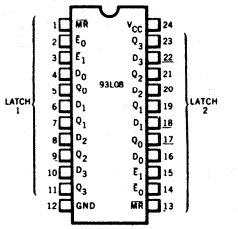


Fig. 2

FLATPAK (TOP VIEW)

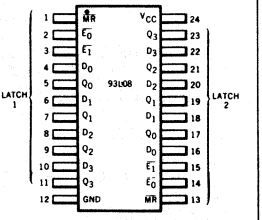


Fig. 3

LOGIC DIAGRAM

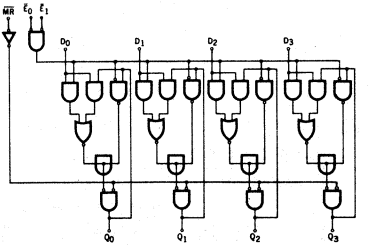


Fig. 4

NOTE: ONLY ONE 4-BIT LATCH SHOWN.

FAIRCHILD SEMICONDUCTOR

LATCH OPERATION — Data can be entered into the latch when both of the enable inputs are low. As long as this logic condition exists, the output of the latch will follow the input. If either of the enable inputs goes high, the data present in the latch at that time is held in the latch and is no longer affected by data input.

The master reset overrides all other input conditions and forces the outputs of all the latches low when a low signal is applied to the master reset input.

TABLE I — TRUTH TABLE

$\overline{MR}$	$\overline{E}_0$	$\overline{E}_1$	D	Q_0	OPERATION
H	L	L	L	L	Data Entry
H	L	L	H	H	Data Entry
H	L	H	X	Q_{n-1}	Hold
H	H	L	X	Q_{n-1}	Hold
H	H	H	X	Q_{n-1}	Hold
L	X	X	X	L	Reset

X = Don't Care
L = Low Voltage Level
H = High Voltage Level
Q_{n-1} = Previous Output State
Q_n = Present Output State

TABLE II — TTμL LOADING RULES

INPUTS	LOADING	
	High	Low
D_0, D_1, D_2, D_3, $\overline{MR}$, $\overline{E}_0$, $\overline{E}_1$	0.75 U.L. 0.5 U.L.	0.375 U.L. 0.25 U.L.

OUTPUTS	DRIVE FACTORS	
	High	Low
All	9.0 UL	2.25 UL

Note: 1 Unit Load (U.L.) = 40 μA High/1.6 mA Low

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (D.C.)	−0.5 V to +5.5 V
*Input Current (D.C.)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output High)	−0.5 V to +V_{CC} value
Output Current (D.C.) (Output Low)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC}) MIN.	TYP.	MAX.	TEMPERATURE
U6N/4M93L0851X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
U6N/4M93L0859X	4.75 V	5.0 V	5.25 V	0°C to 75°C

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	CHARACTERISTIC	LIMITS MIN.	TYP. (Note 5)	MAX.	UNITS	CONDITIONS
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = −0.36 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.15	0.3	Volts	V_{CC} = MIN., I_{OL} = 3.6 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{IH}	Input HIGH Level	2.0			Volts	Guaranteed input logical HIGH voltage for all inputs
V_{IL}	Input LOW Level			0.7	Volts	Guaranteed input logical LOW voltage for all inputs
I_{IL}	Input LOW Current $\overline{E}_0$, $\overline{E}_1$ & $\overline{MR}$		−0.25	−0.40	mA	V_{CC} = MAX., V_{IN} = 0.3 V
	Input LOW Current D_0, D_1, D_2 & D_3		−0.38	−0.64	mA	V_{CC} = MAX., V_{IN} = 0.0 V (See Note 4)
I_{IH}	Input HIGH Current $\overline{E}_0$, $\overline{E}_1$ & $\overline{MR}$ D_0, D_1, D_2 & D_3		2.0 3.0	20 30	μA	V_{CC} = MAX., V_{IN} = 2.4 V
	Input HIGH Current			1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{SC}	Output Short Circuit Current	−2.5	−16	−25	mA	V_{CC} = MAX., V_{OUT} = 0.0 V
I_{CC}	Power Supply Current		20	33	mA	V_{CC} = MAX., all outputs LOW, Pins 2 & 14 GND, other inputs open

NOTES:
(1) The actual Testing Procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this Specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California (see page 1 for address and phone).
(2) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
(3) The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
(4) This current is measured at $V_{IN} = 0.0$ V to insure that no current is being absorbed by the device internally. The maximum value given guarantees that the maximum instantaneous current that can flow out of the input at $V_{IN} = 0.3$ V is 0.6 mA.
(5) Typical limits are at $V_{CC} = 5.0$ V, 25°C, and max. loading.

SWITCHING CHARACTERISTICS ($T_A = 25°C$)

SYMBOL	CHARACTERISTIC	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	CONDITIONS
t_{pd+}	Enable to Output		65		ns	$V_{CC} = 5.0$ V, $C_L = 15$ pF, See Figure 5
t_{pd-}	Enable to Output		40			
t_{pd+}	Data to Output		50		ns	
t_{pd-}	Data to Output		40			
t_s "H"	High Data to Enable		15		ns	
t_s "L"	Low Data to Enable		22			
t_r "H"	High Data to Enable		0		ns	
t_r "L"	Low Data to Enable		0			
t_{pw}	Enable Pulse Width		20		ns	
t_{pw}	Master Reset Pulse Width		22		ns	
t_{pd-}	Master Reset to Output		38			
t_{rec}	Master Reset Recovery Time		6.0		ns	

SET UP TIME: t_s is defined as the time required for the logic level to be present at the Data Input prior to the enable transition from Low to High in order for the latch to recognize and store the new data.
RELEASE TIME: t_r is defined as the time allowed for a new logic level to be present at the data input prior to the enable transition from Low to High in order for the latch not to respond to that new input logic level. A negative release time means the new logic level must not occur until after the enable transition.
RECOVERY TIME: t_{rec} is defined as the time that the Enable must remain Low after the Master Reset transition from Low to High in order for the latch to recognize and store High data.

SWITCHING WAVEFORMS

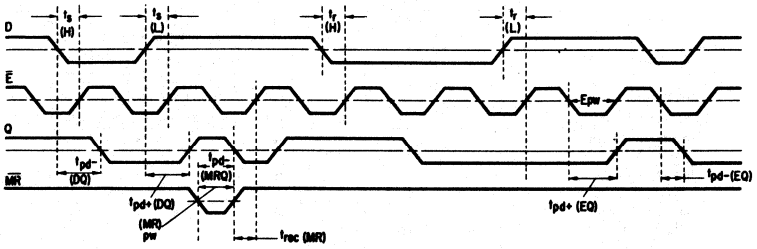


Fig. 5

APPLICATIONS

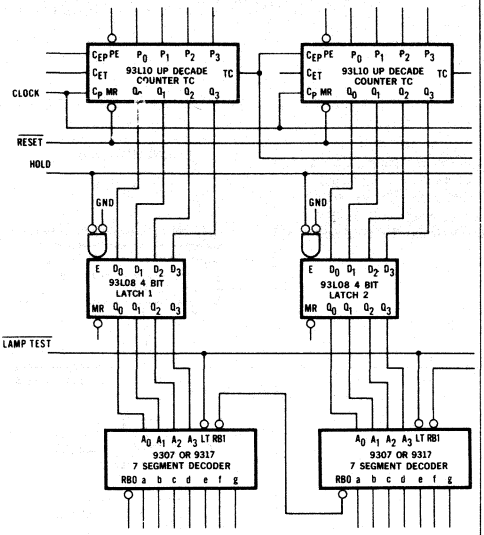


Fig. 6 93L08 AS A HOLDING REGISTER IN COUNTING AND DISPLAY APPLICATIONS

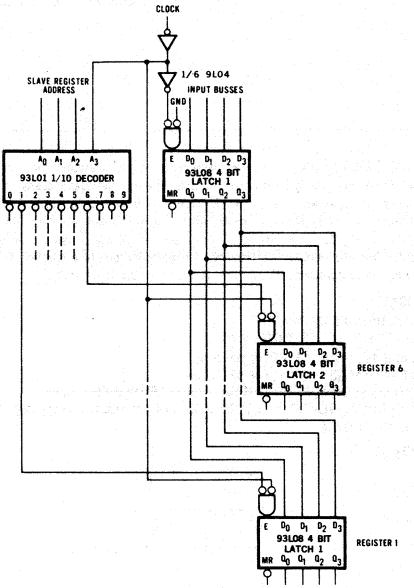


Fig. 7 SINGLE MASTER/MULTIPLE SLAVE FLIP-FLOP

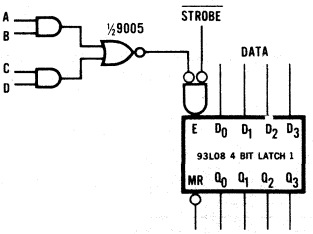
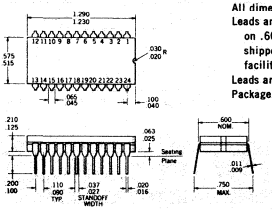


Fig. 8 AND-OR ENABLE SHOWING ACTIVE LEVEL LOW ENABLE GATE UTILITY

PACKAGE INFORMATION

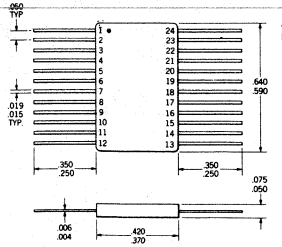
6N — 24 LEAD DUAL IN-LINE PACKAGE



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .600 inch centers. They are purposely shipped with "positive" misalignment to facilitate insertion
Leads are tin-plated kovar
Package weight is 6.5 grams

Fig. 9

4M — 24 LEAD (BeO) FLATPAK



NOTES:
All dimensions in inches
Leads are gold-plated kovar
Package weight is 0.8 gram

Fig. 10

LPTTμL/MSI 93L09

LOW POWER DUAL FOUR-INPUT MULTIPLEXER

A FAIRCHILD TTμL® IC PRODUCT

GENERAL DESCRIPTION — The low power 93L09 is a monolithic, medium speed, dual four-input digital multiplexer circuit, constructed with the Fairchild Planar* epitaxial process. It consists of two multiplexing circuits with common input select logic, each circuit contains four inputs and fully buffered complementary outputs. In addition to operating as a multiplexer, the 93L09 can generate two functions of three variables. Active pullups in the outputs ensure good drive and speed performance. The 93L09 may be cascaded to multiple levels so that any number of lines can be multiplexed onto a single output buss. The circuit uses TTμL technology and is compatible with all other members of the TTμL family.

FEATURES

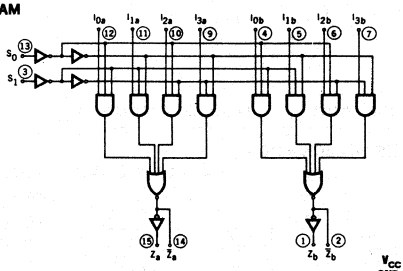
- **MULTIFUNCTION CAPABILITY**
- **ON-CHIP SELECT LOGIC DECODING**
- **TYPICAL PROPAGATION DELAY OF 48 ns**
- **TYPICAL POWER DISSIPATION OF 40 mW**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **ALL CERAMIC "HERMETIC" 16 PIN DUAL IN-LINE AND FLAT PACKAGES**
- **TTμL COMPATIBLE**

PIN NAMES

S_0, S_1	Common Select Inputs
Multiplexer A	
I_{0a}, I_{1a}, I_{2a}, I_{3a}	Multiplexer Inputs
Z_a	Multiplexer Output
$\overline{Z}_a$	Complementary Multiplexer Output
Multiplexer B	
I_{0b}, I_{1b}, I_{2b}, I_{3b}	Multiplexer Inputs
Z_b	Multiplexer Output
$\overline{Z}_b$	Complementary Multiplexer Output

ORDER INFORMATION — Specify U6B93L09XXX for 16-pin Dual In-Line package or U4L93L09XXX for 16-pin Flatpak, where XXX is 51X for the −55°C to +125°C temperature range, or 59X for the 0°C to +75°C temperature range.

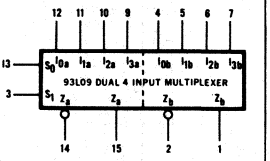
LOGIC DIAGRAM



V_{CC} = PIN 16
GND = PIN 8
○ = PIN NUMBERS

Fig. 4

LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

Fig. 1

CONNECTION DIAGRAM
DIP (TOP VIEW)

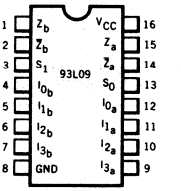


Fig. 2

FLATPAK (TOP VIEW)

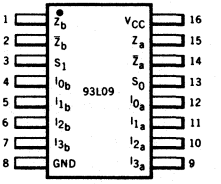


Fig. 3

*Planar is a patented Fairchild process.

FAIRCHILD
SEMICONDUCTOR

FUNCTIONAL DESCRIPTION

The 93L09 dual four input multiplexer is a member of the Fairchild family of compatible Low Power Medium Scale Integrated digital building blocks. It provides this family with the ability to select two bits of either data or control from up to four sources, in one package.

The 93L09 dual four input multiplexer is the logical implementation of a two-pole four-position switch, with the position of the switch being set by the logic levels supplied to the two select inputs. Both assertion and negation outputs are provided for both multiplexers. The logic equations for the outputs are shown below:

$$Z_a = I_{0a} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1a} \cdot \overline{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \overline{S}_0 + I_{3a} \cdot S_1 \cdot S_0$$
$$Z_b = I_{0b} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1b} \cdot \overline{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \overline{S}_0 + I_{3b} \cdot S_1 \cdot S_0$$

A common use of the 93L09 would be the moving of data from a group of registers to a common output buss. The particular register from which the data came would be determined by the state of the select inputs. A less obvious use is as a function generator. The 93L09 can generate two functions of three variables. This is useful for implementing random gating functions.

TABLE I — TRUTH TABLE

SELECT INPUTS		INPUTS				OUTPUTS	
S_0	S_1	I_{0a}	I_{1a}	I_{2a}	I_{3a}	Z_a	$\overline{Z}_a$
L	L	L	X	X	X	L	H
L	L	H	X	X	X	H	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	H	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	H	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	H	L
S_0	S_1	I_{0b}	I_{1b}	I_{2b}	I_{3b}	Z_b	$\overline{Z}_b$
L	L	L	X	X	X	L	H
L	L	H	X	X	X	H	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	H	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	H	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	H	L

L = low voltage level
H = high voltage level
X = either high or low logic level

TABLE II — TTμL LOADING RULES

INPUTS	LOADING	
	HIGH	LOW
I_{0a}, I_{1a}, I_{2a}, I_{3a}, I_{0b}, I_{1b}, I_{2b}, I_{3b}, S_0, S_1	0.5 U.L.	0.25 U.L.

OUTPUTS	DRIVE FACTOR	
	HIGH	LOW
Z_a, Z_b	10 U.L.	2.5 U.L.
$\overline{Z}_a$, $\overline{Z}_b$	10 U.L.	2.25 U.L.

Note: 1 Unit Load (U.L.) = 40 μA High/1.6 mA Low

TYPICAL INPUT AND OUTPUT CIRCUITS

INPUT EQUIVALENT CIRCUIT

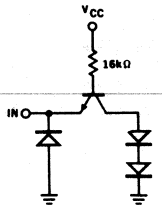


Fig. 5

OUTPUT EQUIVALENT CIRCUIT (Output Low)

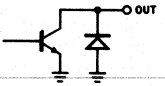


Fig. 6

OUTPUT EQUIVALENT CIRCUIT (Output High)

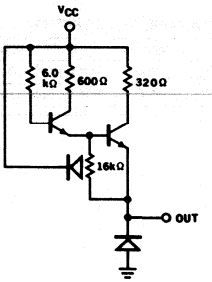


Fig. 7

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (D.C.)	−0.5 V to +5.5 V
*Input Current (D.C.)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output High)	0.5 V to +V_{CC} value
Output Current (D.C.) (Output Low)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC}) MIN.	TYP.	MAX.	TEMPERATURE
U6B/4L93L0951X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
U6B/4L93L0959X	4.75 V	5.0 V	5.25 V	0°C to 75°C

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	CHARACTERISTIC	LIMITS MIN.	TYP.(Note 4)	MAX.	UNITS	CONDITIONS
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = −0.4 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.15	0.3	Volts	V_{CC} = MIN., I_{OL} = 4.0 mA (Pins 1 & 15) I_{OL} = 3.6 mA (Pins 2 & 14) V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{IH}	Input HIGH Level	2.0			Volts	Guaranteed input logical HIGH voltage for all inputs
V_{IL}	Input LOW Level			0.7	Volts	Guaranteed input logical LOW voltage for all inputs
I_{IL}	Input LOW Current		−0.25	−0.4	mA	V_{CC} = MAX., V_{IN} = 0.3 V
I_{IH}	Input HIGH Current		2.0	20	μA	V_{CC} = MAX., V_{IN} = 2.4 V
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{SC}	Output Short Circuit Current	−10	−26	−40	mA	V_{CC} = MAX., V_{OUT} = 0.0 V
I_{CC}	Power Supply Current		7.5	11.5	mA	V_{CC} = MAX.

NOTES:
(1) The actual Testing Procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this Specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California (see page 1 for address and phone).
(2) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
(3) The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
(4) Typical limits are at V_{CC} = 5.0 V, 25°C, and max. loading.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
t_{pd+} (S_0 to Z_e)	Turn Off Delay Input to Output		50		ns	V_{CC} = 5.0 V, C_L = 15 pF
t_{pd-} (S_0 to Z_e)	Turn On Delay Input to Output		45		ns	

APPLICATIONS

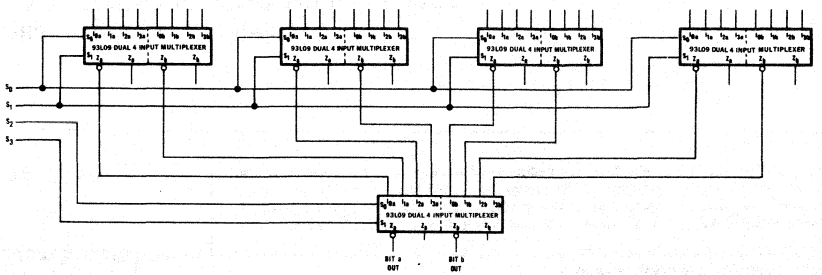


Fig. 5 — MULTIPLEXING TWO BITS FROM SIXTEEN SOURCES

The diagram shows the interconnection of five 93L09 dual four bit multiplexers to provide switching of two bits of data from one of sixteen words onto a two bit data buss. The selection of which word will be transferred to the buss is made by the address supplied to the S_0, S_1, S_2 and S_3 inputs. As an example: if twelve bit words are to be transferred to a twelve bit buss, the above diagram would be repeated six times. Notice that the negative outputs are used at both levels resulting in the assertion output (negation of the negation) at a higher speed due to the fact that the through delay is less on the negation output.

If the word selecting address is held in four TTμL flip flops (two dual packages) enough load capability is available to select between sixteen, sixteen bit words.

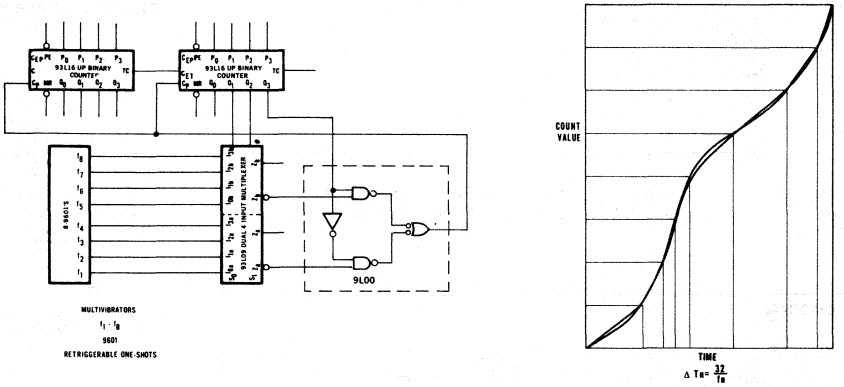


Fig. 6 — NON-LINEAR COUNTER

The rate of the non-linear counter depends on the multivibrator clock frequency selected under control of the three most significant bits of the counter. This makes the count rate a function of both the count value of counter and frequency of clock multivibrator selected.

Clock multiplexing is accomplished by a 93L09 dual 4-input multiplexer and one 9L00 quad gate. Eight line segments representing clock rates of the multivibrators may be adjusted in slope to approximate a non-linear function.

PACKAGE INFORMATION

6B — 16 LEAD DUAL IN-LINE PACKAGE

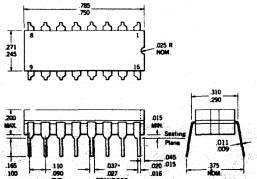


Fig. 7

NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.0 grams
*The .027/.037 dimension does not apply to the corner leads

4L — 16 LEAD (BeO) FLATPAK

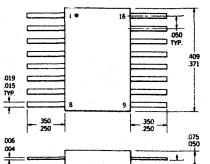


Fig. 8

NOTES:
All dimensions in inches
Leads are gold-plated kovar
Package weight is 0.4 gram

LPTTμL/MSI 93L10

LOW POWER BCD DECADE COUNTER

A FAIRCHILD TTμL® IC PRODUCT

GENERAL DESCRIPTION—The LPTTμL/MSI 93L10 is a medium speed synchronous 8421 BCD decade counter. It is a synchronously presetable, multifunctional MSI building block useful in a large number of counting, digital integration, and conversion applications. Several decades of synchronous operation are obtainable with no external gating packages required through an internal carry look-ahead counting technique.

FEATURES

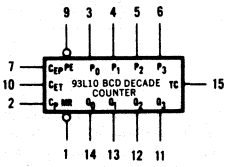
- **SYNCHRONOUS COUNTING AND PARALLEL ENTRY**
- **DECODED TERMINAL COUNT**
- **BUILT-IN CARRY LOOK-AHEAD CIRCUITRY**
- **TYPICAL COUNTING FREQUENCY OF 10 MHz**
- **TYPICAL POWER DISSIPATION OF 85 mW**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED LINE TERMINATION EFFECTS**
- **ALL CERAMIC "HERMETIC" 16-PIN DUAL IN-LINE AND FLAT PACKAGES**
- **TTμL COMPATIBLE**

PIN NAMES

$\overline{PE}$	Parallel Enable (Active Low) Input
P_0, P_1, P_2, P_3	Parallel Inputs
C_{EP}	Count Enable Parallel Input
C_{ET}	Count Enable Trickle Input
C_P	Clock (Active High) Going Edge Input
$\overline{MR}$	Master Reset (Active Low) Input
Q_0, Q_1, Q_2, Q_3	Parallel Outputs
$\overline{TC}$	Terminal Count Output

ORDER INFORMATION — Specify U7B93L10XXX for 16-pin Dual In-Line Package, U4L93L10XXX for 16-pin Flat Package where XXX is 51X for the −55°C to +125°C temperature range, or 59X for the 0°C to 75°C temperature range.

LOGIC SYMBOL



V_{CC} = Pin 16
Gnd = Pin 8

Fig. 1

CONNECTION DIAGRAM
DIP (TOP VIEW)

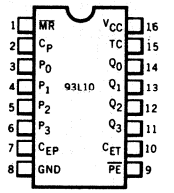


Fig. 2

FLATPAK (TOP VIEW)

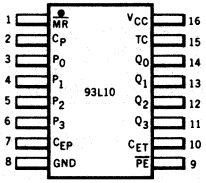


Fig. 3

LOGIC DIAGRAM

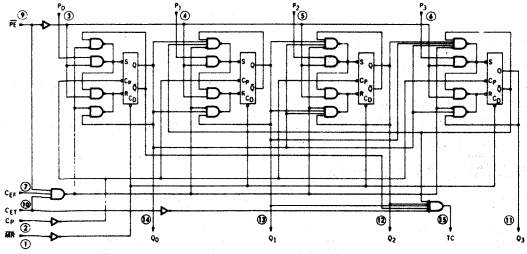


Fig. 4 ○ = PIN NUMBERS V_{CC} = PIN 16 GND = PIN 8

FAIRCHILD SEMICONDUCTOR

FUNCTIONAL DESCRIPTION — The 93L10 is a low power BCD decade counter. The counter is fully synchronous with the clock pulse driving the four master-slave flip-flops in parallel through a clock buffer. During the low to high transition of the clock, the master is inhibited from further change. After the masters are locked out, data is transferred from the master to the slaves and reflected at the outputs. When the clock is high the masters are inhibited and the master-slave data path remains established. During the high to low transition of the clock the slave is inhibited from further change, followed by the enabling of the masters for the acceptance of data from the counting logic or the parallel entry logic.

The three control inputs, Parallel Enable ($\overline{PE}$), Count Enable Parallel (C_{EP}), and Count Enable Trickle (C_{ET}), select the mode of operation as shown in the table. When the conditions for counting are satisfied the rising edge of a clock pulse will change the counter to the next state of the binary sequence shown. The Count Mode is enabled when C_{EP} and C_{ET} inputs are in the high state and $\overline{PE}$ is high.

The 93L10 can be synchronously preset from the four parallel inputs, P_{0-3}, when PE is low. While the parallel enable is low and the clock is low each master of the flip-flops is connected to the appropriate parallel input (P_{0-3}) and the slaves (outputs) are steady in their previous state. When the clock goes high the masters are inhibited and this information is transferred to the slaves and is reflected at the outputs. The parallel enable input overrides both count enable inputs, presetting the counter when low.

Proper logical operation requires that C_P be high during the high-to-low transition of C_{EP} or C_{ET} and the low-to-high transition of $\overline{PE}$. In most applications, this restriction is not a hindrance since logical transitions usually follow the low-to-high transition of the clock pulse, and inputs are steady before C_P goes low. The remaining transitions may be made by following the setup and release times specified under "Switching Characteristics" on the data sheet.

Terminal count is high whenever the counter is at terminal count (state 9) and count enable trickle is high, as is shown in the logic equations. Multistage synchronous counting at high speeds without additional logic is made possible with a high speed lookahead technique utilizing the count enable and terminal count logic. A multistage counter illustrating these techniques is shown and discussed in the application section.

The asynchronous master reset when low overrides all other inputs to reset the four outputs to zero.

LOGIC EQUATIONS

Count Enable = $C_{EP} \bullet C_{ET} \bullet \overline{PE}$

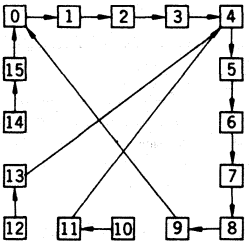
$TC = C_{ET} \bullet Q_0 \bullet \overline{Q}_1 \bullet \overline{Q}_2 \bullet Q_3$

Preset = PE • C_{P^+} (rising clock edge)

Reset = MR

NOTE: PE and MR are active low inputs implying the pins are $\overline{PE}$ and $\overline{MR}$. Therefore Reset = MR implies Pin 1 must be low to reset.

STATE DIAGRAM



NOTE: The 93L10 can be preset to any state, but will not count beyond 9. If preset to state 10, 11, 12, 13, 14, or 15, it will return to its normal sequence within two clock pulses.

MODE SELECTION

$\overline{PE}$	C_{EP}	C_{ET}	MODE
L	L	L	Preset
L	L	H	Preset
L	H	L	Preset
L	H	H	Preset
H	L	L	No Change
H	L	H	No Change
H	H	L	No Change
H	H	H	Count

($\overline{MR}$ = HIGH)
H = HIGH Voltage Level
L = LOW Voltage Level

TTμL LOADING RULES

INPUTS	LOADING	
	HIGH	LOW
C_{EP}, $\overline{MR}$	0.5 U.L.	0.25 U.L.
C_P, $\overline{PE}$, C_{ET}	1.0 U.L.	0.5 U.L.
P_0, P_1, P_2, P_3	0.34 U.L.	0.17 U.L.

OUTPUTS	DRIVE FACTORS	
	HIGH	LOW
Q_0, Q_1, Q_2, Q_3 & TC	8.0 U.L.	2.0 U.L.

Note: 1 Unit Load (U.L.) = 40 μA High/1.6 mA Low

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (D.C.)	−0.5 V to +5.5 V
*Input Current (D.C.)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output High)	−0.5 V to +V_{CC} value
Output Current (D.C.) (Output Low)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC}) MIN.	TYP.	MAX.	TEMPERATURE
U7B/4L93L1051X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
U7B/4L93L1059X	4.75 V	5.0 V	5.25 V	0°C to 75°C

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	CHARACTERISTIC	LIMITS MIN.	TYP. (Note 4)	MAX.	UNITS	CONDITIONS
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = −0.32 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.15	0.3	Volts	V_{CC} = MIN., I_{OL} = 3.2 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{IH}	Input HIGH Level	2.0			Volts	Guaranteed input logical HIGH voltage for all inputs
V_{IL}	Input LOW Level			0.7	Volts	Guaranteed input logical LOW voltage for all inputs
I_{IL}	Input LOW Current $\overline{MR}$, C_{EP} C_P, $\overline{PE}$, C_{ET} P_0, P_1, P_2 & P_3		 −0.25 −0.50 −0.13	 −0.40 −0.80 −0.27	mA	V_{CC} = MAX., V_{IN} = 0.3 V
I_{IH}	Input HIGH Current $\overline{MR}$, C_{EP} C_P, $\overline{PE}$, C_{ET} P_0, P_1, P_2 & P_3		 2.0 4.0 1.0	 20 40 13.3	μA	V_{CC} = MAX., V_{IN} = 2.4 V
	Input HIGH Current			1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{SC}	Output Short Circuit Current	−2.5	−16	−25	mA	V_{CC} = MAX., V_{OUT} = 0.0 V
I_{CC}	Power Supply Current		17	27.5	mA	V_{CC} = MAX.

NOTES:

(1) The actual testing Procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this Specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California (see page 1 for address and phone).

(2) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.

(3) The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

(4) Typical limits are at V_{CC} = 5.0 V, 25°C, and max. loading.

SWITCHING CHARACTERISTICS ($T_A = 25°C$)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS & COMMENTS
t_{pd+} (Q)	Turn-Off Delay		45		ns	$V_{CC} = 5.0$ V, $C_L = 15$ pF (Fig. 5)
t_{pd-} (Q)	Turn-On Delay		45		ns	
t_{pd+} (TC)	Turn-Off Delay for TC		90		ns	
t_{pd-} (TC)	Turn-On Delay for TC		40		ns	
t_s (CE)	Set-Up Time for CE		45		ns	$V_{CC} = 5.0$ V, $C_L = 15$ pF (Fig. 6)
t_r (CE)	Release Time for CE		40		ns	
t_s	Set-Up Time for Data		85		ns	$V_{CC} = 5.0$ V, $C_L = 15$ pF (Fig. 7)
t_r	Release Time for Data		50		ns	
t_s ($\overline{PE}$)	Set-Up Time for PE		75		ns	
t_r ($\overline{PE}$)	Release Time for $\overline{PE}$		55		ns	
t_{pd-} ($\overline{MR}$)	Turn-On Delay for $\overline{MR}$		75		ns	$V_{CC} = 5.0$ V, $C_L = 15$ pF (Fig. 8)
$t_{pd\pm}$	Propagation Delay for C_{ET} to $\overline{TC}$		35		ns	$V_{CC} = 5.0$ V, $C_L = 15$ pF (Fig. 9)

SET-UP TIME: t_s is defined as the minimum time required for the logic level to be present at the logic input prior to the clock transition from low to high in order for the flip-flop(s) to respond.

RELEASE TIME: t_r is defined as the maximum time allowed for the logic level to be present at the logic input prior to the clock transition from low to high in order for the flip-flop(s) not to respond.

SWITCHING TIME WAVEFORMS

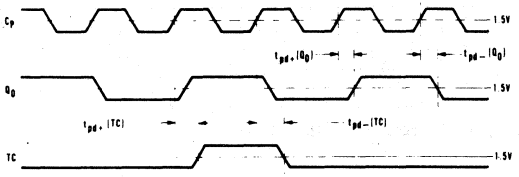


Fig. 5

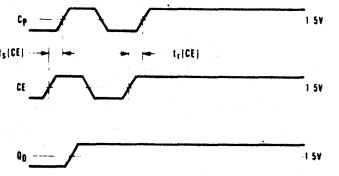


Fig. 6

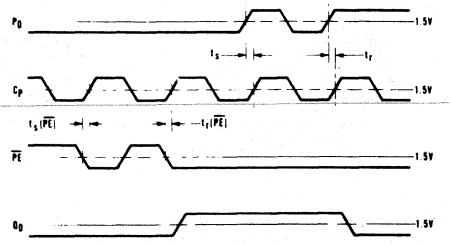


Fig. 8

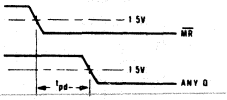


Fig. 7

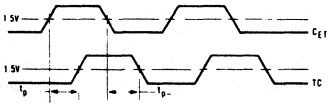


Fig. 9

APPLICATIONS

MULTISTAGE COUNTING

The low power 93L10 decade counters may be cascaded to provide multistage synchronous counting. Two methods commonly used to cascade these counters are shown in Figure 10a and Figure 10b.

In multistage counting, all less significant stages must be at their terminal count before the next more significant counter is enabled. The 93L10 internally decodes the terminal count condition and "ANDs" it with the C_{ET} input to generate the terminal count (TC) output. This arrangement allows one to perform series enabling by connecting the TC output (enable signal) to the C_{ET} input of the following stage, Figure 10a. The setup requires very few interconnections, but has the following drawback: since it takes time for the enable to ripple through the counter stages, there is a reduction in maximum counting speed. To increase the counting rate, it is necessary to decrease the propagation delay of the TC signal, which is done in the second method.

The scheme illustrated in Figure 10b permits multistage counting up to seven stages limited by the fanout of the terminal count. For an alternate scheme for more stages see Application Note 184.

The C_{EP} input of the 93L10 is internally "ANDed" with the C_{ET} input and as a result, both must be high for the counter to be enabled. The C_{ET} inputs are connected as before except for the second stage. There the C_{ET} input is left floating and is therefore high. Also, all C_{EP} inputs are connected to the terminal output of the first stage. The advantage of this method is best seen by assuming all stages except the second and last are in their terminal condition. As the second stage advances to its terminal count, an enable is allowed to trickle down to the last counter stage, but has the full cycle time of the first counter to reach it. Then as the TC of the first stage goes active (high), all C_{EP} inputs are activated, allowing all stages to count on the next clock.

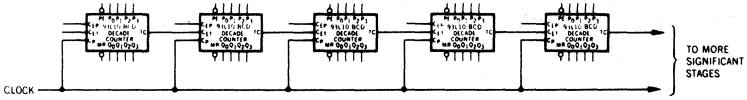


Fig. 10a — MULTISTAGE COUNTER

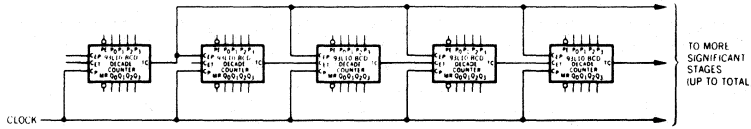
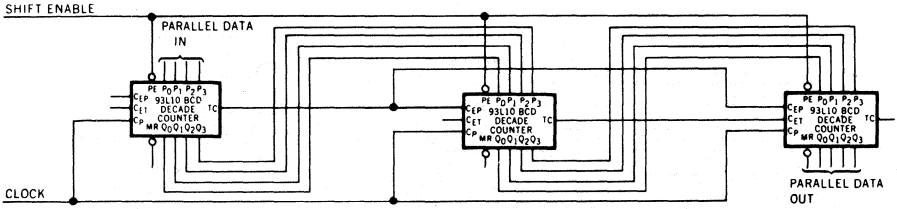


Fig. 10b — SYNCHRONOUS MULTISTAGE COUNTING SCHEME

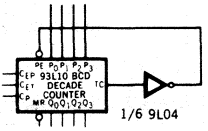


The contents of a 93L10 counter may be shifted out in parallel by decade using the synchronous parallel loading features. When the shift enable is activated (low) the contents of the three decade counters are shifted out in parallel at the outputs of the third decade counter.

Fig. 11 — PARALLEL DECADE SHIFTING SCHEME

APPLICATIONS (Cont'd)

PROGRAMMABLE INPUTS



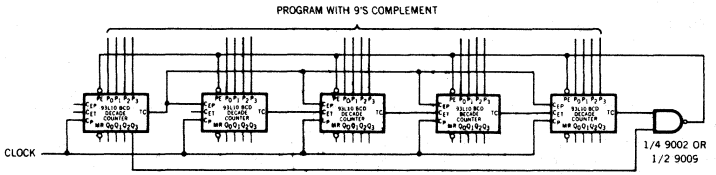
DIVIDE RATIO	INPUT REQUIRED				
		P_0	P_1	P_2	P_3
2	8	L	L	L	H
3	7	H	H	H	L
4	6	L	H	H	L
5	5	H	L	H	L
6	4	L	L	H	L
7	3	H	H	L	L
8	2	L	H	L	L
9	1	H	L	L	L
10	0	L	L	L	L

L = LOW = GROUND
H = HIGH = OPEN OR V_{CC}
(WITH 1 kΩ LIMITING RES.)

PROGRAMMABLE DIVIDER

Although the 93L10 is a modulo 10 counter, the addition of a single inverter allows the counter to be used as a synchronous programmable counter with modules of 2 to 10.

FIG. 12



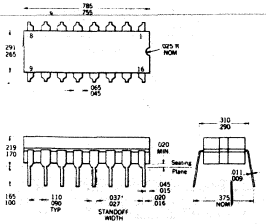
MULTI-STAGE SYNCHRONOUS PROGRAMMABLE DECIMAL COUNTER

A multi-stage synchronous programmable decimal counter is easily implemented by decoding the terminal state of a synchronous counter and utilizing it as a preset signal. In this case, a straight nine's complement is used and the terminal count is decoded one count short of all nine's.

Fig. 13

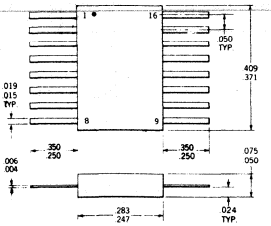
PACKAGE INFORMATION

7B — 16 LEAD DUAL IN-LINE PACKAGE



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.2 grams
*The .027/.037 dimension does not apply to the corner leads

4L—16 LEAD BeO FLATPAK



NOTES:
All dimensions in inches
Leads are gold-plated kovar
Package weight is 0.4 gram

LPTTμL/MSI 93L11

LOW POWER ONE-OF-SIXTEEN DECODER

A FAIRCHILD TTμL® IC PRODUCT

GENERAL DESCRIPTION — The LPTTμL/MSI 93L11 is a multi-purpose decoder designed to accept four inputs and provide 16 mutually exclusive outputs. The circuit uses TTμL technology and is compatible with the Fairchild TTμL family.

FEATURES:

- **MULTI-FUNCTION CAPABILITY**
- **MUTUALLY EXCLUSIVE OUTPUTS**
- **HIGH CAPACITIVE DRIVE CAPABILITY**
- **DEMULTIPLEXING CAPABILITY**
- **TWO INPUT ENABLE GATE**
- **TYPICAL PROPAGATION DELAY OF 70 ns**
- **TYPICAL POWER DISSIPATION OF 58 mW**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **ALL CERAMIC "HERMETIC" 24-PIN DUAL IN-LINE AND FLAT PACKAGES**
- **TTμL COMPATIBLE**

PIN NAMES

A_0, A_1, A_2, A_3	Address Inputs
$\overline{E}_0$, $\overline{E}_1$	AND Enable (Active Low) Inputs
$\overline{0}$ to $\overline{15}$	(Active Low) Outputs

ORDER INFORMATION

Specify U6N93L11XXX for 24-pin Dual In-Line package or U4M93L11XXX for 24-pin Flat Package where XXX is 51X for the −55°C to +125°C temperature range, or 59X for the 0°C to +75°C temperature range.

LOGIC DIAGRAM

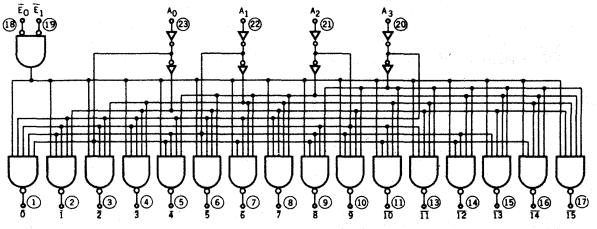


Fig. 4

LOGIC SYMBOL

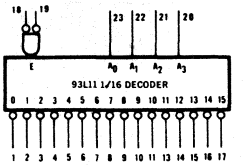


Fig. 1

CONNECTION DIAGRAM

DIP (TOP VIEW)

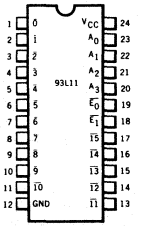


Fig. 2

FLATPAK (TOP VIEW)

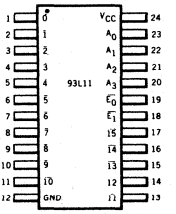


Fig. 3

FAIRCHILD SEMICONDUCTOR

FUNCTIONAL DESCRIPTION — The 93L11 decoder accepts four active high binary inputs and provides 16 mutually exclusive active low outputs, as shown by Figure 1. The active low outputs facilitate memory addressing when inverting drivers are used between decoder and memory elements such as the 9033.

The 93L11 can demultiplex data by routing it from one input to one of sixteen possible decoder outputs. The desired output is addressed and the data is applied to one of the enable inputs. Providing that the other enable is low, the addressed output will follow the state of the applied data.

The Truth Table and Loading Rules for the 93L11 are shown in Table I and Table II.

TABLE I — TRUTH TABLE.

$\bar{E}_0$	$\bar{E}_1$	A_0	A_1	A_2	A_3	$\bar{0}$	$\bar{1}$	$\bar{2}$	$\bar{3}$	$\bar{4}$	$\bar{5}$	$\bar{6}$	$\bar{7}$	$\bar{8}$	$\bar{9}$	$\bar{10}$	$\bar{11}$	$\bar{12}$	$\bar{13}$	$\bar{14}$	$\bar{15}$
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L

H = High Voltage Level
L = Low Voltage Level
X = Level Does Not Affect Output

TABLE II
TTμL LOADING RULES

INPUTS	LOADING	
	High	Low
All Inputs	0.5 U.L.	0.25 U.L.

OUTPUTS	DRIVE FACTOR	
	High	Low
All Outputs	10 U.L.	2.5 U.L.

Note: 1 Unit Load (U.L.) = 40 μA High/1.6 mA Low

TYPICAL INPUT AND OUTPUT CIRCUITS

INPUTS
EQUIVALENT CIRCUIT

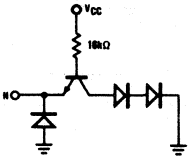


Fig. 5

OUTPUTS
EQUIVALENT CIRCUIT

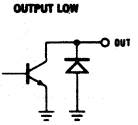


Fig. 6

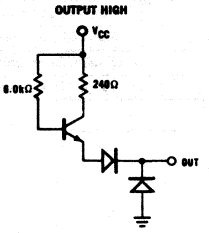


Fig. 7

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (D.C.)	−0.5 V to +5.5 V
*Input Current (D.C.)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output High)	0.5 V to +V_{CC} value
Output Current (D.C.) (Output Low)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC}) MIN.	TYP.	MAX.	TEMPERATURE
U6N/4M93L1151X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
U6N/4M93L1159X	4.75 V	5.0 V	5.25 V	0°C to 75°C

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	CHARACTERISTIC	LIMITS MIN.	TYP. (Note 4)	MAX.	UNITS	CONDITIONS
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = −0.4 V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.15	0.3	Volts	V_{CC} = MIN., I_{OL} = 4.0 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{IH}	Input HIGH Level	2.0			Volts	Guaranteed input logical HIGH voltage for all inputs
V_{IL}	Input LOW Level			0.7	Volts	Guaranteed input logical LOW voltage for all inputs
I_{IL}	Input LOW Current		−0.25	−0.4	mA	V_{CC} = MAX., V_{IN} = 0.3 V
I_{IH}	Input HIGH Current		2.0	20	μA	V_{CC} = MAX., V_{IN} = 2.4 V
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{SC}	Output Short Circuit Current	−2.5	−16	−25	mA	V_{CC} = MAX., V_{OUT} = 0.0 V
I_{CC}	Power Supply Current		11.5	16.5	mA	V_{CC} = MAX.

NOTES:
(1) The actual Testing Procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this Specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California (see page 1 for address and phone).
(2) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
(3) The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
(4) Typical limits are at V_{CC} = 5.0 V, 25°C, and max. loading.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	CHARACTERISTIC	LIMITS MIN.	TYP.	MAX.	UNITS	CONDITIONS
t_{pd+}	Turn Off Delay A Input to Output		75		ns	V_{CC} = 5.0 V C_L = 15 pF See Fig. 8
t_{pd-}	Turn On Delay A Input to Output		65		ns	
t_{pd+}	Turn Off Delay E Input to Output		45		ns	
t_{pd-}	Turn On Delay E Input to Output		50		ns	

SWITCHING TIME WAVEFORMS

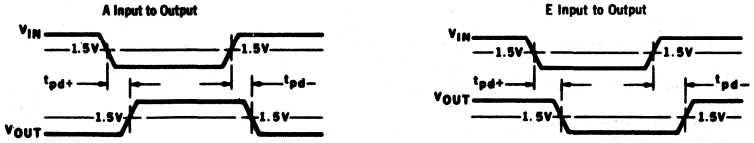
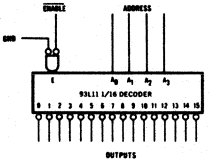


Fig. 8

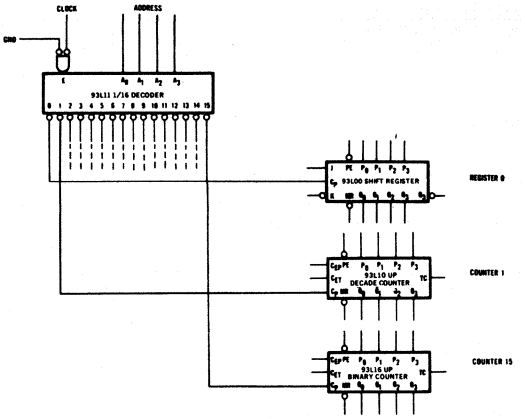
APPLICATIONS



DECIMAL DIGIT	OUTPUT SELECTION BCD CODE 8421	5421	EXCESS 3	GRAY
0	0	0	3	0
1	1	1	4	1
2	2	2	5	3
3	3	3	6	2
4	4	4	7	6
5	5	8	8	7
6	6	9	9	5
7	7	10	10	4
8	8	11	11	12
9	9	12	12	13

Decode any BCD code using a 93L11 element. Any 4 bit BCD code may be decoded by selecting outputs, examples are shown in the table.

Fig. 9 — DECODE ANY BCD CODE

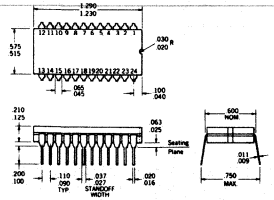


The 93L11 can be used as a clock demultiplexer. The binary address designates to which register or counter the clock is sent. Any sequential circuit in the LPTTμL/MSI family can be used in this configuration.

Fig. 10 — CLOCK DEMULTIPLEXING

PACKAGE INFORMATION

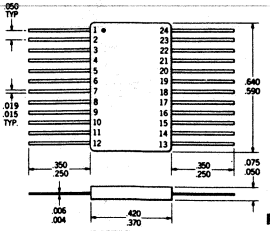
6N — 24 LEAD DUAL IN-LINE PACKAGE



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .600" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Leads are tin-plated kovar
Package weight is 6.5 grams

Fig. 11

4M — 24 LEAD (BeO) FLATPAK



NOTES:
All dimensions in inches
Leads are gold-plated kovar
Package weight is 0.8 gram

Fig. 12

LPTTμL/MSI 93L12

LOW POWER EIGHT-INPUT MULTIPLEXER

A FAIRCHILD TTμL® IC PRODUCT

GENERAL DESCRIPTION — The LPTTμL/MSI 93L12 is a monolithic, medium speed, eight input digital multiplexer circuit. It provides in one package the ability to select one bit of data from up to eight sources. The 93L12 can be used as a universal function generator to generate any logic function of four variables. Both assertion and negation outputs are provided. TTμL circuitry with active pullups on the outputs provides high speed, high fanout operation and is compatible with the Fairchild TTμL family.

FEATURES

- **MULTIFUNCTION CAPABILITY**
- **ON-CHIP SELECT LOGIC DECODING**
- **FULLY BUFFERED COMPLEMENTARY OUTPUTS**
- **TYPICAL PROPAGATION DELAY OF 80 ns**
- **TYPICAL POWER DISSIPATION OF 45 mW**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS.**
- **ALL CERAMIC "HERMETIC" 16 PIN DUAL IN-LINE AND FLAT PACKAGES**
- **TTμL COMPATIBLE**

PIN NAMES

S_0, S_1, S_2	Select Inputs
$\overline{E}$	Enable (Active Low) Input
I_0 to I_7	Multiplexer Inputs
Z	Multiplexer Output
$\overline{Z}$	Complementary Multiplexer Output

ORDER INFORMATION — Specify U7B93L12XXX for 16 pin Dual In-Line Package or U4L93L12XXX for 16 pin Flatpak, where XXX is 51X for the −55°C to +125°C temperature range, or 59X for the 0°C to +75°C temperature range.

LOGIC DIAGRAM

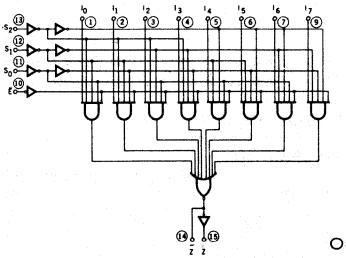


Fig. 4

LOGIC SYMBOL

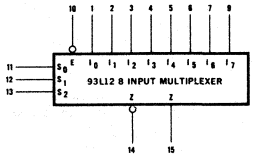


Fig. 1

CONNECTION DIAGRAM
DIP (TOP VIEW)

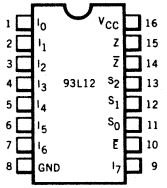


Fig. 2

FLATPAK (TOP VIEW)

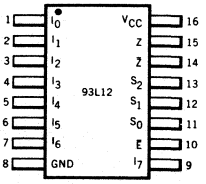


Fig. 3

FAIRCHILD
SEMICONDUCTOR

FUNCTIONAL DESCRIPTION — The 93L12 is a logical implementation of a single pole - 8 position switch with the switch position controlled by the state of three select inputs, S_0, S_1, S_2. Both assertion and negation outputs are provided. The enable input ($\overline{E}$) is active low. When it is not activated the negation output is high and the assertion output is low regardless of all other inputs. The logic function provided at the output is:

$$Z = E \cdot (I_0 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot \overline{S}_2 + I_1 \cdot S_0 \cdot \overline{S}_1 \cdot \overline{S}_2 + I_2 \cdot \overline{S}_0 \cdot S_1 \cdot \overline{S}_2 + I_3 \cdot S_0 \cdot S_1 \cdot \overline{S}_2 + I_4 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot S_2 + I_5 \cdot S_0 \cdot \overline{S}_1 \cdot S_2 + I_6 \cdot \overline{S}_0 \cdot S_1 \cdot S_2 + I_7 \cdot S_0 \cdot S_1 \cdot S_2).$$

The 93L12 provides the ability, in one package, to select from eight sources of data or control information. By proper manipulation of the inputs, the 93L12 can provide any logic function of four variables and its negation.

TABLE I TRUTH TABLE

$\overline{E}$	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	$\overline{Z}$	Z
H	X	X	X	X	X	X	X	X	X	X	X	H	L
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

H = High voltage level
L = Low voltage level
X = Level does not affect output

TABLE II
TTμL LOADING RULES

INPUTS	LOADING	
	HIGH	LOW
All Inputs	0.5 U.L.	0.25 U.L.

OUTPUTS	DRIVE FACTOR	
	High State	Low State
$\overline{Z}$	10 U.L.	2.25 U.L.
Z	10 U.L.	2.5 U.L.

Note: 1 Unit Load (U.L.) = 40 μA High/1.6 mA Low

TYPICAL INPUT AND OUTPUT CIRCUITS

INPUTS
EQUIVALENT CIRCUIT

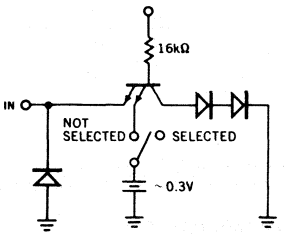


Fig. 5

OUTPUTS
EQUIVALENT CIRCUIT

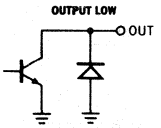


Fig. 6

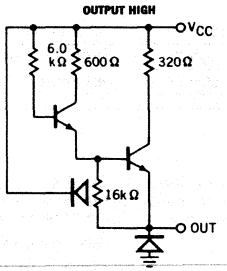


Fig. 7

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (D.C.)	−0.5 V to +5.5 V
*Input Current (D.C.)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output High)	0.5 V to +V_{CC} value
Output Current (D.C.) (Output Low)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC}) MIN.	TYP.	MAX.	TEMPERATURE
U7B/4L93L1251X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
U7B/4L93L1259X	4.75 V	5.0 V	5.25 V	0°C to 75°C

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	CHARACTERISTIC	LIMITS MIN.	TYP. (Note 4)	MAX.	UNITS	CONDITIONS
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = − 0.4 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.15	0.3	Volts	V_{CC} = MIN., I_{OL} = 4.0 mA (Pin 15) 3.6 mA (Pin 14) V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{IH}	Input HIGH Level	2.0			Volts	Guaranteed input logical HIGH voltage for all inputs
V_{IL}	Input LOW Level			0.7	Volts	Guaranteed input logical LOW voltage for all inputs
I_{IL}	Input LOW Current		−0.25	−0.4	mA	V_{CC} = MAX., V_{IN} = 0.3 V
I_{IH}	Input HIGH Current		2.0	20	μA	V_{CC} = MAX., V_{IN} = 2.4 V
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{SC}	Output Short Circuit Current	−10	−22	−40	mA	V_{CC} = MAX., V_{OUT} = 0.0 V
I_{CC}	Power Supply Current		9.0	13.3	mA	V_{CC} = MAX.

NOTES:
(1) The actual Testing Procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this Specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California (see page 1 for address and phone).
(2) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
(3) The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
(4) Typical limits are at V_{CC} = 5.0 V, 25°C, and max. loading.

SWITCHING CHARACTERISTICS (T_A = 25°C)

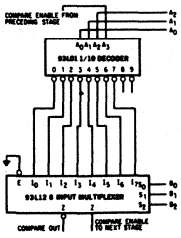
SYMBOL	CHARACTERISTIC	LIMITS MIN.	TYP.	MAX.	UNITS	CONDITIONS
t_{pd+} (S_0 to Z)	Turn Off Delay Input to Output		80		ns	V_{CC} = 5.0 V C_L = 15 pF
t_{pd-} (S_0 to Z)	Turn On Delay Input to Output		80		ns	

APPLICATIONS

3 BIT COMPARATOR

Three bits of data to be compared are supplied to the address and select inputs of the 93L01 and 93L12 respectively. If A_0, A_1, A_2, and B_0, B_1, B_2 compare, the mutually exclusive active low output of the 93L01 1/10 decoder and the selected input of the 93L12 multiplexer will be coincidental and COMPARE OUT will be high. The COMPARE ENABLE must be low to permit compare operation.

3 BIT COMPARATOR



INTERCONNECTION DIAGRAM FOR 9 BITS

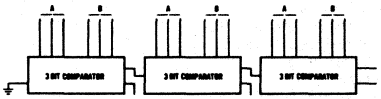


Fig. 8

IMPLEMENTING ANY FOUR-VARIABLE BOOLEAN FUNCTION

The 93L12 eight input multiplexer can (in addition to performing its nominal function) produce any Boolean function of four variables without any additional elements if both the assertion and negation of one of the variables are present. If an assertion and negation are not present, one inverter may be required.

The procedure for implementing a four-variable function, along with an example, is shown in the attached diagram. First, consider the function in terms of a Karnaugh map. If the Q_0, Q_1 and Q_2 variable are connected to the S_0, S_1 and S_2 inputs of the 93L12 then the Karnaugh map will be split, as shown, into eight sections, with each section corresponding to an input to the 93L12. In order to implement the function each input of the 93L12 is connected to one of the following four signals: ground, V_{CC}, the assertion, or negation of the fourth variable.

The contents of the two squares associated with an input, on the Karnaugh map, determine which connection is made to that input. If both squares contain a zero, ground should be connected to the input; if both squares contain a one, the input should be connected to V_{CC}. If the two squares contain a one and a zero then either the assertion or negation of the fourth variable will be required to implement the function. If the single one is located in the square associated with the assertion of the fourth variable then the assertion of the assertion of the fourth variable is connected to that input, and vice versa.

Shown in the illustration below is a 93L12 decoding the condition of a 93L00, producing a one output whenever the register contains two or more transitions. The truth table, Karnaugh map and the connection to the 93L12 for this function are also shown in the illustration.

In many applications, using the 93L12 to implement general logic functions of four variables will result in a sizeable reduction in package count. In many cases use of the 93L12 with additional gates to produce functions of more than four variables will also reduce the package count.

The concept of using the 93L12 eight input-multiplexer as a general logic function generator is described by S. S. Yau and C. K. Tang of Northwestern University in a paper presented at the 1968 Spring Joint Computer Conference in Atlantic City, New Jersey.

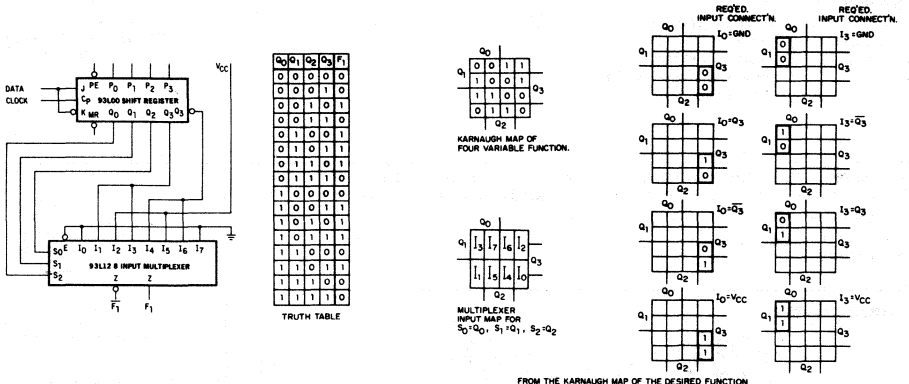
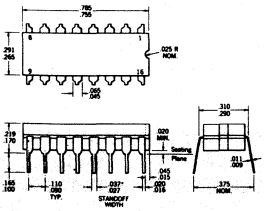


Fig. 9

PACKAGE INFORMATION

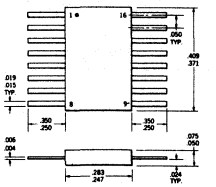
7B — 16 LEAD DUAL IN-LINE PACKAGE



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.2 grams
*The .027/.037 dimension does not apply to the corner leads

Fig. 10

4L — 16 LEAD (BeO) FLATPAK



NOTES:
All dimensions in inches
Leads are gold-plated kovar
Package weight is 0.4 gram

Fig. 11

LPTTμL/MSI 93L14
LOW POWER QUAD LATCH
A FAIRCHILD TTμL® IC PRODUCT

GENERAL DESCRIPTION — The LPTTμL/MSI 93L14 is a multifunctional 4-Bit Latch. The latch is designed for general purpose storage applications in high speed digital systems. The 93L14 uses TTμL technology and is compatible with the Fairchild TTμL family. All inputs feature diode clamping to reduce negative line transients. All outputs have active pull-up circuitry to provide low impedance in both logic states for good A.C. noise immunity.

FEATURES

- **CAN BE USED AS SINGLE INPUT D LATCHES OR SET/RESET LATCHES**
- **ACTIVE LEVEL LOW ENABLE GATE INPUT**
- **OVERRIDING MASTER RESET**
- **TYPICAL PROPAGATION DELAY OF 68 ns**
- **TYPICAL POWER DISSIPATION OF 50 mW**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **ALL CERAMIC "HERMETIC" 16 PIN DUAL IN-LINE AND FLAT PACKAGES**
- **TTμL COMPATIBLE**

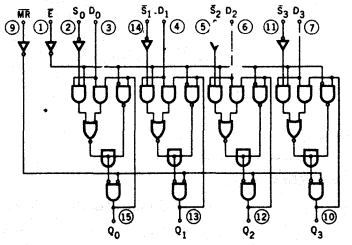
PIN NAMES

$\overline{E}$	(Active Low) Enable Input
D_0, D_1, D_2, D_3	Data Inputs
$\overline{S}_0, \overline{S}_1, \overline{S}_2, \overline{S}_3$	Set (Active Low) Inputs
$\overline{MR}$	Master Reset (Active Low) Input
Q_0, Q_1, Q_2, Q_3	Latch Outputs

ORDER INFORMATION — Specify U7B93L14XXX for 16-pin Dual In-Line package or U4L93L14XXX for 16-pin Flatpak, where XXX is 51X for the −55°C to +125°C temperature range, or 59X for the 0°C to +75°C temperature range.

Electrical Characteristics on Page 3
Notes on Page 3

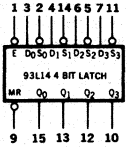
LOGIC DIAGRAM



V_{CC} = PIN 16
GND = PIN 8
○ = PIN NUMBERS

Fig. 4

LOGIC SYMBOL



V_{CC} = Pin 16
Gnd = Pin 8

Fig. 1

CONNECTION DIAGRAM
DIP (TOP VIEW)

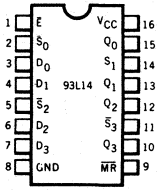


Fig. 2

FLATPAK (TOP VIEW)

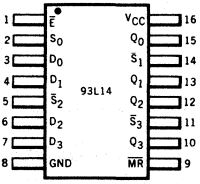


Fig. 3

FAIRCHILD
SEMICONDUCTOR

FUNCTIONAL DESCRIPTION

LATCH OPERATION — The 93L14 consists of four latches with a common active low enable and active low master reset. When the common enable goes high, data present in the latches is stored and the state of a latch is no longer affected by the $\overline{S}$ and D inputs. The master reset when activated overrides all other input conditions forcing all latch outputs low.

Each of the four latches can be operated in one of two modes:

D TYPE LATCH — For D type operation the $\overline{S}$ input of a latch is held low. While the common enable is active the latch output follows the D input. Information presetit at the latch output is stored in the latch when the enable goes high.

SET/RESET LATCH — During set/reset operation when the common enable is low a latch is reset by a low on the D input, and can be set by a low on the $\overline{S}$ input if the D input is high. If both $\overline{S}$ and D inputs are low, the D input will dominate and the latch will be reset. When the enable goes high, the latch remains in the last state prior to disablement.

The two modes of operation of the 93L14 latches are shown in the Truth Table below.

TABLE I — TRUTH TABLE

$\overline{MR}$	$\overline{E}$	D	$\overline{S}$	Q_N	OPERATION
H	L	L	L	L	D MODE
H	L	H	L	H	
H	H	X	X	Q_{N-1}	
H	L	L	L	L	R/S MODE
H	L	H	L	H	
H	L	L	H	L	
H	L	H	H	Q_{N-1}	
H	H	X	X	Q_{N-1}	
L	X	X	X	L	RESET

X = Don't Care
L = Low Voltage Level
H = High Voltage Level
Q_{N-1} = Previous Output State
Q_N = Present Output State

TABLE II — TTμL LOADING RULES

INPUTS	LOADING	
	High	Low
D_0, D_1, D_2, D_3	.75 UL	.375 UL
$\overline{MR}$, $\overline{E}$, $\overline{S}_0$, $\overline{S}_1$, $\overline{S}_2$, $\overline{S}_3$	.5 UL	.25 UL

OUTPUTS	DRIVE FACTORS	
	High	Low
Q_0, Q_1, Q_2, Q_3	10 UL	2.25 UL

Note: 1 Unit Load (U.L.) = 40 μA High/1.6 mA Low

TYPICAL INPUT AND OUTPUT CIRCUITS

INPUTS
EQUIVALENT CIRCUIT

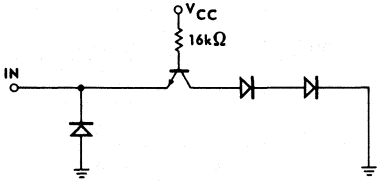


Fig. 5

OUTPUTS
EQUIVALENT CIRCUIT

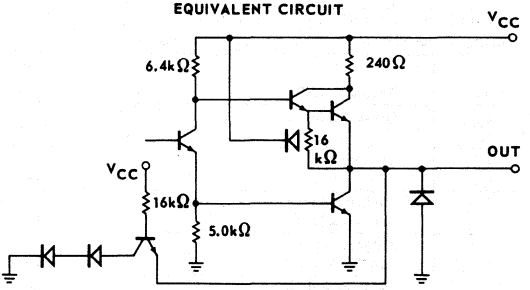


Fig. 6

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (D.C.)	−0.5 V to +5.5 V
*Input Current (D.C.)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output High)	0.5 V to +V_{CC} value
Output Current (D.C.) (Output Low)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC}) MIN.	TYP.	MAX.	TEMPERATURE
U7B/4L93L1451X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
U7B/4L93L1459X	4.75 V	5.0 V	5.25 V	0°C to 75°C

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	CHARACTERISTIC	LIMITS MIN.	TYP. (Note 5)	MAX.	UNITS	CONDITIONS
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = −0.4 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.15	0.3	Volts	V_{CC} = MIN., I_{OL} = 3.6 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{IH}	Input HIGH Level	2.0			Volts	Guaranteed input logical HIGH voltage for all inputs
V_{IL}	Input LOW Level			0.7	Volts	Guaranteed input logical LOW voltage for all inputs
I_{IL}	Input LOW Current $\overline{S}$, $\overline{E}$ & $\overline{MR}$		−0.25	−0.4	mA	V_{CC} = MAX., V_{IN} = 0.3 V
	Input LOW Current D Inputs		−0.38	−0.64	mA	V_{CC} = MAX., V_{IN} = 0.0 V (See Note 4)
I_{IH}	Input HIGH Current $\overline{S}$, $\overline{E}$ & $\overline{MR}$ D Inputs		2.0 3.0	20 30	μA	V_{CC} = MAX., V_{IN} = 2.4 V
	Input HIGH Current			1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{SC}	Output Short Circuit Current	−10	−22	−40	mA	V_{CC} = MAX., V_{OUT} = 0.0 V
I_{CC}	Power Supply Current		10	16.5	mA	V_{CC} = MAX., all outputs LOW, inputs disabled

NOTES:

(1) The actual Testing Procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this Specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California (see page 1 for address and phone).

(2) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.

(3) The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

(4) This current is measured at V_{IN} = 0.0 V to insure that no current is being absorbed by the device internally. The maximum value given guarantees that the maximum instantaneous current that can flow out of the input at V_{IN} = 0.3 V is 0.6 mA.

(5) Typical limits are at V_{CC} = 5.0 V, 25°C, and max. loading.

SWITCHING CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 Volts, Pin 8 = Gnd)

SYMBOL	CHARACTERISTIC	LIMITS MIN.	TYP.	MAX.	UNITS	CONDITIONS
t_{pd+} t_{pd-}	Enable to Output		70 63		ns	See Figure 7
t_{pd+} t_{pd-}	Data to Output		45 70		ns	See Figure 8
t_s "L" t_r "L"	Low Data to Enable Low Data to Enable		50 41		ns	See Figure 9
t_s "H" t_r "H"	High Data to Enable High Data to Enable		10 3.0		ns	See Figure 10
t_{PW}	Enable Pulse Width		50		ns	See Figure 11
t_{PW}	Master Reset Pulse Width		30		ns	See Figure 12
t_{pd-}	Master Reset to Output		35		ns	See Figure 12
t_{rec}	Master Reset Recovery Time		40		ns	See Figure 13
t_{pd+}	Set Enable to Output		60		ns	See Figure 14
t_s "H" t_r "H"	High Data to Set Enable High Data to Set Enable		12 3.0		ns	See Figure 14

SET UP TIME: t_s is defined as the time required for the logic level to be present at the Data Input prior to the enable transition from Low to High in order for the latch to recognize and store the new data.

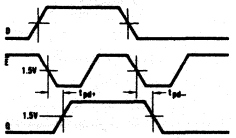
RELEASE TIME: t_r is defined as the time allowed for a new logic level to be present at the data input prior to the enable transition from low to high in order for the latch not to respond to that new input logic level. A negative release time means the new logic level must not occur until after the enable transition.

RECOVERY TIME: t_{rec} is defined as the time that the Enable must remain Low after the Master Reset transition from Low to High in order for the latch to recognize and store High data.

TYPICAL SWITCHING CHARACTERISTICS

All delays are measured with V_{CC} = 5.0 V applied to Pin 16 and Pin 8 grounded. The active input is driven by a 9002 TTμL or equivalent gate with the output loaded with 15 pF (includes jig and probe). Outputs under test are loaded with 15 pF (includes jig and probe). Pins not reference are not connected.

Fig. 7—t_{pd} (ENABLE TO OUTPUT)



Other Conditions: $\bar{S}$ = Gnd

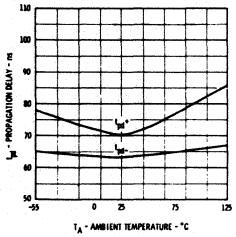
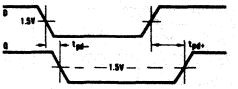


Fig. 8—t_{pd} (DATA TO OUTPUT)



Other Conditions: $\bar{E}$ = Gnd, $\bar{S}$ = Gnd

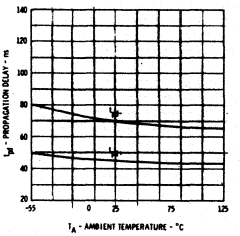
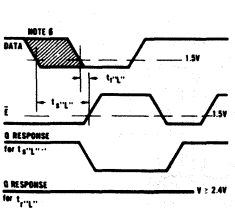


Fig. 9 — t_s "L" t_r "L" (Data to Enable)



Other Conditions: $\bar{S}$ = Gnd

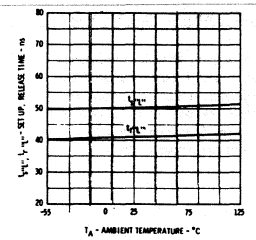
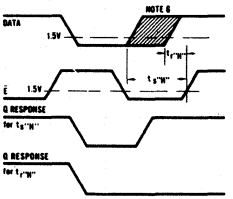


Fig. 10 — t_s "H" t_r "H" (Data to Enable)



Other Conditions: $\bar{S}$ = Gnd

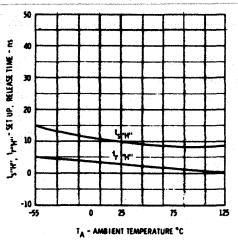
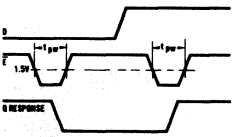
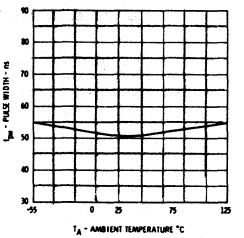


Fig. 11 — t_{PW} (ENABLE PULSE WIDTH)

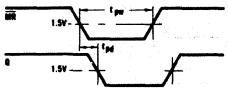


Other Condition: $\bar{S}$ = Gnd



TYPICAL SWITCHING CHARACTERISTICS (cont'd)

Fig. 12 — t_{pW} (MASTER RESET PULSE WIDTH) t_{pd-} (MASTER RESET TO OUTPUT)



Other Conditions: $\overline{S}$ =Gnd
$\overline{E}$ = Gnd

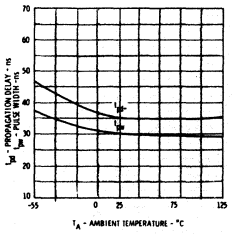
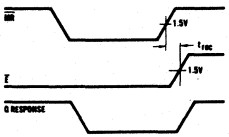


Fig. 13 — t_{rec} (MASTER RESET RECOVERY TIME)



Other Conditions: $\overline{S}$ = Gnd, D = Open

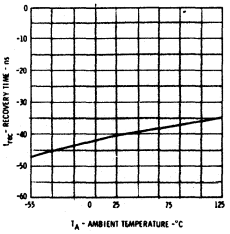
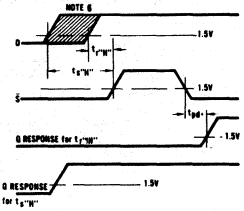
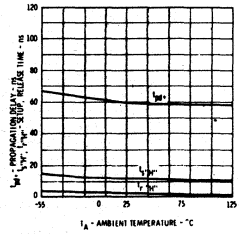


Fig. 14 — t_{pd+} (SET ENABLE TO OUTPUT) t_s "H" t_r "H" (Data to Set Enable)



Other Conditions: $\overline{E}$ = Gnd



NOTE: (6) If data changes during the shaded time, the state of the output cannot be pre-determined.

APPLICATIONS

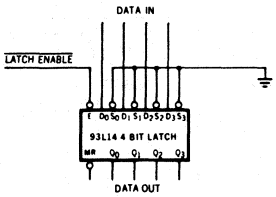


Fig. 15—4 BIT STORAGE LATCH

The figure illustrates the use of the 93L14 as a D type storage latch. Data is stored in the latch when the enable line is high.

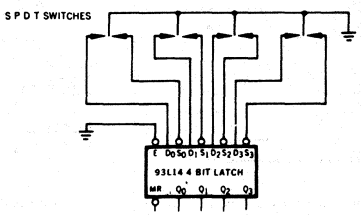


Fig. 16—CONTACT BOUNCE ELIMINATOR

The 93L14 can be used to eliminate mechanical switch bounce for a single pole double throw switch. The latch operation is that of an active low input set/reset latch. The pole of the switch is low so that when in the S position, the output is high, in the D position the output is low.

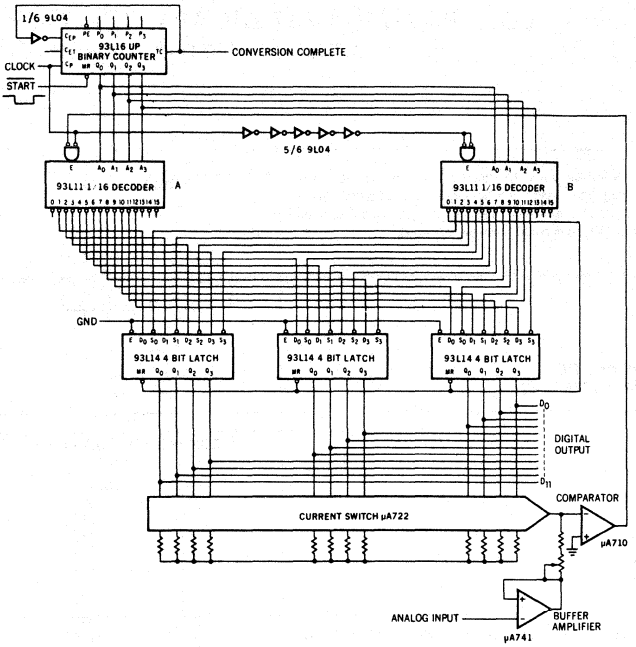


Fig. 17—ANALOG TO DIGITAL CONVERSION

The figure illustrates a 12 bit high speed successive approximation A/D Converter using the 93L14 Quad Latch. Conversion is actually completed in 13 clock periods, but for convenience a 16-clock conversion is used.

At time period "0", decoder B (during the time the input clock is high) resets all stages of the 12-bit register that drive the current switches feeding to the resistance ladder network. At time period 1, output "1" from decoder B sets the first latch, which contains the most significant bit in the register. The comparator then decides whether this binary value is greater or less than its analog equivalent. If it is greater, the comparator resets that latch via decoder A when the clock is low. In this manner the various stages in the holding register are set and reset, or left set until conversion is complete after 13 clock periods. The counter then continues until the terminal count is reached, whereupon an inverter in a feedback path inhibits further counting until another conversion is required.

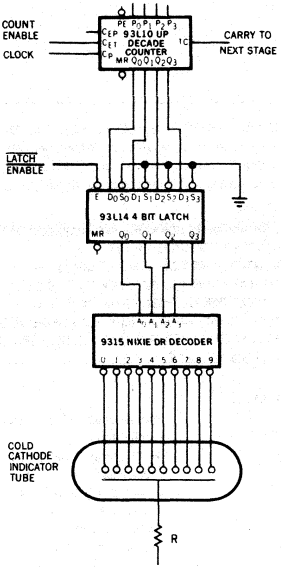
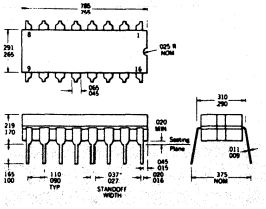


Fig. 18—COUNTING AND HOLDING DISPLAY SYSTEM

The figure illustrates the use of the 93L14 as a D type storage latch used with the 93L10 (decade counter) and the 9315 (one-of-ten decoder/driver). Data is stored when the enable line is high.

PACKAGE INFORMATION

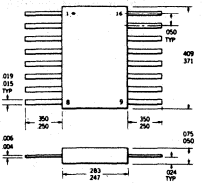
7B — 16 LEAD DUAL IN-LINE PACKAGE



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.2 grams
*The .027/.037 dimension does not apply to the corner leads

Fig. 19

4L — 16 LEAD (BeO) FLATPAK



NOTES:
All dimensions in inches
Leads are gold-plated kovar
Package weight is 0.4 gram

Fig. 20

LPTTμL/MSI 93L16
LOW POWER 4-BIT BINARY COUNTER
A FAIRCHILD TTμL® IC PRODUCT

GENERAL DESCRIPTION — The LPTTμL/MSI 93L16 is a medium speed synchronous 4-bit binary counter. It is a synchronously presetable, multifunctional MSI building block useful in a large number of counting, digital integration, and conversion applications. Several stages of synchronous operation are obtainable with no external gating packages required through an internal carry look-ahead counting technique.

FEATURES

- **SYNCHRONOUS COUNTING AND PARALLEL ENTRY**
- **DECODED TERMINAL COUNT**
- **BUILT-IN CARRY LOOK-AHEAD CIRCUITRY**
- **TYPICAL COUNTING FREQUENCY OF 10 MHz**
- **TYPICAL POWER DISSIPATION OF 85 mW**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **ALL CERAMIC "HERMETIC" 16-PIN DUAL IN-LINE AND FLAT PACKAGES**
- **TTμL COMPATIBLE**

PIN NAMES

$\overline{PE}$	Parallel Enable (Active Low) Input
P_0, P_1, P_2, P_3	Parallel Inputs
C_{EP}	Count Enable Parallel Input
C_{ET}	Count Enable Trickle Input
C_P	Clock (Active High) Going Edge Input
$\overline{MR}$	Master Reset (Active Low) Input
Q_0, Q_1, Q_2, Q_3	Parallel Outputs
TC	Terminal Count Output

ORDER INFORMATION — Specify U7B93L16XXX for 16-pin Dual In-Line Package, U4L93L16XXX for 16-pin Flat Package where XXX is 51X for the −55°C to +125°C temperature range, or 59X for the 0°C to 75°C temperature range.

LOGIC DIAGRAM

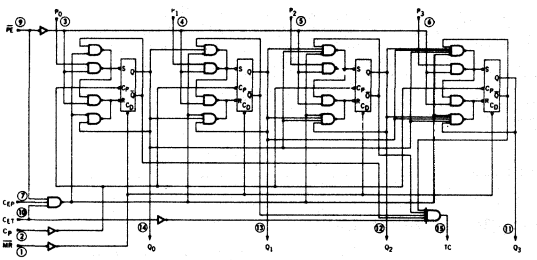
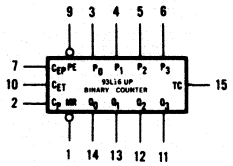


Fig. 4 ○ = PIN NUMBERS V_{CC} = PIN 16 GND = PIN 8

LOGIC SYMBOL



V_{CC} = Pin 16
Gnd = Pin 8

FIG. 1

CONNECTION DIAGRAM
DIP (TOP VIEW)

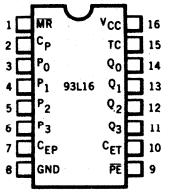


FIG. 2

FLATPAK (TOP VIEW)

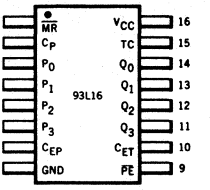


FIG. 3

FAIRCHILD SEMICONDUCTOR

FUNCTIONAL DESCRIPTION — The 93L16 is a low power 4-bit synchronous binary up counter. The counter is fully synchronous with the clock pulse driving the four master-slave flip-flops in parallel through a clock buffer. During the low to high transition of the clock, the master is inhibited from further change. After the masters are locked out, data is transferred from the master to the slaves and reflected at the outputs. When the clock is high the masters are inhibited and the master-slave data path remains established. During the high to low transition of the clock the slave is inhibited from further change, followed by the enabling of the masters for the acceptance of data from the counting logic or the parallel entry logic.

The three control inputs, Parallel Enable ($\overline{PE}$), Count Enable Parallel (C_{EP}), and Count Enable Trickle (C_{ET}), select the mode of operation as shown in the table. When the conditions for counting are satisfied the rising edge of a clock pulse will change the counter to the next state of the binary sequence shown. The Count Mode is enabled when C_{EP} and C_{ET} inputs are in the high state and $\overline{PE}$ is high.

The 93L16 can be synchronously preset from the four parallel inputs, P_{0-3}, when $\overline{PE}$ is low. While the parallel enable is low and the clock is low each master of the flip-flops is connected to the appropriate parallel input (P_{0-3}) and the slaves (outputs) are steady in their previous state. When the clock goes high the masters are inhibited and this information is transferred to the slaves and is reflected at the outputs. The parallel enable input overrides both count enable inputs, presetting the counter when low. Hence the 93L16 acts as a 4-bit dual rank register when parallel enabled.

Proper logical operation requires that C_P be high during the high-to-low transition of C_{EP} or C_{ET} and the low-to-high transition of $\overline{PE}$. In most applications, this restriction is not a hindrance since logical transitions usually follow the low-to-high transition of the clock pulse, and inputs are steady before C_P goes low. The remaining transitions may be made by following the setup and release times specified under "Switching Characteristics" on the data sheet.

Terminal count is high whenever the counter is at terminal count (state 15) and count enable trickle is high, as is shown in the logic equations. Multistage synchronous counting at high speeds without additional logic is made possible with a high speed lookahead technique utilizing the count enable and terminal count logic. A multistage counter illustrating these techniques is shown and discussed in the application section.

The asynchronous master reset when low overrides all other inputs to reset the four outputs to zero.

LOGIC EQUATIONS:

Count Enable = $C_{EP} \bullet C_{ET} \bullet \overline{PE}$

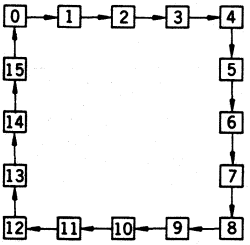
TC = $C_{ET} \bullet Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3$

Preset = PE • C_P+ (rising clock edge)

Reset = MR

NOTE: PE and MR are active low inputs implying the pins are $\overline{PE}$ and $\overline{MR}$. Therefore Reset = MR implies Pin 1 must be low to reset.

STATE DIAGRAM



MODE SELECTION

$\overline{PE}$	C_{EP}	C_{ET}	MODE
L	L	L	Preset
L	L	H	Preset
L	H	L	Preset
L	H	H	Preset
H	L	L	No Change
H	L	H	No Change
H	H	L	No Change
H	H	H	Count

($\overline{MR}$ = HIGH) H = HIGH Voltage Level
L = LOW Voltage Level

TTμL LOADING RULES

INPUTS	LOADING	
	HIGH	LOW
$\overline{MR}$, C_{EP}	0.5 U.L.	0.25 U.L.
C_P, $\overline{PE}$, C_{ET}	1.0 U.L.	0.5 U.L.
P_0, P_1, P_2, P_3	0.34 U.L.	0.17 U.L.

OUTPUTS	DRIVE FACTORS	
	HIGH	LOW
Q_0, Q_1, Q_2, Q_3, TC	8.0 U.L.	2.0 U.L.

Note: 1 Unit Load (U.L.) = 40 μA High/1.6 mA Low

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (D.C.)	−0.5 V to +5.5 V
*Input Current (D.C.)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output High)	−0.5 V to +V_{CC} value
Output Current (D.C.) (Output Low)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC}) MIN.	TYP.	MAX.	TEMPERATURE
U7B/4L93L1651X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
U7B/4L93L1659X	4.75 V	5.0 V	5.25 V	0°C to 75°C

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	CHARACTERISTIC	LIMITS MIN.	TYP. (Note 4)	MAX.	UNITS	CONDITIONS
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = −0.32 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.15	0.3	Volts	V_{CC} = MIN., I_{OL} = 3.2 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{IH}	Input HIGH Level	2.0			Volts	Guaranteed input logical HIGH voltage for all inputs
V_{IL}	Input LOW Level			0.7	Volts	Guaranteed input logical LOW voltage for all inputs
I_{IL}	Input LOW Current $\overline{MR}$, C_{EP} Cp, $\overline{PE}$, C_{ET} P_0, P_1, P_2 & P_3		 −0.25 −0.50 −0.13	 −0.40 −0.80 −0.27	mA	V_{CC} = MAX., V_{IN} = 0.3 V
I_{IH}	Input HIGH Current $\overline{MR}$, C_{EP} Cp, $\overline{PE}$, C_{ET} P_0, P_1, P_2 & P_3		 2.0 4.0 1.0	 20 40 13.3	μA	V_{CC} = MAX., V_{IN} = 2.4 V
	Input HIGH Current			1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{SC}	Output Short Circuit Current	−2.5	−16	−25	mA	V_{CC} = MAX., V_{OUT} = 0.0 V
I_{CC}	Power Supply Current		17	27.5	mA	V_{CC} = MAX.

NOTES:

(1) The actual testing Procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this Specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California (see page 1 for address and phone).

(2) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.

(3) The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

(4) Typical limits are at V_{CC} = 5.0 V, 25°C, and max. loading.

SWITCHING CHARACTERISTICS ($T_A = 25°C$)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS & COMMENTS
t_{pd+} (Q)	Turn-Off Delay		45		ns	$V_{CC} = 5.0$ V, $C_L = 15$ pF (Fig. 5)
t_{pd-} (Q)	Turn-On Delay		45		ns	
t_{pd+} (TC)	Turn-Off Delay for TC		90		ns	
t_{pd-} (TC)	Turn-On Delay for TC		40		ns	
t_s (CE)	Set-Up Time for CE		45		ns	$V_{CC} = 5.0$ V, $C_L = 15$ pF (Fig. 6)
t_r (CE)	Release Time for CE		40		ns	
t_s	Set-Up Time for Data		85		ns	$V_{CC} = 5.0$ V, $C_L = 15$ pF (Fig. 7)
t_r	Release Time for Data		50		ns	
t_s ($\overline{PE}$)	Set-Up Time for $\overline{PE}$		75		ns	
t_r ($\overline{PE}$)	Release Time for $\overline{PE}$		55		ns	
t_{pd-} ($\overline{MR}$)	Turn-On Delay for $\overline{MR}$		75		ns	$V_{CC} = 5.0$ V, $C_L = 15$ pF (Fig. 8)
$t_{pd\pm}$	Propagation Delay for C_{ET} to TC		35		ns	$V_{CC} = 5.0$ V, $C_L = 15$ pF (Fig. 9)

SET-UP TIME: t_s is defined as the minimum time required for the logic level to be present at the logic input prior to the clock transition from low to high in order for the flip-flop(s) to respond.

RELEASE TIME: t_r is defined as the maximum time allowed for the logic level to be present at the logic input prior to the clock transition from low to high in order for the flip-flop(s) not to respond.

SWITCHING TIME WAVEFORMS

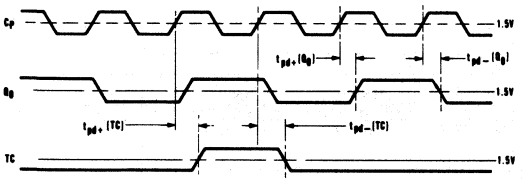


Fig. 5

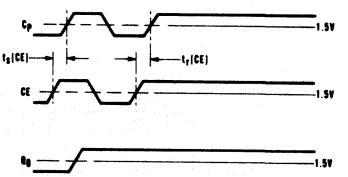


Fig. 6

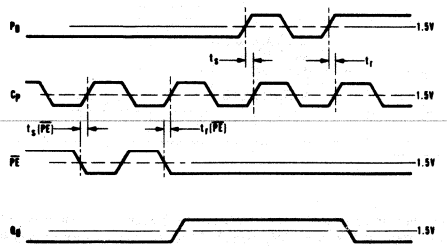


Fig. 7

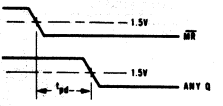


Fig. 8

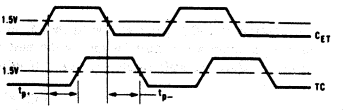


Fig. 9

APPLICATIONS

MULTISTAGE COUNTING

The low power 93L16 binary counters may be cascaded to provide binary multistage synchronous counting. Two methods commonly used to cascade these counters are shown in Figure 10a and Figure 10b.

In multistage counting, all less significant stages must be at their terminal count before the next more significant counter is enabled. The 93L16 internally decodes the terminal count condition and "ANDs" it with the C_{ET} input to generate the terminal count (TC) output. This arrangement allows one to perform series enabling by connecting the TC output (enable signal) to the C_{ET} input of the following stage, Figure 10a. The setup requires very few interconnections, but has the following drawback: since it takes time for the enable to ripple through the counter stages, there is a reduction in maximum counting speed. To increase the counting rate, it is necessary to decrease the propagation delay of the TC signal, which is done in the second method.

The scheme illustrated in Figure 10b permits multistage counting up to seven stages limited by the fanout of the terminal count. For an alternate scheme for more stages see Application Note 184.

The C_{EP} input of the 93L16 is internally "ANDed" with the C_{ET} input and as a result, both must be high for the counter to be enabled. The C_{ET} inputs are connected as before except for the second stage. There the C_{ET} input is left floating and is therefore high. Also, all C_{EP} inputs are connected to the terminal output of the first stage. The advantage of this method is best seen by assuming all stages except the second and last are in their terminal condition. As the second stage advances to its terminal count, an enable is allowed to trickle down to the last counter stage, but has the full cycle time of the first counter to reach it. Then as the TC of the first stage goes active (high), all C_{EP} inputs are activated, allowing all stages to count on the next clock.

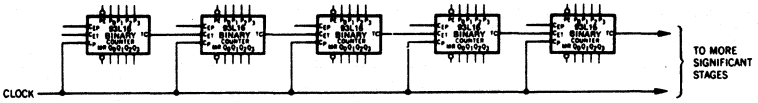


Fig. 10a — MULTISTAGE COUNTER

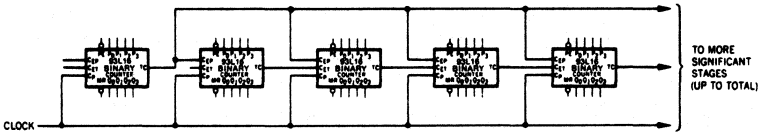
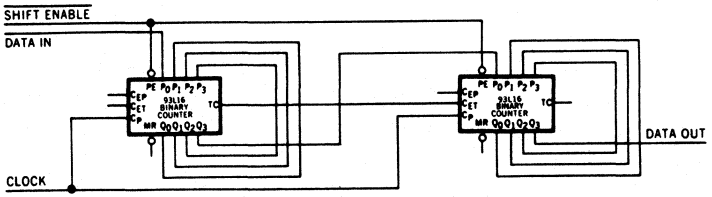


Fig. 10b — SYNCHRONOUS MULTISTAGE COUNTING SCHEME

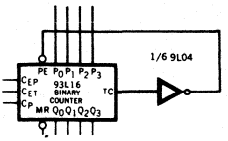


The contents of a 93L16 counter may be shifted out serially using the synchronous parallel loading features. The Q outputs are connected to the next more significant P input for shifting the most significant bit first. With "shift enable" ($\overline{PE}$) high the 93L16's perform the normal counting operation. When the shift enable is activated (low) the contents of the two counters are shifted out serially at the Q_3 output of the last counter.

Fig. 11 — SERIAL SHIFT REGISTER SCHEME

APPLICATIONS (Cont'd)

PROGRAMMABLE INPUTS



DIVIDE RATIO	INPUT REQUIRED				
		P_0	P_1	P_2	P_3
2	14	L	H	H	H
3	13	H	L	H	H
4	12	L	L	H	H
5	11	H	H	L	H
6	10	L	H	L	H
7	9	H	L	L	H
8	8	L	L	L	H
9	7	H	H	H	L
10	6	L	H	H	L
11	5	H	L	H	L
12	4	L	L	H	L
13	3	H	H	L	L
14	2	L	H	L	L
15	1	H	L	L	L
16	0	L	L	L	L

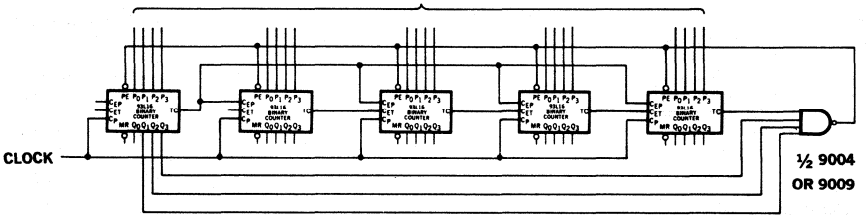
L = LOW = GROUND
H = HIGH = OPEN OR V_{CC}
(WITH 1 kΩ LIMITING RES.)

PROGRAMMABLE DIVIDER

Although the 93L16 is a modulo 16 counter, the addition of a single inverter allows the counter to be used as a synchronous programmable counter with modules of 2 to 16.

Fig. 12

PROGRAM WITH ONE'S COMPLEMENT



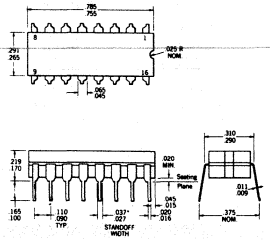
MULTI-STAGE SYNCHRONOUS PROGRAMMABLE DECIMAL COUNTER

Multi-stage synchronous programmable decimal counters are easily implemented by decoding the terminal state of a synchronous counter and utilizing it as a preset signal.

Fig. 13

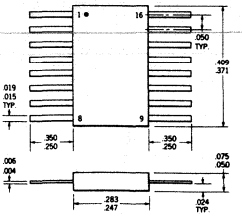
PACKAGE INFORMATION

7B — 16 LEAD DUAL IN-LINE PACKAGE



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.2 grams
*The .027/.037 dimension does not apply to the corner leads

4L — 16 LEAD (BeO) FLATPAK



NOTES:
All dimensions in inches
Leads are gold-plated kovar
Package weight is 0.4 gram

LPTTμL/MSI 93L18

LOW POWER EIGHT-INPUT PRIORITY ENCODER

A FAIRCHILD TTμL® IC PRODUCT

GENERAL DESCRIPTION — The LPTTμL/MSI 93L18 is a multipurpose encoder designed to accept 8 inputs and produce a binary weighted code of the highest order input. The circuit uses TTμL technology for high speed and high fanout capability, and is compatible with all Fairchild TTμL families.

FEATURES:

- **MULTI-FUNCTION CAPABILITY —CODE CONVERSIONS —MULTI-CHANNEL D/A CONVERTER —DECIMAL TO BCD CONVERTER —CASCADING FOR PRIORITY ENCODING OF N BITS**
- **INPUT ENABLE CAPABILITY**
- **PRIORITY ENCODING . . . . AUTOMATIC SELECTION OF HIGHEST PRIORITY INPUT LINE**
- **OUTPUT ENABLE . . . . . ACTIVE LOW WHEN ALL INPUTS HIGH**
- **GROUP SIGNAL OUTPUT . . . ACTIVE WHEN ANY INPUT IS LOW**
- **TYPICAL PROPAGATION DELAY OF 55 ns**
- **TYPICAL POWER DISSIPATION OF 75 mW**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **ALL CERAMIC HERMETIC 16 PIN DUAL IN-LINE AND FLAT PACKAGES**
- **TTμL COMPATIBLE**

PIN NAMES

$\overline{0}$	Priority (Active Low) Input
$\overline{1}$ to $\overline{7}$	Priority (Active Low) Inputs
$\overline{EI}$	Enable (Active Low) Input
$\overline{EO}$	Enable (Active Low) Output
$\overline{GS}$	Group Select (Active Low) Output
$\overline{A}_0$, $\overline{A}_1$, $\overline{A}_2$	Address (Active Low) Outputs

ORDER INFORMATION:

Specify U7B93L18XXX for 16 pin Dual In-Line package or U4L93L18XXX for 16 pin Flatpak where XXX is 51X for −55°C to +125°C temperature or 59X for 0°C to 75°C temperature.

LOGIC DIAGRAM

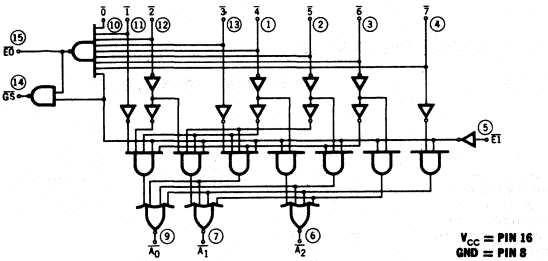


Fig. 4

LOGIC SYMBOL

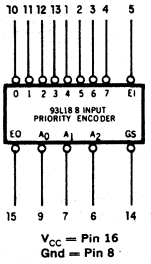


Fig. 1

CONNECTION DIAGRAM

DIP (TOP VIEW)

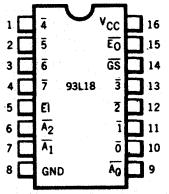


Fig. 2

FLATPAK (TOP VIEW)

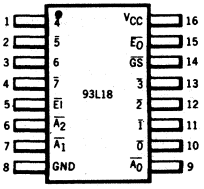


Fig. 3

FAIRCHILD SEMICONDUCTOR

FUNCTIONAL DESCRIPTION: The LPTTμL/MSI 93L18 8 Input Priority Encoder accepts data from 8 active low inputs and provides a binary representation on the 3 active low outputs. A priority is assigned to each input so that when two or more inputs are simultaneously active, the input with the highest priority is represented on the output, with input line 7 having the highest priority.

A high on the input enable ($\overline{EI}$) will force all outputs to the inactive (high) state and allow new data to settle without producing erroneous information at the outputs.

Provided with the 3 data outputs are a group signal output ($\overline{GS}$) and an enable output ($\overline{EO}$). The $\overline{GS}$ is active level low when any input is low; this indicates when any input is active. The $\overline{EO}$ is active level low when all inputs are high. Using the output enable along with the input enable allows priority encoding of N input signals. Both $\overline{EO}$ and $\overline{GS}$ are inactive when the input enable is high.

TABLE I — TRUTH TABLE

$\overline{EI}$	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$	$\overline{GS}$	$\overline{A}_0$	$\overline{A}_1$	$\overline{A}_2$	$\overline{EO}$
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	H	L	L	H
L	X	X	X	X	X	L	H	H	L	L	H	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	L	L	L	H	H
L	X	X	L	H	H	H	H	H	L	H	L	H	H
L	X	L	H	H	H	H	H	H	L	L	H	H	H
L	L	H	H	H	H	H	H	H	L	H	H	H	H

H = High Voltage Level
L = Low Voltage Level
X = Don't Care

TABLE II — TTμL LOADING RULES

INPUTS	LOADING	
	HIGH	LOW
$\overline{0}$	0.5 U.L.	0.25 U.L.
$\overline{EI}, \overline{1}, \overline{2}, \overline{3}, \overline{4}, \overline{5}, \overline{6}, 7$	1.0 U.L.	0.5 U.L.

OUTPUTS	DRIVE FACTOR	
	HIGH	LOW
$\overline{EO}$	10 U.L.	1.25 U.L.
$\overline{GS}$	10 U.L.	1.5 U.L.
$\overline{A}_0, \overline{A}_1, \overline{A}_2$	10 U.L.	2.5 U.L.

Note: 1 Unit Load (U.L.) = 40 μA High/1.6 mA Low

TYPICAL INPUT AND OUTPUT CIRCUITS

INPUTS
EQUIVALENT CIRCUIT

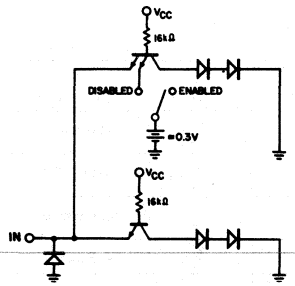


Fig. 5

OUTPUTS
EQUIVALENT CIRCUIT

OUTPUT LOW

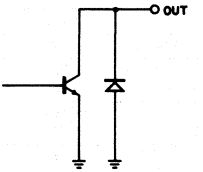


Fig. 6

OUTPUT HIGH

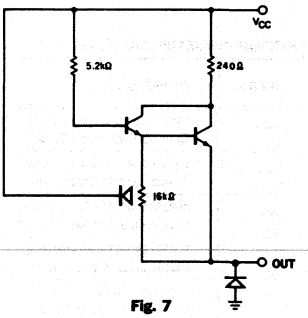


Fig. 7

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (D.C.)	−0.5 V to +5.5 V
*Input Current (D.C.)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output High)	-0.5 V to +V_{CC} value
Output Current (D.C.) (Output Low)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC}) MIN.	TYP.	MAX.	TEMPERATURE
U7B/4L93L1851X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
U7B/4L93L1859X	4.75 V	5.0 V	5.25 V	0°C to 75°C

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	CHARACTERISTIC	LIMITS MIN.	TYP. (Note 4)	MAX.	UNITS	CONDITIONS
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = −0.4 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.15	0.3	Volts	V_{CC} = MIN., I_{OL} = 4.0 mA (Pins 6, 7, 9) I_{OL} = 2.4 mA (Pin 14) I_{OL} = 2.0 mA (Pin 15) V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{IH}	Input HIGH Level	2.0			Volts	Guaranteed input logical HIGH voltage for all inputs
V_{IL}	Input LOW Level			0.7	Volts	Guaranteed input logical LOW voltage for all inputs
I_{IL}	Input LOW Current Input $\overline{0}$ (Pin 10) Inputs $\overline{1}$ thru $\overline{7}$ & $\overline{E}$i		 −0.25 −0.50	 −0.4 −0.8	mA	V_{CC} = MAX., V_{IN} = 0.3 V
I_{IH}	Input HIGH Current Input $\overline{0}$ (Pin 10) Inputs $\overline{1}$ thru $\overline{7}$ & $\overline{E}$i		 2.0 4.0	 20 40	μA	V_{CC} = MAX., V_{IN} = 2.4 V
	Input HIGH Current			1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{SC}	Output Short Circuit Current	−10	−22	−40	mA	V_{CC} = MAX., V_{OUT} = 0.0 V
I_{CC}	Power Supply Current		15	22	mA	V_{CC} = MAX., Pins 4 & 5 at GND

NOTES:
(1) The actual testing Procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this Specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California (see page 1 for address and phone).
(2) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
(3) The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
(4) Typical limits are at V_{CC} = 5.0 V, 25°C, and max. loading.

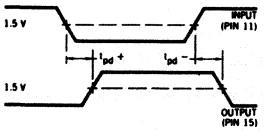
SWITCHING CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V, Pin 8 = GND)

SYMBOL	CHARACTERISTIC	LIMITS MIN.	TYP.	MAX.	UNITS	CONDITIONS
t_{pd+} t_{pd-}	Data Input to Enable Output Data Input to Enable Output		15 80		ns ns	See Figure 8
t_{pd+} t_{pd-}	Enable Input to Group Signal Enable Input to Group Signal		25 45		ns ns	See Figure 9
t_{pd+} t_{pd-}	Enable Input to Enable Output Enable Input to Enable Output		25 80		ns ns	See Figure 10
t_{pd+} t_{pd-}	Enable Input to Data Output Enable Input to Data Output		35 45		ns ns	See Figure 11
t_{pd+} t_{pd-}	Data Input to Group Signal Data Input to Group Signal		90 45		ns ns	See Figure 12
t_{pd+} t_{pd-}	Data Input to Data Output Data Input to Data Output		50 60		ns ns	See Figure 13

SWITCHING CHARACTERISTICS

All measurements are made with V_{CC} = 5.0 V applied to Pin 16 and Pin 8 grounded. The active input is driven by a 9002 TTμL gate. The input and output pins under test are loaded with 15 pF of capacitance. (This includes probe & jig capacitance).

Fig. 8
DATA INPUT TO ENABLE OUTPUT



Other Conditions: Pin 5 — Gnd
Pins 1, 2, 3, 4, 10, 12, 13 — V_{CC} through 750 Ω

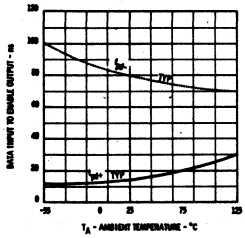
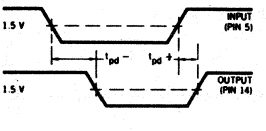


Fig. 9
ENABLE INPUT TO GROUP SIGNAL



Other Conditions: Pin 10 — Gnd
Pins 1, 2, 3, 4, 11, 12, 13 — V_{CC} through 750 Ω

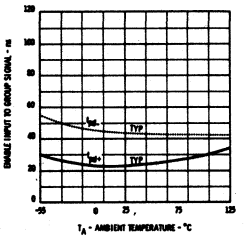
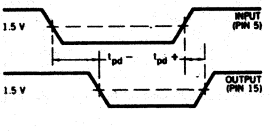


Fig. 10
ENABLE INPUT TO ENABLE OUTPUT



Other Conditions:
Pins 1, 2, 3, 4, 10, 11, 12, 13 — V_{CC} through 750 Ω

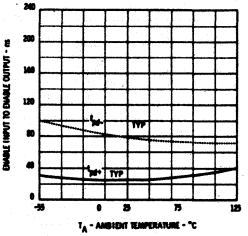
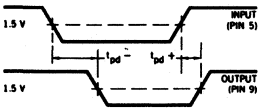


Fig. 11
ENABLE INPUT TO DATA OUTPUT



Other Conditions: Pin 4 — Gnd
Pins 1, 2, 3, 10, 11, 12, 13 — V_{CC} through 750 Ω

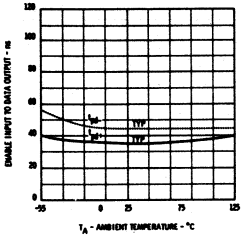
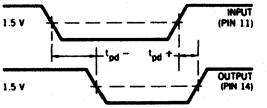


Fig. 12
DATA INPUT TO GROUP SIGNAL



Other Conditions: Pin 5 — Gnd
Pins 1, 2, 3, 4, 10, 12, 13 — V_{CC} through 750 Ω

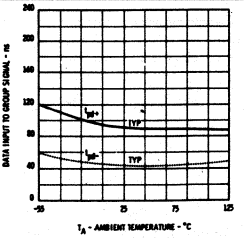
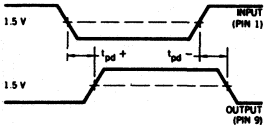
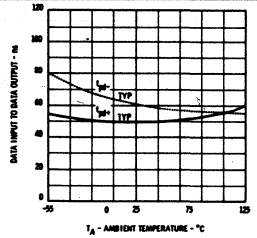


Fig. 13
DATA INPUT TO DATA OUTPUT



Other Conditions: Pins 5, 11 — Gnd
Pins 2, 3, 4, 10, 12, 13 — V_{CC} through 750 Ω



APPLICATIONS

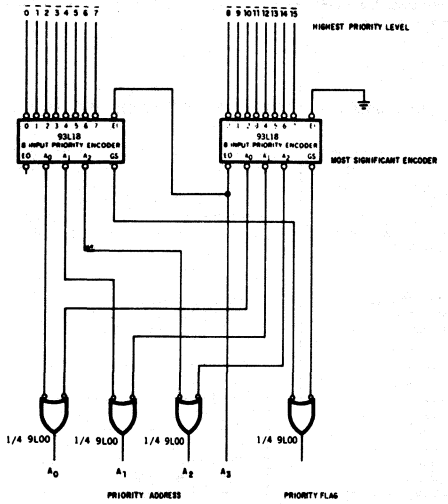


Fig. 14
16 INPUT PRIORITY ENCODER

The number of priority levels can be increased by cascading 93L18 encoders. This may be accomplished by connecting the most significant encoder's enable output ($\overline{EO}$) to the next most significant encoder's enable input ($\overline{EI}$).

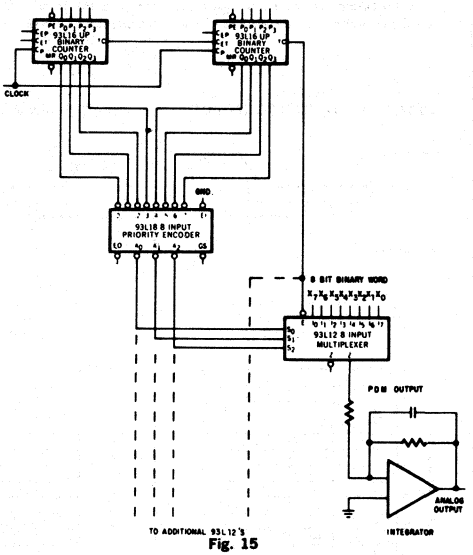


Fig. 15
MULTIPLE CHANNEL *D/A* CONVERTER

The 93L18 supplies a code sequence to the multiplexer, such that the most significant binary input is sampled for 50% of the count cycle, the next most significant input is sampled for 25% of the cycle, and so on. This sampling produces a PDM Output which can be integrated or in many cases, such as panel meters, motors, or audio speakers, fed directly to the analog output device. For each additional channel, a multiplexer and integrator are required.

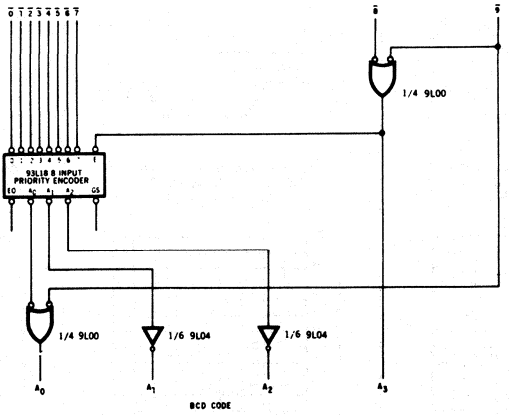


Fig. 16
DECIMAL TO BCD CONVERTER

The converter produces a BCD code corresponding to the most significant active low decimal input.

APPLICATIONS (Cont'd)

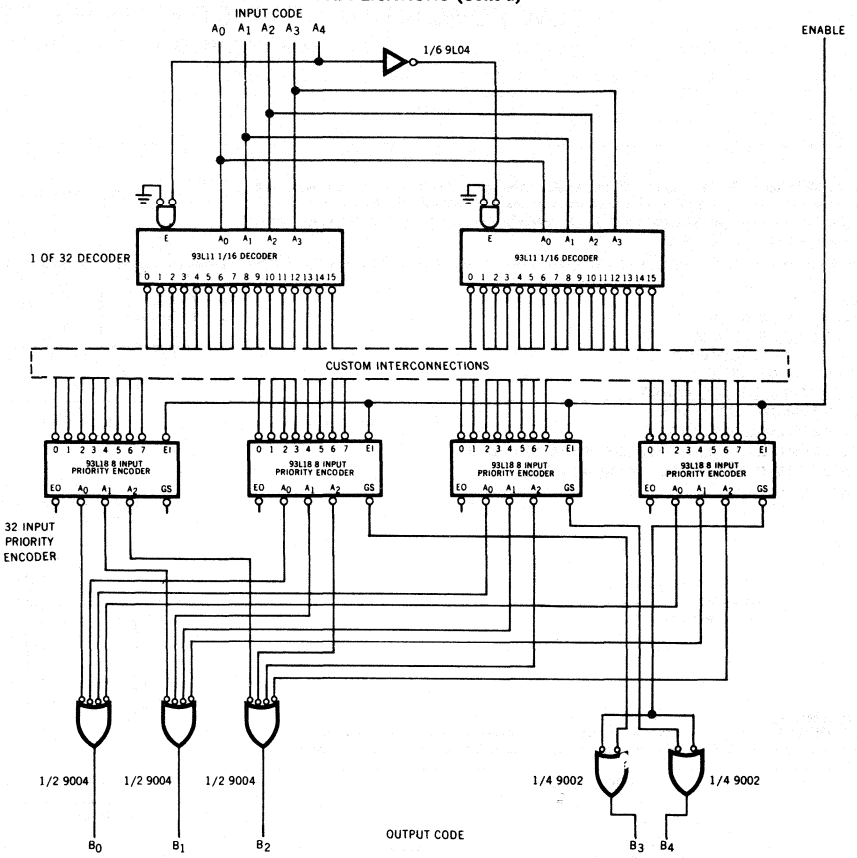
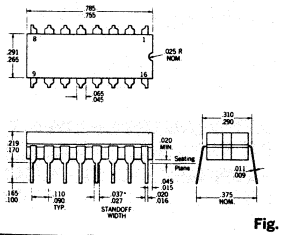


Fig. 17
5 BIT CODE CONVERTER

The 5 bit input code applied to the one of thirty-two decoder produces one low output. This low decoder output can be arbitrarily connected to any encoder input to produce any desired 5 bit output code. To cover all combinations of input codes, wiring connections are made between every possible decoder output and appropriate encoder inputs.

PACKAGE INFORMATION

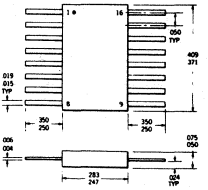
7B — 16 LEAD DUAL IN-LINE PACKAGE



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead
Leads are tin plated kovar
Package weight is 2.2 grams
*The .037 / .027 dimension does not apply to the corner leads

Fig. 18

4L — 16 LEAD (BeO) FLATPAK



NOTES:
All dimensions in inches
Leads are gold-plated kovar
Package weight is 0.4 gram

Fig. 19

LPTTμL/MSI 93L21

LOW POWER DUAL ONE-OF-FOUR DECODER

A FAIRCHILD TTμL IC PRODUCT

GENERAL DESCRIPTION — The LPTTμL/MSI 93L21 consists of two independent multipurpose decoders, each designed to accept 2 inputs and provide 4 mutually exclusive outputs. In addition an active low enable input is provided for each decoder which gives demultiplexing capability. The circuit uses TTμL technology and is compatible with the Fairchild TTμL family.

FEATURES:

- **MULTI-FUNCTION CAPABILITY**
- **MUTUALLY EXCLUSIVE OUTPUTS**
- **HIGH CAPACITIVE DRIVE CAPABILITY**
- **DEMULTIPLEXING CAPABILITY**
- **ACTIVE LOW ENABLE FOR EACH DECODER**
- **TYPICAL PROPAGATION DELAY OF 50 ns**
- **TYPICAL POWER DISSIPATION OF 45 mW**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED LINE TERMINATION EFFECTS**
- **ALL CERAMIC "HERMETIC" 16-PIN DUAL IN-LINE AND FLAT PACKAGES**
- **TTμL COMPATIBLE**

PIN NAMES

Decoder 1 and 2

$\overline{E}$	Enable (Active Low) Input
A_0, A_1	Address Inputs
$\overline{0}$, $\overline{1}$, $\overline{2}$, $\overline{3}$	(Active Low) Outputs

ORDER INFORMATION

Specify U7B93L21XXX for 16-pin Dual In-Line package or U4L93L21XXX for 16-pin Flat Package where XXX is 51X for the −55°C to +125°C temperature range, or 59X for the 0°C to +75°C temperature range.

LOGIC DIAGRAM

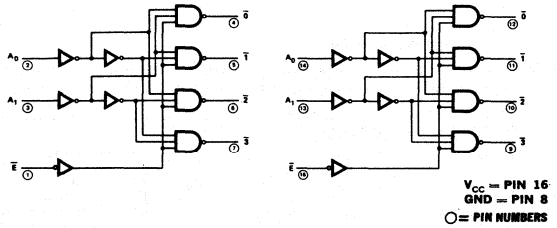


Fig. 4

LOGIC SYMBOL

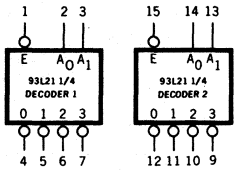


Fig. 1

CONNECTION DIAGRAM

DIP (TOP VIEW)

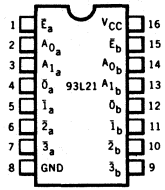


Fig. 2

FLATPAK (TOP VIEW)

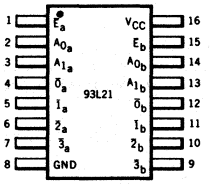


Fig. 3

FAIRCHILD
SEMICONDUCTOR

FUNCTIONAL DESCRIPTION — The 93L21 consists of two separate decoders each designed to accept two binary weighted inputs and provide four mutually exclusive active low outputs as shown in Figure 1. Each decoder can be used as a four output demultiplexer by using the enable as a data input.

The active low outputs facilitate memory addressing for units such as the 4102 associative memory. The active low outputs are also compatible with the active low enables of other LPTTμL/MSI and TTμL/MSI elements making the 93L21 useful in logic selection schemes.

The Truth Table and Loading Rules for the 93L21 are shown in Tables I & II.

TABLE I — TRUTH TABLE

DECODER I & II

$\overline{E}$	A_0	A_1	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L
H	X	X	H	H	H	H

H = High Voltage Level
L = Low Voltage Level
X = Level Does Not Affect Output

TABLE II — LOADING RULES

INPUTS	LOADING	
	High	Low
All Inputs	0.5 U.L.	0.25 U.L.

OUTPUTS	DRIVE FACTOR	
	High	Low
All Outputs	10 U.L.	2.5 U.L.

Note: 1 Unit Load (U.L.) = 40 μA High/1.6 mA Low

TYPICAL INPUT AND OUTPUT CIRCUITS

INPUTS
EQUIVALENT CIRCUIT

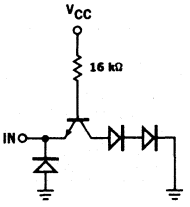


Fig. 5

OUTPUTS
EQUIVALENT CIRCUITS

OUTPUT LOW

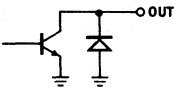


Fig. 6

OUTPUT HIGH

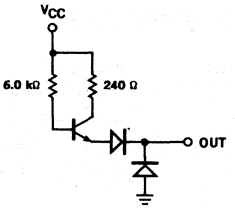


Fig. 7

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (D.C.)	−0.5 V to +5.5 V
*Input Current (D.C.)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output High)	−0.5 V to +V_{CC} value
Output Current (D.C.) (Output Low)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC}) MIN.	TYP.	MAX.	TEMPERATURE
U7B/4L93L2151X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
U7B/4L93L2159X	4.75 V	5.0 V	5.25 V	0°C to 75°C

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	CHARACTERISTIC	LIMITS MIN.	TYP. (Note 4)	MAX.	UNITS	CONDITIONS
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = −0.4 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.15	0.3	Volts	V_{CC} = MIN., I_{OL} = 4.0 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{IH}	Input HIGH Level	2.0			Volts	Guaranteed input logical HIGH voltage for all inputs
V_{IL}	Input LOW Level			0.7	Volts	Guaranteed input logical LOW voltage for all inputs
I_{IL}	Input LOW Current		−0.25	−0.4	mA	V_{CC} = MAX., V_{IN} = 0.3 V
I_{IH}	Input HIGH Current		2.0	20	μA	V_{CC} = MAX., V_{IN} = 2.4 V
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{SC}	Output Short Circuit Current	−2.5	−16	−25	mA	V_{CC} = MAX., V_{OUT} = 0.0 V
I_{CC}	Power Supply Current		9.0	13.2	mA	V_{CC} = MAX., all inputs at GND.

NOTES:
(1) The actual testing Procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this Specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California (see page 1 for address and phone).
(2) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
(3) The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
(4) Typical limits are at V_{CC} = 5.0 V, 25°C, and max. loading.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	CHARACTERISTIC	LIMITS MIN.	TYP.	MAX.	UNITS	CONDITIONS
t_{pd+}	Turn Off Delay A Input to Output		45		ns	V_{CC} = 5.0 V C_L = 15 pF, (See Fig. 8)
t_{pd-}	Turn On Delay A Input to Output		50		ns	
t_{pd+}	Turn Off Delay E Input to Output		35		ns	V_{CC} = 5.0 V C_L = 15 pF, (See Fig. 9)
t_{pd-}	Turn On Delay E Input to Output		40		ns	

SWITCHING TIME AND WAVEFORMS

All measurements are made with V_{CC} = 5.0 V applied to Pin 16 and Pin 8 grounded. The active input is driven by a 9002 TTμL gate. The input and output pins under test are loaded with 15 pF of capacitance (this includes probe and jig capacitance).

DATA INPUT TO DATA OUTPUT

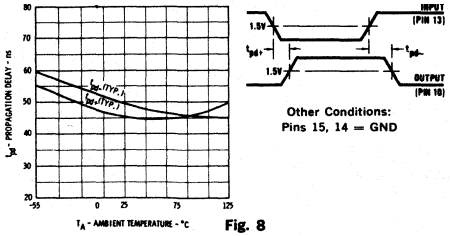


Fig. 8

ENABLE INPUT TO DATA OUTPUT

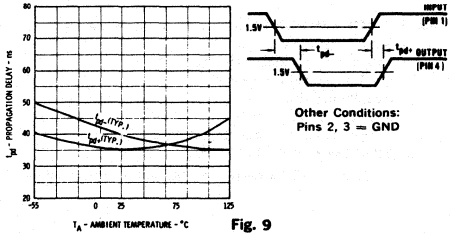


Fig. 9

APPLICATIONS

DUAL 1 OUT OF 10 DECODER WITH ENABLES (ACCEPTS BCD INPUTS)

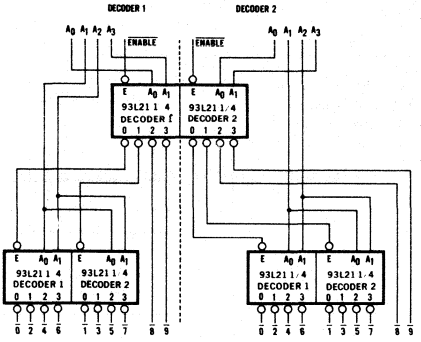
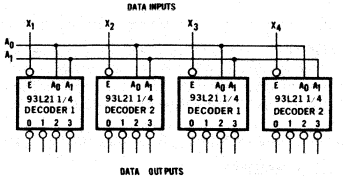


Fig. 10

4 BIT DIGITAL DEMULTIPLEXER



Data may be routed from a source to any of four outputs by addressing that output. All non-addressed outputs remain high.

Fig. 11

4-PHASE CLOCK GENERATOR

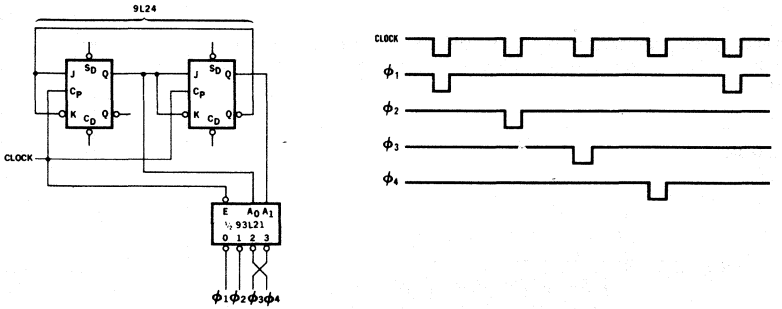
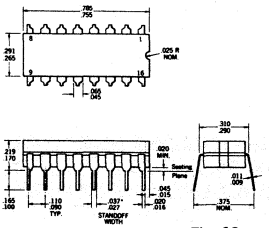


Fig. 12

PACKAGE INFORMATION

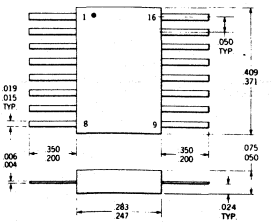
7B — 16 LEAD DUAL IN-LINE PACKAGE



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.2 grams
*The .027/.037 dimension does not apply to the corner leads

Fig. 13

4L — 16 LEAD (BeO) FLATPAK



NOTES:
All dimensions in inches
Leads are gold-plated kovar
Package weight is 0.4 gram

Fig. 14

LPTTμL/MSI 93L22

LOW POWER QUAD TWO-INPUT MULTIPLEXER

A FAIRCHILD TTμL® IC PRODUCT

GENERAL DESCRIPTION — The LPTTμL/MSI 93L22 is a monolithic, medium speed, quad two input digital multiplexer circuit, constructed with the Fairchild Planar* epitaxial process. It consists of four multiplexing circuits with common select and enable logic. Each circuit contains two inputs and one output. The circuit uses TTμL technology and is compatible with the Fairchild TTμL family.

FEATURES

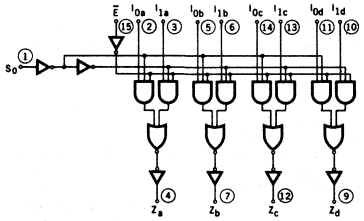
- **MULTIFUNCTION CAPABILITY**
- **ON-CHIP SELECT LOGIC DECODING**
- **TYPICAL PROPAGATION DELAY OF 44 ns**
- **TYPICAL POWER DISSIPATION OF 45 mW**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **ALL CERAMIC "HERMETIC" 16 PIN DUAL IN-LINE AND FLAT PACKAGES**
- **TTμL COMPATIBLE**

PIN NAMES

S	Common Select Input
E	Enable (Active Low) Input
Multiplexers A, B, C, D	
I_0, I_1	Multiplexers Inputs
Z	Multiplexer Output

ORDER INFORMATION — Specify U7B93L22XXX for 16-pin Dual In-Line package or U4L93L22XXX for 16-pin Flatpak, where XXX is 51X for the −55°C to +125°C temperature range, or 59X for the 0°C to +75°C temperature range.

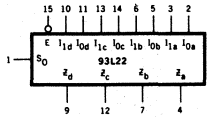
LOGIC DIAGRAM



V_{CC} = PIN 16
GND = PIN 8
○ = PIN NUMBERS

Fig. 4

LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

Fig. 1

CONNECTION DIAGRAM
DIP (TOP VIEW)

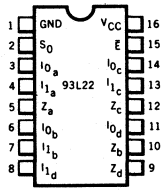


Fig. 2

FLATPAK (TOP VIEW)

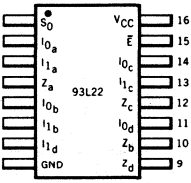


Fig. 3

*Planar is a patented Fairchild process.

FAIRCHILD
SEMICONDUCTOR

FUNCTIONAL DESCRIPTION — The 93L22 quad two input multiplexer is a member of the Fairchild family of Low Power Medium Scale Integrated digital building blocks. It provides, in one package, the ability to select four bits of either data or control from four two bit sources. The enable input (E) is active low. When not activated all outputs (Z) are low regardless of all other inputs. The 93L22 quad two input multiplexer is the logical implementation of a four pole two position switch, with the position of the switch being set by the logic level supplied to the one select input. The logic equations for the outputs are shown below:

$$Z_a = E \cdot (I_{1a} \cdot S_0 + I_{0a} \cdot \overline{S_0}) \qquad Z_b = E \cdot (I_{1b} \cdot S_0 + I_{0b} \cdot \overline{S_0}) \qquad Z_c = E \cdot (I_{1c} \cdot S_0 + I_{0c} \cdot \overline{S_0}) \qquad Z_d = E \cdot (I_{1d} \cdot S_0 + I_{0d} \cdot \overline{S_0})$$

A common use of the 93L22 would be the moving of data from two registers to common output busses. The particular register from which the data came would be determined by the state of the select input. A less obvious use is a function generator. The 93L22 can generate four functions of two variables with one variable common. This is useful implementing gating functions.

TABLE I — TRUTH TABLE
Identical for Each Multiplexer

ENABLE	SELECT INPUT	INPUTS		OUTPUT
$\overline{E}$	S_0	I_{0Y}	I_{1Y}	Z_Y
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = High voltage level
L = Low voltage level
X = Level does not affect output
Y = a, b, c, d

TABLE II — LOADING RULES

INPUTS	LOADING	
	HIGH	LOW
I_{0a}, I_{1a}, I_{0b}, I_{1b}, I_{0c}, I_{1c}, I_{0d}, I_{1d}, S_0, E	0.5 U.L.	0.25 U.L.

OUTPUTS	DRIVE FACTOR	
	HIGH	LOW
Z_a, Z_b, Z_c, Z_d	10 U.L.	2.5 U.L.

Note: 1 Unit Load (U.L.) = 40 μA High/1.6 mA Low

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

INPUTS
EQUIVALENT CIRCUIT

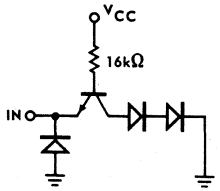


Fig. 5

OUTPUTS
EQUIVALENT CIRCUITS

OUTPUT LOW

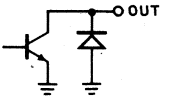


Fig. 6

OUTPUT HIGH

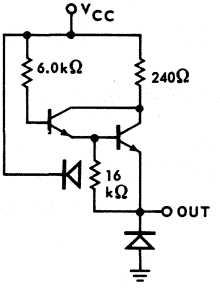


Fig. 7

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (D.C.)	−0.5 V to +5.5 V
*Input Current (D.C.)	− 30 mA to +5.0 mA
Voltage Applied to Outputs (Output High)	0.5 V to +V_{CC} value
Output Current (D.C.) (Output Low)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC}) MIN.	TYP.	MAX.	TEMPERATURE
U7B/4L93L2251X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
U7B/4L93L2259X	4.75 V	5.0 V	5.25 V	0°C to 75°C

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	CHARACTERISTIC	LIMITS MIN.	TYP. (Note 4)	MAX.	UNITS	CONDITIONS
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = −0.4 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.15	0.3	Volts	V_{CC} = MIN., I_{OL} = 4.0 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{IH}	Input HIGH Level	2.0			Volts	Guaranteed input logical HIGH voltage for all inputs
V_{IL}	Input LOW Level			0.7	Volts	Guaranteed input logical LOW voltage for all inputs
I_{IL}	Input LOW Current		−0.25	−0.4	mA	V_{CC} = MAX., V_{IN} = 0.3 V
I_{IH}	Input HIGH Current		2.0	20	μA	V_{CC} = MAX., V_{IN} = 2.4 V
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{SC}	Output Short Circuit Current	−10	−21	−40	mA	V_{CC} = MAX., V_{OUT} = 0.0 V
I_{CC}	Power Supply Current		9.0	13.2	mA	V_{CC} = MAX.

NOTES:
(1) The actual Testing Procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this Specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California (see page 1 for address and phone).
(2) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
(3) The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
(4) Typical limits are at V_{CC} = 5.0 V, 25°C, and max. loading.

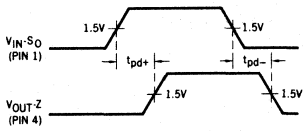
SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	CHARACTERISTIC	LIMITS MIN.	TYP.	MAX.	UNITS	CONDITIONS
t_{pd+} (S_0 to Z)	Turn Off Delay Input to Output		40		ns	V_{CC} = 5.0 V, (See Figure 8) C_L = 15 pF
t_{pd-} (S_0 to Z)	Turn On Delay Input to Output		48		ns	

SWITCHING TIME WAVEFORMS

t_{pd}; S_0 to Z.

CONDITIONS
Pins 2, 15 = GND
Pin 3 = V_{CC}



All inputs are driven by outputs of TTμL 9000 series gates loaded with 15 pF. All outputs are loaded with the same capacitance (referred to as C_L) and only with capacitance.

Fig. 8

APPLICATIONS

DUAL 10 INPUT MULTIPLEXER

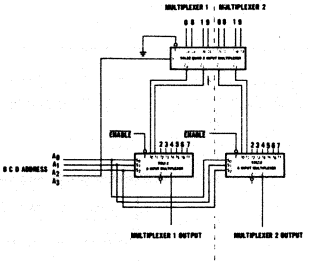
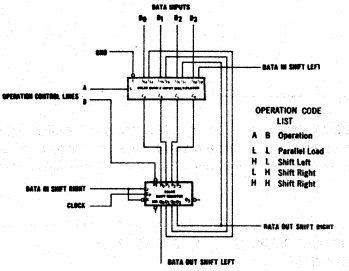


Fig. 9

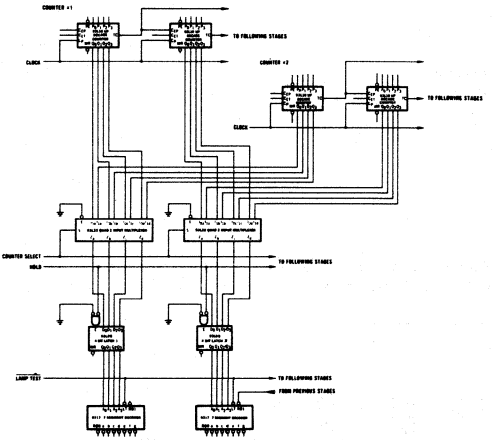
SHIFT LEFT, SHIFT RIGHT, PARALLEL LOAD REGISTER



This register will shift left, shift right, and load 4 bits of parallel data according to the operation code applied to A and B.

Fig. 10

REGISTER SELECTION

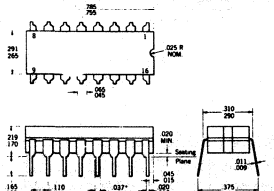


The 93L22 can be used to select parallel data from two multiple bit sources. Illustrated above is a counting and display system where the 93L22 selects the content of one of the counters.

Fig. 11

PACKAGE INFORMATION

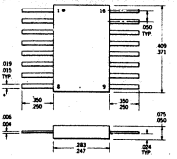
7B — 16 LEAD DUAL IN-LINE PACKAGE



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.2 grams
*The .027/.037 dimension does not apply to the corner leads

Fig. 12

4L — 16 LEAD (BeO) FLATPAK



NOTES:
All dimensions in inches
Leads are gold-plated kovar
Package weight is 0.4 gram

Fig. 13

LPTTμL/MSI 93L24
LOW POWER 5-BIT COMPARATOR
A FAIRCHILD TTμL® IC PRODUCT

GENERAL DESCRIPTION — The LPTTμL/MSI 93L24 is a medium speed expandable comparator which provides comparison between two 5 bit words and gives three outputs, "less than," "greater than," and "equal to." A high level on the active low enable input forces all three outputs low.

FEATURES:
- **THREE SEPARATE OUTPUTS . . . A<B, A>B, A=B**
- **EASILY EXPANDABLE**
- **ACTIVE LOW-LEVEL ENABLE INPUT**
- **HIGH DRIVE OUTPUT CIRCUITRY**
- **TYPICAL PROPAGATION DELAY OF 55 ns (A>B)**
- **TYPICAL POWER DISSIPATION OF 52 mW**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **ALL CERAMIC "HERMETIC" 16 PIN DUAL IN-LINE AND FLAT PACKAGES**
- **TTμL COMPATIBLE**

PIN NAMES

$\overline{E}$	Enable (Active Low) Input
A_0, A_1, A_2, A_3, A_4	Word A Parallel Inputs
B_0, B_1, B_2, B_3, B_4	Word B Parallel Inputs
$A < B$	A Less than B Output
$A > B$	A Greater than B Output
$A = B$	A Equal to B Output

ORDER INFORMATION — Specify U7B93L24XXX for 16 pin Dual In-Line package or U4L93L24XXX for 16 pin Flatpak, where XXX is 51X for the −55°C to +125°C temperature range, or 59X for the 0°C to +75°C temperature range.

LOGIC DIAGRAM

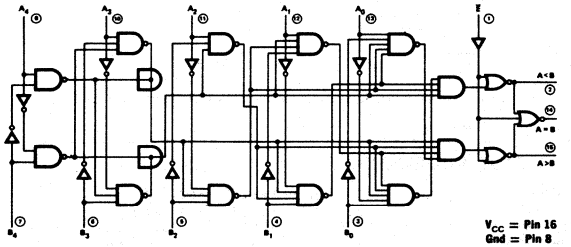


Fig. 4

LOGIC SYMBOL

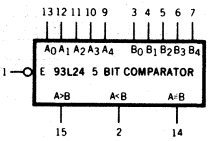


Fig. 1

CONNECTION DIAGRAM
DIP (TOP VIEW)

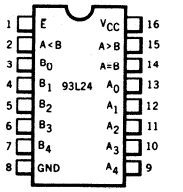


Fig. 2

FLATPAK (TOP VIEW)

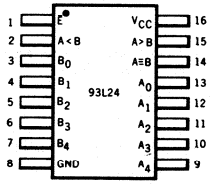


Fig. 3

FAIRCHILD
SEMICONDUCTOR

FUNCTIONAL DESCRIPTION — The 93L24 five bit comparator uses combinational circuitry to directly generate "A greater than B" and "A less than B" outputs. As evident from the logic diagram, these outputs are generated in only three gate delays. The "A equals B" output is generated in one additional gate delay by decoding the "A neither less than nor greater than B" condition with a nor gate. All three outputs are activated by the active low Enable input ($\bar{E}$).

Tying the A > B output from one device into an A input on another device and the A < B output into the corresponding B input permits easy expansion as shown in the applications section of this data sheet.

The A_4 and B_4 inputs are the most significant inputs and A_0, B_0 the least significant. Thus if A_4 is high and B_4 is low, the A > B output will be high regardless of all other inputs except $\bar{E}$.

TRUTH TABLE

$\bar{E}$	A B	A < B	A > B	A = B
H	X X	L	L	L
L	Word A = Word B	L	L	H
L	Word A > Word B	L	H	L
L	Word A < Word B	H	L	L

L = Low voltage level
H = High voltage level
X = Either high or low voltage level

TTμL LOADING RULES

INPUTS	LOADING	
	HIGH	LOW
A_0, A_1, A_2, A_3, A_4	1.0 U.L.	0.5 U.L.
B_0, B_1, B_2, B_3, B_4	1.0 U.L.	0.5 U.L.
$\bar{E}$	1.0 U.L.	0.5 U.L.
OUTPUTS	**DRIVE FACTORS**	
	HIGH	LOW
A < B, A > B	10 U.L.	2.25 U.L.
A = B	10 U.L.	2.5 U.L.

Note: 1 Unit Load (U.L.) = 40 μA High/1.6 mA Low

TYPICAL INPUT AND OUTPUT CIRCUITS

INPUTS
EQUIVALENT CIRCUIT

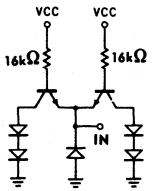


Fig. 5

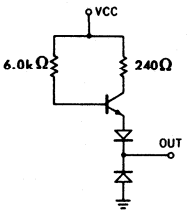


Fig. 6

OUTPUTS
EQUIVALENT CIRCUITS

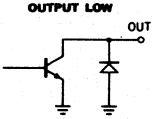


Fig. 7

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (D.C.)	−0.5 V to +5.5 V
*Input Current (D.C.)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output High)	−0.5 V to +V_{CC} value
Output Current (D.C.) (Output Low)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC}) MIN.	TYP.	MAX.	TEMPERATURE
U7B/4L93L2451X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
U7B/4L93L2459X	4.75 V	5.0 V	5.25 V	0°C to 75°C

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

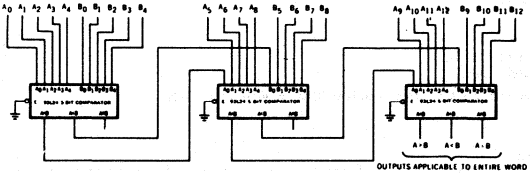
SYMBOL	CHARACTERISTIC	LIMITS MIN.	LIMITS TYP. (Note 4)	LIMITS MAX.	UNITS	CONDITIONS
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = −0.4 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.15	0.3	Volts	V_{CC} = MIN., I_{OL} = 4.0 mA (Pin 14) 3.6 mA (Pins 2 & 15) V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{IH}	Input HIGH Level	2.0			Volts	Guaranteed input logical HIGH voltage for all inputs
V_{IL}	Input LOW Level			0.7	Volts	Guaranteed input logical LOW voltage for all inputs
I_{IL}	Input LOW Current		−0.5	−0.8	mA	V_{CC} = MAX., V_{IN} = 0.3 V
I_{IH}	Input HIGH Current		4.0	40	μA	V_{CC} = MAX., V_{IN} = 2.4 V
	Input HIGH Current			1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{SC}	Output Short Circuit Current	−10	−22	−40	mA	V_{CC} = MAX., V_{OUT} = 0.0 V
I_{CC}	Power Supply Current		10.4	21	mA	V_{CC} = MAX.

NOTES:
(1) The actual testing Procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this Specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California (see page 1 for address and phone).
(2) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
(3) The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
(4) Typical limits are at V_{CC} = 5.0 V, 25°C, and max. loading.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	CHARACTERISTIC	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	CONDITIONS
t_{pd+} t_{pd-}	Enable to Output ($\overline{E}$ to A = B)		32 22		ns ns	C_L = 15 pF V_{CC} = 5.0 V
t_{pd+} t_{pd-}	Data to Output (A_2 to A > B)		53 58		ns ns	
t_{pd+} t_{pd-}	Data to Output (A_2 to A < B)		71 60		ns ns	
t_{pd+} t_{pd-}	Data to Output (A_2 to A = B)		100 80		ns ns	

APPLICATIONS

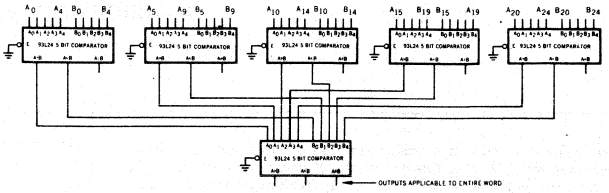


SERIAL EXPANSION OF 93L24 FOR LONGER WORD LENGTHS

For each additional 93L24 added four extra bits can be accommodated.

Fig. 8

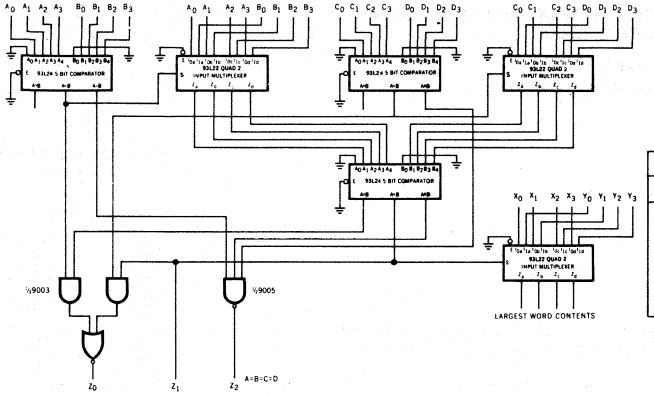
APPLICATIONS (Cont'd)



PARALLEL EXPANSION OF 93L24 FOR LONGER WORD LENGTHS

The above configuration provides comparisons over long word lengths with less delay: up to 25 bits in two 93L24 through delays, up to 125 bits in three delays. The parallel expansion of 93L24's will provide a comparison with less delay than with serial expansion in word lengths of 10 bits or more.

Fig. 9



OUTPUT CODES			CONDITIONS
Z_0	Z_1	Z_2	
H	L	H	A ≥ B, C, D
L	L	H	B ≥ A, C, D
H	H	H	C ≥ A, B, D
L	H	H	D ≥ A, B, C
H	L	L	A = B = C = D

L = LOW VOLTAGE LEVEL

H = HIGH VOLTAGE LEVEL

FOUR-WORD COMPARATOR

Illustrated above is a four-word by four-bit comparator. 93L22 Quad 2-Input Multiplexers are used to switch the larger of two 4-bit words to the next level of comparison. This circut produces an output code signifying the relationship of the input words and the contents of the largest word. This scheme may be expanded to more bits per word or more variables by the addition of more 93L24 and 93L22's.

Fig. 10

PACKAGE INFORMATION

7B — 16 LEAD DUAL IN-LINE PACKAGE

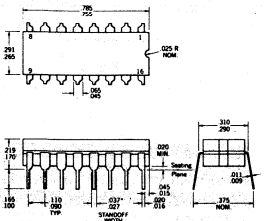


Fig. 11

NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.2 grams
*The .027/.037 dimension does not apply to the corner leads

4L — 16 LEAD (BeO) FLATPAK

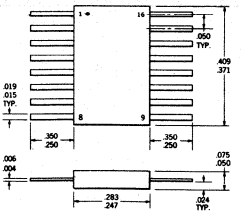


Fig. 12

NOTES:
All dimensions in inches
Leads are gold-plated kovar
Package weight is 0.4 gram

LPTTμL/MSI 93L28

LOW POWER DUAL 8-BIT SHIFT REGISTER

A FAIRCHILD TTμL® IC PRODUCT

GENERAL DESCRIPTION — The LPTTμL/MSI 93L28 is a medium speed serial storage element providing sixteen bits of storage in the form of two eight bit registers that will shift at greater than 5 MHz rates. The multi-functional capability of this device is provided by several features: 1) Additional gating is at the input to both shift registers so that the input is easily multiplexed between two sources. 2) The clock of each register may be provided separately or together. 3) Both the true and complementary outputs are provided from each eight bit register, and both registers may be master reset from a common input.

FEATURES

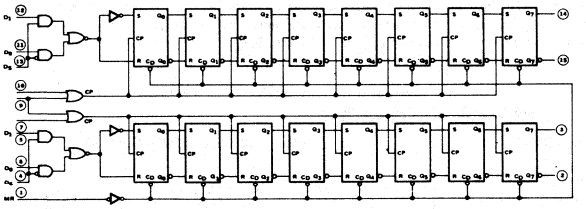
- **10 MHz TYPICAL SHIFT FREQUENCY**
- **TWO INPUT MULTIPLEXER PROVIDED AT DATA INPUT OF EACH REGISTER**
- **GATED CLOCK INPUT CIRCUITRY**
- **BOTH TRUE AND COMPLEMENTARY OUTPUTS PROVIDED FROM LAST BIT OF EACH REGISTER**
- **ASYNCHRONOUS MASTER RESET COMMON TO BOTH REGISTERS**
- **TYPICAL POWER DISSIPATION OF 80 mW**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **ALL CERAMIC "HERMETIC" 16 PIN DUAL IN-LINE AND FLAT PACKAGES**
- **TTμL COMPATIBLE**

PIN NAMES

D_S	Data Select Input
D_0, D_1	Data Inputs
C_P	Clock (Active High) Going Edge Input
	Common
	Separate
$\overline{MR}$	Master Reset (Active Low) Input
Q_7	Last Stage Output
$\overline{Q_7}$	Complementary Output

ORDER INFORMATION — Specify U7B93L28XXX for 16-pin Dual In-Line Package or U4L93L28XXX for 16-pin Flat Package, where XXX is 51X for the −55°C to +125°C temperature range, or 59X for the 0°C to +75°C temperature range.

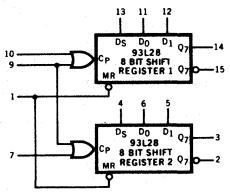
LOGIC DIAGRAM



V_{CC} = PIN 16
GND = PIN 8
○ = PIN NUMBERS

Fig. 4

LOGIC SYMBOL



V_{CC} = Pin 16
Gnd = Pin 8

Fig. 1

CONNECTION DIAGRAM
DIP (TOP VIEW)

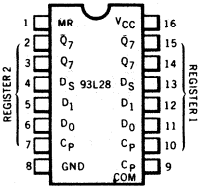


Fig. 2

FLATPAK (TOP VIEW)

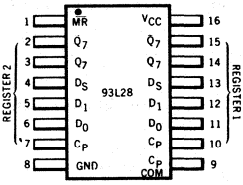


Fig. 3

FAIRCHILD
SEMICONDUCTOR

FUNCTIONAL DESCRIPTION — The two 8 bit shift registers have a common clock input (pin 9) and separate clock inputs (pins 10 & 7). The clocking of each register is controlled by the OR function of the separate and the common clock input. Each register is composed of eight clocked RS master-slave flip-flops and a number of gates. The clock OR gate drives the eight clock inputs of the flip-flops in parallel. When the two clock inputs (the separate and the common) to the OR gate are low, the slave latches are steady, but data can enter the master latches via the R and S input. During the first low to high transition of either, or both simultaneously, of the two clock inputs, the data inputs (R and S) are inhibited so that a later change in input data will not affect the master; then the now trapped information in the master is transferred to the slave. When the transfer is complete, both the master and the slave are steady as long as either or both clock inputs remain high. During the high to low transition of the last remaining high clock input, the transfer path from master to slave is inhibited first, leaving the slave steady in its present state; second the data inputs (R and S) are enabled so that new data can enter the master. Either of the clock inputs can be used as clock inhibit inputs by applying a logic high signal. Each 8 bit shift register has a two input multiplexer in front of the serial data input. The two data inputs D_0 and D_1 are controlled by the data select input D_S following the Boolean expression:
Serial data in: $S_D = \overline{D}_S D_0 + D_S D_1$

An asynchronous master reset is provided which, when activated by a low logic level, will clear all sixteen stages independently of any other input signal.

TABLE I — TTμL LOADING RULES

INPUTS	LOADING	
	High	Low
$\overline{MR}$, D_0, D_1	0.5 U.L.	0.25 U.L.
Separate CP (Pin 7 & 10)	0.75 U.L.	0.375 U.L.
D_S	1.0 U.L.	0.5 U.L.
Common CP (Pin 9)	1.5 U.L.	0.75 U.L.
OUTPUTS	**DRIVE FACTORS**	
	High	Low
Q_7 & $\overline{Q}_7$	8.0 U.L.	2.0 U.L.

Note: 1 Unit Load (U.L.) = 40 μA High/1.6 mA Low

TABLE II — TRUTH TABLE

SHIFT SELECTION

D_S	D_0	D_1	$Q_7(t_{n+8})$
L	L	X	L
L	H	X	H
H	X	L	L
H	X	H	H

n+8 = Indicates state after eight clock pulse
L = Low voltage level
H = High voltage level
X = Either high or low voltage level

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (D.C.)	−0.5 V to +5.5 V
*Input Current (D.C.)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output High)	−0.5 V to +V_{CC} value
Output Current (D.C.) (Output Low)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC}) MIN.	TYP.	MAX.	TEMPERATURE
U7B/4L93L2851X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
U7B/4L93L2859X	4.75 V	5.0 V	5.25 V	0°C to 75°C

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

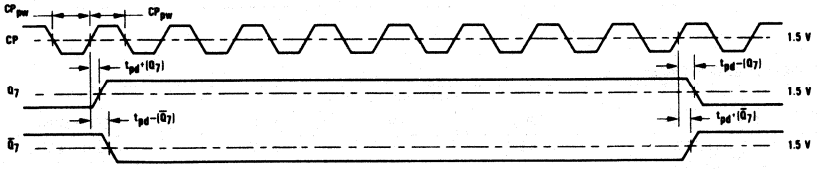
SYMBOL	CHARACTERISTIC	LIMITS MIN.	LIMITS TYP. (Note 4)	LIMITS MAX.	UNITS	CONDITIONS
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = −0.32 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.15	0.3	Volts	V_{CC} = MIN., I_{OL} = 3.2 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{IH}	Input HIGH Level	2.0			Volts	Guaranteed input logical HIGH voltage for all inputs
V_{IL}	Input LOW Level			0.7	Volts	Guaranteed input logical LOW voltage for all inputs
I_{IL}	Input LOW Current $\overline{MR}$, D_0 & D_1 CP (Pins 7 & 10) D_S $\overline{CP}$ (Pin 9)		 −0.25 −0.38 −0.50 −0.75	 −0.4 −0.6 −0.8 −1.2	mA	V_{CC} = MAX., V_{IN} = 0.3 V
I_{IH}	Input HIGH Current $\overline{MR}$, D_0 & D_1 CP (Pins 7 & 10) D_S $\overline{CP}$ (Pin 9)		 2.0 3.0 4.0 6.0	 20 30 40 60	µA	V_{CC} = MAX., V_{IN} = 2.4 V
	Input HIGH Current			1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{SC}	Output Short Circuit Current	−2.5	−16	−25	mA	V_{CC} = MAX., V_{OUT} = 0.0 V
I_{CC}	Power Supply Current		16	25.3	mA	V_{CC} = MAX.

NOTES:
(1) The actual testing Procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this Specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California (see page 1 for address and phone).
(2) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
(3) The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
(4) Typical limits are at V_{CC} = 5.0 V, 25°C, and max. loading.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	CONDITIONS & COMMENTS
t_{pd+} (Q_7 & $\overline{Q}_7$)	Turn-Off Delay (clock to output)		46		ns	V_{CC} = 5.0 V, C_L = 15 pF Fig. 5
t_{pd-} (Q_7 & $\overline{Q}_7$)	Turn-On Delay (clock to output)		65		ns	
t_{pd-} ($\overline{MR}$)	Turn-On Delay (Master reset to output)		90		ns	V_{CC} = 5.0 V, C_L = 15 pF Fig. 6 & 7
$\overline{CP}_{pw}$	Min. Clock Pulse Width		55		ns	V_{CC} = 5.0 V, C_L = 15 pF Fig. 5
$\overline{MR}_{pw}$ (CPH)	Min. Master Reset pulse width with clock high		37		ns	V_{CC} = 5.0 V, C_L = 15 pF Fig. 6
$\overline{MR}_{pw}$ (CPL)	Min. Master Reset pulse width with clock low		55		ns	V_{CC} = 5.0 V, C_L = 15 pF Fig. 7

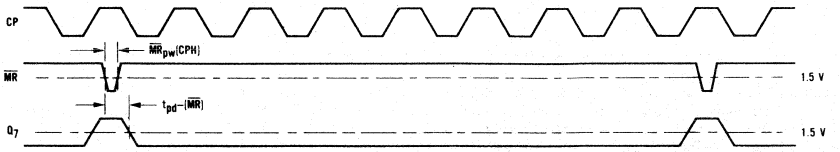
SWITCHING WAVEFORMS



Note: $\overline{Q}_7$ is connected to D_1. Other clock is grounded.

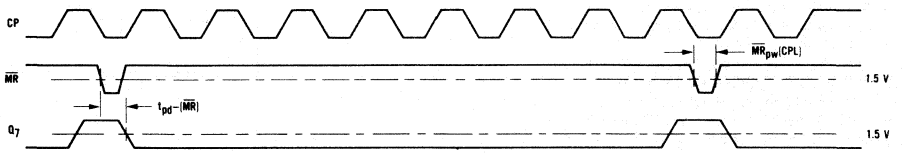
Fig. 5

SWITCHING WAVEFORMS (Cont'd)



Note: D_S, D_1, D_0 are high. Other clock input is grounded.

Fig. 6



Note: D_S, D_1, D_0 are high. Other clock input is grounded.

Fig. 7

APPLICATION

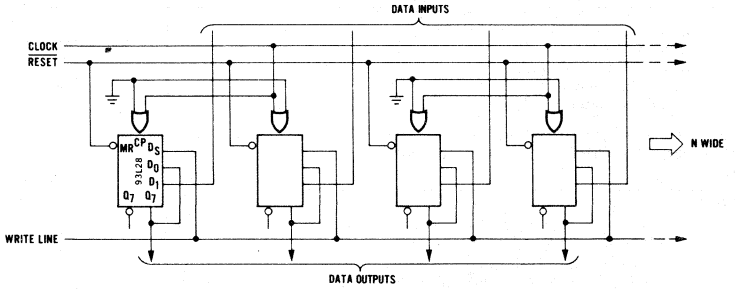


Fig. 8 N-BIT BY 8-WORD HIGH-SPEED MEMORY

PACKAGE INFORMATION

7B — 16 LEAD DUAL IN-LINE PACKAGE

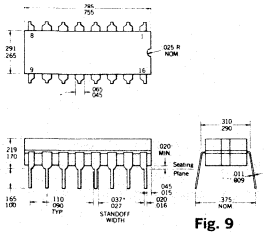


Fig. 9

NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.2 grams
*The .027/.037 dimension does not apply to the corner leads

4L — 16 LEAD (BeO) FLATPAK

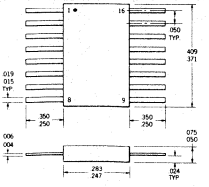


Fig. 10

NOTES:
All dimensions in inches
Leads are gold-plated kovar
Package weight is 0.4 gram

LPTTμL/MSI 93L40

LOW POWER 4-BIT ARITHMETIC LOGIC UNIT

A FAIRCHILD TTμL® IC PRODUCT

GENERAL DESCRIPTION — The low power TTμL/MSI 93L40 is a high speed arithmetic logic unit which can perform in parallel the arithmetic operations add or subtract, or either of six logic functions on two four-bit binary words. The device incorporates full carry-lookahead internally, and provides either a ripple carry output or carry-lookahead outputs. An internal carry input network accepts carry-lookahead outputs from up to three other packages producing a 16 bit full carry-lookahead ALU without additional gates. Ripple carries can be used between additional blocks of 12 bits to further expand the word length.

FEATURES:

- **MULTIFUNCTION CAPABILITY**
  Two Arithmetic Operations—Add, Subtract
  Six Logic Functions—A Ex or B, A and B, Plus Four Others
- **ADD TWO 4-BIT WORDS IN 85 ns**
- **LOOK-AHEAD CARRY INPUT AND OUTPUT NETWORKS ON CHIP**
- **EASILY EXPANDABLE TO LONGER WORD LENGTHS**
- **TYPICAL POWER DISSIPATION OF 110 mW**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **ALL CERAMIC "HERMETIC" 24 PIN DUAL IN-LINE AND FLAT PACKAGES**
- **TTμL COMPATIBLE**

PIN NAMES

$\overline{A}_0$ to $\overline{A}_3$, $\overline{B}_0$ to $\overline{B}_3$	Operand Active Low Inputs
S_0, S_1	Mode Select Inputs
$\overline{CG}_{-1}$	Active Low Carry Generate Input from immediately preceding stage
$\overline{CP}_{-1}$	Active Low Carry Propagate Input from immediately preceding stage
$\overline{CG}_{-2}$	Active Low Carry Generate Input from second preceding stage
$\overline{CP}_{-2}$	Active Low Carry Propagate Input from second preceding stage
$\overline{CG}_{-3}$	Active Low Carry Generate Input from third preceding stage
CO_E	Carry Out Enable Input
$\overline{F}_0$, $\overline{F}_1$, $\overline{F}_2$, $\overline{F}_3$	Function (Active Low) Outputs
$\overline{CO/CG}$	Carry Out/Carry Generate (Active Low) Output
$\overline{CP}$	Carry Propagate (Active Low) Output

ORDER INFORMATION – Specify U6N93L40XXX for 24 pin Dual In-Line Package or U4M93L40XXX for 24 pin Flatpak, where XXX is 51X for the −55°C to +125°C temperature range, or 59X for the 0°C to +75°C temperature range.

LOGIC DIAGRAM

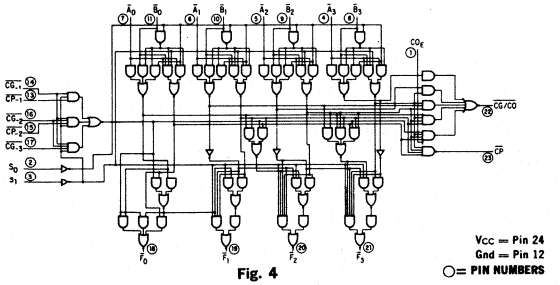


Fig. 4

LOGIC SYMBOL

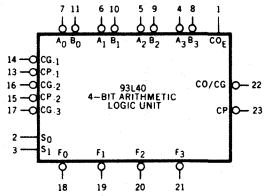


Fig. 1

CONNECTION DIAGRAM

DIP (TOP VIEW)

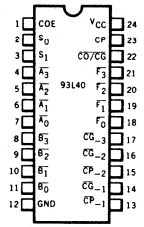


Fig. 2

FLATPAK (TOP VIEW)

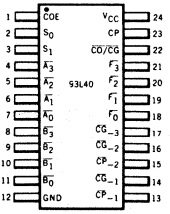


Fig. 3

FAIRCHILD
SEMICONDUCTOR

FUNCTIONAL DESCRIPTION — The 93L40 accepts two four-bit words, A_0, A_1, A_2, A_3 (A_{0-3}) and B_0, B_1, B_2, B_3 (B_{0-3}), and produces a four-bit output, F_0, F_1, F_2, F_3 (F_{0-3}). The output function is determined by the states on the control lines S_0 and S_1. The inputs and outputs of the 93L40 may be considered to be active level low or active level high. Logic equivalents for four representations of the 93L40 are shown in Figure 5a, b, c, and d.

The add and subtract operations are performed on the entire word, with carries or borrows propagated between bits of different weight. The arithmetic may be performed in 1's complement, 2's complement, or sign-magnitude notation. In the logic modes, carries are inhibited and the device acts like four gates of the type shown in Figure 5.

To achieve high speed operation, the 93L40 is designed to be used in a carry lookahead system. Full carry lookahead is used inside the device to propagate carries between bits. Carry lookahead functions over the four bit block are available as outputs. These outputs are labeled $\overline{CO/CG}$ (Carry Out/Carry Generate) and $\overline{CP}$ (Carry Propagate) on the logic symbol. The carry in to the device is formed from a set of Carry Generate and Carry Propagate inputs (equation 1) so that three 93L40's can be interconnected without any additional gates to form a 12 bit full carry lookahead ALU with a carry in. The pin labeled CO_E (Carry Out Enable) controls the $\overline{CO/CG}$ output according to equation 2. When CO_E is high, $\overline{CO/CG}$ becomes a Carry Out which can be used to ripple carries between blocks of 12 bits. The $\overline{CG_{-1}}$ input can be used for a ripple carry input, since this signal is sufficient to produce a carry in.

Both ripple carry and carry lookahead are illustrated in Figure 6 in the applications section which shows a 16 bit ALU and indicates how it can be expanded.

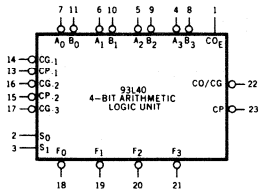
(1) $(\overline{CG_{-1}}) + (\overline{CP_{-1}})(\overline{CG_{-2}}) + (\overline{CP_{-1}})(\overline{CP_{-2}})(\overline{CG_{-3}}) = C_{in}$ (internal)

(2) $\overline{CO/CG} = (\overline{CG}) + (\overline{CP})(C_{in})(CO_E)$

Fig. 5 — FUNCTION TABLES FOR LOGIC EQUIVALENTS OF THE 93L40

Note that when the input operants are defined as active high, the carry lookahead inputs and outputs are not formally carry generate and carry propagate. Consequently, these pins have been relabeled CX and CY in the active high cases. However, the signals are connected in the same manner as $\overline{CG}$ and $\overline{CP}$.

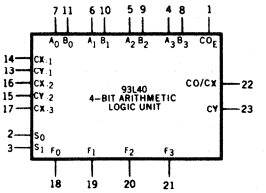
5a — ACTIVE LOW OPERANDS



V_{CC} = Pin 24
Gnd = Pin 12

CONTROL INPUTS S_0	CONTROL INPUTS S_1	OPERATION	EQUIVALENT LOGIC
L	L	A SUBTRACT B	
H	L	A ADD B	
L	H	A EX OR B	
H	H	A AND B	

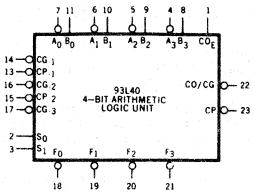
5b — ACTIVE HIGH OPERANDS



V_{CC} = Pin 24
Gnd = Pin 12

CONTROL INPUTS S_0	CONTROL INPUTS S_1	OPERATION	EQUIVALENT LOGIC
L	L	A SUBTRACT B	
H	L	A ADD B	
L	H	A EQUIV B	
H	H	A OR B	

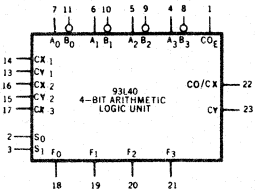
5c — ACTIVE LOW OPERANDS WITH INVERTED B



V_{CC} = Pin 24
Gnd = Pin 12

CONTROL INPUTS S_0	CONTROL INPUTS S_1	OPERATION	EQUIVALENT LOGIC
L	L	A ADD B	
H	L	A SUBTRACT B	
L	H	A EQUIV B	
H	H	A AND $\overline{B}$	

5d — ACTIVE HIGH OPERANDS WITH INVERTED B



V_{CC} = Pin 24
Gnd = Pin 12

CONTROL INPUTS S_0	CONTROL INPUTS S_1	OPERATION	EQUIVALENT LOGIC
L	L	A ADD B	
H	L	A SUBTRACT B	
L	H	A EX OR B	
H	H	A OR $\overline{B}$	

TTμL LOADING RULES

INPUTS	LOADING HIGH	LOADING LOW
S_0, S_1, $\overline{CP}_{-1}$, $\overline{CP}_{-2}$, $\overline{CG}_{-3}$	0.5U.L.	0.25U.L.
CO_E	0.5U.L.	0.375U.L.
$\overline{CG}_{-2}$	1.0U.L.	0.50U.L.
A_0 - A_3, B_0 - B_3, $\overline{CG}_{-1}$	1.5U.L.	0.75U.L.
OUTPUTS	**DRIVE FACTORS HIGH**	**DRIVE FACTORS LOW**
$\overline{F_0}$, $\overline{F_1}$, $\overline{F_2}$, $\overline{F_3}$, $\overline{CP}$, $\overline{CG/CO}$	10U.L.	2.5U.L.

Note: 1 Unit Load (U.L.) = 40 μA High/1.6 mA Low

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (D.C.)	−0.5 V to +5.5 V
*Input Current (D.C.)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output High)	−0.5 V to +V_{CC} value
Output Current (D.C.) (Output Low)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC}) MIN.	TYP.	MAX.	TEMPERATURE
U6N/4M93L4051X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
U6N/4M93L4059X	4.75 V	5.0 V	5.25 V	0°C to 75°C

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

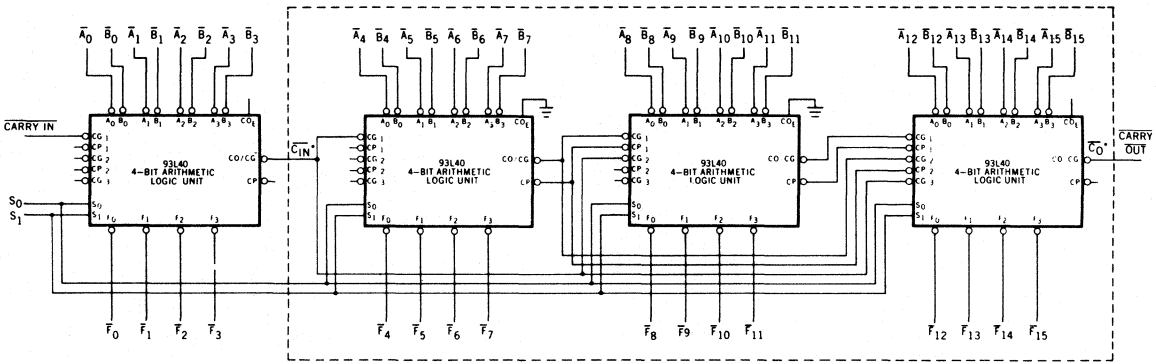
SYMBOL	CHARACTERISTIC	LIMITS MIN.	TYP. Note 4	MAX.	UNITS	CONDITIONS
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = −0.4 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.15	0.3	Volts	V_{CC} = MIN., I_{OL} = 4.0 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{IH}	Input HIGH Level	2.0			Volts	Guaranteed input logical HIGH voltage for all inputs
V_{IL}	Input LOW Level			0.7	Volts	Guaranteed input logical LOW voltage for all inputs
I_{IL}	Input LOW Current S_0, S_1, $\overline{CP}_1$, $\overline{CP}_2$ & $\overline{CG}_3$ CO_E $\overline{CG}_2$ $\overline{A}$, $\overline{B}$, $\overline{CG}_1$		 −0.25 −0.38 −0.50 −0.75	 −0.4 −0.6 −0.8 −1.2	mA	V_{CC} = MAX., V_{IN} = 0.3 V
I_{IH}	Input HIGH Current S_0, S_1, $\overline{CP}_1$, $\overline{CP}_2$, $\overline{CG}_3$ & CO_E $\overline{CG}_2$ $\overline{A}$, $\overline{B}$, $\overline{CG}_1$		 2.0 4.0 6.0	 20 40 60	μA	V_{CC} = MAX., V_{IN} = 2.4 V
	Input HIGH Current			1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{SC}	Output Short Circuit Current	−10	−22	−40	mA	V_{CC} = MAX., V_{OUT} = 0.0 V
I_{CC}	Power Supply Current		22	37	mA	V_{CC} = MAX.

NOTES:
(1) The actual testing Procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this Specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California (see page 1 for address and phone).
(2) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
(3) The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
(4) Typical limits are at V_{CC} = 5.0 V, 25°C, and max. loading.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	CHARACTERISTIC	TYPICAL LIMITS ADD	SUBTRACT	UNITS	CONDITIONS
t_{pd+} t_{pd-}	Data Input to Data Output ($\overline{B}_0$ to $\overline{F}_3$)	92 74	92 91	ns ns	
t_{pd+} t_{pd-}	Data Input to Carry Output ($\overline{B}_0$ to $\overline{CO/CG}$)	62 44	59 61	ns ns	C_L = 15 pF V_{CC} = 5.0 V
t_{pd+} t_{pd-}	Carry Input to Carry Output ($\overline{CG}_{-1}$ to $\overline{CO/CG}$)	53 45	53 45	ns ns	
t_{pd+} t_{pd-}	Carry Input to Data Output ($\overline{CG}_{-1}$ to $\overline{F}_3$)	85 75	85 75	ns ns	

APPLICATIONS



For 1's complement arithmetic, connect $\overline{\text{Carry In}}$ to $\overline{\text{Carry Out}}$
For 2's complement arithmetic, connect $\overline{\text{Carry In}}$ to S_0

FUNCTION TABLE

S_0	S_1	FUNCTION
L	L	A SUBTRACT B
H	L	A ADD B
L	H	A EX OR B
H	H	A AND B

H = High Voltage Level
L = Low Voltage Level

DELAY TABLE

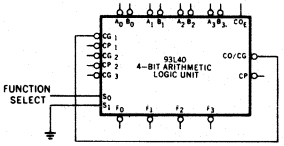
WORD LENGTH (in bits)	ADD (in ns)	SUBTRACT (in ns)
1-4	85	95
5-16	135	145
17-28	185	195
29-40	235	245
41-52	285	295
53-64	335	345

Fig. 6 – 93L40 16-BIT FULL LOOKAHEAD CARRY ALU

Shown above is a 16 bit ALU with full carry lookahead. For 2's complement arithmetic a carry-in must be forced in subtraction; this may be done by connecting the $\overline{\text{carry in}}$ to the S_0 control line. For 1's complement arithmetic, an "end around carry" is required, so the $\overline{\text{carry out}}$ should be connected to the $\overline{\text{carry in}}$. Care must be exercised in 1's complement mode due to problems associated with logic oscillations between the two possible representations of zero.

The portion shown within the dashed lines is a 12 bit full lookahead ALU with a carry in $\overline{C_{in}}^*$ and carry out $\overline{C_0}^*$. If an ALU longer than 16 bits is required, then additional 12 bit blocks like the one shown may be added with a ripple carry between the blocks, $\overline{C_0}^*$ of one block goes to $\overline{C_{in}}^*$ of the next. In the 16 bit ALU, the very first 93L40 does not add any delay, even though it is used in a triple carry mode, because the $\overline{\text{carry in}}$ appears at $\overline{\text{CO/CG}}$ just as fast as the input operands appear. Note that this is true only for the first 93L40, because only at this point are the inputs and the carry in available simultaneously.

APPLICATIONS (CONT'D)



S_0	FUNCTION
L	A SUBTRACT B
H	A ADD B

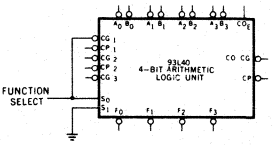


Fig. 7a — FOUR BIT ADDER/SUBTRACTOR USING 1's COMPLEMENT ARITHMETIC

This figure illustrates a 1's complement Adder/Subtractor with active low inputs and outputs. Connection from $\overline{CO/CG}$ to $\overline{CG_{-1}}$ represents end around carry from the most significant to the least significant unit. Care must be exercised in this mode due to problems associated with logic oscillations between the two possible representations of zero.

Fig. 7b — FOUR BIT ADDER/SUBTRACTOR USING 2's COMPLEMENT ARITHMETIC

This figure shows a 2's complement Adder/Subtractor with low inputs and outputs. The S_0 terminal is connected to the $\overline{CG_{-1}}$ so as to provide an addition of one to the least significant bit during subtraction.

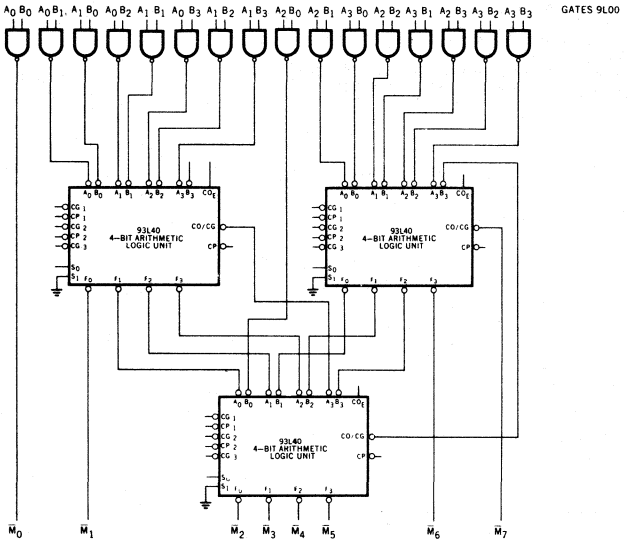
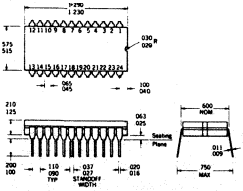


Fig. 8 — 4x4 MULTIPLICATION

This figure illustrates a 4x4 multiplier which uses four 9L00 gate packages preceding a network of 93L40 arithmetic logic units connected as adders. This scheme can be extended to provide multiplication over larger word lengths.

PACKAGE INFORMATION

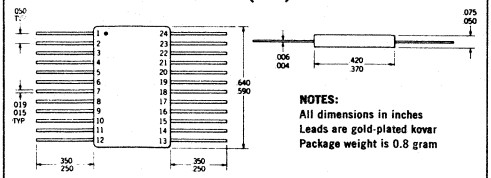
6N — 24 LEAD DUAL IN-LINE PACKAGE



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .600" centers. They are purposely shipped with "positive" misalignment to facilitate insertion
Leads are tin-plated kovar
Package weight is 6.5 grams

Fig. 9

4M — 24 LEAD (BeO) FLATPAK



NOTES:
All dimensions in inches
Leads are gold-plated kovar
Package weight is 0.8 gram

Fig. 10

TTL/MSI 93H00
HIGH SPEED UNIVERSAL 4-BIT SHIFT REGISTER

GENERAL DESCRIPTION — The 93H00 is a TTL / MSI 4-Bit Universal Shift Register offering a typical shift frequency to 55 MHz and guaranteed minimum value of 45 MHz. These features make the 93H00 useful in a wide range of high speed register and counter applications. These include serial-serial, shift left, shift right, serial-parallel, parallel-serial and parallel-parallel data registers.

The 93H00 is pin compatible with the 9300A and 93L00 shift registers. Major electrical differences are the speed of operation and resulting power dissipation.

- 55 MHz TYPICAL SHIFT FREQUENCY
- ASYNCHRONOUS COMMON RESET
- J, $\overline{K}$ INPUTS TO FIRST STAGE
- SYNCHRONOUS PARALLEL ENTRY
- TYPICAL POWER DISSIPATION OF 350 mW
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- PIN FOR PIN COMPATIBLE WITH 9300A AND 93L00 DEVICES

PIN NAMES		LOADING (Note 1)
$\overline{PE}$	Parallel Enable (Active LOW) Input	1 U.L.
P_0, P_1, P_2, P_3	Parallel Inputs	1 U.L.
J	First Stage J (Active HIGH) Input	1 U.L.
$\overline{K}$	First Stage K (Active LOW) Input	1 U.L.
CP	Clock (Active HIGH) Going Edge Input	2 U.L.
MR	Master Reset (Active LOW) Input	1 U.L.
Q_0, Q_1, Q_2, Q_3	Parallel Outputs (Note 2)	10 U.L.
$\overline{Q}_3$	Complementary Last Stage Output (Note 2)	10 U.L.

NOTES:
(1) 1 Unit Load (U.L.) = 40 μA High/−1.6 mA Low
(2) 10 U.L. is the output Low drive factor and 20 U.L. is the output High drive factor.

LOGIC DIAGRAM

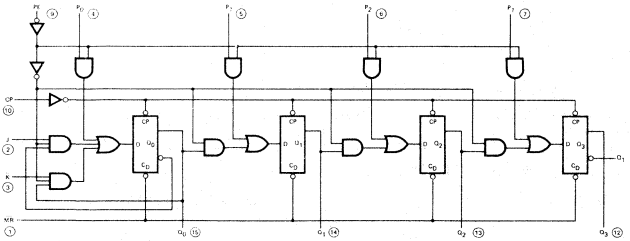
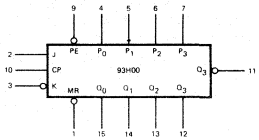


Fig. 4 ◯ = Pin Numbers

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

Fig. 1

CONNECTION DIAGRAM
DIP (TOP VIEW)

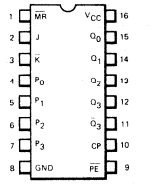


Fig. 2

FLATPAK (TOP VIEW)

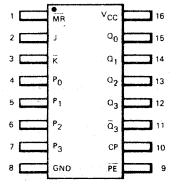


Fig. 3

FAIRCHILD
SEMICONDUCTOR

FUNCTIONAL DESCRIPTION – The logic symbol of Figure 2 provides an indication of the functional characteristics of the 93H00 4-bit shift register. Several special logical features of the 93H00 design which provide a high degree of general usefulness are described below:

1. A $J\overline{K}$ input is provided to the first flip flop in the register. This type of input is the same as the more common JK input except that the low voltage level activates the $\overline{K}$ input. This provides the greater power of the JK type input for more general applications and at the same time the simple D type input that is most appropriate for a shift register can be easily obtained by simply tying the two inputs together.
2. There is no restriction on the activity of the J or $\overline{K}$ inputs for logical operation—except for the set up and release time requirements.
3. Parallel inputs for all four stages are provided. These will determine the next condition of the shift register synchronous with the clock input, whenever the Parallel Enable input is LOW. With the Parallel Enable input LOW the element appears as four common clocked D flip flops. When the Parallel Enable is HIGH, or not connected, the shift register performs a one bit shift for each clock input. In both cases the next state of the flip flops occurs after the LOW to HIGH transition of the clock input.
4. An internal clock buffer provides both reduced clock input loading, and the ability to gate the clock with only a single NAND gate.
5. The active HIGH output is provided for all four stages and an active LOW output is provided for the last stage.
6. A master asynchronous reset input allows the setting to zero of all stages, independent of the condition of any other inputs.

TRUTH TABLES

TABLE I – SERIAL ENTRY
($\overline{PE}$ = HIGH, $\overline{MR}$ = HIGH)

J	$\overline{K}$	Q_0 at t_{n+1}
L	L	L
L	H	Q_0 at t_n (no change)
H	L	$\overline{Q}_0$ at t_n (toggles)
H	H	H

TABLE II – SERIAL ENTRY
($\overline{PE}$ = HIGH, $\overline{MR}$ = HIGH)

J&$\overline{K}$ Connected	Q_0 at t_{n+1}
L	L
H	H

TABLE III – PARALLEL ENTRY
($\overline{PE}$ = LOW, $\overline{MR}$ = HIGH)

D-Input (P_0, P_1, P_2 or P_3)	Output Q at t_{n+1} (Q_0, Q_1, Q_2 or Q_3).
L	L
H	H

(n+1) = Indicates state after next clock

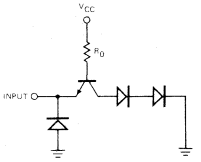
TABLE IV – MODE SELECTION

	$\overline{PE}$	P_0	P_1	P_2	P_3	J	$\overline{K}$	$\overline{MR}$
Serial Entry	H	X	X	X	X	Refer to Table I & II		H
Parallel Entry	L	Refer to Table III				X	X	H

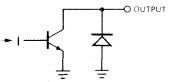
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

TYPICAL INPUT AND OUTPUT CIRCUITS

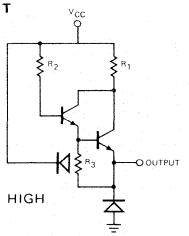
INPUTS EQUIVALENT CIRCUIT



OUTPUTS EQUIVALENT CIRCUIT



LOW



HIGH

Fig. 5
INPUT CURRENT VERSUS INPUT VOLTAGE

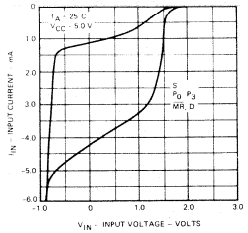


Fig. 6
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE LOW STATE

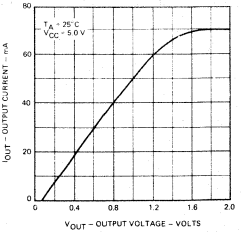
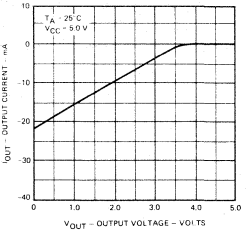


Fig. 7
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE HIGH STATE



ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (D.C.)	−0.5 V to +5.5 V
*Input Current (D.C.)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (D.C.) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			AMBIENT TEMPERATURE
	MIN.	TYP.	MAX.	
U7B/4L93H0051X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
U7B/4L93H0059X	4.75 V	5.0 V	5.25 V	0°C to 75°C

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	CHARACTERISTIC	LIMITS MIN.	LIMITS TYP. (Note 4)	LIMITS MAX.	UNITS	CONDITIONS
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = −0.64 mA (−0.8 mA, Pin 11) V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.2	0.4	Volts	V_{CC} = MIN., I_{OL} = 12.8 mA (16 mA, Pin 11) V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{IH}	Input HIGH Level	2.0			Volts	Guaranteed Input Logical HIGH Voltage for All Inputs
V_{IL}	Input LOW Level			0.8	Volts	Guaranteed Input Logical LOW Voltage for All Inputs
I_{IL}	Input LOW Current J, $\overline{K}$, $\overline{MR}$, P_0, P_1, P_2 & P_3, $\overline{PE}$ CP		 −0.96 −1.92	 −1.6 −3.2	mA	V_{CC} = MAX., V_{IN} = 0.4 V
I_{IH}	Input HIGH Current J, $\overline{K}$, $\overline{MR}$, P_0, P_1, P_2 & P_3, $\overline{PE}$ CP			 40 80	µA	V_{CC} = MAX., V_{IN} = 2.4 V
	Input HIGH Current			1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{SC}	Output Short Circuit Current (Note 5)	−30	−75	−100	mA	V_{CC} = MAX., V_{OUT} = 0.0 V
I_{CC}	Power Supply Current 51X		65	102	mA	V_{CC} = MAX.
	Power Supply Current 59X		65	112		

NOTES:
(1) The actual Testing Procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this Specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California (see page 1 for address and phone).
(2) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
(3) The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
(4) Typical limits are at V_{CC} = 5.0 V, 25°C, and max. loading.
(5) Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	CHARACTERISTIC	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS	
f_{sr}	Shift Right Frequency	45	55		MHz	Fig. 8	V_{CC} = 5.0 V, C_L = 15 pF
t_{PLH}	Turn Off Delay from Clock to Output		10	16	ns		
t_{PHL}	Turn on Delay from Clock to Output		14.5	21	ns		
t_{PHL} ($\overline{MR}$)	Turn on Delay from $\overline{MR}$ to Output (Except $\overline{Q}_3$)		21	28	ns	Fig. 9	

SWITCHING SET-UP REQUIREMENTS (T_A = 25°C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS	
t_{pw} (CP)	Clock Pulse Width	12	9		ns	Fig. 8	V_{CC} = 5.0 V
t_s (Data)	Set-Up Time Data to Clock	12	6		ns	Fig. 10	
t_h (Data)	Hold Time Data to Clock	0	−5		ns		
t_s ($\overline{PE}$)	Set-Up Time $\overline{PE}$ to Clock	15	8		ns	Fig. 11	
t_h ($\overline{PE}$)	Hold Time $\overline{PE}$ to Clock	0	−7		ns		
t_{pw} ($\overline{MR}$)	Master Reset Pulse Width	19	11		ns	Fig. 9	
t_{rec} ($\overline{MR}$)	Recovery Time Master Reset to Clock	7	3		ns		

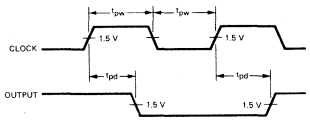
SET-UP TIME (t_s) is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to insure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

RECOVERY TIME (t_{rec}) is defined as the minimum time required between the end of the Reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH Data to the Q outputs.

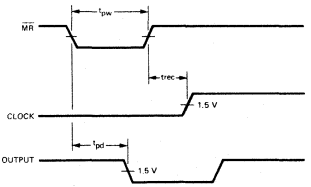
MSI 93H00 SWITCHING TIME WAVEFORMS

The shaded areas indicate when the input is permitted to change for predictable output performance.



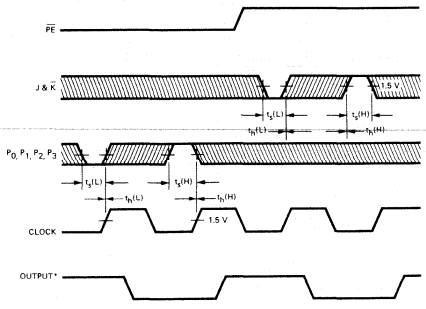
Other Conditions: $J = \overline{PE} = \overline{MR} = H$
$\overline{K} = L$

Fig. 8 — CLOCK TO OUTPUT DELAYS & CLOCK PULSE WIDTH



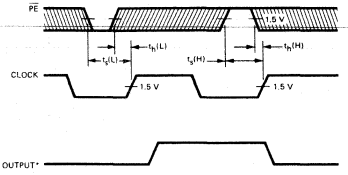
Other Conditions: $\overline{PE}$ = L
$P_0 = P_1 = P_2 = P_3 = H$

Fig. 9 — MASTER RESET PULSE WIDTH, MASTER RESET TO OUTPUT DELAY & MASTER RESET TO CLOCK RECOVERY TIME



Other Conditions: $\overline{MR}$ = H
*J&$\overline{K}$ Set-Up Time Affects Q_0 Only

Fig. 10 — SET-UP (t_s) AND HOLD (t_h) TIME FOR SERIAL DATA (J&$\overline{K}$) AND PARALLEL DATA (P_0, P_1, P_2, P_3)



Other Conditions: $\overline{MR}$ = H, J = $\overline{K}$ = L
$P_0 = P_1 = P_2 = P_3 = H$
*t_s(H) and t_h(H) Affects Q_0 Only

Fig. 11 — SET-UP (t_s) AND HOLD (t_h) TIME FOR $\overline{PE}$ INPUT

APPLICATIONS

APPLICATIONS – The 93H00 has been designed to be useful in a wide variety of applications. The multifunctional capability of the Fairchild 93H00 is illustrated by the applications shown below.

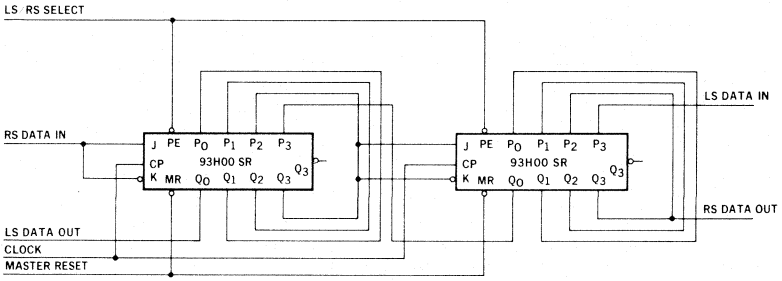


Fig. 12 – 8-BIT LEFT/RIGHT SHIFT REGISTER

This register shifts Left or Right on each shift clock, depending upon the condition of the $\overline{LS}$/RS SELECT input. If this input is HIGH, Right Shift occurs and if LOW, Left Shift occurs.

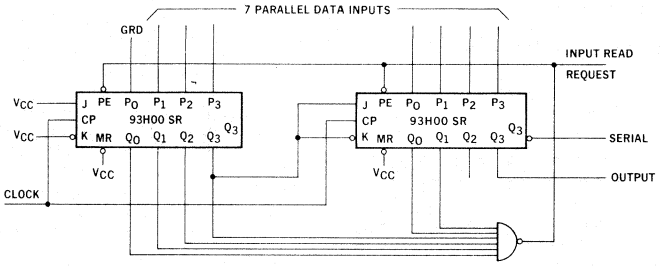


Fig. 13 – 7-BIT PARALLEL TO SERIAL CONVERTER

This parallel to serial converter uses a marker bit, to count the data bits shifted out, so that a parallel load enable is generated to load the next parallel word for conversion at the correct time.

APPLICATIONS (Cont'd)

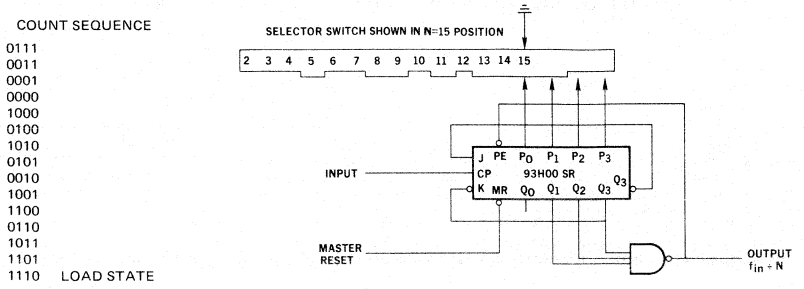


Fig. 14 – DIVIDE BY N COUNTER FOR N = 2 TO 15

This counter produced an output pulse for every N input pulses, where the number N is determined by the setting of the slide selector switch as shown or by logic inputs to the parallel data lines from an external source.

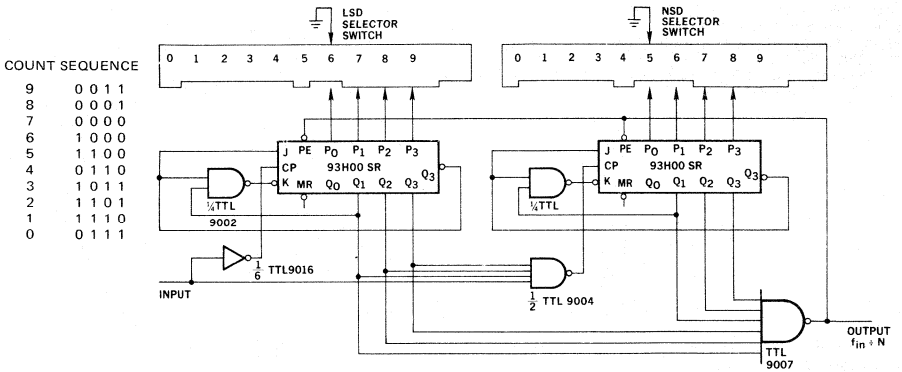


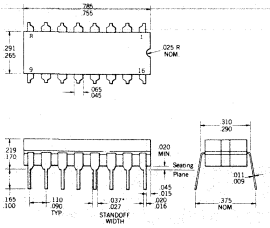
Fig. 15 – TWO DECADE PROGRAMMABLE DIVIDER

This circuit divides by any number "N" from 1 to 100. The selected N is one greater than is shown on the slide switches. As an example the switches are showing 56, therefore the circuit will divide by 57 with this setting.

ORDER INFORMATION – Specify UXX93H0059X for the 0°C to +75°C temperature range, or UXX93H0051X for the –55°C to +125°C temperature range, where XX is 78 for the 16 pin Dual In-Line package or 4L for the 16 pin Flatpak.

PACKAGE INFORMATION

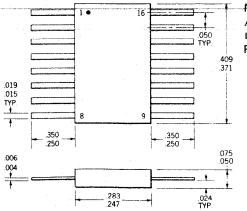
7B – 16 LEAD DUAL IN-LINE PACKAGE



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.2 grams
*The .037/.027 dimension does not apply to the corner leads

Fig. 16

4L – 16 LEAD (BeO) FLATPAK



NOTES:
All dimensions in inches
Leads are gold-plated kovar
Package weight is 0.4 gram

Fig. 17

TTL/MSI 93H72
HIGH SPEED 4-BIT SHIFT REGISTER WITH ENABLE

GENERAL DESCRIPTION – The 93H72 high speed MSI four-bit shift register is a multifunctional sequential logic block which is useful in a wide variety of register applications. It may be used in serial-serial, shift left, shift right, serial-parallel, parallel-serial, and parallel-parallel data transfers. The circuit is compatible with all Fairchild 9300 MSI TTL Integrated circuits.

The 93H72 has three synchronous modes of operation, shift, parallel load and hold (do nothing). The hold capability permits information storage in the register independent of the clock.

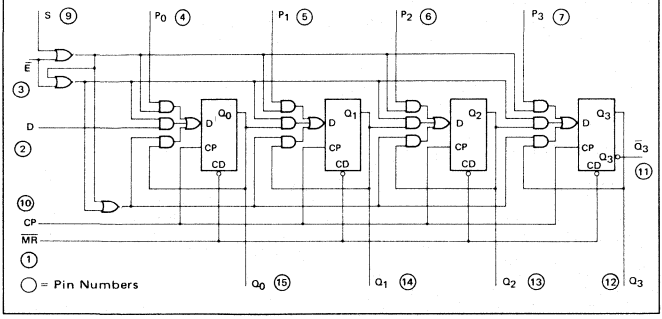
FEATURES

- **55–60 MHz TYPICAL SHIFT FREQUENCY**
- **SYNCHRONOUS PARALLEL ENTRY**
- **DATA HOLD (DO NOTHING) INDEPENDENT OF CLOCK**
- **FULLY SYNCHRONOUS WITH EDGE TRIGGERED TYPE CHARACTERISTICS ON INPUTS (EXCEPT $\overline{MR}$)**
- **ASYNCHRONOUS MASTER RESET**
- **TYPICAL POWER DISSIPATION OF 475 mW**
- **TTL COMPATIBLE**
- **ALL CERAMIC "HERMETIC" 16 PIN DUAL IN-LINE AND FLAT PACKAGES**
- **INPUT CLAMP DIODES**

PIN NAMES		LOADING
$\overline{E}$	Active Low Enable Input	2 U.L.
S	Shift Enable Input	1 U.L.
P_0, P_1, P_2, P_3	Parallel Data Inputs	1 U.L.
CP	Clock Input	2 U.L.
$\overline{MR}$	Master Reset Input	1 U.L.
Q_0 to Q_3	Parallel Outputs	10 U.L.*
$\overline{Q}_3$	Last Stage Complementary Output	10 U.L.*
D	Serial Data Input	1 U.L.

1 Unit Load (U.L.) = 40 μA High/1.6 mA Low
*Note: 10 U.L. is the output Low drive factor and 20 U.L. is the output High drive factor.

LOGIC DIAGRAM



Order information on last page.

LOGIC SYMBOL

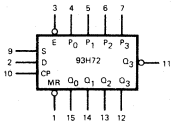


Fig. 1

CONNECTION DIAGRAM DIP (TOP VIEW)

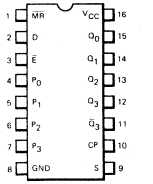


Fig. 2

FLAT PAK (TOP VIEW)

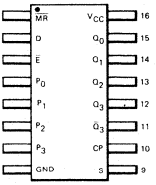


Fig. 3

FAIRCHILD SEMICONDUCTOR

FUNCTIONAL DESCRIPTION – The 93H72 is a four-bit shift register with three modes of operation: shift, parallel load and hold (do nothing). The register is fully synchronous with any output change occurring after the rising clock edge. The 93H72 features edge triggered type characteristics on all inputs (except $\overline{MR}$) which means there are no restrictions on the activity of these inputs (S, $\overline{E}$, P_0, P_1, P_2, P_3, D) for logic operation except for the set up requirements prior to the low to high clock transition.

The mode of operation of the 93H72 is determined by the two inputs, shift enable (S) and enable ($\overline{E}$) as shown in Table I. The active low enable, when high places the register in the hold mode with the register flip-flops retaining their information. When the enable is activated (low) the shift enable (S) determines whether the register operates in a shift or parallel data entry modes.

When the enable is low and the shift control input is low the parallel inputs are selected and will determine the next condition of the register synchronously with the clock as shown in Table II. In this mode the element appears as four common clocked D flip-flops. With $\overline{E}$ low and the shift input high the device acts as a four-bit shift register with serial data entry through the D input shown in Table III. In both cases, as mentioned before, the next state of the flip-flops occur after the low to high transition of the clock input.

The asynchronous active low master reset overrides all inputs and clears the register forcing outputs Q_{0-3} low and $\overline{Q}_3$ high.

Table I. MODE SELECTION

MODE	S	$\overline{E}$	$\overline{MR}$	P_0	P_1	P_2	P_3	D
Parallel Load	L	L	H	See Table II				X
Serial Shift	H	L	H	X	X	X	X	See Table III
Hold	X	H	H	X	X	X	X	X
Reset	X	X	L	X	X	X	X	X

Table III. SERIAL DATA ENTRY

D INPUT AT t_n	Q_0 AT t_{n+1}
L	L
H	H

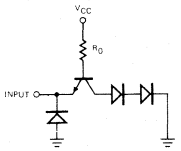
Table II. PARALLEL DATA ENTRY

P_0, P_1, P_2 OR P_3 INPUT AT t_n	Q at t_{n+1}
L	L
H	H

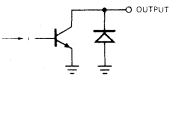
L = Low Voltage Level
H = High Voltage Level
X = Don't Care
t_n = Present State
t_{n+1} = State After Next Clock

TYPICAL INPUT AND OUTPUT CIRCUITS

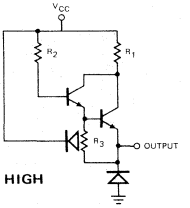
INPUTS EQUIVALENT CIRCUIT



OUTPUTS EQUIVALENT CIRCUITS



LOW



HIGH

Fig. 5
INPUT CURRENT VERSUS INPUT VOLTAGE

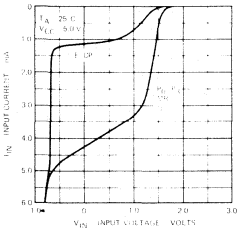


Fig. 6
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE LOW STATE

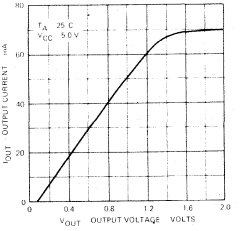
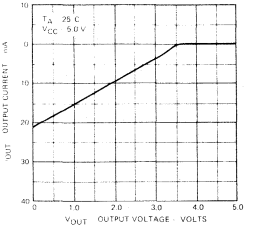


Fig. 7
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE HIGH STATE



ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (D.C.)	−0.5 V to +5.5 V
*Input Current (D.C.)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output High)	0.5 V to +V_{CC} value
Output Current (D.C.) (Output Low)	+30 mA

*Either Input Voltage Limit or Input Current is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
U7B/U4L93H7251X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
U7B/U4L93H7259X	4.75 V	5.0 V	5.25 V	0°C to 75°C

ELECTRICAL CHARACTERISTICS (Over operating temperature ranges)

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		MIN.	TYP.	MAX.		
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input High Threshold For All Inputs
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input Low Threshold For All Inputs
V_{OH}	Output HIGH Voltage	2.4	2.7		Volts	V_{CC} = MIN., I_{OH} = −800 μA
V_{OL}	Output LOW Voltage		0.25	0.4	Volts	V_{CC} = MIN., I_{OL} = 16.0 mA
I_{IL}	Input Load Current $\overline{MR}$, D, P_0, P_1, P_2, P_3, S		−1.08	−1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V
I_{IL}	Input Load Current $\overline{E}$, CP		−2.16	−3.2	mA	V_{CC} = MAX., V_{IN} = 0.4 V
I_{IH}	Input Leakage Current $\overline{MR}$, D, P_0, P_1, P_2, P_3, S		10	40	μA	V_{CC} = MAX., V_{IN} = 2.4 V
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{IH}	Input Leakage Current $\overline{E}$, CP		20	80	μA	V_{CC} = MAX., V_{IN} = 2.4 V
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{PD}	Supply Current		95	120	mA	V_{CC} = MAX., 51X
			100	135	mA	V_{CC} = MAX., 59X
I_{SC}	Short-Circuit Output Current	30	75	100	mA	V_{CC} = MAX., V_{OUT} = 0.0 V, Only One Output Shorted at Any Time

SWITCHING CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V, C_L = 15 pF)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS AND COMMENTS
f_{max}	Maximum Shift Frequency	45	57		MHz	
t_{pd-}	Turn On Delay from Positive Clock Edge to Any Output		14.5	21	ns	Fig. 8
t_{pd+}	Turn Off Delay from Positive Clock Edge to Any Output		10	16	ns	Fig. 8
t_{pd-} ($\overline{MR}$)	Delay from Master Reset to Any Output		19	28	ns	Fig. 11
t_s (Data)	Setup Time for Data (D, P_0, P_1, P_2, P_3)	7.0	3.5		ns	Fig. 10
t_s ($\overline{E}$)	Setup Time for Enable, $\overline{E}$	17	9.0		ns	Fig. 9
t_s (S)	Setup Time for Shift Control, S	19	10		ns	Fig. 8
t_{rec}($\overline{MR}$)	Recovery Time for $\overline{MR}$	7.0	3.0		ns	Fig. 11
t_{pw} $\overline{MR}$	Required Pulse Width for $\overline{MR}$		11	19	ns	Fig. 11
t_{HOLD} (Data) ($\overline{E}$) or (S)	Hold Time for Data, $\overline{E}$, or S	0			ns	Fig. 8, 9 and 10

NOTES
1. The actual Testing Procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this Specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. SET-UP TIME: t_s is defined as the minimum time required for the logic level to be present at the logic input prior to the clock transition from low to high in order for the register to respond.
5. HOLD TIME: t_{HOLD} is defined as the minimum time following the clock transition from low to high that the logic level must be maintained to insure continued recognition.
6. RECOVERY TIME FOR $\overline{MR}$: t_{rec} ($\overline{MR}$) is defined as the minimum time required between the end of the reset pulse and the clock transition from low to high in order for the flip-flop(s) to respond to the clock.

SWITCHING TIME WAVEFORMS

The shaded areas indicate when the input is permitted to change for predictable output performance.

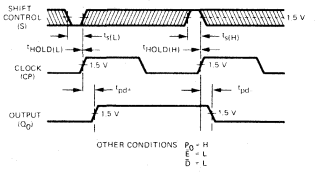


Fig. 8 SET UP TIME (t_s) FOR SHIFT CONTROL

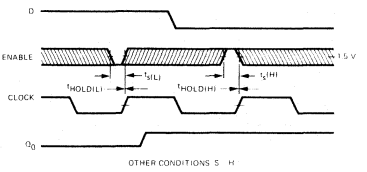


Fig. 9 SET UP TIME (t_s) FOR ENABLE ($\overline{E}$)

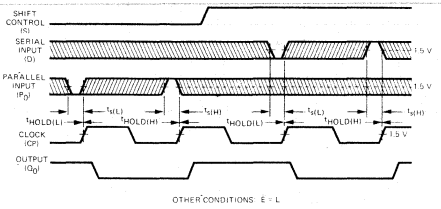
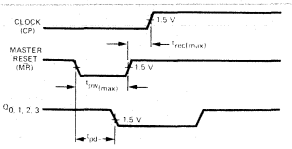


Fig. 10 SET UP TIME (t_s) FOR DATA (D, P_0, 1, 2, 3)



Other conditions:
$\overline{E}$ = L, S = L, P_0 = P_1 = P_2 = P_3 = H

Fig. 11 DELAY FROM MR TO OUTPUT (t_{pd-})
MASTER RESET RECOVERY TIME (t_{rec})
REQUIRED MASTER RESET PULSE WIDTH

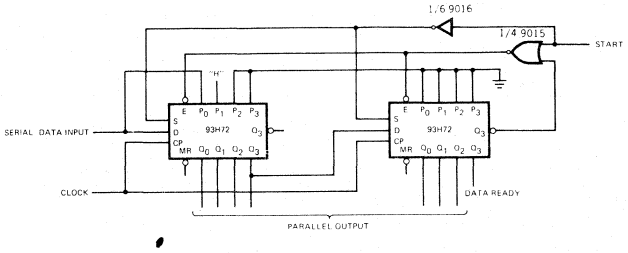
APPLICATIONS

The 93H72 four-bit shift register is basically similar to the 9300 universal shift register, but it offers higher speed and an overriding active low enable facility that allows it to hold data irrespective of the clock (do nothing mode). The $J\overline{K}$ input of the 9300 has been replaced by a D input on the 93H72.

The active low enable overrides all register operations except for reset and allows the synchronous enabling of shifting and parallel load for parallel/serial data transfer applications. The active low polarity of the enable is compatible with other MSI units such as decoders to provide easy selection of registers in multi-register applications.

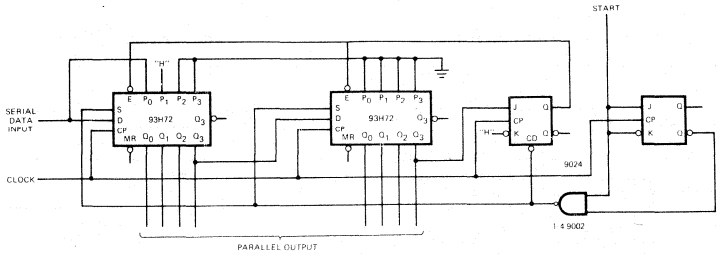
The 9300 or one of its versions (93L00, low power or 93H00, high speed) should be used where serial $J\overline{K}$ input flexibility is required such as in shift counter applications. Where speed requirements are not critical but reduced power consumption is important, the use of a low power or standard 9300 is recommended.

Fig. 12 SELF STOPPING SERIAL TO PARALLEL CONVERTERS



(a) 7-Bit S/P Converter

This seven-bit serial to parallel converter starts its conversion cycle on the first clock pulse after the falling edge of the start pulse. It stops and retains this parallel information as soon as the "one" that had been loaded into the first bit has propagated into the last bit, acting as a "data ready" signal. A new start input will clear the register and insert a leading one.



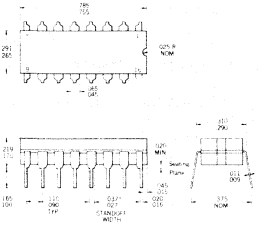
(b) 8-Bit S/P Converter

This eight-bit serial to parallel converter starts its conversion cycle after the rising edge of the start pulse and stops (by the same mechanism as the 7-bit converter) after 8-bits of data have been shifted in. Since an edge detector is employed at the start input, a new conversion cycle is only initiated after the start input is low for at least one clock period.

ORDER INFORMATION – Specify UXX93H7259X for the 0°C to +75°C temperature range, or UXX93H7251X for the –55°C to +125°C temperature range, where XX is 7B for the 16 pin Dual In-Line package or 4L for the 16 pin Flat package.

PACKAGE INFORMATION

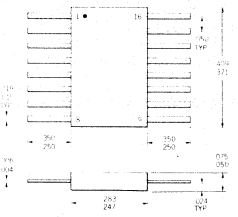
7B – 16 LEAD DUAL IN-LINE PACKAGE



NOTES:

All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.2 grams
*The .037/.027 dimension does not apply to the corner leads

4L – 16 LEAD (BeO) FLATPAK



NOTES:

All dimensions in inches
Leads are gold-plated kovar
Package weight is 0.4 gram

TTμL MEMORY 93400 . 93400B . 93401

256-BIT READ/WRITE MEMORY & DECODER/DRIVER

FAIRCHILD TTμL® IC PRODUCT FORMERLY 4100 . 4100B . 4101

GENERAL DESCRIPTION – The 93400 256 bit read/write memory and the 93401 decoder/driver are components for use in high speed memory systems. The 93400 is a fast 256 x 1 random access read/write memory which is addressed with a partially decoded x-y coincident selection scheme. There are two grades of device, with the 93400B having a slower access time than the 93400. The companion decoder and buffer driver, 93401, converts binary addresses into the partially decoded form required by the 93400, and provides sufficient drive to connect to 32 93400's. Both devices are supplied in 16 pin Dual In-Line Packages.

FEATURES

93400/93400B

TTμL COMPATIBLE
16 PIN PACKAGE
OUTPUT WIRED–OR CAPABILITY
70 ns TYPICAL ACCESS TIME (93400)
125 ns TYPICAL ACCESS TIME (93400B)
LOW INPUT LOADING

93401

TTμL COMPATIBLE
16 PIN PACKAGE
20 ns TYPICAL THROUGH DELAY
LOW INPUT LOADING
4 ENABLE INPUTS FOR CHIP SELECTION
DRIVES UP TO 32 93400's

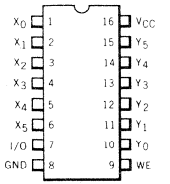
ABSOLUTE MAXIMUM RATINGS

V_{CC} Pin Potential to Ground Pin	-0.5 V to + 7.0 V
Input Voltage	-0.5 V to + 5.25 V
Voltage Applied to Output when Output is High	-0.5 V to + V_{CC}
Current into Output when Output is Low	+ 25 mA
Storage Temperature	-65°C to + 150°C

ORDER INFORMATION – Specify A7B9340059X, A7B9340059B or A7B9340159X respectively for 93400, 93400B and 93401 devices. These product codes specify 16-pin Dual In-Line package operational in 0° C to +75° C temperature range.

PIN CONFIGURATION

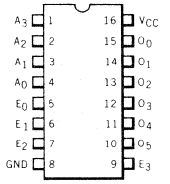
93400 • 93400B



V_{CC} = 16
Gnd = 8

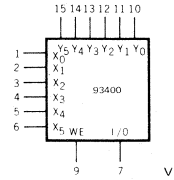
PIN CONFIGURATION

93401



V_{CC} = 16
Gnd = 8

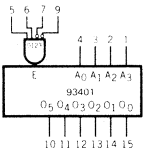
93400 • 93400B LOGIC SYMBOL



V_{CC} = 16
Gnd = 8

Fig. 1

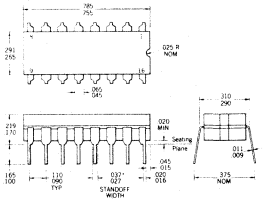
93401 LOGIC SYMBOL



V_{CC} = 16
Gnd = 8

Fig. 2

7B - 16 LEAD DUAL IN-LINE PACKAGE



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.2 grams
*The .037/.027 dimension does not apply to the corner leads

FAIRCHILD
SEMICONDUCTOR

FUNCTIONAL DESCRIPTIONS

The 93400 and 93400B contain 256 bipolar storage cells arranged in a 16 by 16 format. Any one of the 256 cells may be accessed by supplying an address code on the X address inputs and the Y address inputs. Internal decoders decode the X and Y addresses into one of 16 rows and one of 16 columns in the matrix of storage cells. Data may be written into or read out from the cell lying at the intersection of the selected row and column.

The X and Y addresses supplied to the 93400 and 93400B are partially decoded in a "3 out of 6" code. Of the six X address lines and the six Y address lines there are always three lines high and three lines low. There are 20 such combinations, 16 of which are decoded by the internal row and column decoders. The four unused combinations of 3 out of 6 will not select any row or column. If there are more than three lines high in either the X or Y address, then multiple row or column selection will occur. The sixteen 3 out of 6 codes used by the 93400 and 93400B are generated by the 93401 decoder/driver.

Data enters and leaves the memory on a single input/output (I/O) line, pin 7. The I/O line is an open collector output, so many 93400 I/O lines can be connected together in a wire-OR configuration. Input data must be applied to the I/O lines through an open collector gate. Each I/O line requires a pull-up resistor to V_{CC}. The magnitude of the pull-up resistor is determined by the number of 93400 I/O lines tied together. The I/O of a 93400 which is not addressed will be high.

Read/Write selection is determined by the state of pin 9, the active high Write Enable. When WE is high, the data on the I/O line will be written into the selected address in the 93400. When the Write Enable line is low, then data will be read out of the addressed location.

The 93401 is a partial decoder and driver for the 93400. It accepts a four bit binary code on the Address inputs (A_0–A_3) and produces a 3 out of 6 code on the six output pins (O_0–O_5). The decoder also features four separate Enables, two of which are active high and two of which are active low. All four enables must be active before the decoder will produce a 3 of 6 code. Since two of the enables are high and two are low, it is possible to route two binary coded lines to four different 93401's to get two additional bits of decoding with no extra packages. This is illustrated in the memory addressing scheme shown in Figure 14, page 6.

Ordinarily in memory systems, 93400 memory devices will be arranged in a matrix of rows and columns, as shown in Figure 14. Each column will store a particular bit and each row of 93400's will be 256 words. A 93401 driver will be used for each row and each column in the matrix. One 93401 can drive up to 32 93400 X or Y address lines. The usual driving scheme is to connect the four LSB's of address to each of the column decoders. The next four bits of address are connected to each of the row decoders. Additional address bits are decoded to the chip selects on the row decoders. Each column decoder drives the Y address lines on up to 32 93400's in a column. Each row decoder drives the address lines on up to 32 93400's in a row.

THE THREE OUT OF SIX CODE

The 3 out of six code used in the 93400 and produced by the 93401 is a tradeoff between memory chip complexity and pin count. The simplest 256 bit memory chip would be a 16 by 16 matrix of storage cells, with all 16 rows and 16 column select lines brought off chip. The lowest pin count for a 256 bit memory chip would be achieved by fully decoded X and Y select lines reducing the 32 lines of the simple scheme to only 8 lines. However, full binary decoding of the X and Y lines on chip significantly increases to complexity of the memory chip. The 93400 and 93401 are designed to gain the good features of both alternatives. The 16 X and Y lines are decoded into 6 lines each, allowing the memory to fit into a 16 pin package and still keeping the memory chip fairly simple, since the 3 out of 6 code does not require a complex decoder. The table on the right below shows the conversion of four bit binary to 3 out of 6 code by the 93401, and also the internal column or row selected by the 3 out of 6 to 1 of 16 decoder inside the 93400.

TTμL LOAD AND DRIVE FACTORS

93400 • 93400B

INPUT	LOAD
X Lines Y Lines WE	0.33/0.125
OUTPUT	DRIVE FACTOR
Output I/O	Open Collector 3.1

93401

INPUT	LOAD
E_0, E_1 E_2, E_3 A_0, A_1, A_2, A_3	0.33/0.25
OUTPUT	DRIVE FACTOR
O_0, O_1, O_2, O_3, O_4, O_5	16/6

Numerator = high level load
(1 load = 0.06 mA)
Denominator = low level load
(1 load = ~ 1.6 mA)

93401 CODE CONVERSION EQUATIONS

$O_0 = \overline{A_3}$

$O_1 = (\overline{A_1} + A_0)(\overline{A_3} + A_1)(\overline{A_2} + A_0)$

$O_2 = (\overline{A_1} + \overline{A_0})(\overline{A_3} + \overline{A_0})(\overline{A_2} + \overline{A_1})$

$O_3 = (\overline{A_1} + A_0)(\overline{A_3} + A_0)(\overline{A_2} + \overline{A_1})$

$O_4 = (\overline{A_1} + \overline{A_0})(\overline{A_3} + \overline{A_1})(\overline{A_2} + \overline{A_0})$

$O_5 = \overline{A_2}$

TRUTH TABLE

BINARY INPUT TO 93401				3 OUT OF 6 CODE OUTPUT OF 93401; INPUT TO 93400 (L = 0 OR X OR Y)						93400 93400B INTERNAL X OR Y ADDRESS
A_3	A_2	A_1	A_0	L_0	L_1	L_2	L_3	L_4	L_5	Row or Column
L	L	L	L	H	H	L	L	L	H	0
L	L	L	H	H	L	H	L	L	H	1
L	L	H	L	H	L	L	H	L	H	2
L	L	H	H	H	L	L	L	H	H	3
L	H	L	L	H	H	H	L	L	L	4
L	H	L	H	H	L	H	L	H	L	5
L	H	H	L	H	H	L	H	L	L	6
L	H	H	H	H	L	L	H	H	L	7
H	L	L	L	L	H	L	H	L	H	8
H	L	L	H	L	H	H	L	L	H	9
H	L	H	L	L	L	L	H	H	H	10
H	L	H	H	L	L	H	L	H	H	11
H	H	L	L	L	H	H	H	L	L	12
H	H	L	H	L	H	H	L	H	L	13
H	H	H	L	L	H	L	H	H	L	14
H	H	H	H	L	L	H	H	H	L	15

NOTE: Enables on 93401 must be LLHH. Any other state on the Enable inputs causes 93401 outputs to go Low, and addresses no internal row or column in the 93400 memory matrix.

93400 • 93400B ELECTRICAL CHARACTERISTICS ($T^* = 0°C$ to $75°C$ in operation; $V_{CC} = 5.0\ V \pm 5\%$)

SYMBOL	CHARACTERISTIC	LIMITS 0°C MIN.	MAX.	25°C MIN.	TYP.	MAX.	75°C MIN.	MAX.	UNITS	CONDITIONS AND COMMENTS
V_{OL}	Output Low Voltage		0.45		0.20	0.45		0.45	Volts	$I_{OL} = 5\ mA$, $V_{CC} = 4.75\ V$,
								0.55		$I_{OL} = 10\ mA$, See Figure 5.
I_{CE}	Output Leakage Current		100			100		100	μA	$V_{CC} = 5.25\ V$, $V_{CE} = 4.5\ V$ All Inputs Grounded
V_{IL}	Address, Write Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed Low Input Threshold
V_{IH}	Address, Write Input High Voltage	2.0		2.0			2.0		Volts	Guaranteed High Input Threshold
I_{FI}	Data Input Forward Current		-250			-250		-250	μA	$V_{CC} = 5.25\ V$, $V_F = 0.45\ V$
I_{FX}	X Address Input Forward Current		-250			-250		-250	μA	$V_F = 0.45\ V$, $V_{CC} = 5.25\ V$ 2 other X Lines. 3 Y Lines @ 4.5 V Remaining X and Y Lines @ .45 V
I_{FY}	Y Address Input Forward Current		-250			-250		-250	μA	$V_F = 0.45\ V$, $V_{CC} = 5.25\ V$ 2 other Y Lines. 3 X Lines @ 4.5 V Remaining X and Y Lines @ .45 V
I_{RX}	Address Input		20			20		20	μA	$V_{CC} = 5.25\ V$, $V_R = 4.5\ V$
I_{RY}	Leakage Current		20			20		20		Other X and Y inputs grounded
I_{FW}	Write Input Forward Current		-250			-250		-250	μA	$V_{CC} = 5.25\ V$, $V_F = 0.45\ V$
I_{RW}	Write Input Leakage Current		20			20		20	μA	$V_{CC} = 5.25\ V$, $V_R = 4.5\ V$
I_{VCC}	Supply Current				100	140			mA	$V_{CC} = 5.0\ V$, all inputs at ground

*Case Temperature

93401 ELECTRICAL CHARACTERISTICS ($T^* = 0°C$ to $75°C$ in operation; $V_{CC} = 5.0\ V \pm 5\%$)

SYMBOL	CHARACTERISTIC	LIMITS 0°C MIN.	MAX.	+25°C MIN.	TYP.	MAX.	+75°C MIN.	MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	$V_{CC} = 4.75\ V$, $I_{OH} = 1.0\ mA$ V_{IL} = value indicated below on this table
V_{OL}	Output Low Voltage		0.45		0.3	0.45		0.45	Volts	$V_{CC} = 4.75\ V$, $I_{OL} = 10\ mA$
V_{IH}	Input High Voltage	2.0		2.0			2.0		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_{FA}	Add. Input Load Current		-0.4			-0.4		-0.4	mA	$V_{CC} = 5.25\ V$, $V_E = 0.45\ V$, $V_R =$
I_{FE}	Enable Input Load Current		-0.4			-0.4		-0.4	mA	$V_{CC} = 5.25\ V$, 4.5 V on other inputs
I_{RA} & I_{RE}	Input Leakage Current		20			20		20	μA	$V_{CC} = 5.25\ V$, $V_R = 4.5\ V$, Gnd. on other inputs
I_{CC}	Power Supply Current		140		120	140		140	mA	$V_{CC} = 5.25\ V$

*Case Temperature

93401 SWITCHING CHARACTERISTICS ($V_{CC} = 5.0\ V$, $T_A = 25°C$) (See Fig. 4)

SYMBOL	CHARACTERISTICS	LIMITS C_L = 90 pF (Equiv. to 32 X Lines) TYP.	MAX.	C_L = 500 pF (Equiv. to 32 Y Lines) TYP.	MAX.	UNITS
t_A^{++}, t_A^{+-} t_A^{-+}, t_A^{--}	Delay from address going low or high to output going low or high	20	25	30	40	ns
t_E^{++}, t_E^{+-} t_E^{-+}, t_E^{--}	Delay from enable going active or inactive to output going high or low	20	25	30	40	ns

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C.) C_L = 47 pF; Equivalent to eight OR–tied 4100 outputs

SYMBOL	CHARACTERISTIC	93400 LIMITS			93400B LIMITS			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
t_{AX}	Read Access Time. Time from good X address to good data at output	30	70	100	30	100	200	ns
t_{AY}	Read Access Time. Time from good Y address to good data at output	15	45	65		45	100	ns
t_{RR}	Read Recovery Time. Time for output to go high after removal of address			100			150	ns
t_{WP}	Write Pulse Width. Width of pulse on WE required to write data into memory.	80			100			ns
t_{SH}	Data Setup Time. Time high or low data must be present before end of write pulse to write proper data into memory			t_{WP}+10			100	ns
t_{SL}				70 (Note 2)			70 (Note 3)	ns
t_{RH}	Data Release Time. This is the minimum set-up time. Removal of data after the release time will not affect the data written into the memory. See note 1.	0			0			ns
t_{RL}		10			10			ns
C_O	Output Capacitance		7.0			7.0		pF
C_{AX}	Input Capacitance for X address line		3.0			3.0		pF
C_{AY}	Input Capacitance for Y address line		15			15		pF
t_{AS}	Address Set Up Time. Time address must be good before end of write pulse during write operation. (See Fig. 3b)	80			80			ns
t_{AP}	Address Pulse Width. Time that address must remain good for write operation. (See Fig. 3b)	100			100			ns
t_{WR}	Write Recovery Time. Time in write-read cycle from end of write pulse to valid output data.			120			120	ns

NOTES

1: The set up and release times define a window during which devices are responding to the data and/or address. Inputs must remain good at all times in between the set up and release time limits.

2: Applies for write pulse less than 150 ns.

3: Applies for write pulse more than 160 ns.

Fig. 3a 93400 TYPICAL READ CYCLE

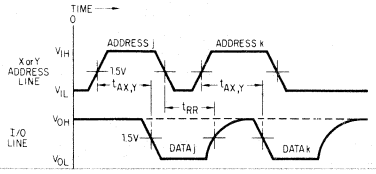
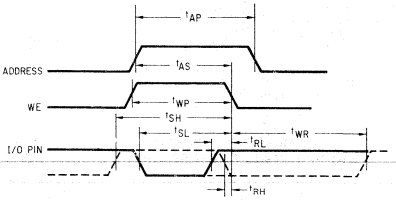


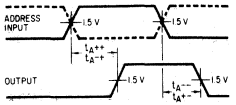
Fig. 3b 93400 WRITE CYCLE

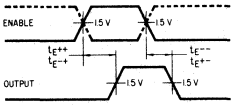


$t_{AX,Y}$ is the time from a good address to good data on the output. Note that the access time may be overlapped with the recovery time to improve speed on consecutive Read operations.

The address must be maintained for 100 ns. The simplest write cycle is achieved by applying the data, then simultaneously raising the address and write pulses for 100 ns. If the write pulse width is less than 100 ns, then the address should come up at about the same time as the write pulse and should be held on after the write pulse. The address should not be applied more than 25 ns before the write pulse, because an early address will cause a read operation to begin, disrupting data on the I/O lines (see t_{RR}). For a longer write pulse, the address pulse may appear anytime as long as it starts before t_{AS} and lasts at least t_{AP}.

Fig. 4 93401 SWITCHING WAVEFORMS





TEST LOAD CONDITIONS

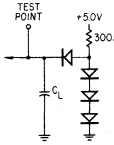
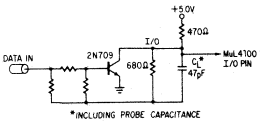


Fig. 5
93400
TEST LOAD CONDITIONS



'Low' Level ≤ 0.45 V
'High' Level ≥ 3.0 V
Rise, Fall Time = 10 ± 5 ns

Fig. 6
93400 STANDARD INPUT PULSE

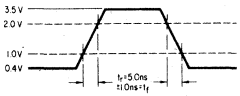
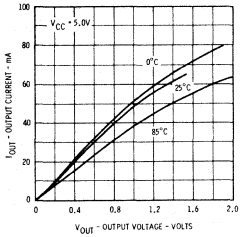


Fig. 7
93400, 93400B
OUTPUT CHARACTERISTICS



The timing curves in Figures 8 through 13 are obtained using the pulse shape in Figure 6 and the loading in Figure 5. In Figures 12 and 13 the C_L value in the load is varied.

Fig. 8
INPUT THRESHOLD VOLTAGE VERSUS TEMPERATURE

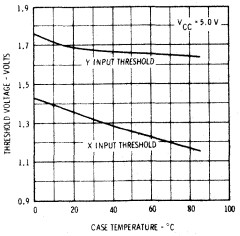


Fig. 9
X ACCESS TIME VERSUS TEMPERATURE

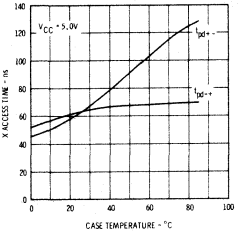


Fig. 10
Y ACCESS TIME VERSUS TEMPERATURE

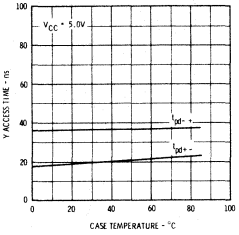


Fig. 11
MINIMUM WRITE PULSE WIDTH VERSUS TEMPERATURE

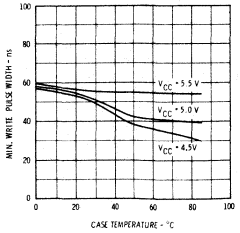


Fig. 12
X ACCESS TIME VERSUS LOAD CAPACITANCE

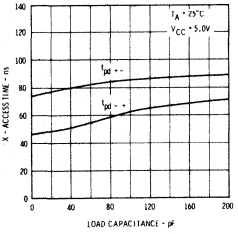
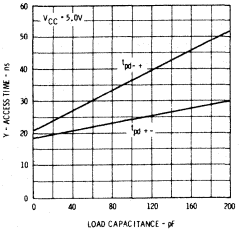
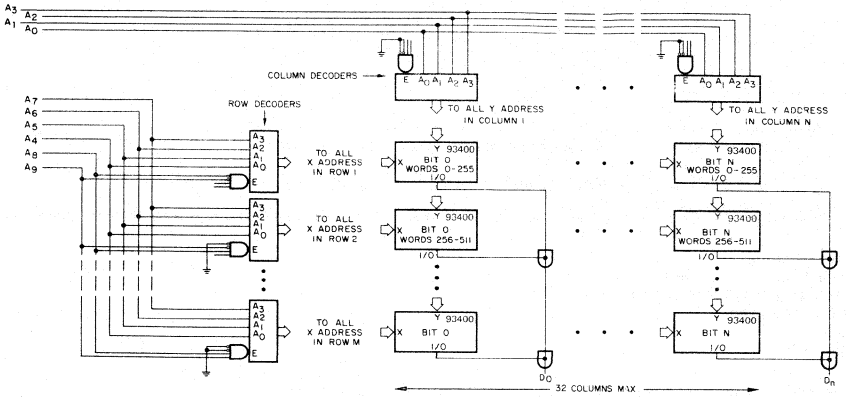


Fig. 13
Y ACCESS TIME VERSUS LOAD CAPACITANCE



APPLICATIONS

BASIC SCHEME FOR ADDRESSING AN ARRAY OF 93400'S USING THE 93401 DECODER/DRIVER.

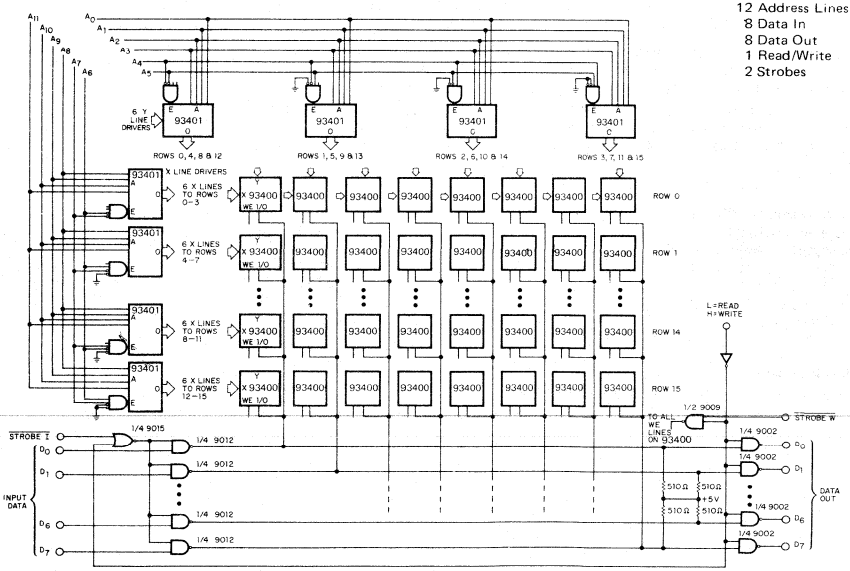


The faster Y Lines are used in the columns to allow high speed "pipelining" of up to 256 locations from the same chip.

FIG. 14

4096 WORD X 8 BIT MEMORY SYSTEM

12 Address Lines
8 Data In
8 Data Out
1 Read/Write
2 Strobes



The 93400's are arranged in an 8 x 16 matrix, with the eight columns representing the 8 bits per word. The 93400's in the 16 rows are selected by an interlaced arrangement of the X and Y drivers. X drivers select groups of 4 continuous rows while Y drivers select groups of 4 rows spaced 4 apart. Every 93401 is driving 32 – 93400's. The strobe I and strobe W lines can be used for timing control of input data and write pulse in critical high speed operations.

Fig. 15

TTμL MEMORY 93402

16-BIT ASSOCIATIVE/CONTENT ADDRESSABLE MEMORY

FAIRCHILD TTμL® IC PRODUCT FORMERLY 4102

GENERAL DESCRIPTION — The 93402 is a high speed 16-bit associative random access memory. It is a linear select 4-word by 4-bit array in which the equality search is performed on all bits in parallel. The 93402 is TTμL compatible.

An hermetically sealed 24-pin dual In-Line package is used. The 93402 is available with temperature range from −55°C to +125°C or from 0°C to +75°C.

- **25 ns TYPICAL MATCH TIME**
- **MULTIPLE MATCHING AND ADDRESSING**
- **UNCOMMITTED COLLECTOR OUTPUTS FOR WIRE-OR CAPABILITY**
- **LINEAR SELECT ADDRESSING**
- **BIT MASKING**
- **TTμL COMPATIBLE**

OPERATION — With the bit enable lines ($\overline{E_0}$ - $\overline{E_3}$) low, the outputs (M_0 - M_3) go high if associated stored data matches the descriptor bits (D_0 - D_3). If a bit enable line is held high, a match is forced on the corresponding bit in all the words regardless of the state of the descriptor bit (D_0 - D_3). An inverter is connected to the match output M_0 to give its negation $\overline{M_0}$.

A word is addressed by having an active low on the appropriate address line ($\overline{A_0}$ - $\overline{A_3}$). Any number of words may be addressed simultaneously.

Data can be written into the memory through the data inputs ($\overline{D_0}$ - $\overline{D_3}$) under control of the address inputs and the appropriate bit enable ($\overline{E_0}$ - $\overline{E_3}$) when the write enable ($\overline{WE}$) is low.

Reading can occur either during an equality search or a write operation. If a single word is addressed that word will appear at the data outputs ($\overline{O_0}$ - $\overline{O_3}$). If multiple addressing is used, then the word appearing at the data output is the AND *(positive logic)* or the OR *(negative logic)* of the addressed words.

All outputs are uncommitted collectors which allows a maximum flexibility in output connection. In many applications such as memory expansion, the outputs of many 93402's can be tied together. In other applications, the wired OR is not used. In either case an external pull up resistor must be used to attain a high at an output.

ABSOLUTE MAXIMUM RATINGS

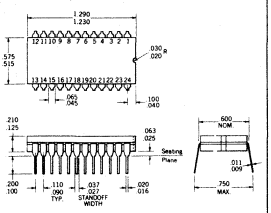
Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground	−0.5 V to +7.0 V
Input Pin Voltage	−0.5 V to +5.5 V
Current into Output Terminal	50 mA
Output Voltage	−0.5 V to +8.0 V

ORDER INFORMATION

Specify A6N9340259X for the 0°C to +75°C temperature range.

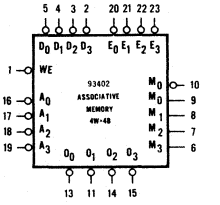
PHYSICAL DIMENSIONS

24 Lead Dual In-Line



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .600" centers. They are purposely shipped with "positive" misalignment to facilitate insertion
Leads are tin-plated kovar
Package weight is 6.5 grams

LOGIC DIAGRAM



V_{CC} = PIN 24
GND = PIN 12

FAIRCHILD
SEMICONDUCTOR

LOADING RULES

	HIGH LEVEL (TTμL Unit Loads)	LOW LEVEL (TTμL Unit Loads)
Address	1.0	1.0
Bit Enable	1.5	1.5
Write Enable	1.5	1.5
Data Input	1.0	1.0
Data Output	Open Collector	6.2
Match Output	Open Collector	6.2

1 Low Level TTμL Unit Load = −1.6 mA
1 High Level TTμL Unit Load = 60 μA

The external pull-up resistor R is selected to lie in the range as shown.

$$\frac{5.1}{10 - \text{F.O. (1.6)}} \leq R \leq \frac{2.1}{NL + \text{F.O. (0.06)}}$$

R is in kΩ
N = number of wired-OR outputs
F.O. = number of TTμL loads driven
L = Sum of all I_{CEX} of wired-OR outputs

The minimum value of R is limited by output current sinking ability. The maximum value of R is determined by the output and input leakage current (I_{CEX} and I_R) which must be supplied to hold the output at 2.4 V.

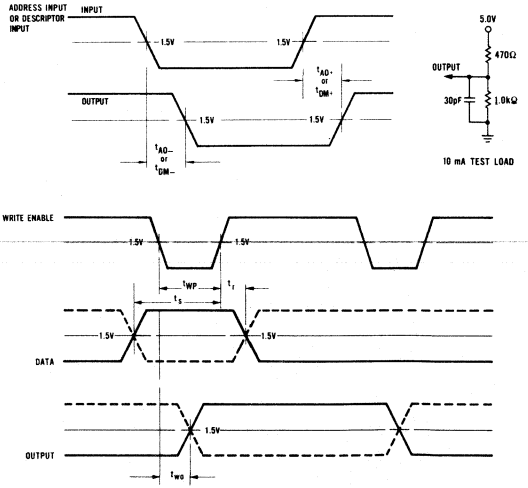
F.O.	Maximum number of Wired-OR's
1	66
2	52
3	38
4	24
5	10
5.7	0

SWITCHING CHARACTERISTICS ($T_A = 25°C$, $V_{CC} = 5.0$ V)

SYMBOL	TEST	LIMIT (ns) TYP.	CONDITIONS LOAD	C	NOTE
t_{AO-}	Address to Output Turn-On Delay	20	10 mA	30 pF	1
t_{AO+}	Address to Output Turn-Off Delay	25	10 mA	30 pF	1
t_{DM+}	Descriptor to Output Match Turn-On Delay	25	10 mA	30 pF	2
t_{DM-}	Descriptor to Output Match Turn Off Delay	30	10 mA	30 pF	2
t_{WP}	Write Pulse Width Required to Write	33	10 mA	30 pF	
t_{WO}	Write Delay	50	10 mA	30 pF	
t_s	Maximum Set-up Time on Data Input	33	10 mA	30 pF	3
t_r	Release Time (Minimum Set-up Time) on Data Input	0	10 mA	30 pF	3

NOTE 1: To test t_{AO+} and t_{AO-} a "Low" must be stored in the cell under test.
NOTE 2: To test t_{DM-} and t_{DM+}, a mismatch must occur in at least one bit of the word under test.
NOTE 3: Setup and release times are measured with respect to the rising edge of the Write enable. To guarantee writing in the correct data, the data input must be good by t_s and remain good until after t_r.
The typical capacitance of one 93402 output is 7.0 pF.

SWITCHING WAVE FORMS



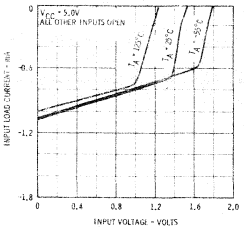
ELECTRICAL CHARACTERISTICS (T_A = 0°C to 75°C, V_{CC} = 5.0 V ±5%) (units are pulse tested)

SYMBOL	TEST	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	CONDITIONS
I_{FA}	Address Input Load Current		−1.6		−1.6		−1.6	mA	V_{CC} = 5.25 V V_A = 0.45 V
I_{FB}	Bit Enable Load Current		−2.4		−2.4		−2.4	mA	V_{CC} = 5.25 V V_{CS} = 0.45 V
I_{FWE}	Write Enable Load Current		−2.4		−2.4		−2.4	mA	V_{CC} = 5.25 V V_W = 0.45 V
I_{FI}	Data Input Load Current		−1.6		−1.6		−1.6	mA	V_{CC} = 5.25 V V_D = 0.45 V
I_{RA}	Address Input Leakage Current		60		60		60	μA	V_{CC} = 5.25 V V_A = 4.5 V
I_{RBE}	Bit Enable Input Leakage Current		90		90		90	μA	V_{CC} = 5.25 V V_{CS} = 4.5 V
I_{RWE}	Write Enable Leakage Current		90		90		90	μA	V_{CC} = 5.25 V V_W = 4.5 V
I_{RI}	Data Input Leakage Current		60		60		60	μA	V_{CC} = 5.25 V V_D = 4.5 V
I_{CEX}	Output Leakage Current (Note 1)		50		50		50	μA	V_{CC} = 5.25 V V_{CEX} = 5.25 V
$I_{CEX\ M0}$	Output Leakage Current for M_0		110		110		110	μA	V_{CC} = 5.25 V V_{CEX} = 5.25 V
V_{OL}	Output "Low" Voltage (Note 2)		0.45		0.45		0.45	V	V_{CC} = 4.75 V I_{OL} = 10 mA One Word Addressed
V_{IL}	Input "Low" Voltage (Note 3)		0.85		0.85		0.85	V	V_{CC} = 5.0 V, Monitor Appropriate Output To Guarantee This Test Limit
V_{IH}	Input "High" Voltage (Note 3)	2.0		2.0		2.0		V	V_{CC} = 5.0 V, Monitor Appropriate Output To Guarantee This Test Limit
I_{PD}	Supply Current		125		125		125	mA	V_{CC} = 5.25 V, Worst Case

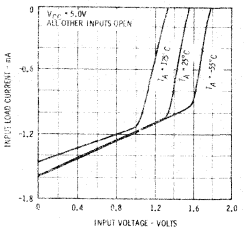
NOTE 1: For all outputs except M_0
NOTE 2: For all outputs.
NOTE 3: For all inputs.

TYPICAL ELECTRICAL CHARACTERISTICS

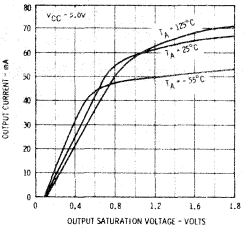
DATA AND ADDRESS INPUT LOAD CURRENT VERSUS INPUT VOLTAGE



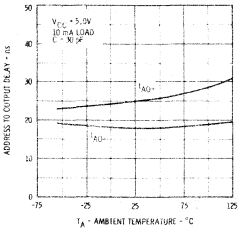
WRITE ENABLE AND BIT ENABLE INPUT LOAD CURRENT VERSUS INPUT VOLTAGE



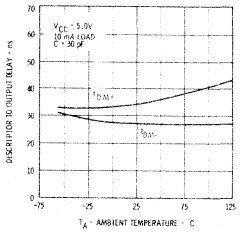
OUTPUT CURRENT VERSUS OUTPUT SATURATION VOLTAGE ALL OUTPUTS



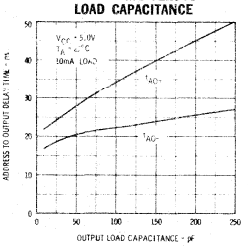
ADDRESS TO OUTPUT DELAY TIME VERSUS AMBIENT TEMPERATURE



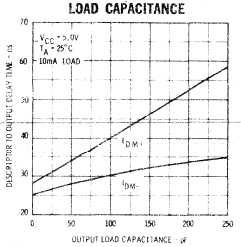
DESCRIPTOR TO OUTPUT DELAY TIME VERSUS AMBIENT TEMPERATURE



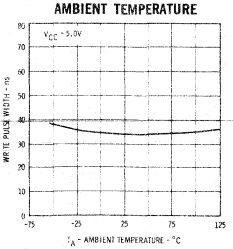
ADDRESS TO OUTPUT DELAY TIME VERSUS LOAD CAPACITANCE



DESCRIPTOR TO OUTPUT DELAY TIME VERSUS LOAD CAPACITANCE



WORST CASE WRITE PULSE WIDTH VERSUS AMBIENT TEMPERATURE



APPLICATIONS

WORD EXPANSION

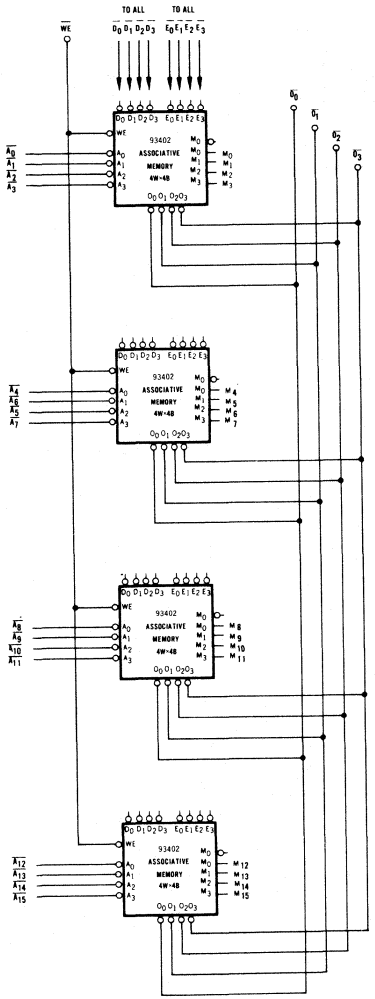


Fig. 1 — EXPANSION OF ASSOCIATIVE MEMORY TO 16 WORDS BY 4 BITS

BIT EXPANSION

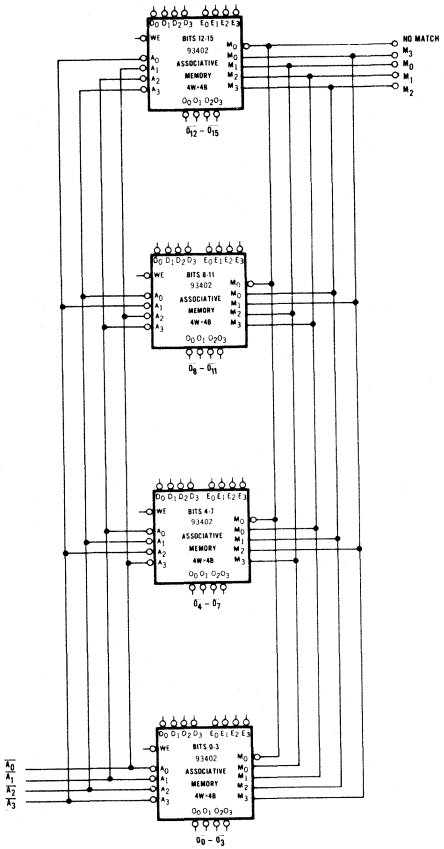


Fig. 2 — EXPANSION OF ASSOCIATIVE MEMORY TO 4 WORDS BY 16 BITS

Words are in staggered locations so that a match for any word will appear in one of the M_0's. If there is no match, all M_0's will be low and the wired-OR of $\overline{M}_0$ will be high.

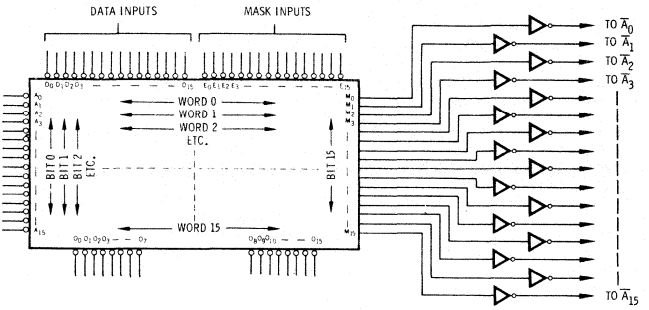


Figure 3
A 16-bit-by-16-word associative field memory formed from 93402's. Match outputs are inverted and used to address words which produced the match.

MULTIFIELD ASSOCIATION

Information can be stored in a multifield associative memory in such a manner that data in one field can be used to obtain related data from the other fields by using a match in one field to address the entire word. This is illustrated in Figure 3 which shows a 16-bit-by-16-word associative field memory formed from word and bit expansions of sixteen 4102's.

The field concept can be applied to this array to make a two-way table. The eight bits of memory on the left could be loaded with one set of data, and the eight bits on the right with a corresponding set of data. For instance, the left side of each word might contain a binary number x, and the right side of the same word a binary number for log x. The data inputs for the corresponding bits are tied together and the Enable inputs for each half connected as shown in Figure 4.

If the Select input is HIGH, all left-field bits will be enabled and all right-field bits masked. A binary number presented on the Data inputs will be compared with data on the left side of the memory. If the Select input is LOW, data will be compared with the right side of the memory and the left side will be masked. Match signals are fed back to address the entire word producing the match. If a number x is placed on the Data inputs and the Select input is HIGH, the outputs will contain x on the left and log x on the right. If the Select is LOW, the outputs will contain x on the right and antilog x on the left. A match in the preselected field causes corresponding information from both fields to appear at the output.

This scheme can be broadened to include more than two fields. For example, five fields might be used in an air traffic control system: (1) plane identification, (2) range, (3) altitude, (4) speed, and (5) status code.

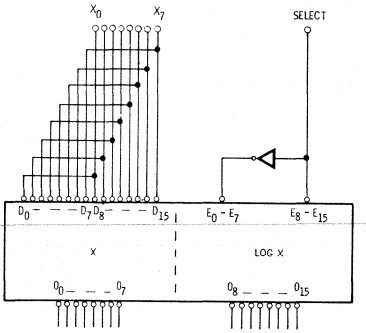


Figure 4
A two-field associative memory useful as a two-way table. Numbers are stored in left field and logs in right field. Either field can be used to obtain the corresponding number from the other field.

TTμL MEMORY 93403

64-BIT FULLY DECODED READ/WRITE MEMORY

FAIRCHILD TTμL® IC PRODUCT FORMERLY 4103

GENERAL DESCRIPTION – The 93403 is a high speed 64 bit read/write memory organized 16 words by 4 bits. Four address lines are buffered and decoded "on chip" for word selection. The 93403 is made with TTμL circuitry and all inputs are equivalent to one TTμL load.

OPERATION – When the 93403 receives a low at the Chip Select ($\overline{CS}$) input, the binary address (A_0, A_1, A_2 and A_3) is decoded to select one of sixteen four bit words. If the Write Enable ($\overline{WE}$) is at a high level, the contents of the selected word are non-destructively read out and the sense amplifier outputs (O_0, O_1, O_2 and O_3) reflect the state of the stored data in the four bits of the selected word. If the Write Enable is low, the data present on the Data Input lines (D_0, D_1, D_2 and D_3) is written into the four bits of the selected word and also appears on the data outputs. Note that there is inversion through the device in a read operation.

- **OUTPUT WIRED-OR CAPABILITY**
- **ON CHIP DECODING**
- **NON-DESTRUCTIVE READOUT**
- **CHIP SELECT FOR SYSTEM WORD EXPANSION**
- **TTμL COMPATIBLE**

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	-65°C to + 150°C
Temperature (Case) Under Bias	-55°C to + 125°C
V_{CC} Pin Potential to Ground	-0.5 V to + 8.0 V
Input Pin Voltage	-1.5 V to + 5.5 V
Current Into Output Terminal	100 mA
Output Voltage (external circuit dependent)	-0.5 V to + 8.0 V

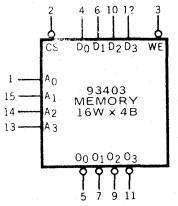
ORDER INFORMATION

FLAT PACKAGE – Specify A4L93403XXX

DUAL IN-LINE PACKAGE – Specify A7B93403XXX

Where XXX is 51X for the –55°C to +125°C temperature range, or 59X for 0°C to +75°C temperature range.

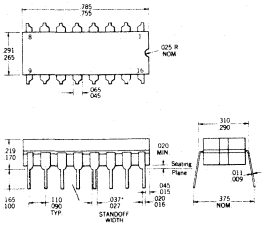
LOGIC SYMBOL AND PIN CONFIGURATION



V_{CC} = PIN 16
GND = PIN 8

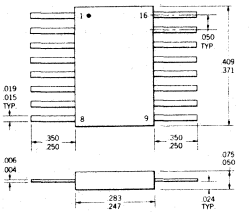
PHYSICAL DIMENSIONS

16 Lead Dual In-Line



NOTES:
All dimensions in inches
Leads are intended for insertion in hole Rows on .300" centers. They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .002 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.2 grams
*The .037/.027 dimension does not apply to the corner leads

FLAT PACKAGE



NOTES:
All dimensions in inches
Leads are gold-plated Kovar
Package weight is 0.4 gram

FAIRCHILD
SEMICONDUCTOR

ELECTRICAL CHARACTERISTICS (T_{CASE} = -55°C to 125°C, V_{CC} = 5.0 V ± 10%) *(units are pulse tested)*

SYMBOL	TEST	LIMITS -55°C MIN.	LIMITS -55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS
I_{FA}	Address Input Load Current		-1.6		-1.6		-1.6	mA	V_{CC} = 5.5 V, V_A = 0.45 V
I_{FCS}	Chip Select Load Current		-1.6		-1.6		-1.6	mA	V_{CC} = 5.5 V, V_{CS} = 0.45 V
I_{FWE}	Write Enable Load Current		-1.6		-1.6		-1.6	mA	V_{CC} = 5.5 V, V_W = 0.45 V
I_{FD}	Data Input Load Current		-1.6		-1.6		-1.6	mA	V_{CC} = 5.5 V, V_D = 0.45 V
I_{RA}	Address Input Leakage Current		60		60		60	μA	V_{CC} = 5.5 V, V_A = 4.5 V
I_{RCS}	Chip Select Input Leakage Current		60		60		60	mA	V_{CC} = 5.5 V, V_{CS} = 4.5 V
I_{RWE}	Write Enable Leakage Current		60		60		60	μA	V_{CC} = 5.5 V, V_W = 4.5 V
I_{RD}	Data Input Leakage Current		60		60		60	μA	V_{CC} = 5.5 V, V_D = 4.5 V
I_{CEX}	Output Leakage Current		100		100		100	μA	V_{CC} = 5.5 V, V_{CEX} = 5.5 V 3.0 V on Chip Select
V_{OL}	Output "Low" Voltage		0.45		0.45		0.45	V	V_{CC} = 4.5 V, I_{OL} = 16 mA $\overline{CS}$ = V_{IL}, $\overline{WE}$ = V_{IH}
V_{IL}	Input "Low" Voltage		0.8		0.8		0.8	V	V_{CC} = 5.0 V, Monitor Appropriate Output To Guarantee This Test Limit
V_{IH}	Input "High" Voltage	2.1		2.1		2.1		V	V_{CC} = 5.0 V, Monitor Appropriate Output To Guarantee This Test Limit
I_{CC}	Supply Current		115		115		115	mA	V_{CC} = 5.5 V, Write Enable = 3.0 V, other inputs Grounded
V_{CD}	Clamp Voltage, All Inputs		-1.0		-1.0		-1.0	V	I_{CD} = -5.0 mA
BV_X	Breakdown Voltage, All Inputs	5.5		5.5		5.5		V	I_X = 1.0 mA

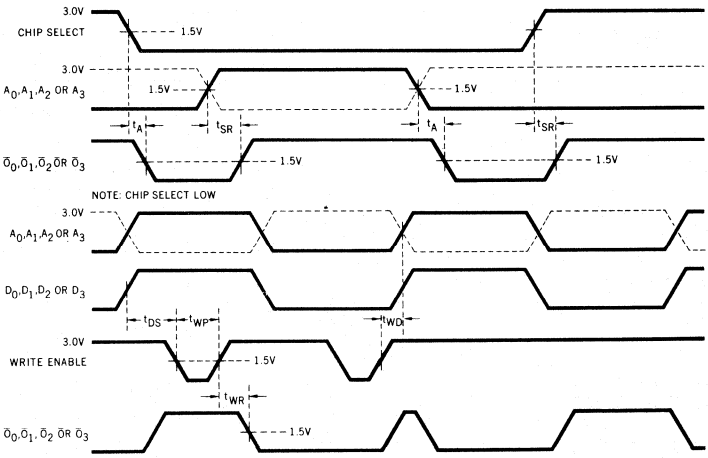
ELECTRICAL CHARACTERISTICS (T_{case} = 0°C to 75°C, V_{CC} = 5.0 V ±5%) (units are pulse tested)

SYMBOL	TEST	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	CONDITIONS
I_{FA}	Address Input Load Current		-1.6		-1.6		-1.6	mA	V_{CC} = 5.25 V, V_A = 0.45 V
I_{FCS}	Chip Select Load Current		-1.6		-1.6		-1.6	mA	V_{CC} = 5.25 V, V_{CS} = 0.45 V
I_{FWE}	Write Enable Load Current		-1.6		-1.6		-1.6	mA	V_{CC} = 5.25 V, V_W = 0.45 V
I_{FD}	Date Input Load Current		-1.6		-1.6		-1.6	mA	V_{CC} = 5.25 V, V_D = 0.45 V
I_{RA}	Address Input Leakage Current		60		60		60	μA	V_{CC} = 5.25 V, V_A = 4.5 V
I_{RCS}	Chip Select Input Leakage Current		60		60		60	mA	V_{CC} = 5.25 V, V_{CS} = 4.5 V
I_{RWE}	Write Enable Leakage Current		60		60		60	μA	V_{CC} = 5.25 V, V_W = 4.5 V
I_{RD}	Data Input Leakage Current		60		60		60	μA	V_{CC} = 5.25 V, V_D = 4.5 V
I_{CEX}	Output Leakage Current		100		100		100	μA	V_{CC} = 5.25 V, V_{CEX} = 5.25V 3.0 on Chip Select
V_{OL}	Output "Low" Voltage		0.45		0.45		0.45	V	V_{CC} = 4.75 V, I_{OL} = 16 mA $\overline{CS}$ = V_{IL}, $\overline{WE}$ = V_{IH}
V_{IL}	Input "Low" Voltage		0.85		0.85		0.85	V	V_{CC} = 5.0 V, Monitor Appropriate Output To Guarantee This Test Limit
V_{IH}	Input "High" Voltage	2.0		2.0		2.0		V	V_{CC} = 5.0 V, Monitor Appropriate Output To Guarantee This Test Limit
I_{CC}	Supply Current		110		110		110	mA	V_{CC} = 5.25 V, Write Enable = 3.0 V, other inputs Grounded
V_{CD}	Clamp Voltage, All Inputs		-1.0		-1.0		-1.0	V	I_{CD} = -5.0 mA
BV_X	Breakdown Voltage, All Inputs	5.5		5.5		5.5		V	I_X = 1.0 mA

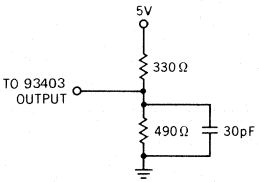
SWITCHING CHARACTERISTICS

SYMBOL	CHARACTERISTIC	DEFINITION	LIMITS 25°C MIN.	TYP.	MAX.	UNITS
t_A	Read Access Time	Time From Switching Address Or Chip Select To Data At Output		45	60	ns
t_{SR}	Sense Recovery Time	Time From Switching Address Or Chip Select To Output High		45	60	ns
t_{WP}	Write Pulse	Write Pulse Width - Width of Pulse Guaranteed to Write	45	30		ns
t_{WR}	Write Recovery Time	Time From Write Pulse Going High To Output Low			65	ns
t_{DH}	Data Hold Time	Time From Write Pulse Going High To Change Data Or Address			5.0	ns
t_{DS}	Data Set-Up Time	Time Data Must Be Present Before Write Pulse	5.0	0		ns
t_{AS}	Address Set-Up Time	Time Address Must Be Present in Order to Write	5.0	10	45	ns

WAVEFORMS

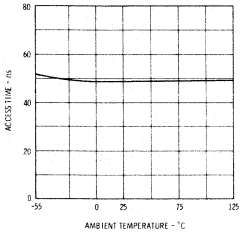


SWITCHING TEST CIRCUIT
15 mA LOAD

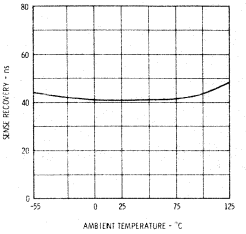


TYPICAL ELECTRICAL CHARACTERISTICS

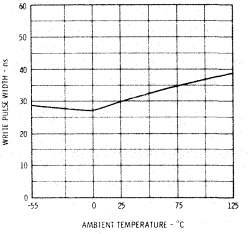
ACCESS TIME (t_A) VERSUS TEMPERATURE



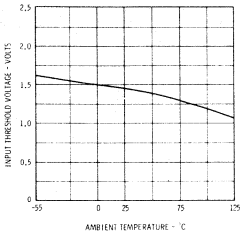
SENSE RECOVERY TIME (t_{SR}) VERSUS TEMPERATURE



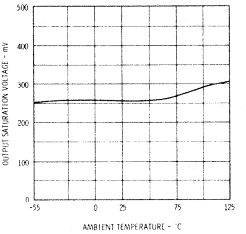
WRITE PULSE WIDTH (t_{WP}) VERSUS TEMPERATURE



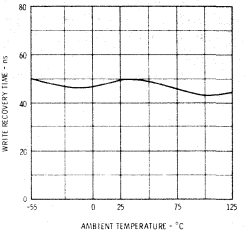
INPUT THRESHOLD VOLTAGE VERSUS TEMPERATURE



OUTPUT SATURATION VOLTAGE VERSUS TEMPERATURE



WRITE RECOVERY TIME (t_{WR}) VERSUS TEMPERATURE



TTμL LOADING RULES

	HIGH LEVEL	LOW LEVEL
Address	1 U. L.	1 U. L.
Chip Select	1 U. L.	1 U. L.
Write Enable	1 U. L.	1 U. L.
Data Input	1 U. L.	1 U. L.
Data Output	Open Collector	10 U. L.

1 Low Level TTμL Unit Load (U. L.) = -1.6 mA
1 High Level TTμL Unit Load (U. L.) = 60 μA

Uncommitted collector outputs are provided on the 93403 to allow maximum flexibility in output connection. In many applications such as memory expansion, the outputs of many 93403 can be tied together. In other applications the wired-OR is not used. In either case an external pullup resistor of value R_L must be used to provide a high at the output when it is off. Any value of R_L within the range specified below may be used.

$$\frac{5.05}{16 - \text{F.O.}\,(1.6)} \leqslant R_L \leqslant \frac{2.1}{N\,(0.1) + \text{F.O.}\,(0.06)}$$

R_L is in kΩ
N = number of wired-OR outputs
F.O. = number of TTμL loads driven
V_{CC} = 5.0 V ± 10%

The minimum value of R_L is limited by output current sinking ability. The maximum value of R_L is determined by the output and input leakage current (I_{CEX} and I_R) which must be supplied to hold the output at 2.4 V.

TTL MEMORY 93406*

1024-BIT READ ONLY MEMORY

*FORMERLY 4106

GENERAL DESCRIPTION – The Fairchild 93406 is a 1024-bit Bipolar Read Only Memory organized 256 words by 4-bits. An 8-bit binary address is used to select the desired word. The four outputs are uncommitted collectors which permit "OR" tying of the outputs for expanding the memory in the word direction. The customer can specify the active level of the 2 input chip select gate. CS_1 and CS_2 both will be active LOW unless otherwise specified by the customer. The programmable enable feature allows expansion of the memory to 1024 words without any external gates.

The contents of the memory are mask programmed to the customers specification. The customer can specify the desired ROM code on either the 93406 Coding Form(s) or by punched cards using the 93406 Data Card Format.

FEATURES

- DTL AND TTL COMPATIBLE
- ACCESS TIME – 50 ns MAX
- FULLY DECODED – ON CHIP ADDRESS DECODER AND BUFFER
- 2 CHIP SELECT INPUTS PROVIDING EASY MEMORY EXPANSION
- PROGRAMMABLE CHIP SELECTS
- OR-TIE CAPABILITY
- STANDARD 16 PIN DUAL IN-LINE PACKAGE

PIN NAMES

A_0 to A_7	Address Inputs
CS_1, CS_2	Chip Select Inputs
O_0 to O_3	Data Outputs

ORDER INFORMATION – Specify A7K9340659X, where 59X is for the 0°C to +75°C range.

LOGIC DIAGRAM

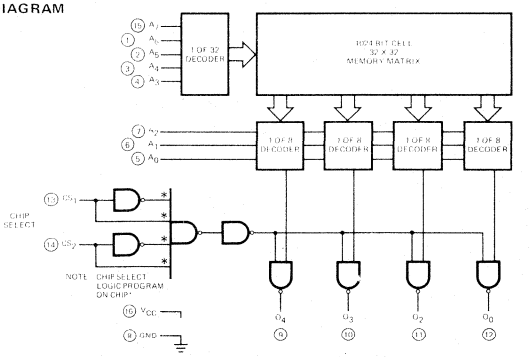
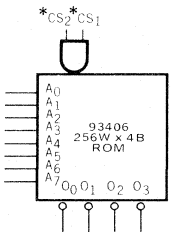


Fig. 3 *Per customer request. Unless otherwise specified CS_1 and CS_2 will be active low.

LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

*Chip selects active level may be programmed per customer requirements. If not specified both CS will be active low.

Fig. 1

PIN CONFIGURATION

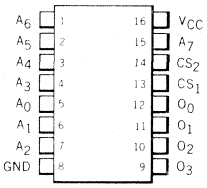


Fig. 2

FAIRCHILD SEMICONDUCTOR

93406 DATA CARD FORMAT

The most efficient method of ordering the 93406 is to punch the desired truth table on a punched card in the format described below. Fairchild will generate mask and test program data directly from these inputs. This eliminates the chance of error when transcribing inputs from a hand written truth table.

Data should be provided on a deck of 34 standard 80 column cards containing the following information.

CARD NO. 1 – Customs Identification

Column	Content
1	Blank
2–28	Customer Name, Drawing or Specification control number.
29–32	Blank
33–39	FAIRCHILD PART NUMBER. This part number is supplied by the factory through your Fairchild sales representative.
40–64	Blank
65–72	Date
73–80	Blank

CARD NO. 2 – Chip Select Option

Column	Content
1–11	Punch "Chip Select"
12	Blank
13, 14	Punch Charts '00', '01', '10' or '11', depending on the chip select code option. (First bit represents CS_1 input, second bit represents CS_2 input. '0' = Low, '1' = High.)
15–32	Blank
33–39	Repeat FAIRCHILD PART NUMBER (This is used for positive identification).
40–80	Blank

CARDS NO. 3 through 34 – Truth Table Deck

Each card will contain instructions for the output levels for 8 input words.

Column	Content
1–7	Punch the numerals representing the first and last words on that card (i.e.: 000-007, 008-015, 016-023. . .248-255). Word order is determined by the value of the binary address – A_7 = MSB, A_0 = LSB.
8–9	Blank
10–13	Punch the desired combination of "1's" and "0's" representing the output levels for outputs O_3, O_2, O_1 and O_0 (in that order), for the first word on the card, '0' = Low, '1' = High.
14	Blank
15–18	Punch the desired combination of "1's" and "0's" representing the output levels for the second word on the card.
19	Blank
20–23	Punch the desired combination of "1's" and "0's" representing the output levels for the third word on the card.
24	Blank
25–28	Punch the desired combination of "1's" and "0's" representing the output levels for the fourth word on the card.
29	Blank
30–33	Punch the desired combination of "1's" and "0's" representing the output levels for the fifth word on the card.
34	Blank

CARDS NO. 3 through 34 – Truth Table Deck (cont'd)

Column	Content
35–38	Punch the desired combination of "1's" and "0's" representing the output levels for the sixth word on the card.
39	Blank
40–43	Punch the desired combination of "1's" and "0's" representing the output levels for the seventh word on the card.
44	Blank
45–48	Punch the desired combination of "1's" and "0's" representing the output levels for the eighth word on the card.
49	Blank
50–51	Repeat chip select code option as in columns 13 and 14 of card number 2.
52–59	Blank
60–66	Repeat FAIRCHILD PART NUMBER (this number is used for positive identificaiton).
67	Blank
68–80	Use optional.

93406 Address Scheme

The 93406 is organized 256 words by 4 bits. The words are numbered 0 through 255 and are addressed using sequential addressing of address inputs A_0 through A_7, with A_0 as the least significant digit.

	INPUTS							
WORD	Pin 15	Pin 1	Pin 2	Pin 3	Pin 4	Pin 7	Pin 6	Pin 5
	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
WORD 0	0	0	0	0	0	0	0	0
WORD 1	0	0	0	0	0	0	0	1
WORD 2	0	0	0	0	0	0	1	0
WORD 3	0	0	0	0	0	0	1	1
↓	↓	↓	↓	↓	↓	↓	↓	↓
WORD 255	1	1	1	1	1	1	1	1

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	0°C to +75°C
V_{CC} Pin Potential to Ground	−0.5 V to +8.0 V
Input Pin Voltage	−1.5 V to +5.5 V
Current into Output Terminal	100 mA
Output Voltages	−0.5 V to V_{CC} Value

D.C. ELECTRICAL CHARACTERISTICS (T_A = 0°C to +75°C, V_{CC} = 5.0 V ±5%)

SYMBOL	CHARACTERISTIC	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	CONDITIONS
I_{CEX}	Output Leakage Current			40	μA	V_{CC} = 5.25 V, V_{CEX} = 5.25V Address any HIGH output
V_{OL}	Output LOW Voltage			0.45	Volts	V_{CC} = 4.75 V, I_{OL} = 15 mA Address any LOW output
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed input logical HIGH voltage for all inputs
V_{IL}	Input LOW Voltage			0.85	Volts	Guaranteed input logical LOW voltage for all inputs
I_F	Input LOW Current				mA	V_{CC} = 5.25 V, V_F = 0.45 V
	I_{FA} (Address Inputs)			0.8		
	I_{FCS} (Chip Select Inputs)			0.8		
I_R	Input HIGH, Current				μA	V_{CC} = 5.25 V, V_R = 4.5 V
	I_{RA} (Address Inputs)			40		
	I_{RCS} (Chip Select Input)			40		
I_{PD}	Power Supply Current		114	130	mA	V_{CC} = 5.25 V, Outputs open Inputs grounded and chip selected
C_O	Output Capacitance		6.5		pF	V_{CC} = 5.0 V, V_O = 5.0 V, f = 1.0 MHz
V_C	Input Clamp Diode Voltage		−0.8	−1.0	Volts	V_{CC} = 4.75 V, I_A = −5.0 mA

TTL LOADING RULES

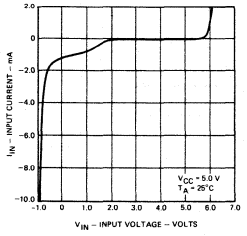
INPUT	LOADING HIGH	LOADING LOW
A_7 to A_0	1 U.L.	0.5 U.L.
$\overline{CS}_1$, CS_2	1 U.L.	0.5 U.L.

1 U.L. = 40 μA HIGH/1.6 mA LOW

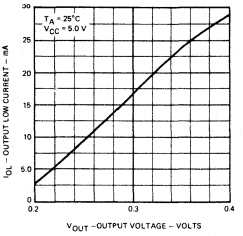
OUTPUTS	DRIVE FACTOR HIGH	DRIVE FACTOR LOW
O_0 to O_3	OPEN COLLECTOR	9.3

TYPICAL ELECTRICAL CHARACTERISTICS

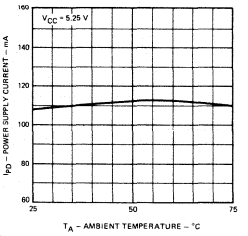
INPUT CURRENT VERSUS INPUT VOLTAGE



OUTPUT LOW CURRENT VERSUS OUTPUT VOLTAGE



POWER SUPPLY CURRENT VERSUS AMBIENT TEMPERATURE



SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 0°C to +75°C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITION
t_{pd++}	Propagation Delay Time, LOW to HIGH Output from Chip Select (or Address) LOW to HIGH			50	ns	C_L = 30 pF R_{L1} = 300Ω R_{L2} = 600Ω See Fig. 4
t_{pd+-}	Propagation Delay Time, HIGH to LOW Output from Chip Select (or Address) LOW to HIGH			50	ns	
t_{pd-+}	Propagation Delay Time, LOW to HIGH Output from Chip Select (or Address) HIGH to LOW			50	ns	
t_{pd--}	Propagation Delay Time, HIGH to LOW Output from Chip Select (or Address) HIGH to LOW		30	50	ns	

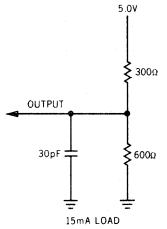
NOTE:
First + or – of t_{pd} indicates change in chip select, or address line. Second + or – indicates change in output.

"+" ≡ Low Voltage to High Voltage

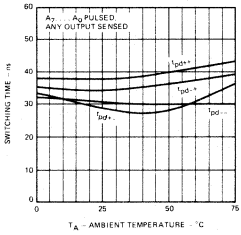
"–" ≡ High Voltage to Low Voltage

NOTES:
(1) To test CS delay, apply input pulse to CS input. The word selected must contain a '0' in the bit under test.
(2) To test t_{pd++} and t_{pd--} delay, apply input pulse to the address input under test. The word selected must contain '0' when the input pulse is low, and a '1' when the input pulse is high in the bit under test.
(3) To test t_{pd+-} and t_{pd-+} delay, apply input pulse to the address input under test. The word selected must contain a '1' when the input pulse is low, and a '0' when the input pulse is high in the bit under test.

SWITCHING TEST OUTPUT LOAD



SWITCHING TIME VERSUS AMBIENT TEMPERATURE



CHIP SELECT DELAY TIME VERSUS AMBIENT TEMPERATURE (CS_1 TO O_0)

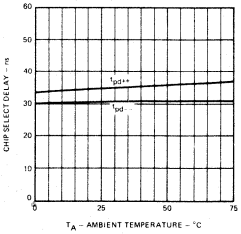
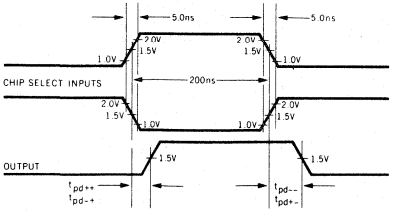
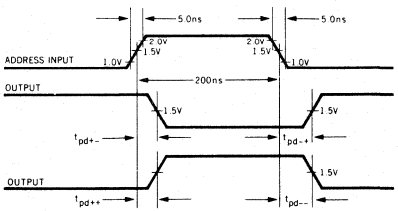


Fig. 4

SWITCHING WAVEFORMS





APPLICATIONS

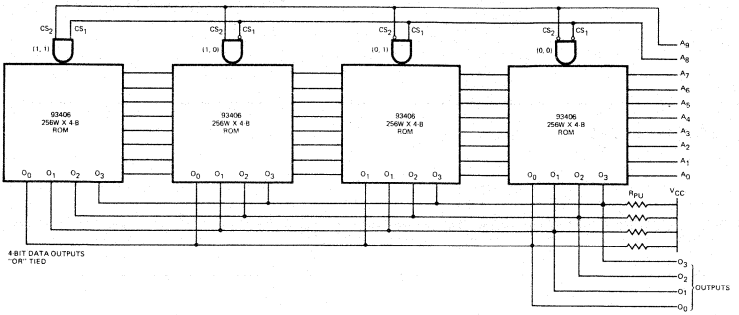


Fig. 5 1024 WORD X 4-BIT ROM PROGRAMMED CHIP SELECT (NO EXTERNAL GATING REQUIRED)

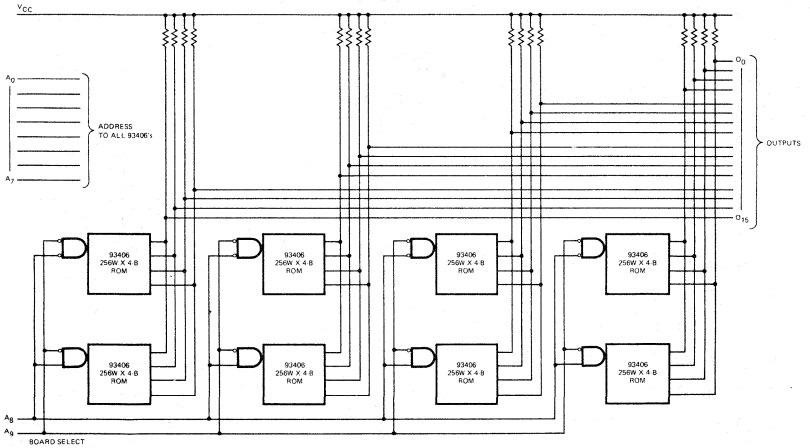
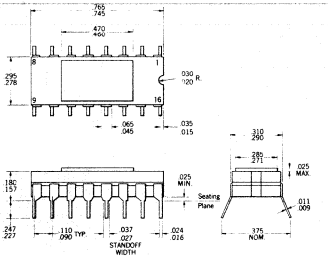


Fig. 6 512 WORD BY 16-BIT READ ONLY MEMORY

PHYSICAL DIMENSIONS

16 Lead MSI Dual In-Line



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" rhisalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin plated kovar
Package weight is 2.2 grams
* The .037/.027 dimensions does not apply to the corner leads

TTL MEMORY 93406
1024-BIT READ ONLY MEMORY
CUSTOMER CODING FORM

CUSTOM ROM TRUTH TABLE

CUSTOMER _____ Location _____

Cust. P/N _____ Cust. Dwg. # _____

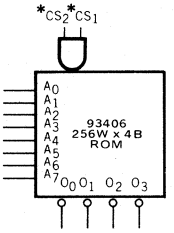
Function _____ SL # _____

Chip Select Code – CS_1 (13) = ___, CS_2 (14) = ___.*

*If not specified, ship select code will be '00'. Package pin numbers are shown in parenthesis.

Input								Word	Output			
MSB									MSB			
A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	#	O_3	O_2	O_1	O_0
0	0	0	0	0	0	0	0	0				
0	0	0	0	0	0	0	1	1				
0	0	0	0	0	0	1	0	2				
0	0	0	0	0	0	1	1	3				
0	0	0	0	0	1	0	0	4				
0	0	0	0	0	1	0	1	5				
0	0	0	0	0	1	1	0	6				
0	0	0	0	0	1	1	1	7				
0	0	0	0	1	0	0	0	8				
0	0	0	0	1	0	0	1	9				
0	0	0	0	1	0	1	0	10				
0	0	0	0	1	0	1	1	11				
0	0	0	0	1	1	0	0	12				
0	0	0	0	1	1	0	1	13				
0	0	0	0	1	1	1	0	14				
0	0	0	0	1	1	1	1	15				
15	1	2	3	4	7	6	5	Pkg. Pin #	9	10	11	12

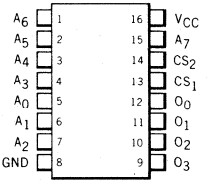
LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

*Chip selects active level may be programmed per customer requirements. If not specified both CS will be active low.

PIN CONFIGURATION



FAIRCHILD
SEMICONDUCTOR

TTL MEMORY 93406

Input								Word	Output			
MSB									MSB			
A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	#	O_3	O_2	O_1	O_0
0	0	0	1	0	0	0	0	16				
0	0	0	1	0	0	0	1	17				
0	0	0	1	0	0	1	0	18				
0	0	0	1	0	0	1	1	19				
0	0	0	1	0	1	0	0	20				
0	0	0	1	0	1	0	1	21				
0	0	0	1	0	1	1	0	22				
0	0	0	1	0	1	1	1	23				
0	0	0	1	1	0	0	0	24				
0	0	0	1	1	0	0	1	25				
0	0	0	1	1	0	1	0	26				
0	0	0	1	1	0	1	1	27				
0	0	0	1	1	1	0	0	28				
0	0	0	1	1	1	0	1	29				
0	0	0	1	1	1	1	0	30				
0	0	0	1	1	1	1	1	31				
0	0	1	0	0	0	0	0	32				
0	0	1	0	0	0	0	1	33				
0	0	1	0	0	0	1	0	34				
0	0	1	0	0	0	1	1	35				
0	0	1	0	0	1	0	0	36				
0	0	1	0	0	1	0	1	37				
0	0	1	0	0	1	1	0	38				
0	0	1	0	0	1	1	1	39				
0	0	1	0	1	0	0	0	40				
0	0	1	0	1	0	0	1	41				
0	0	1	0	1	0	1	0	42				
0	0	1	0	1	0	1	1	43				
0	0	1	0	1	1	0	0	44				
0	0	1	0	1	1	0	1	45				
0	0	1	0	1	1	1	0	46				
0	0	1	0	1	1	1	1	47				
0	0	1	1	0	0	0	0	48				
0	0	1	1	0	0	0	1	49				
0	0	1	1	0	0	1	0	50				
15	1	2	3	4	7	6	5	Pkg. Pin #	9	10	11	12

Input								Word	Output			
MSB									MSB			
A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	#	O_3	O_2	O_1	O_0
0	0	1	1	0	0	1	1	51				
0	0	1	1	0	1	0	0	52				
0	0	1	1	0	1	0	1	53				
0	0	1	1	0	1	1	0	54				
0	0	1	1	0	1	1	1	55				
0	0	1	1	1	0	0	0	56				
0	0	1	1	1	0	0	1	57				
0	0	1	1	1	0	1	0	58				
0	0	1	1	1	0	1	1	59				
0	0	1	1	1	1	0	0	60				
0	0	1	1	1	1	0	1	61				
0	0	1	1	1	1	1	0	62				
0	0	1	1	1	1	1	1	63				
0	1	0	0	0	0	0	0	64				
0	1	0	0	0	0	0	1	65				
0	1	0	0	0	0	1	0	66				
0	1	0	0	0	0	1	1	67				
0	1	0	0	0	1	0	0	68				
0	1	0	0	0	1	0	1	69				
0	1	0	0	0	1	1	0	70				
0	1	0	0	0	1	1	1	71				
0	1	0	0	1	0	0	0	72				
0	1	0	0	1	0	0	1	73				
0	1	0	0	1	0	1	0	74				
0	1	0	0	1	0	1	1	75				
0	1	0	0	1	1	0	0	76				
0	1	0	0	1	1	0	1	77				
0	1	0	0	1	1	1	0	78				
0	1	0	0	1	1	1	1	79				
0	1	0	1	0	0	0	0	80				
0	1	0	1	0	0	0	1	81				
0	1	0	1	0	0	1	0	82				
0	1	0	1	0	0	1	1	83				
0	1	0	1	0	1	0	0	84				
0	1	0	1	0	1	0	1	85				
15	1	2	3	4	7	6	5	Pkg. Pin #	9	10	11	12

TTL MEMORY 93406

Input									Output				Input									Output			
MSB								Word	MSB				MSB								Word	MSB			
A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	#	O_3	O_2	O_1	O_0	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	#	O_3	O_2	O_1	O_0
0	1	0	1	0	1	1	0	86					0	1	1	1	1	0	0	1	121				
0	1	0	1	0	1	1	1	87					0	1	1	1	1	0	1	0	122				
0	1	0	1	1	0	0	0	88					0	1	1	1	1	0	1	1	123				
0	1	0	1	1	0	0	1	89					0	1	1	1	1	1	0	0	124				
0	1	0	1	1	0	1	0	90					0	1	1	1	1	1	0	1	125				
0	1	0	1	1	0	1	1	91					0	1	1	1	1	1	1	0	126				
0	1	0	1	1	1	0	0	92					0	1	1	1	1	1	1	1	127				
0	1	0	1	1	1	0	1	93					1	0	0	0	0	0	0	0	128				
0	1	0	1	1	1	1	0	94					1	0	0	0	0	0	0	1	129				
0	1	0	1	1	1	1	1	95					1	0	0	0	0	0	1	0	130				
0	1	1	0	0	0	0	0	96					1	0	0	0	0	0	1	1	131				
0	1	1	0	0	0	0	1	97					1	0	0	0	0	1	0	0	132				
0	1	1	0	0	0	1	0	98					1	0	0	0	0	1	0	1	133				
0	1	1	0	0	0	1	1	99					1	0	0	0	0	1	1	0	134				
0	1	1	0	0	1	0	0	100					1	0	0	0	0	1	1	1	135				
0	1	1	0	0	1	0	1	101					1	0	0	0	1	0	0	0	136				
0	1	1	0	0	1	1	0	102					1	0	0	0	1	0	0	1	137				
0	1	1	0	0	1	1	1	103					1	0	0	0	1	0	1	0	138				
0	1	1	0	1	0	0	0	104					1	0	0	0	1	0	1	1	139				
0	1	1	0	1	0	0	1	105					1	0	0	0	1	1	0	0	140				
0	1	1	0	1	0	1	0	106					1	0	0	0	1	1	0	1	141				
0	1	1	0	1	0	1	1	107					1	0	0	0	1	1	1	0	142				
0	1	1	0	1	1	0	0	108					1	0	0	0	1	1	1	1	143				
0	1	1	0	1	1	0	1	109					1	0	0	1	0	0	0	0	144				
0	1	1	0	1	1	1	0	110					1	0	0	1	0	0	0	1	145				
0	1	1	0	1	1	1	1	111					1	0	0	1	0	0	1	0	146				
0	1	1	1	0	0	0	0	112					1	0	0	1	0	0	1	1	147				
0	1	1	1	0	0	0	1	113					1	0	0	1	0	1	0	0	148				
0	1	1	1	0	0	1	0	114					1	0	0	1	0	1	0	1	149				
0	1	1	1	0	0	1	1	115					1	0	0	1	0	1	1	0	150				
0	1	1	1	0	1	0	0	116					1	0	0	1	0	1	1	1	151				
0	1	1	1	0	1	0	1	117					1	0	0	1	1	0	0	0	152				
0	1	1	1	0	1	1	0	118					1	0	0	1	1	0	0	1	153				
0	1	1	1	0	1	1	1	119					1	0	0	1	1	0	1	0	154				
0	1	1	1	1	0	0	0	120					1	0	0	1	1	0	1	1	155				
15	1	2	3	4	7	6	5	Pkg. Pin #	9	10	11	12	15	1	2	3	4	7	6	5	Pkg. Pin #	9	10	11	12

TTL MEMORY 93406

Input MSB A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Word #	Output MSB O_3	O_2	O_1	O_0
1	0	0	1	1	1	0	0	156				
1	0	0	1	1	1	0	1	157				
1	0	0	1	1	1	1	0	158				
1	0	0	1	1	1	1	1	159				
1	0	1	0	0	0	0	0	160				
1	0	1	0	0	0	0	1	161				
1	0	1	0	0	0	1	0	162				
1	0	1	0	0	0	1	1	163				
1	0	1	0	0	0	0	0	164				
1	0	1	0	0	1	0	1	165				
1	0	1	0	0	1	1	0	166				
1	0	1	0	0	1	1	1	167				
1	0	1	0	1	1	0	0	168				
1	0	1	0	1	0	0	1	169				
1	0	1	0	1	0	1	0	170				
1	0	1	0	1	0	1	1	171				
1	0	1	0	1	1	0	0	172				
1	0	1	0	1	1	0	1	173				
1	0	1	0	1	1	1	0	174				
1	0	1	0	1	1	1	1	175				
1	0	1	1	0	0	0	0	176				
1	0	1	1	0	0	0	1	177				
1	0	1	1	0	0	1	0	178				
1	0	1	1	0	0	1	1	179				
1	0	1	1	0	1	0	0	180				
1	0	1	1	0	1	0	1	181				
1	0	1	1	0	1	1	0	182				
1	0	1	1	0	1	1	1	183				
1	0	1	1	1	0	0	0	184				
1	0	1	1	1	0	0	1	185				
1	0	1	1	1	0	1	0	186				
1	0	1	1	1	0	1	1	187				
1	0	1	1	1	1	0	0	188				
1	0	1	1	1	1	0	1	189				
1	0	1	1	1	1	1	0	190				
15	1	2	3	4	7	6	5	Pkg. Pin #	9	10	11	12

Input MSB A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Word #	Output MSB O_3	O_2	O_1	O_0
1	0	1	1	1	1	1	1	191				
1	1	0	0	0	0	0	0	192				
1	1	0	0	0	0	0	1	193				
1	1	0	0	0	0	1	0	194				
1	1	0	0	0	0	1	1	195				
1	1	0	0	0	1	0	0	196				
1	1	0	0	0	1	0	1	197				
1	1	0	0	0	1	1	0	198				
1	1	0	0	0	1	1	1	199				
1	1	0	0	1	0	0	0	200				
1	1	0	0	1	0	0	1	201				
1	1	0	0	1	0	1	0	202				
1	1	0	0	1	0	1	1	203				
1	1	0	0	1	1	0	0	204				
1	1	0	0	1	1	0	1	205				
1	1	0	0	1	1	1	0	206				
1	1	0	0	1	1	1	1	207				
1	1	0	1	0	0	0	0	208				
1	1	0	1	0	0	0	1	209				
1	1	0	1	0	0	1	0	210				
1	1	0	1	0	0	1	1	211				
1	1	0	1	0	1	0	0	212				
1	1	0	1	0	1	0	1	213				
1	1	0	1	0	1	1	0	214				
1	1	0	1	0	1	1	1	215				
1	1	0	1	1	0	0	0	216				
1	1	0	1	1	0	0	1	217				
1	1	0	1	1	0	1	0	218				
1	1	0	1	1	0	1	1	219				
1	1	0	1	1	1	0	0	220				
1	1	0	1	1	1	0	1	221				
1	1	0	1	1	1	1	0	222				
1	1	0	1	1	1	1	1	223				
1	1	1	0	0	0	0	0	224				
1	1	1	0	0	0	0	1	225				
15	1	2	3	4	7	6	5	Pkg. Pin #	9	10	11	12

Input									Output			
MSB								Word	MSB			
A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	#	O_3	O_2	O_1	O_0
1	1	1	0	0	0	1	0	226				
1	1	1	0	0	0	1	1	227				
1	1	1	0	0	1	0	0	228				
1	1	1	0	0	1	0	1	229				
1	1	1	0	0	1	1	0	230				
1	1	1	0	0	1	1	1	231				
1	1	1	0	1	0	0	0	232				
1	1	1	0	1	0	0	1	233				
1	1	1	0	1	0	1	0	234				
1	1	1	0	1	0	1	1	235				
1	1	1	0	1	1	0	0	236				
1	1	1	0	1	1	0	1	237				
1	1	1	0	1	1	1	0	238				
1	1	1	0	1	1	1	1	239				
1	1	1	1	0	0	0	0	240				
1	1	1	1	0	0	0	1	241				
1	1	1	1	0	0	1	0	242				
1	1	1	1	0	0	1	1	243				
1	1	1	1	0	1	0	0	244				
1	1	1	1	0	1	0	1	245				
1	1	1	1	0	1	1	0	246				
1	1	1	1	0	1	1	1	247				
1	1	1	1	1	0	0	0	248				
1	1	1	1	1	0	0	1	249				
1	1	1	1	1	0	1	0	250				
1	1	1	1	1	0	1	1	251				
1	1	1	1	1	1	0	0	252				
1	1	1	1	1	1	0	1	253				
1	1	1	1	1	1	1	0	254				
1	1	1	1	1	1	1	1	255				
15	1	2	3	4	7	6	5	Pkg. Pin #	9	10	11	12

Customers Authorizing Signature _____

Date _____

Qualified FSC Representative _____

Date _____

TTL ISOPLANAR MEMORY 93410
256-BIT FULLY DECODED READ/WRITE MEMORY

GENERAL DESCRIPTION – The 93410 is a high speed 256-bit TTL read/write memory with full decoding on chip. The memory organized as 256 words x 1 bit is designed for scratch pad, buffer and distributed main memory applications.

The 93410 has three chip select lines to simplify its use in larger memory systems. Address input pin locations are specifically chosen to permit maximum packaging density and for ease of PC board layout. An uncommitted collector output is provided to permit "OR-ties" for ease of memory expansion.

The 93410 is manufactured with the Fairchild Isoplanar technology. It is fully compatible with standard DTL and TTL logic families.

- **ORGANIZATION - 256 WORDS X 1 BIT**
- **THREE HIGH SPEED CHIP SELECT INPUTS**
- **50 ns READ ACCESS TIME**
- **NON INVERTED DATA OUTPUT**
- **ON CHIP DECODING**
- **POWER DISSIPATION - 2 mW/BIT**
- **TTL COMPATIBLE**

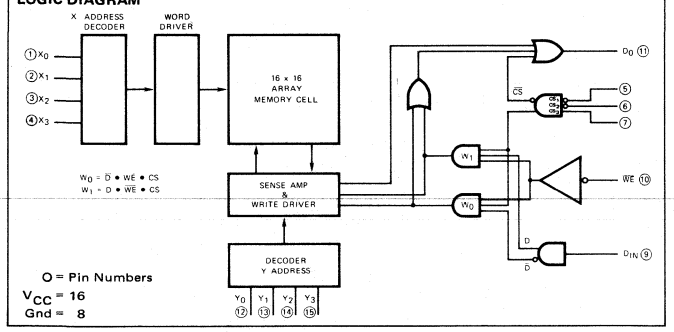
PIN NAMES

$\overline{CS}_1$ $\overline{CS}_2$ CS_3	Chip Select Input
X_0 X_1 X_2 X_3	X Address Inputs
Y_0 Y_1 Y_2 Y_3	Y Address Inputs
D_{IN}	Data Input
D_{OUT}	Data Output
$\overline{WE}$	Write Enable

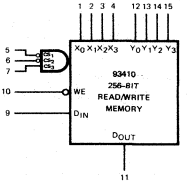
ORDER INFORMATION

Specify A7B9341059X for the 0°C to +75°C temperature range in the 16 pin Dual In-Line package.

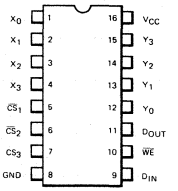
LOGIC DIAGRAM



LOGIC SYMBOL



CONNECTION DIAGRAM
DIP (TOP VIEW)



FAIRCHILD
SEMICONDUCTOR

FUNCTIONAL DESCRIPTION

The 93410 is a fully decoded 256-bit read/write memory organized 256 words by 1 bit. Bit selection is achieved by means of an 8-bit address split into two groups of 4; X_0, X_1, X_2, X_3 and Y_0, Y_1, Y_2, Y_3.

Three chip select inputs are provided, two are active Low ($\overline{CS_1}$ and $\overline{CS_2}$) and the third active High (CS_3) for maximum logic flexibility. This permits memory array expansion up to 2048 words without the need for additional external decoders. For larger memories the fast chip select access time permits the decoding of chip select, CS, from the address without affecting system performance.

The read and write operations are controlled by the state of the active Low Write Enable $\overline{WE}$ (pin 10). With $\overline{WE}$ held Low and the chip selected, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held High and the chip selected. Data in the specified location is presented at D_{OUT} and is non-inverted.

Uncommitted collector outputs are provided on the 93410 to allow maximum flexibility in output connection. In many applications such as memory expansion, the outputs of many 93410 can be tied together. In other applications the wired-OR is not used. In either case an external pullup resistor of value R_L must be used to provide a High at the output when it is off. Any value of R_L within the range specified below may be used.

$$\frac{5.25}{16\text{-F.O. } (1.6)} \leqslant R_L \leqslant \frac{2.25}{N\ (0.05) + \text{F.O. } (0.04)}$$

R_L is in kΩ
N = number of wired-OR output
F.O. = number of TTL loads driven
V_{CC} = 5.0V ± 5%

The minimum value of R_L is limited by output current sinking ability. The maximum value of R_L is determined by the output and input leakage current (I_{CEX} = 50 μA and I_R) which must be supplied to hold the output at 2.4V.

TABLE I – TRUTH TABLE

INPUTS			OUTPUT	MODE
CS*	$\overline{WE}$	DI	Open Collector	
H	X	X	H	NOT SELECTED
L	L	L	H	WRITE "0"
L	L	H	H	WRITE "1"
L	H	X	D_0	READ

*CS High or Low in this table refers to the function – not to individual pins
CS Low = $L_{Pin\ 5} \bullet L_{Pin\ 6} \bullet H_{Pin\ 7}$
CS High = $\overline{\text{CS Low}}$

H = High Voltage
L = Low Voltage
X = Don't Care (High or Low)

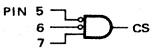


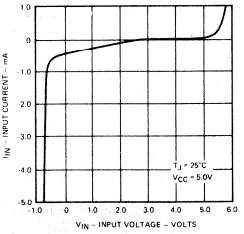
TABLE II – TTL LOADING RULES

INPUTS	LOADING	
	LOW LEVEL	HIGH LEVEL
X_0, X_1, X_2, X_3	0.5 U.L.	0.5 U.L.
Y_0, Y_1, Y_2, Y_3	0.5 U.L.	0.5 U.L.
$\overline{WE}$	0.5 U.L.	0.5 U.L.
$\overline{CS_1}$, $\overline{CS_2}$, CS_3	0.5 U.L.	0.5 U.L.
D_{IN}	0.5 U.L.	0.5 U.L.
OUTPUT	DRIVE FACTOR	
	HIGH	LOW
D_{OUT}	Open Collector	10 U.L.

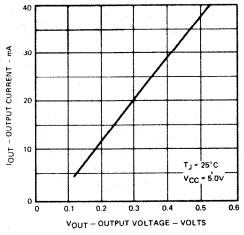
1 Low Level TTL Unit Load (U.L.) = 1.6 mA
1 High Level TTL Unit Load (U.L.) = 40 μA

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

INPUT CURRENT VERSUS INPUT VOLTAGE



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (LOW STATE)



ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +6.0 V
*Input Voltage (D.C.)	−0.5 V to +5.25 V
*Input Current (D.C.)	−12 mA to +5.0 mA
Voltage Applied to Outputs (Output High)	0.5 V to +5.25 V
Output Current (D.C.) (Output Low)	+20 mA

*All inputs tied to V_{CC} or 5.25V must have a 1.5kΩ resistor in series with the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC}) MIN.	TYP.	MAX.	CASE TEMPERATURE
A7B9341059X	4.75 V	5.0 V	5.25 V	0°C to 75°C

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	CHARACTERISTIC	LIMITS MIN.	TYP. (Note 4)	MAX.	UNITS	CONDITIONS
V_{OL}	Output Low Voltage		0.3	0.45	Volts	V_{CC} = MIN I_{OL} = 16 mA
V_{IH}	Input High Level	2.0	1.6		Volts	Guaranteed input logical High Voltage for all inputs
V_{IL}	Input Low Level		1.5	0.95	Volts	Guaranteed input logical Low Voltage for all inputs
I_{IL}	Input Low Current		−530	−750	μA	V_{CC} = MAX, V_{IN} = 0V
I_{IH}	Input High Current		1.0	20	μA	V_{CC} = MAX, V_{IN} = 4.5V
I_{CEX}	Output Leakage Current		1.0	50	μA	V_{CC} = MAX, V_{OUT} = 5.25V
BV_{IN}	Input Breakdown Voltage	5.25			Volts	V_{CC} = MAX, I_{IN} = 1.0 mA (See Note 5)
V_C	Input Diode Clamp Voltage		−1.0	−1.5	Volts	V_{CC} = MAX, I_{IN} = −10 mA
I_{CC}	Power Supply Current		95	125	mA	V_{CC} = MAX, V_{IN} = 0V All inputs grounded

NOTES:

(1) The actual Testing Procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this Specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California (see page 1 for address and phone).

(2) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.

(3) The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

(4) Typical limits are at V_{CC} = 5.0V, 25°C, and max. loading.

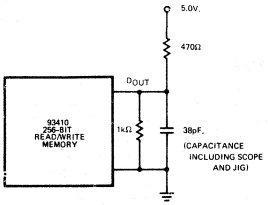
(5) All inputs tied to V_{CC} or 5.25V must have a 1.5kΩ resistor in series with the inputs.

SWITCHING CHARACTERISTICS (T_J = 25°C)

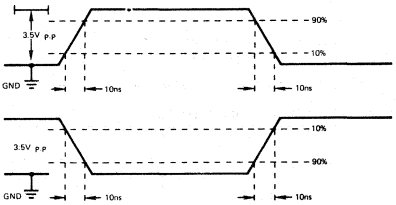
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
READ MODE						
t_{ACS}	Chip Select Access Time		30		ns	V_{CC} = 5.0V See Test Circuit
t_{RCS}	Chip Select Recovery Time		30		ns	
t_{AA}	Address Access Time		50		ns	
WRITE MODE						
t_W	Write Pulse Width		20		ns	V_{CC} = 5.0V See Test Circuit
t_{WSD}	Data Set-up Time Prior to Write		0		ns	
t_{WHD}	Data Hold Time After Write		0		ns	
t_{WSA}	Address Set-Up Time		0		ns	
t_{WHA}	Address Hold Time		5.0		ns	
t_{WSCS}	Chip Select Set-Up Time		0		ns	
t_{WHCS}	Chip Select Hold Time		0		ns	
t_{WS}	Write Disable Time		30		ns	
t_{WR}	Write Recovery Time		30		ns	
C_{IN}	Input Pin Capacitance		4.0		pF	Measure With a Pulse Technique
C_{OUT}	Output Pin Capacitance		7.0		pF	

93410 A.C. TEST LOAD AND WAVEFORM

LOADING CONDITION



INPUT PULSES

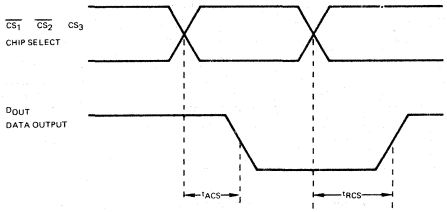


(ALL TIME MEASUREMENTS REFERENCED TO 1.5 V)

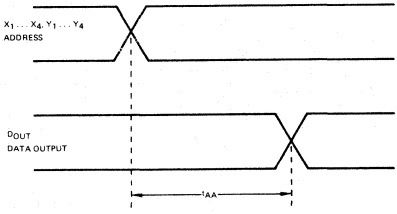
SWITCHING WAVEFORMS

READ MODE

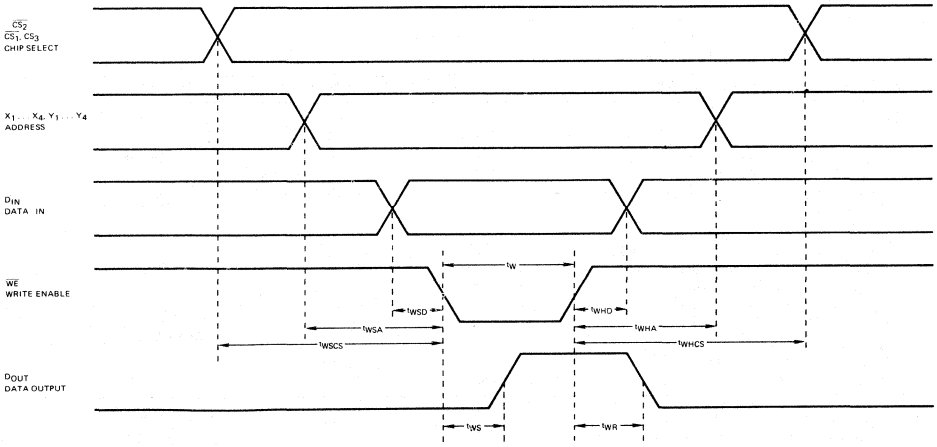
PROPAGATION DELAY FROM CHIP SELECT



PROPAGATION DELAY FROM ADDRESS

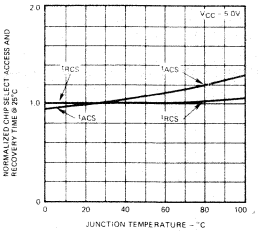


WRITE MODE

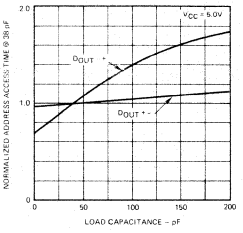


TYPICAL ELECTRICAL CHARACTERISTICS

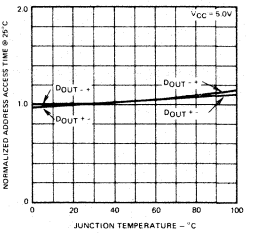
NORMALIZED CHIP SELECT ACCESS AND RECOVERY TIME VERSUS TEMPERATURE



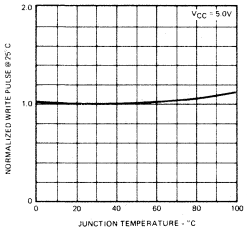
NORMALIZED ADDRESS ACCESS TIME VERSUS LOAD CAPACITANCE



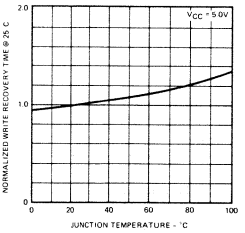
NORMALIZED ADDRESS ACCESS TIME VERSUS TEMPERATURE



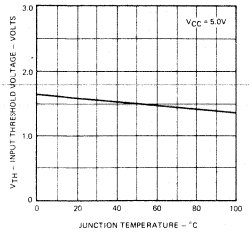
NORMALIZED WRITE PULSE WIDTH VERSUS TEMPERATURE



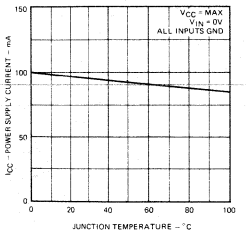
NORMALIZED WRITE RECOVERY TIME VERSUS TEMPERATURE



INPUT THRESHOLD VOLTAGE VERSUS TEMPERATURE



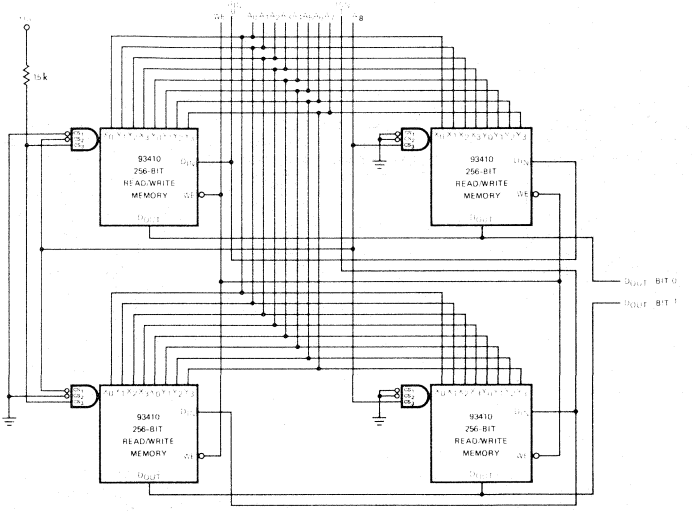
POWER SUPPLY CURRENT VERSUS TEMPERATURE



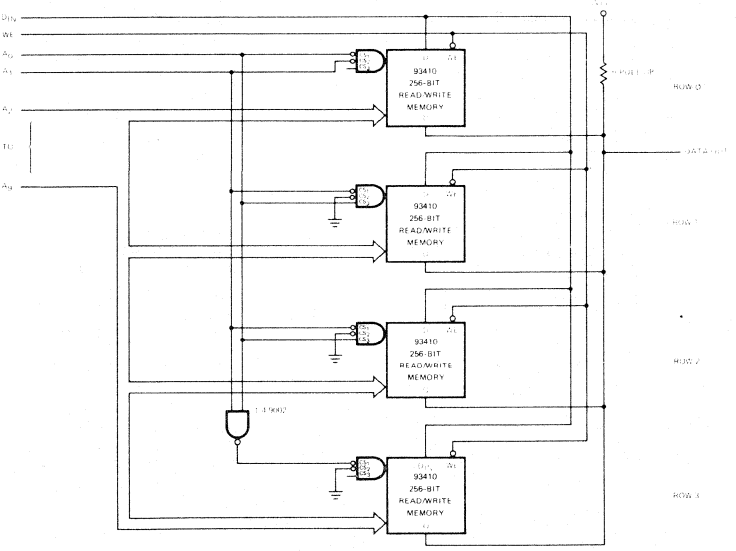
TYPICAL THERMAL RESISTANCE:

$\Theta_{J\text{-}C}$ (Junction to Case) = 40°C/Watt
$\Theta_{C\text{-}A}$ (Case to Ampient) = 75°C/Watt (Still Air)

APPLICATIONS

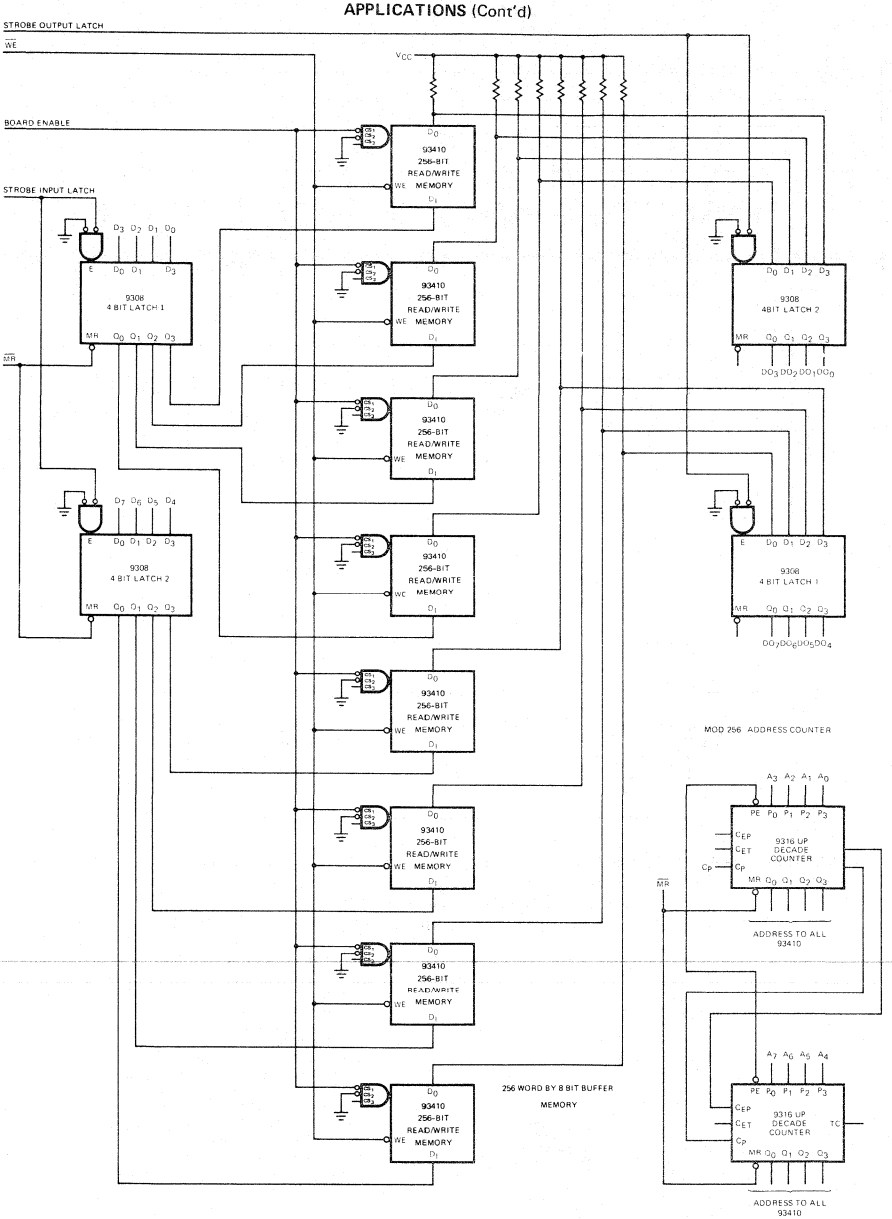


512 WORD X 2 BIT ARRAY



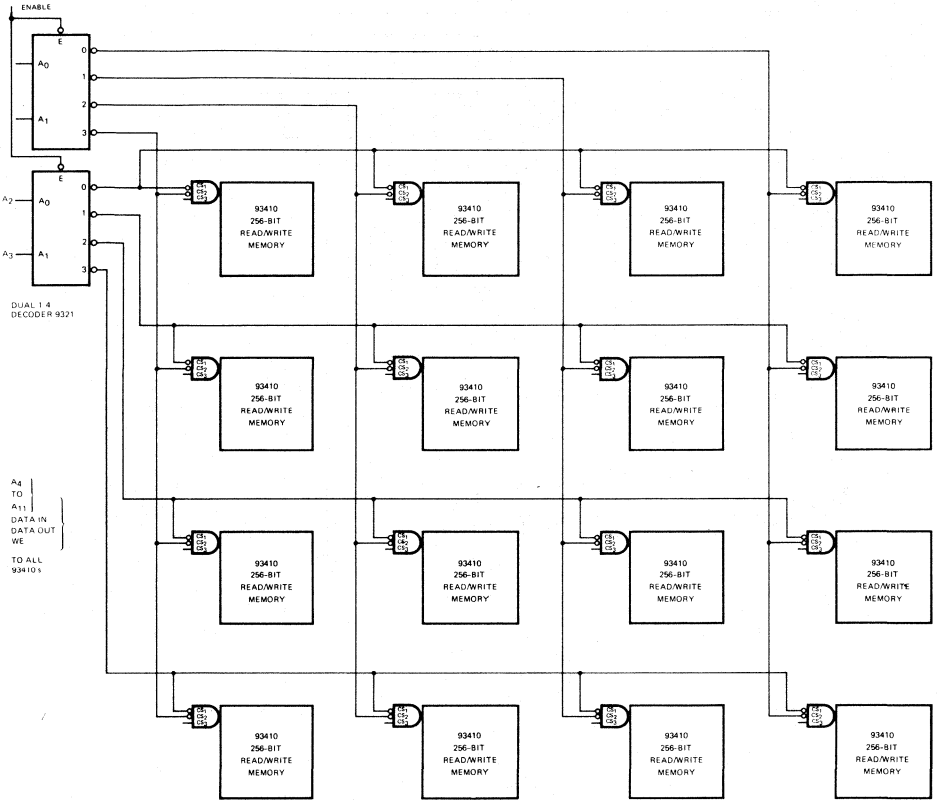
1024 WORD SYSTEM USING 93410's REQUIRES ONLY A SINGLE NAND GATE FOR ROW SELECTION

APPLICATIONS (Cont'd)



256 WORD BY 8 BIT BUFFER MEMORY SYSTEM

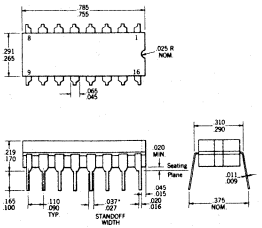
APPLICATIONS (Cont'd)



ADDRESSING FOR A 4096 BIT MEMORY PLANE (4k BY 1) REQUIRES ONLY ONE MSI DEVICE, A DUAL 1/4 DECODER.

PACKAGE INFORMATION

7B – 16 LEAD DUAL IN-LINE PACKAGE



NOTES:
All dimension in inches.
Leads are intended for insertion in hole rows on .300" centers.
They are purposely shipped with "positive" misalignment to facilitate insertion.
Board-drilling dimensions should equal your practice for .020 inch diameter lead.
Hermetically sealed alumina ceramic package.
Leads are tin-plated kovar.
Package weight is 2.2 grams.
The .037/.027 dimension does not apply to the *corner leads*.

TTμL MEMORY 93407 . 93433

16-BIT COINCIDENT SELECT READ/WRITE MEMORY

FAIRCHILD TTμL® IC PRODUCT FORMERLY 5033 . 9033

GENERAL DESCRIPTION — These devices are Planar* epitaxial integrated 16-bit, bit-oriented, non-destructive readout memory cells, compatible with Fairchild Transistor-Transistor Micrologic® (TTμL). These memory cells, organized as 16 words by one bit, are designed for high-speed scratch-pad memory applications. The 93407 and 93433 are electrically identical, but with different pin configurations.

OPERATION — The memory cell consists of 16 R-S flip-flops arranged in an addressable four-by-four matrix. The desired bit location is selected by raising the coincident X-Y address lines to a logic "H" level (>2.1 volts) and holding the non-selected address lines at logic "L" level (<0.7 volts). As many as four locations may be addressed simultaneously without destroying stored information. The stored data and its complement at the addressed bit location may be read at the output terminals. If the addressed bit location contains a "1", the S_1 output will be low and the S_0 output will be high. If the addressed bit location contains a "0", the S_1 output will be high and the S_0 output will be low.

Writing is accomplished by activating one of the write amplifiers. To write a "1", the desired bit location is addressed and the input of the "write one" (W_1) amplifier is raised to a High level. To write a "0", the input of the "write zero" (W_0) amplifier is raised to a High level.

The outputs are open-collector, which may be wire "OR"ed for word expansion. (The output transistors are off when none of the bits are selected.) An external resistor should be returned to V_{CC} to pull-up the wire "OR"ed outputs.

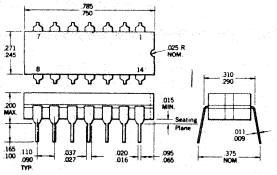
FEATURES

- **TTμL COMPATIBLE**
- **OUTPUT WIRED-OR CAPABILITY**
- **TRUE AND COMPLEMENTARY OUTPUTS ARE PROVIDED**
- **NON DESTRUCTIVE READ OUT**
- **FANOUT AVAILABLE IN TWO GRADES, 1 = 40 mA, 2 = 20 mA**

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

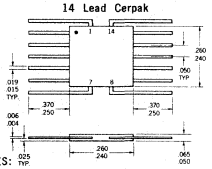
Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground	−0.5 V to +8.0 V
Input Pin Voltage	−1.5 V to +5.5 V
Current Into Output Terminal	100 mA
Output Voltage	−0.5 V to +8.0 V

PHYSICAL DIMENSIONS
in accordance with JEDEC (TO-116) outline
14 Lead Dual-In-line



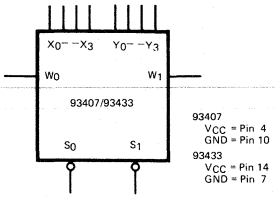
NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers.
They are purposely shipped with "positive" misalignment to facilitate insertion.
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.0 grams
*The .037 dimension does not apply .027 to the corner leads

PHYSICAL DIMENSIONS
in accordance with JEDEC (TO-86) outline
14 Lead Cerpak



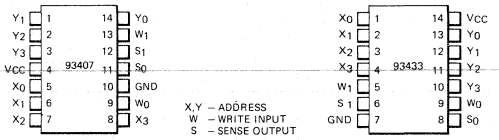
NOTES:
All dimensions in inches
Leads are gold-plated kovar
Package weight is 0.26 gram

BLOCK DIAGRAM



93407
V_{CC} = Pin 4
GND = Pin 10
93433
V_{CC} = Pin 14
GND = Pin 7

PIN CONFIGURATION



X,Y – ADDRESS
W – WRITE INPUT
S – SENSE OUTPUT

*Planar is a patented Fairchild process.

FAIRCHILD
SEMICONDUCTOR

ELECTRICAL CHARACTERISTICS ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$)

SYMBOL	TEST	LIMITS MIN.	LIMITS MAX.	UNITS	TEST CONDITIONS
I_{FX}	X Address Input Load Current		11	mA	$V_{CC} = 5.5\ V$, $V_X = 0\ V$, $V_Y = 4.5\ V$, other X inputs grounded
I_{FY}	Y Address Input Load Current		11	mA	$V_{CC} = 5.5\ V$, $V_Y = 0\ V$, $V_X = 4.5\ V$, other Y inputs grounded
I_{RX}	X Address Input Leakage Current		400	μA	$V_{CC} = 5.5\ V$, $V_X = 4.5\ V$, other X and Y inputs grounded
I_{RY}	Y Address Input Leakage Current		400	μA	$V_{CC} = 5.5\ V$, $V_Y = 4.5\ V$, other X and Y inputs grounded
I_{FW}	Write Input Load Current		1.5	mA	$V_{CC} = 5.5\ V$, $V_W = 0\ V$
I_{RW}	Write Input Leakage Current		100	μA	$V_{CC} = 5.5\ V$, $V_W = 4.5\ V$,
I_{CC}	Power Supply Current		65	mA	$V_{CC} = 5.5\ V$, All Inputs Grounded
I_{RV}	Power Supply Current at $V_{CC} = 7\ V$		84	mA	$V_{CC} = 7.0\ V$, All Inputs Grounded
I_{CEX}	Output Leakage Current		250	μA	$V_{CC} = 5.5\ V$, $V_{CEX} = 5.5\ V$, all inputs grounded
V_{OL}	Output Low Voltage		0.40	V	$V_{CC} = 4.5\ V$, One Bit Selected $I_{OL} = 20$ mA for 512 grade.
$V_{X(W)}$	Address Input Threshold to Prevent Writing		0.75	V[2]	$V_{CC} = 5.0\ V$, other X and Y grounded. Alternately pulse W_0 and W_1, cell must not change state.
$V_{X(W)}$	Address Input Threshold to insure Writing	2.1		V[2]	$V_{CC} = 5.0\ V$, other X and Y grounded. Alternately pulse W_0 and W_1, cell state must alternate.
$V_{X(R)}$	Address Input Threshold to Prevent Reading		0.8	V	$V_{CC} = 5.0\ V$, other inputs grounded. Both outputs must be on "high" state.
$V_{X(R)}$	Address Input Threshold to Insure Reading	2.1		V[2]	$V_{CC} = 5.0\ V$, other X and Y grounded. Alternately pulse W_0 and W_1, cell state must alternate.
$V_{W(W)}$	Write Input Threshold to Prevent Writing		0.8	V[2]	$V_{CC} = 5.0\ V$, one X and one Y to 4.5 V, other X and Y grounded. One write input to $V_{W(W)}$, pulse the other write input. If W_0 is pulsed, S_0 will assume low state. If W_1 is pulsed, S_1 will assume low state.
$V_{W(W)}$	Write Input Threshold to Insure Writing	2.1		V[2]	$V_{CC} = 5.0\ V$, one X and one Y to 4.5 V, other X and Y grounded. One write input to $V_{W(W)}$, pulse the other write input. If W_0 is pulsed, S_1 will assume low state. If W_1 is pulsed, S_0 will assume low state.

ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $75°C$, $V_{CC} = 5.0\ V \pm 5\%$)

SYMBOL	TEST	LIMITS MIN.	LIMITS MAX.	UNITS	TEST CONDITIONS
I_{FX}	X Address Input Load Current		11	mA	$V_{CC} = 5.25\ V$, $V_X = 0\ V$, $V_Y = 4.5\ V$, other X inputs grounded
I_{FY}	Y Address Input Load Current		11	mA	$V_{CC} = 5.25\ V$, $V_Y = 0\ V$, $V_X = 4.5\ V$, other X inputs grounded
I_{RX}	X Address Input Leakage Current		400	μA	$V_{CC} = 5.25\ V$, $V_X = 4.5\ V$, other X and Y inputs grounded
I_{RY}	Y Address Input Leakage Current		400	μA	$V_{CC} = 5.25\ V$, $V_Y = 4.5\ V$, other X and Y inputs grounded
I_{FW}	Write Input Load Current		1.5	mA	$V_{CC} = 5.25\ V$, $V_W = 0\ V$
I_{RW}	Write Input Leakage Current		100	μA	$V_{CC} = 5.25\ V$, $V_W = 4.5\ V$
I_{CC}	Power Supply Current		65	mA	$V_{CC} = 5.25\ V$, All Inputs Grounded
I_{RV}	Power Supply Current at $V_{CC} = 7\ V$		95	mA	$V_{CC} = 7.0\ V$, All Inputs Grounded
I_{CEX}	Output Leakage Current		250	μA	$V_{CC} = 5.25\ V$, $V_{CEX} = 5.5\ V$, all inputs grounded
V_{OL}	Output Low Voltage		0.45	V	$V_{CC} = 4.75\ V$, One bit selected $I_{OL} = 20$ mA for 592 grade. $I_{OL} = 40$ mA for 591 grade.
$V_{X(R)}$	Address Input Threshold to Prevent Writing		0.8	V[2]	$V_{CC} = 5.0\ V$, other X and Y grounded. Alternately pulse W_0 and W_1, cell must not change state.
$V_{X(W)}$	Address Input Threshold to insure Writing	2.0		V[2]	$V_{CC} = 5.0\ V$, other X and Y grounded. Alternately pulse W_0 and W_1, cell state must alternate.
$V_{X(R)}$	Address Input Threshold to Prevent Reading		1.0	V	$V_{CC} = 5.0\ V$, other inputs grounded. Both outputs must be on "high" state.
$V_{X(R)}$	Address Input Threshold to Insure Reading	2.0		V	$V_{CC} = 5.0\ V$, other X and Y grounded. Alternately pulse W_0 and W_1, cell state must alternate.
$V_{W(W)}$	Write Input Threshold to Prevent Writing		1.0	V[2]	$V_{CC} = 5.0\ V$, one X and one Y to 4.5 V, other X and Y grounded. One write input to $V_{W(W)}$, pulse the other write input. If W_0 is pulsed, S_0 will assume low state. If W_1 is pulsed, S_1 will assume low state.
$V_{W(W)}$	Write Input Threshold to Insure Writing	2.0		V[2]	$V_{CC} = 5.0\ V$, one X and one Y to 4.5 V, other X and Y grounded. One write input to $V_{W(W)}$, pulse the other write input. If W_0 is pulsed, S_1 will assume low state. If W_1 is pulsed, S_0 will assume low state.

[2] Amplitude of the pulse $\geq 2.5\ V$, pulse width ≥ 100 ns. The cell state is determined 35 ns after pulse disappears.

TTμL LOADING RULES

	HIGH LEVEL	LOW LEVEL
Address Input	6.5 U.L.	6.5 U.L.
Write Input	1.5 U.L.	0.9 U.L.
Sense Output	Open Collector	591 grade = 25 U.L. 512 or 592 grade = 12.5 U.L.

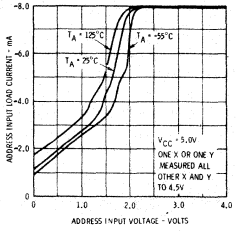
1 Low Level TTμL Unit Load (U.L.) = -1.6 mA
1 High Level TTμL Unit Load (U.L.) = 60 μA

ORDER INFORMATION

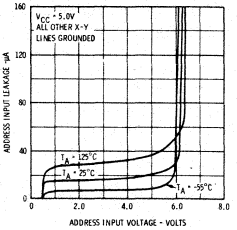
Flat Package — Specify A3I93407XXX or A3I93433XXX. Dual In-Line Package — Specify A6A93407XXX or A6A93433XXX where XXX is 51X for $-55°C$ to $+125°C$ Temperature Range, or XXX is 59X for $0°C$ to $+75°C$ Temperature Range; the last X in the order code is 1 for 40 mA Fanout and 2 for 20 mA Fanout.

TYPICAL ELECTRICAL CHARACTERISTICS

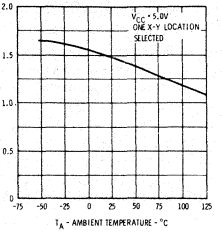
ADDRESS INPUT LOAD CURRENT VERSUS INPUT VOLTAGE



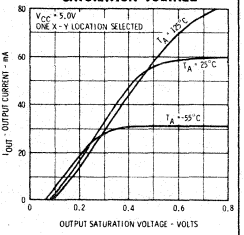
ADDRESS INPUT LEAKAGE CURRENT VERSUS INPUT VOLTAGE



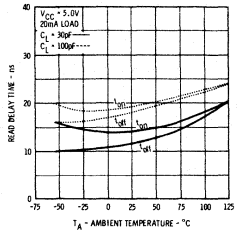
ADDRESS INPUT READ THRESHOLD VOLTAGE VERSUS AMBIENT TEMPERATURE



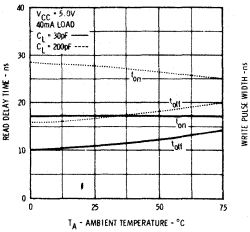
OUTPUT CURRENT VERSUS OUTPUT SATURATION VOLTAGE



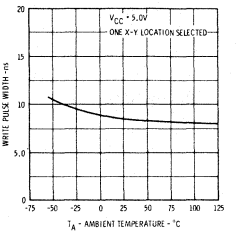
READ DELAY VERSUS AMBIENT TEMPERATURE 20 mA LOAD



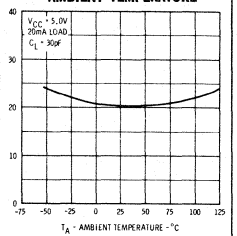
READ DELAY VERSUS AMBIENT TEMPERATURE 40 mA LOAD



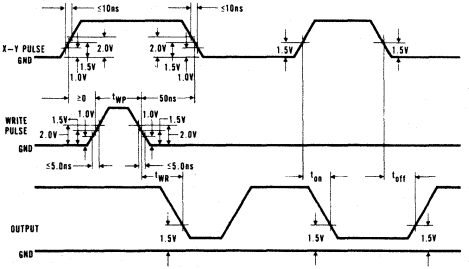
WRITE PULSE WIDTH VERSUS AMBIENT TEMPERATURE

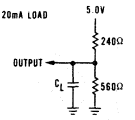


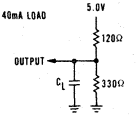
WRITE RECOVERY TIME VERSUS AMBIENT TEMPERATURE



SWITCHING TIME TEST CIRCUIT AND WAVEFORMS







SWITCHING CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V, One X-Y Location Selected.)

SYMBOL	CHARACTERISTICS	512 GRADE MIN.	512 GRADE MAX.	591 GRADE MIN.	591 GRADE MAX.	592 GRADE MIN.	592 GRADE MAX.	UNITS	CONDITIONS LOAD (mA)	CONDITIONS C_L (pF)
t_{WP}	Write Pulse Width	25		25		25		ns	40	
									20	
t_{WR}	Write Recovery Time		40		35		35	ns	40	30
									20	30
t_{on}	Turn On Delay			20				ns	40	30
				30					40	200
			25			20			20	30
			35			30			20	100
t_{off}	Turn Off Read Delay			20				ns	40	30
				30					40	200
			25			20			20	30
			35			30			20	100

APPLICATION:

A memory utilizing these memory cells may have any desired word length. The number of words in the memory is a multiple of four words. The following example of a 64 word memory illustrates how a number of 16 bit memory cells may be used to construct a typical memory.

The 64 word memory as shown in Figure A consists of groups of four memory cells. Each of the groups of four memory cells supplies one bit for each of the 64 words stored in the memory. All bits belonging to one word are stored in the same address location. Therefore, the address of a word in the memory is the address of each of the bits of the addressed word in the groups of four memory cells. The equal outputs of the four memory cells are tied together so that each group of four memory cells has one high and one low level output.

The six memory address lines from an external source are decoded at the first level with two 9301 decoders. The fourth input to each of the two decoders can be used as an enable control input to the 64 word memory. If the address enable is at a low logic level, one and only one of the eight outputs, 0 to 7, in the illustration assumes a low logic level. If the address enable is at a high logic level, the outputs 0 to 7 of the two decoders assume a high logic level, thus none of the 64 words stored in the memory is addressed. The outputs, 0 to 7, of the two decoders serve as X-and-Y address lines. The output signals of the decoders are connected to driving transistors which provide the necessary current to address the memory cells.

The example given above is only one of the many organizations and is presented as an illustration. Obviously many address decoding schemes may be utilized depending on memory size, driver fan-out, decoder fan-out, wiring, heat dissipation, etc.

Figures B through D show alternative schemes to enter data into the memory cell.

LOGIC DIAGRAM

Fig. A

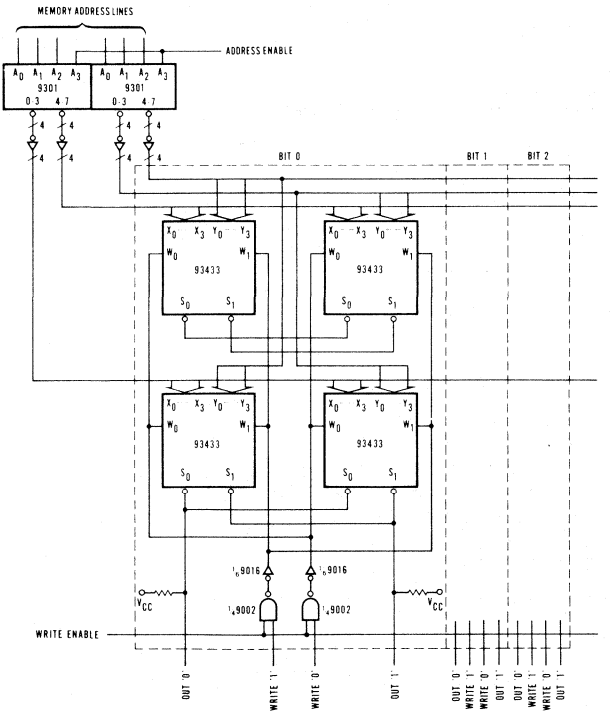


Fig. B
DOUBLE RAIL ACTIVE
LOW INPUTS AND ENABLE

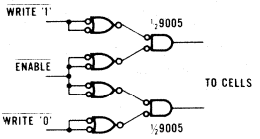


Fig. C
SINGLE RAIL ACTIVE
HIGH INPUT AND ENABLE

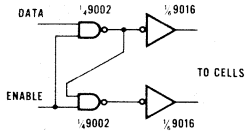
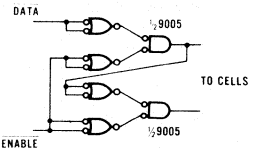


Fig. D
SINGLE RAIL ACTIVE
LOW INPUT AND ENABLE



TTμL MEMORY 93434

256-BIT READ-ONLY MEMORY

FAIRCHILD TTμL® IC PRODUCT FORMERLY 9034

GENERAL DESCRIPTION — The Fairchild 93434 is a 256-bit bipolar TTμL read-only memory. The memory is organized as 32 words of 8-bits each. The words are selected through 5 address lines. The 8 outputs of the words are uncommitted collectors which may be Wired-OR'd with the outputs of other ROMs. An Enable input is provided for additional decoding flexibility. A high on the Enable input forces all outputs to be high.

The contents of the memory are permanently programmed to customer order. A customer order form is available on request.

FEATURES:

- **TTμL COMPATIBLE**
- **OUTPUT WIRED-OR'D CAPABILITY**
- **SINGLE TTL LOAD INPUTS**
- **INPUT CLAMP DIODES**

ABSOLUTE MAXIMUM RATINGS

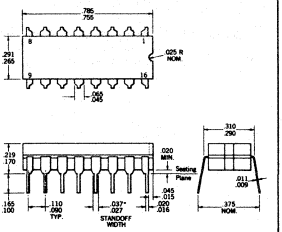
Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground	−0.5 V to +8.0 V
Input Pin Voltage	−1.5 V to 5.5 V
Current Into Output Terminal	100 mA
Output Voltages	−0.5 V to V_{CC} Value

ORDER INFORMATION

The 93435 is custom coded for each application. Please contact your local Fairchild sales office for ordering information. Specify A7B9343451X for −55°C to +125°C, and A7B9343459X for 0°C to +75°C temperature range.

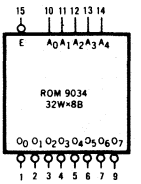
PHYSICAL DIMENSIONS

16 Lead Dual In-Line



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers.
They are purposely shipped with "positive" misalignment to facilitate insertion.
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.0 grams
*The .037/.027 dimension does not apply to the corner leads

LOGIC DIAGRAM



V_{CC} = Pin 16
Gnd = Pin 8

FAIRCHILD
SEMICONDUCTOR

ELECTRICAL CHARACTERISTICS ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$) (units are pulse tested)

SYMBOL	TEST	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	TEST CONDITIONS
I_{FA}	Address Input Load Current		−1.6		−1.6		−1.6	mA	$V_{CC} = 5.5\ V$ $V_A = 0.4\ V$
I_{FE}	Enable Input Load Current		−1.6		−1.6		−1.6	mA	$V_{CC} = 5.5\ V$ $V_E = 0.4\ V$
I_{RA}	Address Input Leakage Current		100		100		100	μA	$V_{CC} = 5.5\ V$ $V_A = 4.5\ V$
I_{RE}	Enable Input Leakage Current		100		100		100	μA	$V_{CC} = 5.5\ V$ $V_E = 4.5\ V$
I_{CEX}	Output Leakage Current		200		200		200	μA	$V_{CC} = 5.5\ V$ $V_{CEX} = 5.5\ V$ Enable input to 2.0 V
V_{OL}	Output Low Voltage		0.4		0.4		0.4	V	$V_{CC} = 4.5\ V$ $I_{OUT} = 10\ mA$ The word containing a "0" bit is selected when performing this test.
V_{IL}	Input Low Voltage		0.8		0.9		0.8	V	$V_{CC} = 5.5\ V$ Enable input grounded. Monitor appropriate output to guarantee this test.
V_{IH}	Input High Voltage	2.0		1.7		1.4		V	$V_{CC} = 4.5\ V$ Enable input grounded. Monitor appropriate output to guarantee this test.
I_{PD}	Power Supply Current		80		80		80	mA	$V_{CC} = 5.5\ V$ All inputs grounded

ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0\ V \pm 5\%$) (units are pulse tested)

SYMBOL	TEST	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	TEST CONDITIONS
I_{FA}	Address Input Load Current		−1.6		−1.6		−1.6	mA	$V_{CC} = 5.25\ V$ $V_A = 0.45\ V$
I_{FE}	Enable Input Load Current		−1.6		−1.6		−1.6	mA	$V_{CC} = 5.25\ V$ $V_E = 0.45\ V$
I_{RA}	Address Input Leakage Current		100		100		100	μA	$V_{CC} = 5.25\ V$ $V_A = 4.5\ V$
I_{RE}	Enable Input Leakage Current		100		100		100	μA	$V_{CC} = 5.25\ V$ $V_E = 4.5\ V$
I_{CEX}	Output Leakage Current		200		200		200	μA	$V_{CC} = 5.25\ V$ $V_{CEX} = 5.25\ V$ Enable input to 2.0 V
V_{OL}	Output Low Voltage		0.45		0.45		0.45	V	$V_{CC} = 4.75\ V$ $I_{OUT} = 10\ mA$ The word containing a "0" bit is selected when performing this test.
V_{IL}	Input Low Voltage		0.85		0.85		0.85	V	$V_{CC} = 5.25\ V$ Enable input grounded. Monitor appropriate output to guarantee this test.
V_{IH}	Input High Voltage	1.9		1.8		1.6		V	$V_{CC} = 4.75\ V$ Enable input grounded. Monitor appropriate output to guarantee this test.
I_{PD}	Power Supply Current		80		80		80	mA	$V_{CC} = 5.25\ V$ All inputs grounded

SWITCHING TIME CHARACTERISTICS ($T_A = 25°C$)

SYMBOL	TEST	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS
$t_{1,+}$	Enable and Address Delay		*	50	ns	10 mA load. See Note 1.
$t_{+,-}$	Enable and Address Delay		*	50	ns	10 mA load. See Note 1.
$t_{+,-}$	Address Delay		*	50	ns	10 mA load. See Note 2.
$t_{-,+}$	Address Delay		*	50	ns	10 mA load. See Note 2.

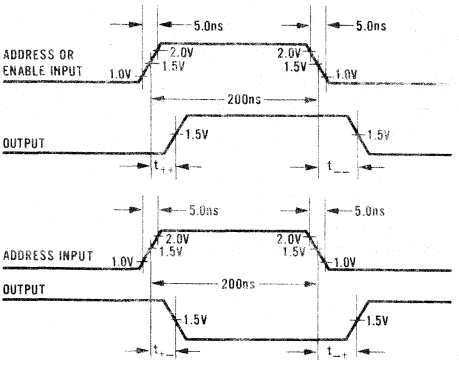
*See Typical Electrical Characteristics curves.

NOTES:

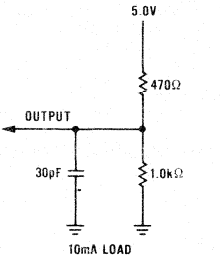
(1) To test Enable delay, apply input pulse to Enable input. The word selected must contain a "0" in the bit under test. To test Address delay, the Enable input must be low. Apply the input pulse to the Address input under test. The words selected must contain a "1" when input pulse is low and a "0" when input pulse is high in the bit under test.

(2) To test Address delay, the Enable input must be low. Apply the input pulse to the Address input under test. The words selected must contain a "0" when input pulse is low and a "1" when input pulse is high in the bit under test.

SWITCHING TIME TEST CONDITIONS AND WAVEFORMS



SWITCHING TEST OUTPUT LOAD



LOADING RULES

TTμL INPUT LOAD AND DRIVE FACTORS

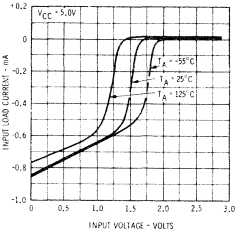
INPUTS	LOADING
Low Level	1.7 U.L.
High Level	1.0 U.L.

OUTPUTS	DRIVE FACTOR
All outputs	Open Collector 6.25 U.L.

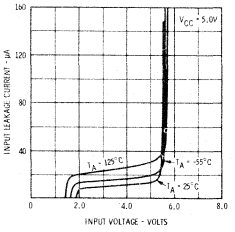
1 Low Level TTμL Unit Load (U.L.) = −1.6 mA
1 High Level TTμL Unit Load (U.L.) = 60 μA

TYPICAL ELECTRICAL CHARACTERISTICS

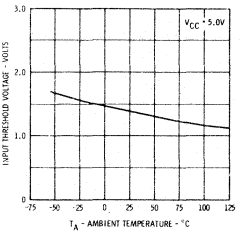
INPUT LOAD CURRENT VERSUS INPUT VOLTAGE



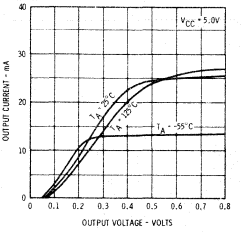
INPUT LEAKAGE CURRENT VERSUS INPUT VOLTAGE



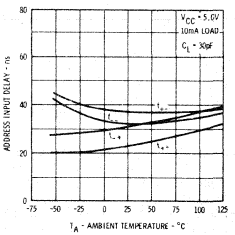
INPUT THRESHOLD VOLTAGE VERSUS AMBIENT TEMPERATURE



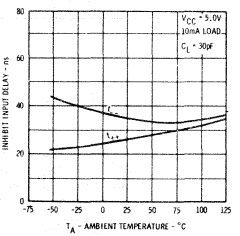
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE



ADDRESS INPUT DELAY VERSUS AMBIENT TEMPERATURE



ENABLE INPUT DELAY VERSUS AMBIENT TEMPERATURE



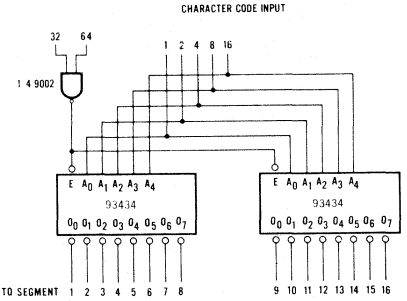
APPLICATIONS:

The Fairchild 93434 Read-Only Memory has many storage and display applications. Two main uses of the memory are for microprogrammed subroutines (core replacements) and character generator display systems.

APPLICATION OF THE 93434 READ-ONLY MEMORY IN DIFFERENT TYPES OF DISPLAY SYSTEMS.

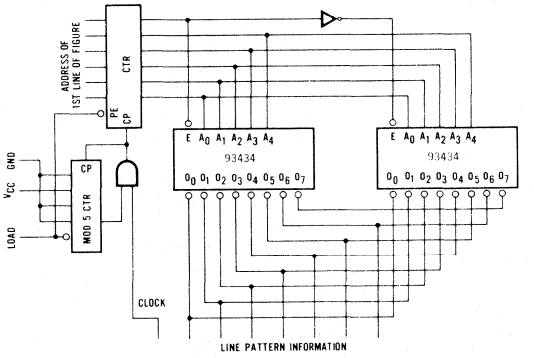
In the application of this ROM as display storage, the Enable input is the most important control, since every display system requires a number of ROM's organized in parallel to each other. The effectiveness of such a character storage system depends on the flexibility in addressing a desired character. Most of the character storage systems will be character code oriented.

16 SEGMENT DECODER



This figure illustrates the use of two 93434 ROMs for driving a 16 segment decoder. The character code is used directly as a control for both ROMs. One additional 2-input gate controlling the enable inputs of the two ROMs is required for selecting the group of codes within the ASCII system which refer to the characters. For uninterrupted control, two ROMs are required for each of the 16 segment display units.

DISPLAY GENERATOR 5 x 8 DOT MATRIX



The five 8-bit words representing the 5 x 8 dot pattern of a figure are stored in sequence. The external source which calls for a figure has to supply the address of the first 8-bit word of this figure. The clock will increment this address by one each time the generated pattern has been displayed until all five 8-bit patterns have been used. The mod. 5 counter calls for the first line address of the next figure automatically.

If these data are used to control a CRT display the outputs of the two 93434 ROMs may be connected to an 8-channel multiplexer (3705) which serves as an interface to the Z modulation input of the display unit. The eight channels are selected in sequence by a mod. 8 counter of which the eight output generates the control pulses for the mod. 5 and the address counter.

TTμL MEMORY 93435

64-BIT LINEAR SELECT READ/WRITE MEMORY

FAIRCHILD TTμL® IC PRODUCT FORMERLY 9035

GENERAL DESCRIPTION — The 93435 is a high speed 64-bit read/write memory cell designed for use in high speed scratch pad memories. It is a linear select 16 word by 4-bit array.

The 93435 is available in the hermetically sealed 36-pin ceramic dual in-line package and will operate over the temperature range from −55°C to +125°C.

OPERATION — In addition to 16 address inputs, 4 data outputs, and 4 data inputs, the 93435 has a chip select and a write enable. When the chip select is high, a word may be addressed by a high on one of the address inputs. Data is written into the addressed word location only when the write enable is held low. While the address is present, the outputs continuously show the contents of the word selected. Readout is non-destructive.

Up to four words may be addressed and read simultaneously with the OR function of each bit appearing at the outputs. Data can be written into two locations simultaneously.

Uncommitted collector outputs are provided on the 93435 to allow maximum flexibility in output connection. In many applications such as memory expansion, the outputs of many 93435's can be tied together. In other applications the wired-OR is not used. In either case an external pullup resistor of value R must be used to provide a high at the output when it is off. Any value of R within the range specified below may be used.

$$\frac{5.1}{10 - \text{F.O.}\ (1.6)} \leq R \leq \frac{2.1}{N(0.1) + \text{F.O.}\ (0.06)}$$

R is in kΩ
N = number of wired-OR outputs
F.O. = number of TTμL loads driven

The minimum value of R is limited by output current sinking ability. The maximum value of R is determined by the output and input leakage current (I_{CEX} and I_R) which must be supplied to hold the output at 2.4 V.

FEATURES:

- **35 ns MAXIMUM ACCESS TIME—20 ns TYPICAL**
- **CHIP SELECT AND WRITE ENABLES**
- **UNCOMMITTED COLLECTOR OUTPUTS FOR WIRE OR CAPABILITY**
- **LINEAR SELECT**
- **ON CHIP ADDRESS LINE BUFFERING**
- **TTμL COMPATIBLE**

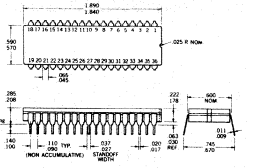
ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground	−0.5 V to +7.0 V
Input Pin Voltage	−0.5 V to +5.5 V
Current into Output Terminal	50 mA
Output Voltage	−0.5 V to +8.0 V

ORDER INFORMATION — Specify A6P93435XXX where XXX is 51X for the −55°C to +125°C temperature range or 59X for the 0°C to 75°C temperature range.

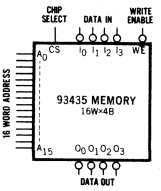
PHYSICAL DIMENSIONS

36 Lead Dual In-Line

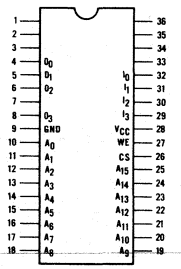


NOTES:
All dimensions in inches.
Leads are intended for insertion in hole rows on .600" centers. They are purposely shipped with "positive" misalignment to facilitate insertion.
Leads are tin-plated kovar.
Package weight is 14.3 grams.

LOGIC DIAGRAM



PIN CONFIGURATION



FAIRCHILD SEMICONDUCTOR

LOADING RULES

	HIGH LEVEL (TTμL Unit Loads)	LOW LEVEL (TTμL Unit Loads)
Address	1.67	1
Chip Select	26.7	1 (see note 1)
Write Enable	1.67	1
Data Input	3.34	2
Data Output	Open Collector	6.2

1 Low Level TTμL Unit Load = −1.6 mA
1 High Level TTμL Unit Load = 60 μA

ELECTRICAL CHARACTERISTICS (T_A = −55°C to 125°C, V_{CC} = 5.0 V ±10%) (units are pulse tested)

SYMBOL	TEST	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS
I_{FA}	Address Input Load Current		−1.6		−1.6		−1.6	mA	V_{CC} = 5.5 V, V_A = 0.4 V
I_{FCS}	Chip Select Load Current		−1.6		−1.6		−1.6	mA	V_{CC} = 5.5 V, V_{CS} = 0.4 V See Note 1
I_{FWE}	Write Enable Load Current		−1.6		−1.6		−1.6	mA	V_{CC} = 5.5 V, V_W = 0.4 V
I_{FD}	Data Input Load Current		−3.2		−3.2		−3.2	mA	V_{CC} = 5.5 V, V_D = 0.4 V
I_{RA}	Address Input Leakage Current		100		100		100	μA	V_{CC} = 5.5 V, V_A = 4.5 V
I_{RCS}	Chip Select Input Leakage Current		1.6		1.6		1.6	mA	V_{CC} = 5.5 V, V_{CS} = 4.5 V
I_{RWE}	Write Enable Leakage Current		100		100		100	μA	V_{CC} = 5.5 V, V_W = 4.5 V
I_{RD}	Data Input Leakage Current		200		200		200	μA	V_{CC} = 5.5 V, V_D = 4.5 V
I_{CEX}	Output Leakage Current		100		100		100	μA	V_{CC} = 5.5 V, V_{CEX} = 5.5 V Write Enable Input Grounded
V_{OL}	Output "Low" Voltage		0.4		0.4		0.4	V	V_{CC} = 4.5 V, I_{OL} = 10 mA One Word Addressed
V_{IL}	Input "Low" Voltage		0.8		0.9		0.8	V	V_{CC} = 5.0 V, Monitor Appropriate Output To Guarantee This Test Limit
V_{IH}	Input "High" Voltage	2.1		2.0		2.0		V	V_{CC} = 5.0 V, Monitor Appropriate Output To Guarantee This Test Limit
I_{PD}	Supply Current		118		118		118	mA	V_{CC} = 5.5 V, One Word Addressed

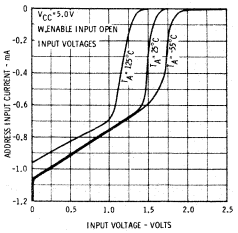
ELECTRICAL CHARACTERISTICS (T_A = 0°C to 75°C, V_{CC} = 5.0 V ±5%) (units are pulse tested)

SYMBOL	TEST	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	CONDITIONS
I_{FA}	Address Input Load Current		−1.6		−1.6		−1.6	mA	V_{CC} = 5.25 V, V_A = 0.45 V
I_{FCS}	Chip Select Load Current		−1.6		−1.6		−1.6	mA	V_{CC} = 5.25 V, V_{CS} = 0.45 V See Note 1
I_{FWE}	Write Enable Load Current		−1.6		−1.6		−1.6	mA	V_{CC} = 5.25 V, V_W = 0.45 V
I_{FD}	Data Input Load Current		−3.2		−3.2		−3.2	mA	V_{CC} = 5.25 V, V_D = 0.45 V
I_{RA}	Address Input Leakage Current		100		100		100	μA	V_{CC} = 5.25 V, V_A = 4.5 V
I_{RCS}	Chip Select Input Leakage Current		1.6		1.6		1.6	mA	V_{CC} = 5.25 V, V_{CS} = 4.5 V
I_{RWE}	Write Enable Leakage Current		100		100		100	μA	V_{CC} = 5.25 V, V_W = 4.5 V
I_{RD}	Data Input Leakage Current		200		200		200	μA	V_{CC} = 5.25 V, V_D = 4.5 V
I_{CEX}	Output Leakage Current		100		100		100	μA	V_{CC} = 5.25 V, V_{CEX} = 5.25 V Write Enable Input Grounded
V_{OL}	Output "Low" Voltage		0.45		0.45		0.45	V	V_{CC} = 4.75 V, I_{OL} = 10 mA One Word Addressed
V_{IL}	Input "Low" Voltage		0.85		0.85		0.85	V	V_{CC} = 5.0 V, Monitor Appropriate Output To Guarantee This Test Limit
V_{IH}	Input "High" Voltage	2.0		2.0		2.0		V	V_{CC} = 5.0 V, Monitor Appropriate Output To Guarantee This Test Limit
I_{PD}	Supply Current		124		124		124	mA	V_{CC} = 5.25 V, One Word Addressed

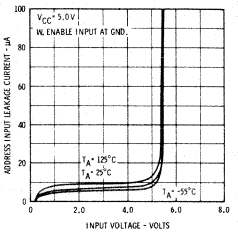
NOTE 1: I_{FCS} increases by 1.6 mA for each address input held at a logical 1.

TYPICAL ELECTRICAL CHARACTERISTICS

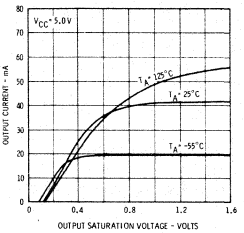
ADDRESS INPUT LOAD CURRENT VERSUS INPUT VOLTAGE



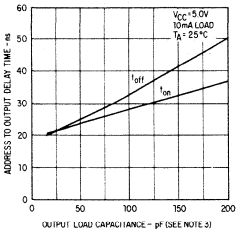
ADDRESS INPUT LEAKAGE CURRENT VERSUS INPUT VOLTAGE



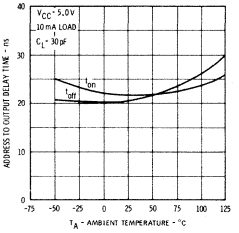
OUTPUT CURRENT VERSUS OUTPUT SATURATION VOLTAGE



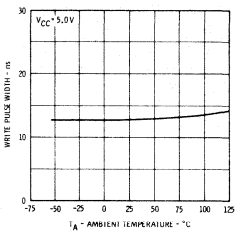
ADDRESS TO OUTPUT DELAY TIME VERSUS OUTPUT LOAD CAPACITANCE



ADDRESS TO OUTPUT DELAY TIME VERSUS TEMPERATURE



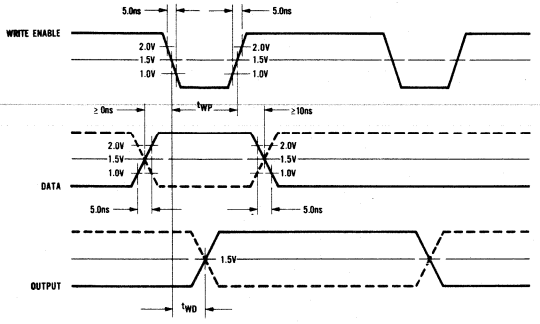
WRITE PULSE WIDTH VERSUS TEMPERATURE

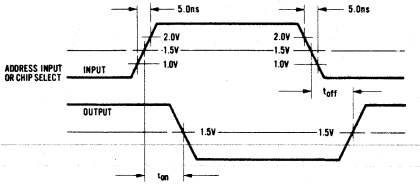


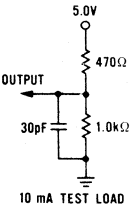
SWITCHING CHARACTERISTICS ($T_A = 25°C$, $V_{CC} = 5.0$ V)

SYMBOL	TEST	LIMIT (ns)			CONDITION		
		MIN.	TYP.	MAX.	LOAD	C	NOTE
t_{on}	Address to Output Turn-On Delay	10	22	35	10 mA	30 pF	1
t_{off}	Address to Output Turn-Off Delay	10	20	35	10 mA	30 pF	1
t_{WP}	Write Pulse Width Required to Write	25	15		10 mA	30 pF	2
t_{WD}	Write Delay	10	30	50	10 mA	30 pF	2

NOTE 1: To test t_{on} and t_{off}, a "Low" must be stored in the cell under test.
NOTE 2: One word is selected during the test.
NOTE 3: The typical capacitance of one 9035 output is 7.0 pF



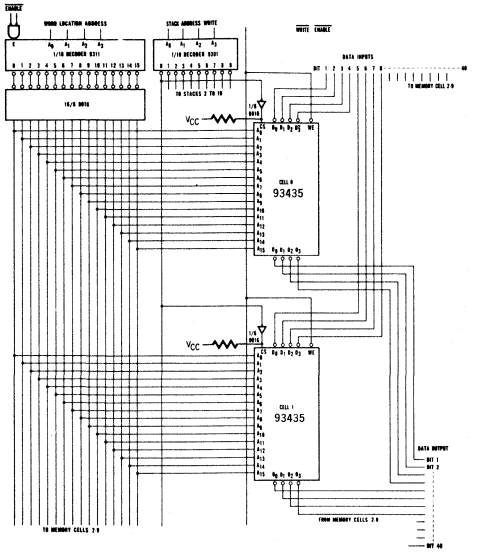




10 mA TEST LOAD

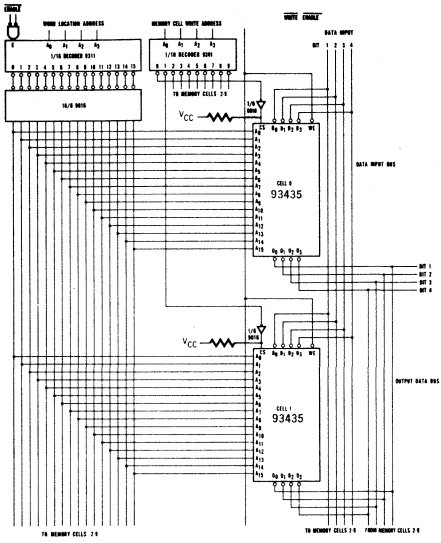
P

APPLICATIONS



MEMORY STACK 160 WORDS OF 40-BITS

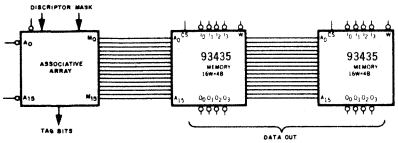
There are 16 words by 40 bits for each stack. The outputs of all stacks are tied together. Stack 1 contains words 0-15, stack 2, 16-31, and so on through 143-159 for the 10th stack. The stack address decoder tells which word group (0-15 or 16-31, etc.) is addressed while the word location decoder addresses one of the 16 words of the stack addressed. The entire memory has 40 data input lines, 40 data output lines, 8 address lines, and a write enable line.



MEMORY EXPANSION: 160 WORDS BY 4-BITS

In this application the 93435 memory cells are connected in parallel and two levels of decoding are performed. One of the cells is selected by the 9301 decoder and then a word is addressed by the 9311.

Memory system formed by interconnection of associative and ordinary read/write memories.



Memory system formed by interconnection of associative and ordinary read/write memories.

BUFFER MEMORY APPLICATIONS

The 93402, in association with the 93435 Read/Write Memory, can be of great value in speeding up memory access in a computer. The basic scheme is illustrated below. Match signals from the associative memory are used to address locations in the 93435 memory. The associative section will ordinarily contain some kind of descriptive information about corresponding data in the 93435's. Data is written into both types of memory simultaneously. (Writing into a word in the 93402 always causes the match line for that word to go HIGH.)

One application of such a scheme is a kind of indirect addressing. The associative memory contains a virtual address for data. Whenever that address is called, a match signal is generated, causing the 93435 to produce the true address for the data. This system makes it a simple matter to assign and alter memory location addresses, with a minimal time required to locate information.

Another way to use this kind of arrangement is to store data addresses (or "page" addresses) in associative memory and data in semiconductor read/write memory.

For further details see Fairchild Application Note #187. "Using the 93402 Associative Memory."

TTμL/INTERFACE 9600
RETRIGGERABLE RESETTABLE MONOSTABLE MULTIVIBRATOR
A FAIRCHILD TTμL® IC PRODUCT

GENERAL DESCRIPTION — The TTμL 9600 is a DC level sensitive retriggerable resettable monostable multivibrator which provides an output pulse whose duration and accuracy is a function of external timing components only. The 9600 has excellent immunity to noise on the V_{CC} and ground lines. The 9600 uses TTμL for high speed and high fanout capability and is compatible with all devices in the TTμL family of integrated circuits.

FEATURES:

- **50 ns TO ∞ OUTPUT PULSE WIDTH RANGE**
- **RETRIGGERABLE 0 TO 100% DUTY CYCLE**
- **RESETTABLE**
- **COMPLEMENTARY D.C. LEVEL SENSITIVE INPUTS**
- **COMPLEMENTARY OUTPUTS**
- **TTμL COMPATIBLE**
- **OPTIONAL RETRIGGER LOCK-OUT CAPABILITY**
- **IMPROVED PULSE WIDTH TEMPERATURE STABILITY**

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) .Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground (See Note 1)	−0.5 V to +8.0 V
Input Voltage (D.C.) (See Note 2)	−0.5 V to +5.5 V
Input Current (See Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output When Output is High	−0.5 V to +V_{CC} value
Current Into Output When Output is Low	50 mA

ORDER INFORMATION:

Specify U3I96005XX for flat package and U6A96005XX for Dual In-Line package, where 5XX is 51X for −55°C to +125°C temperature range or 59X for the 0°C to +75°C temperature range.

NOTES:

(1) The maximum V_{CC} value of 8.0 volts is not the primary factor in determining the maximum V_{CC} which may be applied to a number of interconnected devices. The voltage at a high output is approximately 1 V_{BE} below the V_{CC} voltage, so the primary limit on the V_{CC} is that the voltage at any input may not go above 5.5 V unless the current is limited, so this effectively limits the system V_{CC} to approximately 7.0 volts.

(2) Because of the input clamp diodes, excess current can be drawn out of the inputs if the D.C. input voltage is more negative than −0.5 V. The diode is designed to clamp off large negative A.C. swings associated with fast fall times and long lines. This maximum rating is intended only to limit the steady state input voltage and current.

LOGIC DIAGRAM

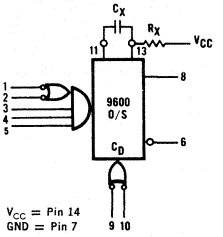
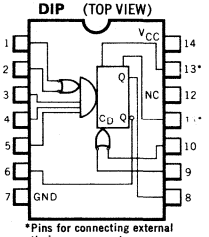


Fig. 1

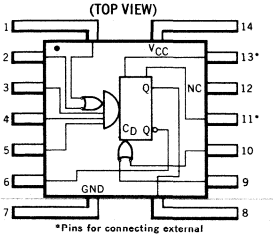
CONNECTION DIAGRAM
DIP (TOP VIEW)



*Pins for connecting external timing components

Fig. 2

FLAT PAK
(TOP VIEW)



*Pins for connecting external timing components

Fig. 3

FAIRCHILD
SEMICONDUCTOR

FUNCTIONAL DESCRIPTION

The 9600 monostable multivibrator has five inputs, three of which are active level high and two active level low. This allows a choice of leading edge or trailing edge triggering. The inputs are D.C. coupled making triggering independent of input transition times.

Each time the input conditions for triggering are met, the external capacitor is discharged in a short time and a new cycle is begun. Successive inputs with a period shorter than the delay time retrigger the 9600 and result in a continuous true output. Retriggering may be inhibited by tying the negation ($\bar{Q}$) output back to an active level high input.

The output pulse may be terminated at any time by taking either or both reset pins to a low logic level.

Active pullups are provided for good drive capability into capacitive loads.

OPERATION RULES

1. An external resistor R_X and an external capacitor C_X are required as shown in the logic diagram. The values of R_X may vary from 5.0 kΩ to 50 kΩ for 0 to +75°C operation, and 5.0 kΩ to 25 kΩ for −55 to +125°C operation. C_X may vary from 0 to any value necessary and obtainable.
2. If a fixed value of R_X is used, the following values are recommended: $R_X = 30$ kΩ for 0 to +75°C operation; $R_X = 10$ kΩ for −55 to +125°C operation.
3. The output pulse width T is defined as follows:

   $T = 0.32\ R_X C_X\ [1 + \frac{0.7}{R_X}]$ (For C_X greater than 10^3 pF)

   Where R_X is in kΩ
   C_X is in pF
   T is in ns

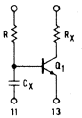
   For $C_X < 10^3$ pF, see Fig. 14

4. If long pulse widths are desired either electrolytic capacitors or the following arrangement can be used (Retrigger may not be used with these circuit arrangements). If electrolytic capacitors are to be used, a minimum voltage rating of 20 volts is recommended. This is to insure that the slight reverse voltage applied during retriggering will not damage the capacitor.

   This circuit allows a large value of timing resistor.

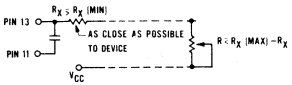
   The pulse width T for the circuit is defined as follows:

   $T \approx 0.30\ RC_X\ [1 + \frac{0.7}{R}]$ Where: R is in kΩ
   C_X is in pF
   T is in ns



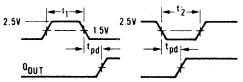
This circuit also amplifies C_X allowing for longer output pulse width.
$R < R_X\ (0.7)\ (h_{fe}Q_1)$
R_X (min) $< R_X < R_X$ (max)
Q_1: Any NPN silicon device with sufficient h_{FE} at low currents, such as 2N2511.

5. To obtain variable pulse width, by remote trimming, the following circuit is recommended:

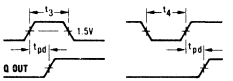


6. Under any operating condition, C_X and R_X (min) must be kept as close to the circuit as possible to minimize stray capacitance and reduce noise pickup.
7. Input Trigger Pulse Rules.

Input to Pin 1 (2)
Pins 2, (1), 3, 4, & 5 = High

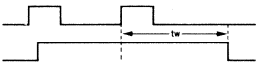


Input to Pin 3, 4 or 5
Other Inputs = High
Pins 1 or 2 = Low



t_1, t_3 = Min. positive input pulse width > 40 ns
t_2, t_4 = Min. negative input pulse width > 40 ns

8. The retrigger pulse width is calculated as shown below:



$t_w = t_{pw} + t_{pd+} = 0.32\ R_X C_X\ (1 + \frac{0.7}{R_X}) + t_{pd+}$

The retrigger pulse width is equal to the pulse width t_{pw} plus a delay time. For pulse widths greater than 500 ns, t_w can be approximated as t_{pw}.

NOTE: Retriggering will not occur if the retrigger pulse comes within $.32\ R_X C_X\ (\frac{.7}{R_X})$ ns after the initial trigger pulse.

9. Reset Operation—Two overriding active low level resets are provided. By applying a low to either or both resets, any timing cycle can be terminated and/or any new cycle inhibited until both reset inputs are restored to a high level. Trigger inputs will not produce spikes in the output when either or both resets are held low.

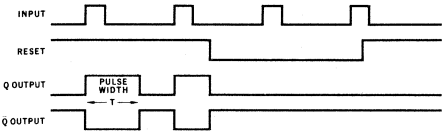


TABLE I — ELECTRICAL CHARACTERISTICS ($T_A = -55°C$ to $125°C$, $V_{CC} = 5\ V \pm 10\%$) (Part No. U3I/6A960051X)

SYMBOL	CHARACTERISTIC	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS (Note 1)
V_{OH}	Output High Voltage	2.4		2.4	3.3		2.4		Volts	$V_{CC} = 4.5\ V$, $I_{OH} = -0.96\ mA$ (Note 2)
V_{OL}	Output Low Voltage		0.4		0.2	0.4		0.4	Volts	$V_{CC} = 4.5\ V$, $I_{OL} = 9.92\ mA$ (Note 2) $V_{CC} = 5.5\ V$, $I_{OL} = 12.8\ mA$
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high
V_{IL}	Input Low Voltage		0.85			0.90		0.85	Volts	Guaranteed input low
I_F	Input Load Current		−1.6		−1.1	−1.6		−1.6	mA	$V_{CC} = 5.5\ V$, $V_F = 0.4\ V$
			−1.24		−0.97	−1.24		−1.24	mA	$V_{CC} = 4.5\ V$, $V_F = 0.4\ V$
I_R	Input Leakage Current				15	60		60	μA	$V_{CC} = 5.5\ V$, $V_R = 4.5\ V$
I_{SC}	Short Circuit Current					25			mA	$V_{CC} = 5.5\ V$, $V_{OUT} = 0\ V$ (Note 2)
I_{pd}	Quiescent Power Supply Drain		24		19	24		24	mA	$V_{CC} = 5.0\ V$
t_{pd+}	Negative Trigger Input to True Output				29	45			ns	$V_{CC} = 5.0\ V$ $R_X = 5.0\ k\Omega$ $C_X = 0$, $C_L = 15\ pF$
t_{pd-}	Negative Trigger Input to Complement Output				29	40			ns	$V_{CC} = 5.0\ V$ $R_X = 5.0\ k\Omega$ $C_X = 0$, $C_L = 15\ pF$
$t_{pw(min)}$	Minimum True Output Pulse Width				74	100			ns	$V_{CC} = 5.0\ V$ $R_X = 5.0\ k\Omega$ $C_X = 0$, $C_L = 15\ pF$
	Minimum Complement Output Pulse Width					112			ns	
t_{pw}	Pulse Width			3.20	3.42	3.76			μs	$V_{CC} = 5.0\ V$, $R_X = 10\ k\Omega$, $C_X = 1000\ pF$
C_{STRAY}	Maximum Allowable Wiring Cap. (Pin 13)		50			50		50	pF	Pin 13 to Ground
R_X	Timing Resistor	5.0	25	5.0		25	5.0	25	kΩ	

TABLE II — ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $75°C$, $V_{CC} = 5\ V \pm 5\%$) (Part No. U3I/6A960059X)

SYMBOL	CHARACTERISTIC	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	CONDITIONS (Note 1)
V_{OH}	Output High Voltage	2.4		2.4	3.4		2.4		Volts	$V_{CC} = 4.75\ V$, $I_{OH} = -0.96\ mA$ (Note 2)
V_{OL}	Output Low Voltage		0.45		0.2	0.45		0.45	Volts	$V_{CC} = 4.75\ V$, $I_{OL} = 11.3\ mA$ (Note 2) $V_{CC} = 5.25\ V$, $I_{OL} = 12.8\ mA$
V_{IH}	Input High Voltage	1.9		1.8			1.65		Volts	Guaranteed input high
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low
I_F	Input Load Current		−1.6		−1.0	−1.6		−1.6	mA	$V_{CC} = 5.25\ V$, $V_F = 0.45\ V$
			−1.41			−1.41		−1.41	mA	$V_{CC} = 4.75\ V$, $V_F = 0.45\ V$
I_R	Input Leakage Current				15	60		60	μA	$V_{CC} = 5.25\ V$, $V_R = 4.5\ V$
I_{SC}	Short Circuit Current					35			mA	$V_{CC} = 5.25\ V$, $V_{OUT} = 0\ V$ (Note 2)
I_{pd}	Quiescent Power Supply Drain		26		19	26		26	mA	$V_{CC} = 5.0\ V$ Ground Pins 1 and 2
t_{pd+}	Negative Trigger Input to True Output				29	56			ns	$V_{CC} = 5.0\ V$ $R_X = 5.0\ k\Omega$ $C_X = 0$, $C_L = 15\ pF$
t_{pd-}	Negative Trigger Input to Complement Output				29	47			ns	$V_{CC} = 5.0\ V$ $R_X = 5.0\ k\Omega$ $C_X = 0$, $C_L = 15\ pF$
$t_{pw(min)}$	Minimum True Output Pulse Width				74	120			ns	$V_{CC} = 5.0\ V$ $R_X = 5.0\ k\Omega$ $C_X = 0$, $C_L = 15\ pF$
	Minimum Complement Output Pulse Width					130			ns	
t_{pw}	Pulse Width			3.08	3.42	3.76			μs	$V_{CC} = 5.0\ V$, $R_X = 10\ k\Omega$, $C_X = 1000\ pF$
C_{STRAY}	Maximum Allowable Wiring Cap. (Pin 13)		50			50		50	pF	Pin 13 to Ground
R_X	Timing Resistor	5.0	50	5.0		50	5.0	50	kΩ	

NOTES:

(1) Unless otherwise noted, 10 kΩ resistor placed between Pin 13 and V_{CC}, for all tests. (R_X)

(2) Ground Pin 11 for V_{OL} Pin 6 or V_{OH} Pin 8 or I_{SC} Pin 8.
Open Pin 11 for V_{OL} Pin 8 or V_{OH} Pin 6 or I_{SC} Pin 6.

TYPICAL ELECTRICAL CHARACTERISTICS

Fig. 4
INPUT LOAD CURRENT VERSUS INPUT VOLTAGE

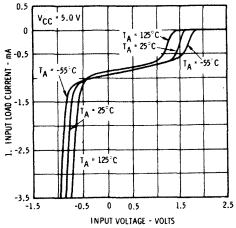


Fig. 5
INPUT LEAKAGE CURRENT VERSUS INPUT VOLTAGE

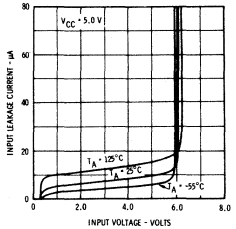


Fig. 6
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (LOW STATE)

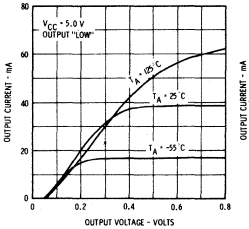


Fig. 7
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (HIGH STATE)

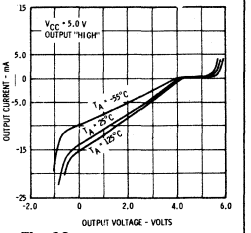


Fig. 8
MINIMUM PULSE WIDTH TO TRIGGER VERSUS AMBIENT TEMPERATURE (POSITIVE EDGE TRIGGER INPUT)

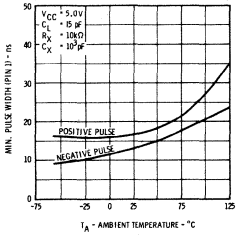


Fig. 9
MINIMUM PULSE WIDTH TO TRIGGER VERSUS AMBIENT TEMPERATURE (NEGATIVE EDGE TRIGGER INPUT)

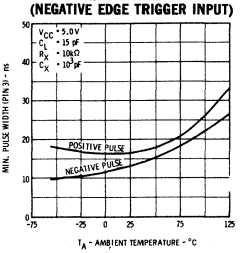


Fig. 10
MINIMUM TIME DELAY, RESET TO OUTPUT VERSUS AMBIENT TEMPERATURE

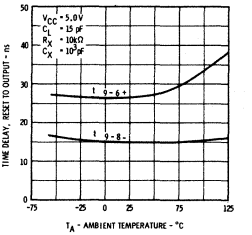


Fig. 11
NORMALIZED OUTPUT PULSE WIDTH VERSUS AMBIENT TEMPERATURE

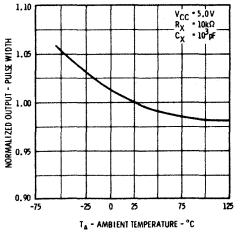


Fig. 12
PULSE WIDTH VERSUS TIMING RESISTOR

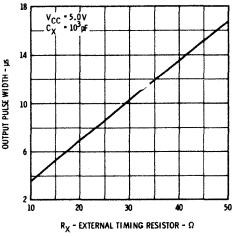


Fig. 13
POWER DISSIPATION VERSUS AMBIENT TEMPERATURE

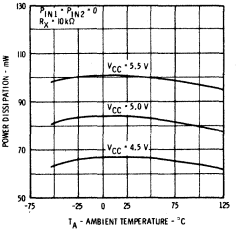


Fig. 14
NORMALIZED OUTPUT PULSE WIDTH VERSUS SUPPLY VOLTAGE

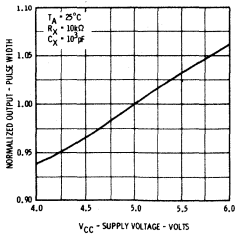


Fig. 15
MINIMUM OUTPUT PULSE WIDTH VERSUS AMBIENT TEMPERATURE

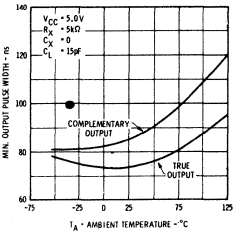
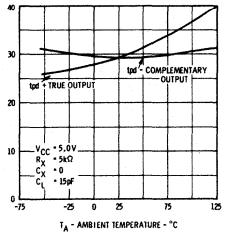


Fig. 16
NEGATIVE TRIGGER DELAY TIME VERSUS AMBIENT TEMPERATURE



OUTPUT PULSE WIDTH VERSUS TIMING RESISTANCE AND CAPACITANCE

For $C_X < 10^3$ pF [For $C_X \geq 10^3$ pF, $t_{pw} = 0.32 R_X C_X (1+0.7)$]

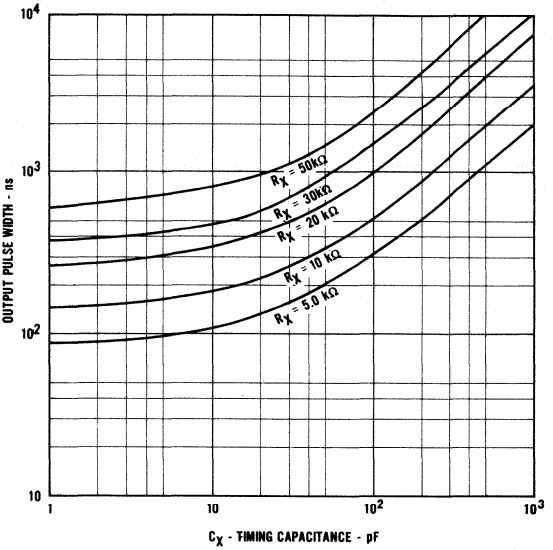
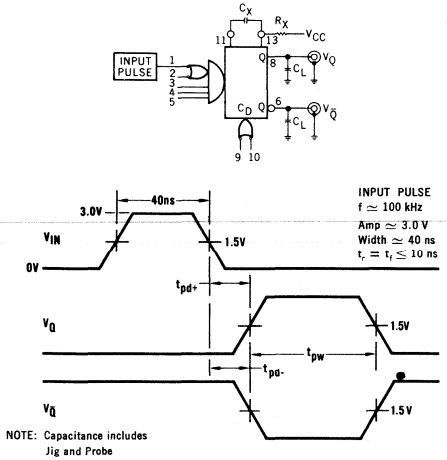


Fig. 17

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



NOTE: Capacitance includes Jig and Probe

Fig. 18

LOADING RULES

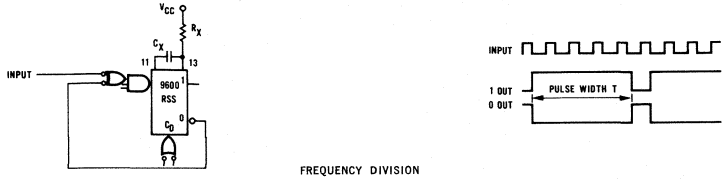
TTμL INPUT LOAD AND DRIVE FACTORS

INPUTS	LOAD	
	HIGH	LOW
1,2,3,4,5,9,10	1 U.L.	1 U.L.

OUTPUTS	DRIVE FACTOR	
	HIGH	LOW
6, 8	16 U.L.	8 U.L.

Note: 1 Unit Load (U.L.) = 60 μA High/1.6 mA Low

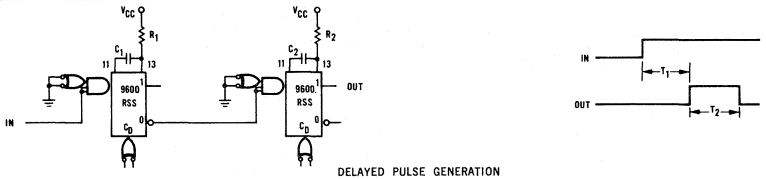
APPLICATIONS



FREQUENCY DIVISION

This configuration makes the 9600 non-retriggerable and capable of frequency division.

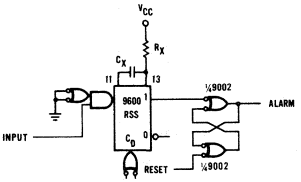
Fig. 19



DELAYED PULSE GENERATION

The first 9600 determines the time T_1 before the initiation of the output pulse.
The second 9600 determines T_2, the output pulse width.

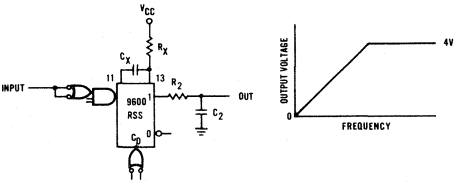
Fig. 20



MALFUNCTION INDICATOR

The output of the retriggerable single shot will only remain high if the input frequency is above some fixed value. The input may be a flip flop which normally has a fixed frequency of operation. A system malfunction is indicated when the flip flop frequency drops and retriggering operation of single shot ceases.

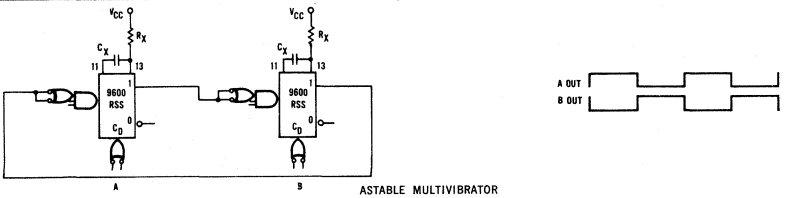
Fig. 21



DISCRIMINATOR

The 9600 can be used to produce a voltage output proportional to input frequency. For a fixed TC of Rx and Cx, the duty cycle of the output will vary with frequency. This is integrated by R_2 C_2 producing a voltage proportional to frequency.

Fig. 22



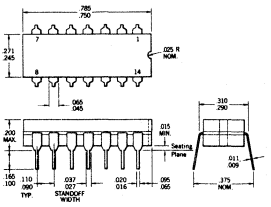
ASTABLE MULTIVIBRATOR

Frequency of operation is dependent upon value of Rx and Cx.

Fig. 23

PACKAGE INFORMATION

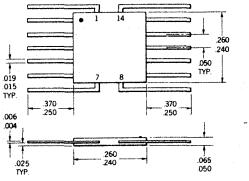
In Accordance With JEDEC (TO-116) Outline 6A — 14 Lead Dual In-Line



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers.
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.0 grams

Fig. 24

In Accordance With JEDEC (TO-86) Outline 31 — 14 Lead Cerpak



NOTES:
All dimensions in inches
Leads are gold-plated kovar
Package weight is 0.26 gram

Fig. 25

9601

RETRIGGERABLE MONOSTABLE MULTIVIBRATOR

Transistor-Transistor Micrologic® Integrated Circuits

A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

GENERAL DESCRIPTION — The TTμL 9601 is a DC level sensitive retriggerable monostable multivibrator which provides an output pulse whose duration and accuracy is a function of external timing components only. The 9601 has excellent immunity to noise on the V_{CC} and ground lines. The 9601 uses TTμL for high speed and high fanout capability and is compatible with all devices in the CCSL family of integrated circuits.

FEATURES:

- **50 ns TO ∞ OUTPUT PULSE WIDTH RANGE**
- **RETRIGGERABLE 0 TO 100% DUTY CYCLE**
- **COMPLEMENTARY D.C. LEVEL SENSITIVE INPUTS**
- **COMPLEMENTARY OUTPUTS**
- **CCSL COMPATIBLE**
- **OPTIONAL RETRIGGER LOCK-OUT CAPABILITY**
- **PULSE WIDTH COMPENSATED FOR V_{CC} AND TEMPERATURE VARIATIONS**

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground (See Note 1)	−0.5 V to +8.0 V
Input Voltage (D.C.) (See Note 2)	−0.5 V to +5.5 V
Input Current (See Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output When Output is High	0 V to +V_{CC} value
Current Into Output When Output is Low	50 mA

ORDER INFORMATION:

Specify U3I96015XX for flat package and U6A96015XX for Dual-In-Line package, where 5XX is 51X for −55°C to +125°C temperature range or 59X for the 0°C to +75°C temperature range.

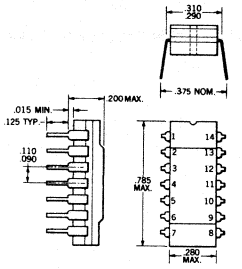
NOTES:

(1) The maximum V_{CC} value of 8.0 volts is not the primary factor in determining the maximum V_{CC} which may be applied to a number of interconnected devices. The voltage at a high output is approximately 1 V_{BE} below the V_{CC} voltage, so the primary limit on the V_{CC} is that the voltage at any input may not go above 5.5 V unless the current is limited, so this effectively limits the system V_{CC} to approximately 7.0 volts.

(2) Because of the input clamp diodes, excess current can be drawn out of the inputs if the D.C. input voltage is more negative than −0.5 V. The diode is designed to clamp off large negative A.C. swings associated with fast fall times and long lines. This maximum rating is intended only to limit the steady state input voltage and current.

PHYSICAL DIMENSIONS

Similar to JEDEC (TO-116) Outline



TYPICAL FLAT PACKAGE

(Top View)

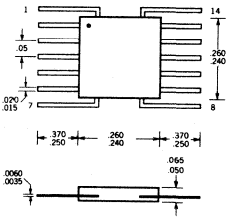
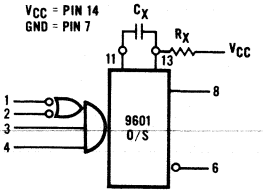


Fig. 1

LOGIC DIAGRAM



NOTE: All dimensions in inches

Fig. 2

FAIRCHILD

SEMICONDUCTOR

FAIRCHILD RETRIGGERABLE MONOSTABLE MULTIVIBRATOR 9601

FUNCTIONAL DESCRIPTION

The 9601 monostable multivibrator has four inputs, two of which are active level high and two active level low. This allows a choice of leading edge or trailing edge triggering. The inputs are D.C. coupled making triggering independent of input transition times.

Each time the input conditions for triggering are met, the external capacitor is discharged in a short time and a new cycle is begun. Successive inputs with a period shorter than the delay time retrigger the 9601 and result in a continuous true output. Retriggering may be inhibited by tying the negation ($\bar{Q}$) output back to an active level high input.

Active pullups are provided for good drive capability into capacitive loads.

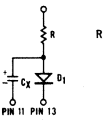
OPERATION RULES

1. An external resistor R_X and an external capacitor C_X are required as shown in the logic diagram. The values of R_X may vary from 5.0 kΩ to 50 kΩ for 0 to +75°C operation, and 5.0 kΩ to 25 kΩ for −55 to +125°C operation. C_X may vary from 0 to any value necessary and obtainable.
2. If a fixed value of R_X is used, the following values are recommended: $R_X = 30$ kΩ for 0 to +75°C operation; $R_X = 10$ kΩ for −55 to +125°C operation.
3. The output pulse width T is defined as follows:

   $T = 0.32\ R_X C_X\ [1 + \frac{0.7}{R_X}]$ (For C_X greater than 10^3 pF)

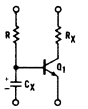
   Where R_X is in kΩ
   C_X is in pF
   T is in ns

   For $C_X < 10^3$ pF, see Fig. 14
4. If electrolytic type capacitors are to be used, the following two arrangements are recommended:



$R < 0.6\ R_X$ (Max)

D_1: any silicon type diode, such as FD700



This circuit also amplifies Cx allowing for longer output pulse width.

$R < R_X\ (0.7)\ (h_{fe}Q_1)$

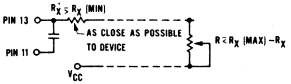
R_X (min) $< R_X < R_X$ (max)

Q_1: Any NPN silicon device with sufficient h_{FE} at low currents, such as 2N2511

Both circuits prevent reverse voltage across C_X. The pulse width T for the circuits is defined as follows:

$T \approx 0.36\ RC_X\ [1 + \frac{0.7}{R}]$ Where: R is in kΩ
C_X is in pF
T is in ns

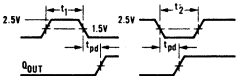
5. To obtain variable pulse width, by remote trimming, the following circuit is recommended:



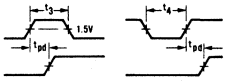
6. Under any operating condition, C_X and R_X (min) must be kept as close to the circuit as possible to minimize stray capacitance and reduce noise pickup.
7. Input Trigger Pulse Rules.

Input to Pin 1 (2)
Pins 2, (1), 3 & 4 = 1

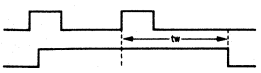
t_1, t_4 = Setup time > 40 ns
t_2, t_3 = Release time > 40 ns



Input to Pin 3 (4)
Pin 4 (3) = 1. Pins 1 or 2 = 0



8. The retrigger pulse width is calculated as shown below:



$tw = tpw + tpd+ = 0.32\ RxCx\ (1 + \frac{0.7}{Rx}) + tpd+$

The retrigger pulse width is equal to the pulse width tpw plus a delay time. For pulse widths greater than 500 ns, tw can be approximated as tpw.

NOTE: Retriggering will not occur if the retrigger pulse comes within $.32\ RxCx\ (\frac{.7}{Rx})$ ns after the initial trigger pulse.

FAIRCHILD RETRIGGERABLE MONOSTABLE MULTIVIBRATOR 9601

TABLE I —
ELECTRICAL CHARACTERISTICS ($T_A = -55°C$ to $125°C$, $V_{CC} = 5\ V \pm 10\%$)

SYMBOL	CHARACTERISTIC	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS (Note 1)
V_{OH}	Output High Voltage	2.4		2.4	3.3		2.4		Volts	$V_{CC} = 4.5\ V$, $I_{OH} = -0.72\ mA$ (Note 2)
V_{OL}	Output Low Voltage		0.4		0.2	0.4		0.4	Volts	$V_{CC} = 4.5\ V$, $I_{OL} = 10\ mA$ (Note 2)
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	$V_{CC} = 4.5\ V$ (Note 3)
V_{IL}	Input Low Voltage		0.85			0.90		0.85	Volts	$V_{CC} = 5.5\ V$
I_F	Input Load Current		−1.6		−1.1	−1.6		−1.6	mA	$V_{CC} = 5.5\ V$, $V_F = 0.4\ V$
I_R	Input Leakage Current				15	60		60	μA	$V_{CC} = 5.5\ V$, $V_R = 4.5\ V$
I_{SC}	Short Circuit Current			−10		−40			mA	$V_{CC} = 5.0\ V$, $V_{OUT} = 0\ V$ (Note 2)
I_{pd}	Quiescent Power Supply Drain		25			25		25	mA	$V_{CC} = 5.5\ V$
t_{pd+}	Negative Trigger Input to True Output				25	40			ns	$V_{CC} = 5.0\ V$, $R_X = 5.0\ k\Omega$, $C_X = 0$, $C_L = 15\ pF$
t_{pd-}	Negative Trigger Input to Complement Output				25	40			ns	$V_{CC} = 5.0\ V$, $R_X = 5.0\ k\Omega$, $C_X = 0$, $C_L = 15\ pF$
$t_{pw(min)}$	Minimum True Output Pulse Width				45	65			ns	$V_{CC} = 5.0\ V$, $R_X = 5.0\ k\Omega$, $C_X = 0$, $C_L = 15\ pF$
Δt_{pw}	Pulse Width Variation			3.08	3.42	3.76			μsec	$V_{CC} = 5.0\ V$, $R_X = 10\ k\Omega$, $C_X = 1000\ pF$
C_{STRAY}	Maximum Allowable Wiring Cap. (Pin 13)		50			50		50	pF	Pin 13 to Ground
R_X	Timing Resistor	5.0	25	5.0		25	5.0	25	kΩ	

TABLE II —
ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $75°C$, $V_{CC} = 5\ V \pm 5\%$)

SYMBOL	CHARACTERISTIC	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	CONDITIONS (Note 1)
V_{OH}	Output High Voltage	2.4		2.4	3.4		2.4		Volts	$V_{CC} = 4.75\ V$, $I_{OH} = -0.96\ mA$ (Note 2)
V_{OL}	Output Low Voltage		0.45		0.2	0.45		0.45	Volts	$V_{CC} = 4.75\ V$, $I_{OL} = 12.8\ mA$ (Note 2)
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	$V_{CC} = 4.75\ V$ (Note 3)
V_{IL}	Input Low Voltage		.85			0.85		0.85	Volts	$V_{CC} = 5.25\ V$
I_F	Input Load Current		−1.6		−1.0	−1.6		−1.6	mA	$V_{CC} = 5.25\ V$, $V_F = 0.45\ V$
I_R	Input Leakage Current				15	60		60	μA	$V_{CC} = 5.25\ V$, $V_R = 4.5\ V$
I_{SC}	Short Circuit Current			−10		−40			mA	$V_{CC} = 5.0\ V$, $V_{OUT} = 0\ V$ (Note 2)
I_{pd}	Quiescent Power Supply Drain		25			25		25	mA	$V_{CC} = 5.25\ V$ Ground Pins 1 and 2
t_{pd+}	Negative Trigger Input to True Output				25	40			ns	$V_{CC} = 5.0\ V$, $R_X = 5.0\ k\Omega$, $C_X = 0$, $C_L = 15\ pF$
t_{pd-}	Negative Trigger Input to Complement Output				25	40			ns	$V_{CC} = 5.0\ V$, $R_X = 5.0\ k\Omega$, $C_X = 0$, $C_L = 15\ pF$
$t_{pw(min)}$	Minimum True Output Pulse Width				45	65			ns	$V_{CC} = 5.0\ V$, $R_X = 5.0\ k\Omega$, $C_X = 0$, $C_L = 15\ pF$
Δt_{pw}	Pulse Width Variation			3.08	3.42	3.76			μsec	$V_{CC} = 5.0\ V$, $R_X = 10\ k\Omega$, $C_X = 1000\ pF$
C_{STRAY}	Maximum Allowable Wiring Cap. (Pin 13)		50			50		50	pF	Pin 13 to Ground
R_X	Timing Resistor	5.0	50	5.0		50	5.0	50	kΩ	

NOTES:
(1) Unless otherwise noted, 10 kΩ resistor placed between Pin 13 and V_{CC}, for all tests. (R_X)
(2) Ground Pin 11 for V_{OL} Pin 6 or V_{OH} Pin 8 or I_{SC} Pin 8.
Open Pin 11 for V_{OL} Pin 8 or V_{OH} Pin 6 or I_{SC} Pin 6.
(3) Pulse Test to determine V_{IH} and V_{IL} (Min PW 40 ns).

TYPICAL ELECTRICAL CHARACTERISTICS

INPUT LOAD CURRENT VERSUS INPUT VOLTAGE

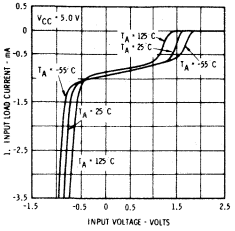


Fig. 3

INPUT LEAKAGE CURRENT VERSUS INPUT VOLTAGE

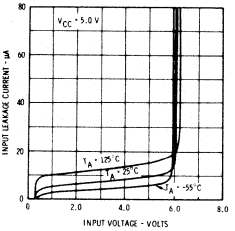


Fig. 4

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (LOW STATE)

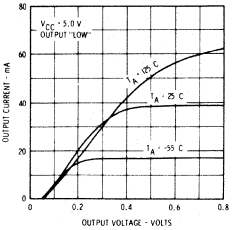


Fig. 5

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (HIGH STATE)

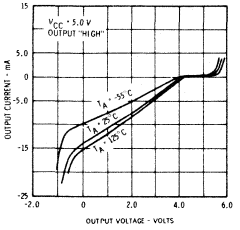


Fig. 6

POWER DISSIPATION VERSUS AMBIENT TEMPERATURE

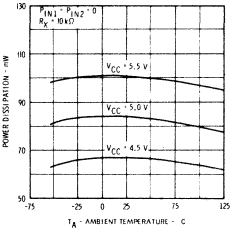


Fig. 7

NEGATIVE TRIGGER DELAY TIME VERSUS AMBIENT TEMPERATURE

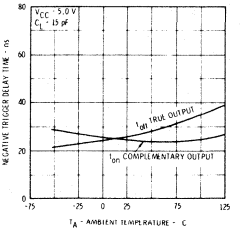


Fig. 8

NORMALIZED OUTPUT PULSE WIDTH VERSUS AMBIENT TEMPERATURE

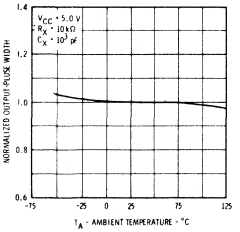


Fig. 9

NORMALIZED OUTPUT PULSE WIDTH VERSUS SUPPLY VOLTAGE

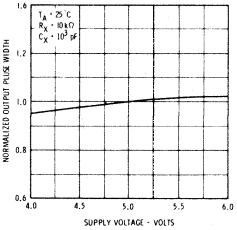


Fig. 10

NORMALIZED OUTPUT PULSE WIDTH VERSUS OPERATING DUTY CYCLE

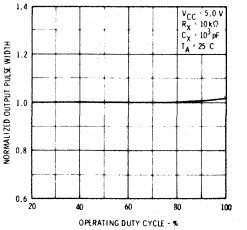


Fig. 11

PULSE WIDTH VERSUS TIMING RESISTANCE

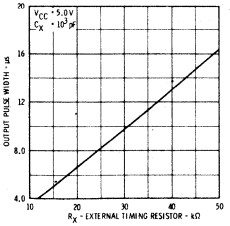


Fig. 12

OUTPUT PULSE WIDTH VERSUS AMBIENT TEMPERATURE

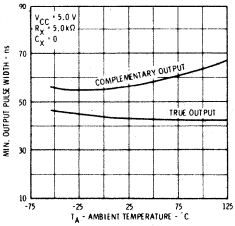


Fig. 13

OUTPUT PULSE WIDTH VERSUS TIMING RESISTANCE AND CAPACITANCE

For $C_X < 10^3$ pF (For $C_X \geq 10^3$ pF, $t_{pw} = 0.32\, R_X C_X \left(1 + \frac{0.7}{R_X}\right)$

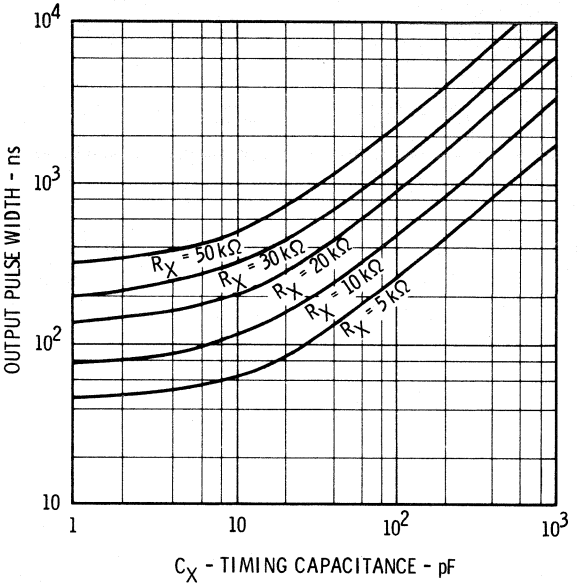
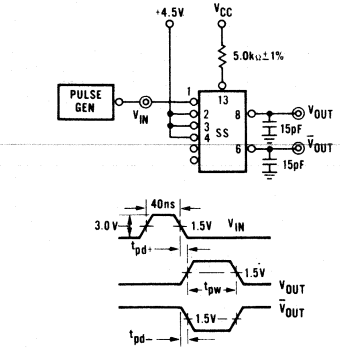


Fig. 14

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



NOTE: Capacitance includes Jig and Probe

LOADING RULES

TTμL INPUT LOAD AND DRIVE FACTORS

−55°C to +125°C

INPUT LEVEL	LOAD FACTOR
High	1
Low	1
OUTPUT STATE	DRIVE FACTOR
High	12
Low	6

0°C to 75°C

INPUT LEVEL	LOAD FACTOR
High	1
Low	1
OUTPUT STATE	DRIVE FACTOR
High	16
Low	8

CCSL INPUT LOAD AND DRIVE FACTORS

−55°C to +125°C

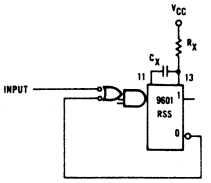
INPUT LEVEL	LOAD FACTOR
High	12
Low	10
OUTPUT STATE	DRIVE FACTOR
High	144
Low	62

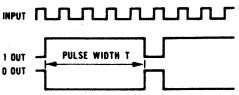
0°C to 75°C

INPUT LEVEL	LOAD FACTOR
High	12
Low	10.5
OUTPUT STATE	DRIVE FACTOR
High	192
Low	85

FAIRCHILD RETRIGGERABLE MONOSTABLE MULTIVIBRATOR 9601

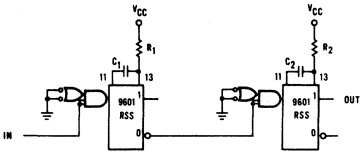
APPLICATIONS

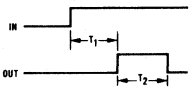




FREQUENCY DIVISION

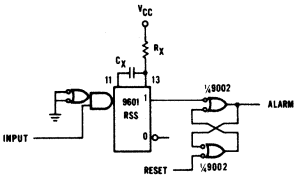
This configuration makes the 9601 non-retriggerable and capable of frequency division.





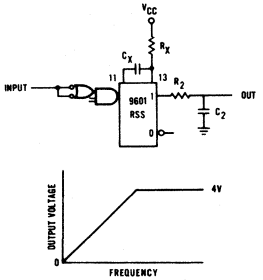
DELAYED PULSE GENERATION

The first 9601 determines the time T_1 befere the initiation of the output pulse.
The second 9601 determines T_2, the output pulse width.



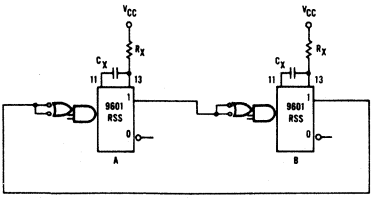
MALFUNCTION INDICATOR

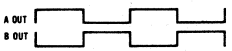
The output of the retriggerable single shot will only remain high if the input frequency is above some fixed value. The input may be a flip flop which normally has a fixed frequency of operation. A system malfunction is indicated when the flip flop frequency drops and retriggering operation of single shot ceases.



DISCRIMINATOR

The 9601 can be used to produce a voltage output proportional to input frequency. For a fixed TC of R_X and C_X, the duty cycle of the output will vary with frequency. This is integrated by R_2 C_2 producing a voltage proportional to frequency.





ASTABLE MULTIVIBRATOR

Frequency of operation is dependent upon value of R_X and C_X.

9602

DUAL TTμL® IC RETRIGGERABLE RESETTABLE MONOSTABLE MULTIVIBRATOR

A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

GENERAL DESCRIPTION — The TTμL 9602 is a DC dual level sensitive retriggerable, resettable monostable multivibrator which provides an output pulse whose duration and accuracy is a function of external timing components only. The 9602 has excellent immunity to noise on the V_{CC} and ground lines. The 9602 uses TTμL for high speed and high fanout capability and is compatible with all devices in the CCSL family of integrated circuits.

- **50 ns TO ∞ OUTPUT PULSE WIDTH RANGE**
- **RETRIGGERABLE 0 TO 100% DUTY CYCLE**
- **COMPLEMENTRY D.C. LEVEL SENSITIVE INPUTS**
- **COMPLEMENTARY OUTPUTS**
- **CCSL COMPATIBLE**
- **OPTIONAL RETRIGGER LOCK-OUT CAPABILITY**
- **PULSE WIDTH COMPENSATED FOR V_{CC} AND TEMPERATURE VARIATIONS**
- **RESETTABLE**

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	0°C to +75°C
V_{CC} Pin Potential to Ground (See Note 1)	−0.5 V to +8.0 V
Input Voltage (D.C.) (See Note 2)	−0.5 V to +5.5 V
Input Current (See Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output When Output is High	0 V to +V_{CC} value
Current Into Output When Output is Low	50 mA

NOTES:

(1) The maximum V_{CC} value of 8.0 volts is not the primary factor in determining the maximum V_{CC} which may be applied to a number of interconnected devices. The voltage at a high output is approximately 1 V_{BE} below the V_{CC} voltage, so the primary limit on the V_{CC} is that the voltage at any input may not go above 5.5 V unless the current is limited, so this effectively limits the system V_{CC} to approximately 7.0 volts.

(2) Because of the input clamp diodes, excess current can be drawn out of the inputs if the D.C. input voltage is more negative than −0.5 V. The diode is designed to clamp off large negative A.C. swings associated with fast fall times and long lines. This maximum rating is intended only to limit the steady state input voltage and current.

LOGIC DIAGRAM

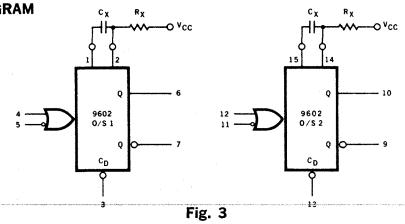


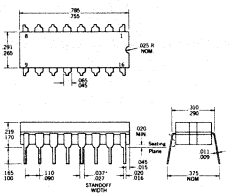
Fig. 3

V_{CC} = Pin 16
Gnd. = Pin 8

ORDER INFORMATION:

Specify U4L9602XXX for flat package and U7B9602XXX for 16-pin Dual In-Line package, where XXX is 59X for the 0°C to +75°C temperature range.

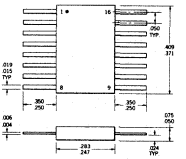
DUAL IN-LINE



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020" diameter lead
Leads are tin-plated Kovar
Package weight is 2.2 grams
*The .037/.027 dimension does not apply to the corner leads

Fig. 1

FLAT PACKAGE



NOTES:
All dimensions in inches
Leads are gold-plated Kovar
Package weight is 0.4 gram

Fig. 2

FAIRCHILD
SEMICONDUCTOR

FUNCTIONAL DESCRIPTION

The 9602 Dual resettable, retriggerable monostable multivibrator has two inputs per function, one of which is active level high and one of which is active level low. This allows a choice of leading edge or trailing edge triggering. The inputs are D.C. coupled making triggering independent of input transition times.

Each time the input conditions for triggering are met, the external capacitor is instantly discharged and a new charging cycle is begun. Successive inputs with a period shorter than the delay time retrigger the one-shot and result in a continuous true output.

The output pulse may be terminated at any time by taking the Reset Pin to a low logic level.

Active pullups are provided for good drive capability into capacitive loads.

OPERATION RULES

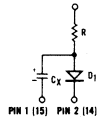
1. An external resistor R_X and an external capacitor C_X are required as shown in the logic diagram. The values of R_X may vary from 5.0 kΩ to 50 kΩ for 0 to +75°C operation, C_X may vary from 0 to any value necessary and obtainable.
2. If a fixed value of R_X is used, the following value is recommended: $R_X = 30$ kΩ for 0 to +75°C operation.
3. The output pulse width t is defined as follows:

$$t = 0.35\ R_X C_X \left[1 + \frac{0.85}{R_X}\right] \text{ (For } C_X \text{ greater than } 10^3 \text{ pF)}$$

Where: R_X is in kΩ
C_X is in pF
t is in ns

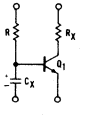
For $C_X < 10^3$ pF, see Fig. 5

4. If electrolytic type capacitors are to be used, the following two arrangements are recommended:



$R < 0.6\ R_X$ (Max)

D_1: any silicon type diode, such as FD700



This circuit also amplifies C_X allowing for linger output pulse width.

$R < R_X\ (0.7)\ (h_{fe}Q_1)$

R_X (min) $< R_X < R_X$ (max)

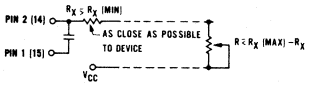
Q_1: Any NPN silicon device with sufficient h_{FE} at low currents, such as 2N2511

Both circuits prevent reverse voltage across C_X. The pulse width t for the circuits is defined as follows:

$$t \approx 0.35\ RC_X \left[1 + \frac{0.85}{R}\right]$$

Where: R is in kΩ
C_X is in pF
t is in ns

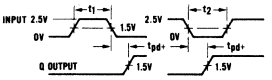
5. To obtain variable pulse width, by remote trimming, the following circuit is recommended:



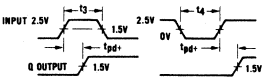
6. Under any operating condition, C_X and R_X (min) must be kept as close to the circuit as possible to minimize stray capacitance and reduce noise pickup.

7. Input Trigger Pulse Rules.

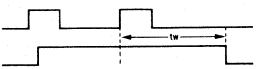
Input to Pin 5 (11)
Pin 4 (12) = Low
Pin 3 (13) = High
t_1, t_3 = Min. Positive Input Pulse Width > 40 ns
t_2, t_4 = Min. Negative Input Pulse Width > 40 ns



Input to Pin 4 (12)
Pin 5 (11) = High
Pin 3 (13) = High



8. The retrigger pulse width is calculated as shown below:

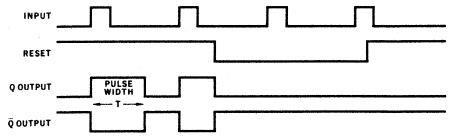


$$tw = tpw + t_{pd+} = 0.35\ R_X C_X \left(1 + \frac{0.85}{R_X}\right) + t_{pd+}$$

The retrigger pulse width is equal to the pulse width tpw plus a delay time. For pulse widths greater than 500 ns, tw can be approximated as tpw.

NOTE: Retriggering or resetting will not occur if the retrigger pulse comes within $0.35\ R_X C_X \left(\frac{0.85}{R_X}\right)$ ns after the initial trigger pulse.

9. Reset Operation—An overriding active low level reset is provided on each oneshot. By applying a low to the reset, any timing cycle can be terminated or any new cycle inhibited until the low reset input is removed. Trigger inputs will not produce spikes in the output when the reset is held low.



ELECTRICAL CHARACTERISTICS (T_A = 0°C to 75°C, V_{CC} = 5 V ±5%)

SYMBOL	CHARACTERISTIC	LIMITS 0°C MIN.	0°C MAX.	+25°C MIN.	+25°C TYP.	+25°C MAX.	+75°C MIN.	+75°C MAX.	UNITS	CONDITIONS (Note 1)
V_{OH}	Output High Voltage	2.4		2.4	3.4		2.4		Volts	V_{CC} = 4.75 V, I_{OH} = −0.96 mA (Note 2)
V_{OL}	Output Low Voltage		0.45		0.25	0.45		0.45	Volts	V_{CC} = 4.75 V, I_{OL} = 11.3 mA V_{CC} = 5.25 V, I_{OL} = 12.8 mA (Note 2)
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold
I_F	Input Load Current		−1.41 −1.6		−0.91 −1.0	−1.41 −1.6		−1.41 −1.6	mA	V_{CC} = 4.75 V, V_F = 0.45 V V_{CC} = 5.25 V
I_R	Input Leakage Current				15	60		60	μA	V_{CC} = 5.25 V, V_R = 4.5 V
I_{SC}	Short Circuit Current			−8.0		− 50			mA	V_{CC} = 5.25 V, V_{out} = 1.0 V, (Note 2)
I_{pd}	Quiescent Power Supply Drain				35				mA	V_{CC} = 5.0 V Ground Pins 5 and 11
t_{pd+}	Negative Trigger Input to True Output				27				ns	V_{CC} = 5.0 V, C_L = 15 pF R_X = 5.0 kΩ, C_X = 0
t_{pd-}	Negative Trigger Input to Complement Output				27				ns	V_{CC} = 5.0 V, C_L = 15 pF R_X = 5.0 kΩ, C_X = 0
$t_{pw(min)}$	Minimum True Output Pulse Width				80				ns	V_{CC} = 5.0 V, C_L = 15 pF R_X = 5.0 kΩ, C_X = 0
t_{pw}	Pulse Width				3.8				μs	V_{CC} = 5.0 V, R_X = 10 kΩ, C_X = 1000 pF
R_X	Timing Resistor	5.0	50	5.0		50	5.0	50	kΩ	External timing resistor

NOTES:
(1) Unless otherwise noted, 10 kΩ resistor placed between Pin 2 (14) and V_{CC}, for all tests. (R_X)
(2) Ground Pin 1 (15) for V_{OL} Pin 7 (9) or V_{OH} Pin 6 (10) or I_{SC} 6 (10), also apply momentary ground to pin 4 (12)
Open Pin 1 (15) for V_{OL} Pin 6 (10) or V_{OH} Pin 7 (9) or I_{SC} Pin 7 (9).

LOADING RULES

TTμL INPUT LOAD AND DRIVE FACTORS

INPUTS	LOAD HIGH	LOAD LOW
3, 4, 5, 11, 12, 13	1 U.L.	1 U.L.

OUTPUTS	DRIVE FACTOR HIGH	DRIVE FACTOR LOW
6, 7, 9, 10	16 U.L.	8 U.L.

1 U.L. = 1 TTμL Gate Input Load

CCSL INPUT LOAD AND DRIVE FACTORS

INPUTS	LOAD HIGH	LOAD LOW
3, 4, 5, 11, 12, 13	12	10.5

OUTPUTS	DRIVE FACTOR HIGH	DRIVE FACTOR LOW
6, 7, 9, 10	192	85

SWITCHING CIRCUITS AND WAVEFORMS

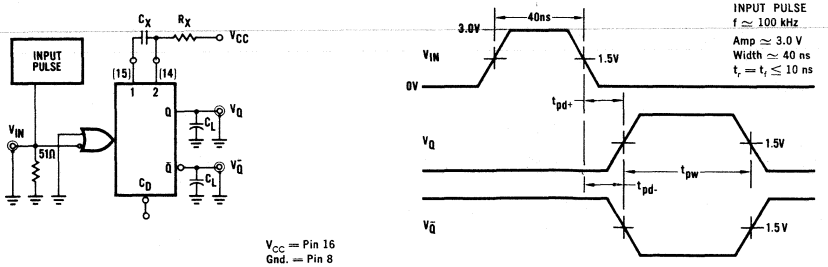


Fig. 4

OUTPUT PULSE WIDTH VERSUS TIMING RESISTANCE AND CAPACITANCE

For $C_X < 10^3$ pF

For $C_X \geq 10^3$ pF, $t_{pw} = 0.35\ R_X C_X\ (1 + \frac{0.85}{R_X})$

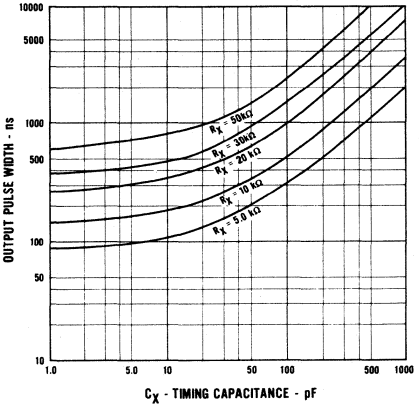
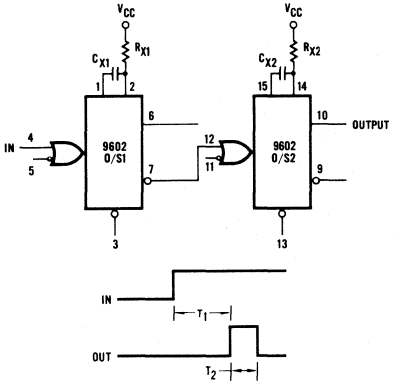


Fig. 5

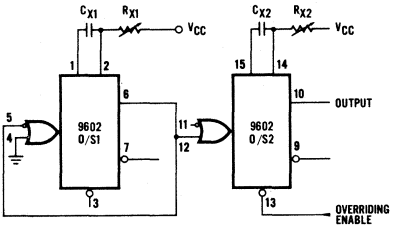
APPLICATIONS



DELAYED PULSE GENERATION

The first one-shot determines the time T_1 before the initiation of the output pulse. The second one-shot determines T_2 the output pulse width.

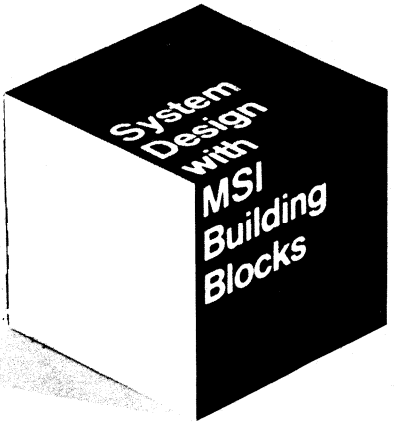
Fig. 6



PULSE GENERATOR

The output frequency produced with the above configuration is determined by C_{X1} and R_{X1}, while the pulse width is determined by C_{X2} and R_{X2}. O/S 1 forms an astable multivibrator with an output pulse width of approximately 25 ns, while O/S 2 extends the pulse width to the required value.

Fig. 7


System
Design
with
MSI
Building
Blocks

General Description

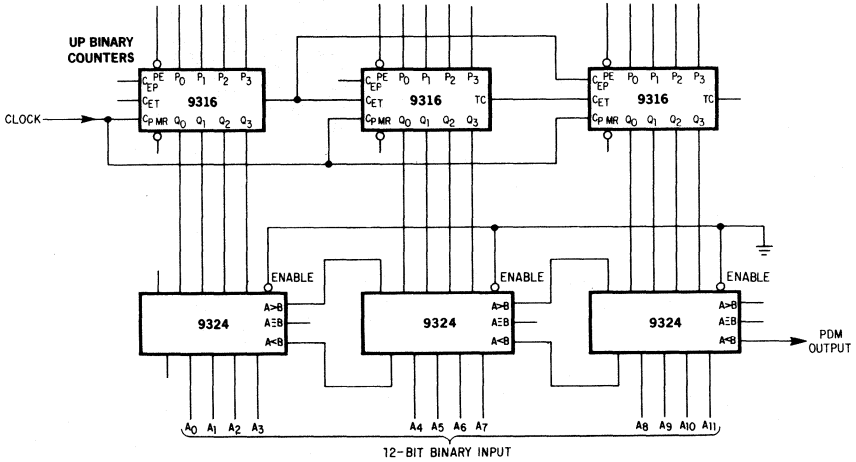
This 12-bit D to A converter offers simple construction (six MSI packages VS 58 discrete IC packages) by taking advantage of the unique characteristics of the 9324 comparator. This comparator generates both the greater-than or less-than function as well as the equal-to, and is easily expanded to N bit words. Also the PDM (pulse duration modulation) output, when coupled with a fast response, low-pass filter, allows precise conversion of a unique digital wavetrain to an analog value (i.e., the filter responds to both frequency and/or duty cycle variations in the digital waveform). The application shown allows easy expansion to multiple stages.

Operation

The 9316 counters are continually counting. The 9324's are expanded for 12 bits by connecting the greater-than and less-than outputs of the preceding stage to the A_i and B_i inputs of the following stage. The PDM output stays low until the 12-bit binary input word "equals" the count. The resulting PDM output can be converted to voltage with a low-pass filter. A unique analog output is associated with each binary input. To obtain a precise analog output, a precision voltage reference can be used as an input to switch circuit that is keyed by the A<B output of the last comparator.

A minimum clock rate of 3 MHz should be maintained on the 9316 counter to guarantee sufficient cycle time for the low-pass filter.

High Speed 12-Bit Digital-To-Analog Conversion Technique



General Description

The 9306 Decade Up/Down Counter provides a high-speed building block in the construction of analog-to-digital converters that work in 8421 BCD code for display or control purposes. The device can be used in a continuous conversion mode of operation where one or two decade counters count up and down in an attempt to follow the digital count value of the analog signal.

Here the maximum analog data input frequency is primarily dependent on the response time capability of the comparator circuit (μA710). With a fast response time comparator, video signals up to 4 MHz can be converted.

Operation

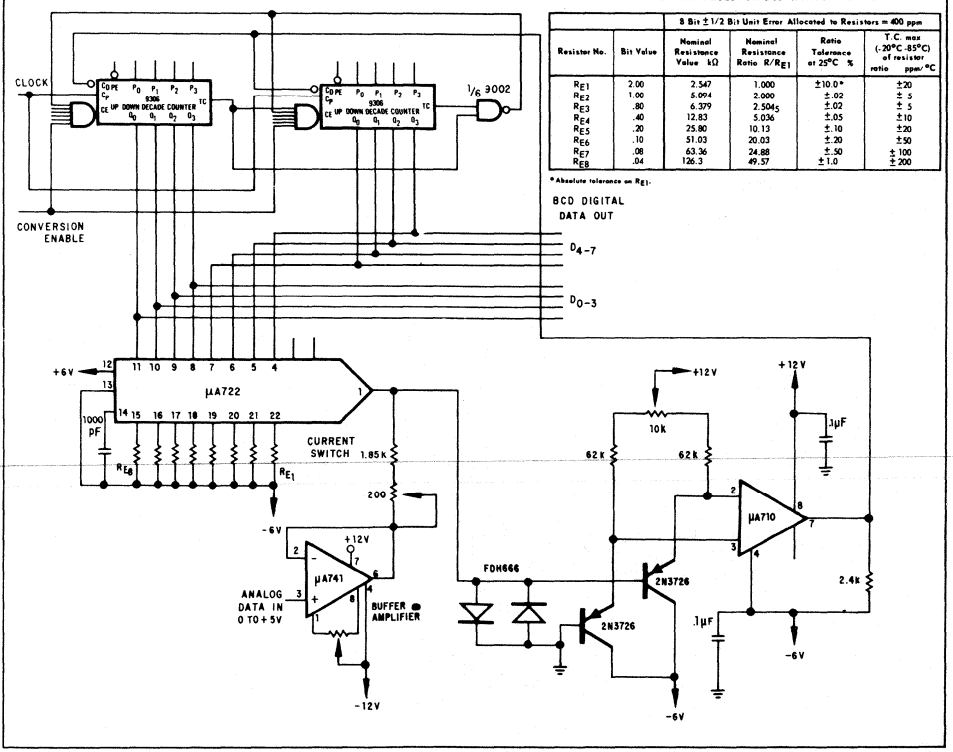
The outputs of the 9306 counters are applied to a set of current switches (μA722). The ladder resistors are chosen to generate a weighted 8421 BCD code analog value of current at the output of the programmable current switch. The analog voltage whose digital equivalent is required is buffered off by a unity gain voltage follower. The voltage seen at the comparator input is the input voltage minus the current representation of the present count subtracted across the nominal 2K scaling resistor. If the comparison voltage is above ground, the digital value applied to the current switch is too small, and the output of the comparator goes high. Then the counter counts up until the input analog voltage exceeds the digital value derived from the network when the output of the comparator goes low, and the counter starts to count down. The output of the two 9306 counters is thereby a digital value in 8421 BCD code of the input analog voltage. In the feedback path between the final terminal count and the count enable inputs of both counters, there is a two-input gate that inhibits the counters from recirculating whenever the input analog voltage is greater than the specified value. The counters effectively saturate at states 00 to 99 if the maximum input level specified is exceeded.

Continuous Analog-To-Digital Conversion

FIXED RESISTOR VALUES FOR BCD RESISTOR ARRAYS

		8 Bit ±1/2 Bit Unit Error Allocated to Resistors = 400 ppm			
Resistor No.	Bit Value	Nominal Resistance Value kΩ	Nominal Resistance Ratio R/R_{E1}	Ratio Tolerance at 25°C %	T.C. max (-20°C-85°C) of resistor ratio ppm/°C
R_{E1}	2.00	2.547	1.000	±10.0*	±20
R_{E2}	1.00	5.094	2.000	±.02	± 5
R_{E3}	.80	6.379	2.504_5	±.02	± 5
R_{E4}	.40	12.83	5.036	±.05	±10
R_{E5}	.20	25.80	10.13	±.10	±20
R_{E6}	.10	51.03	20.03	±.20	±50
R_{E7}	.08	63.36	24.88	±.50	±100
R_{E8}	.04	126.3	49.57	±1.0	±200

* Absolute tolerance on R_{E1}.



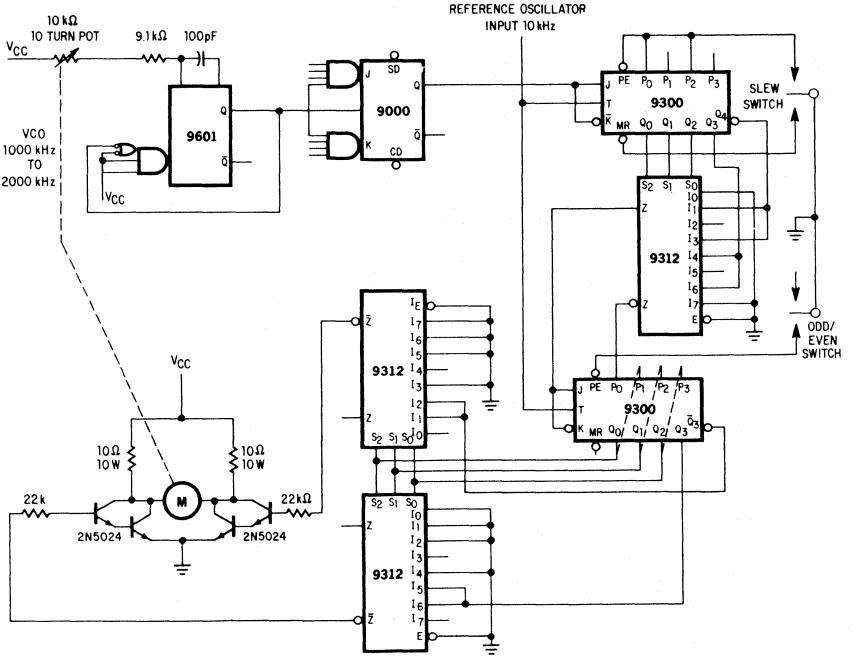
General Description

Crystal controlled tuning of a communications receiver provides the ability to *automatically* and *accurately* tune to specified frequency without any signal present at that frequency. Here is an inexpensive method of generating exact local oscillator frequencies with a simple MSI design. This method offers significant cost savings when a large number of channels is required.

Operation

To select a channel, the slew switch is operated in the proper direction until the display indicates the desired channel frequency range. The slew switch is then released, bringing into operation the two-stage digital frequency discriminator, constructed with two 9300's and three 9312's. The output of two 9312 multiplexers drive the DC tuning motor, CW or CCW. When the local oscillator frequency (as generated by the 9000 flip-flop) is synchronous with the 10 KHz crystal reference, both of the motor driving multiplexers will have a zero duty cycle output. When the frequency is either too high or low the appropriate multiplexer output will increase its duty cycle to return the frequency to the correct value.

Crystal Controlled Detent Tuning With Automatic Dial Calibration



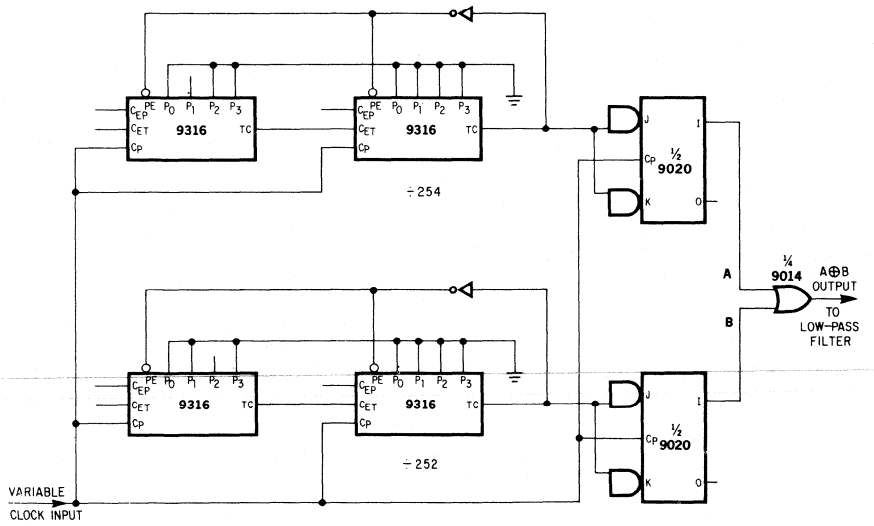
General Description

A sine-wave generator, adjustable for a wide range of frequencies is formed using only five MSI packages and a low-pass filter. Again, the *synchronous presettable characteristic* of all Fairchild MSI counters and shift registers is employed to minimize timing problems and simplify design.

Operation

The 9316's (presettable hexidecimal counters) form divide-by-254 and divide-by-252 frequency dividers. The output of the fnal stage is fed back to the parallel enable for simple, synchronous, resetting. When the output of the 9316 frequency dividers is combined through an exclusive OR gate, and sensed through a low-pass filter, a sine-wave results. The frequency of the sine-wave is controlled by varying the clock input frequency of the frequency dividers.

Sine-Wave Generation Technique



General Description

Here is a design to distribute 8-bit words of serial PCM data to holding registers for sixteen channels. In the application shown, the words are distributed sequentially. This method offers very high speed distribution, yet is implemented with only 20 MSI packages and two (2) discrete IC packages. Alternate designs with discrete IC's require at least 86 packages.

Operation

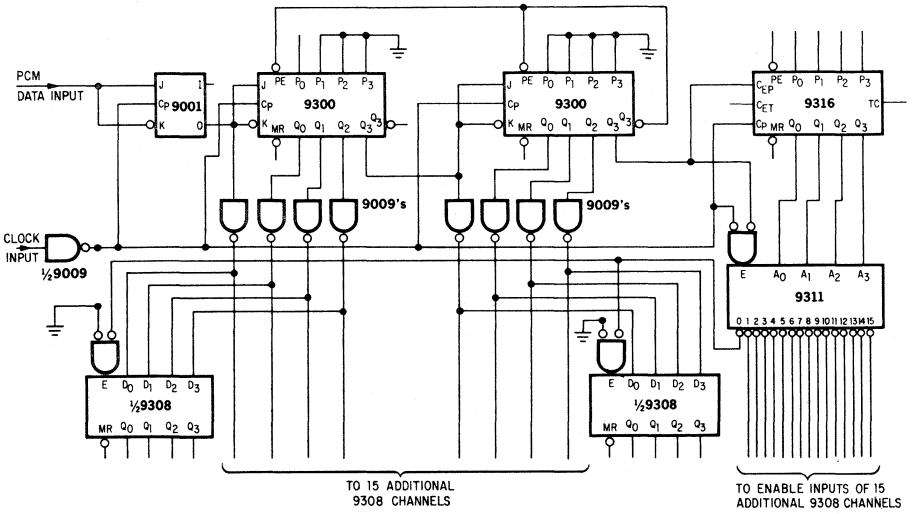
The PCM data is serially stored in the combination of the 9001 flip-flop and two 9300's in 8-bit bytes. When the 8-bits have been shifted in, the Q_3 output of the second 9300 will go high. This action will disable the channel selector decoder (9311) and will enable the channel selector (9316) so that it will count on the next clock input. At the same time, the Q_3 output of the same 9300 will be low, thus enabling the parallel entry of the 9300's so that the parallel information (1000 0000) will enter on the next clock input. (Remember — the parallel enable is synchronous with the clock on all Fairchild shift registers and counters.)

On the next clock pulse, the parallel data will enter the 9300's, the 9316 will count one, the 9300's parallel enable will go high, the counter (9316) will be disabled and the selector decoder (9311) will be enabled again.

The serial PCM data will again be shifted in with each successive clock pulse and this data will be stored in the selected channel (9308) in 8-bit bytes.

The 9009 dual buffers are used to supply sufficient drive for sixteen 9308 channels.

16-Channel PCM Distribution Technique



General Description

How about a *simple* method for converting keyboard switch closures to a binary code? Three MSI and two discrete packages can do it, yet provide fast rollover, insensitivity to contact bounce, and elimination of ambiguity usually caused when several keys are depressed.

In fact, the addition of a few more MSI elements would add even greater capability to this design. As an example, the addition of another 9312, 9316, and 9601 can result in a single serial binary PDM output group in response to each key depression. Additional control inputs could be used to restrict the range of the scan counter if only certain keys should be enabled in a certain mode as is the case in key punch machines. Addition of a 9034 Read-Only Memory would allow the selection of any code output with a single keyboard design. A single monolithic parity generator could be added to provide parity at very little additional cost. Or, you might want to add two Read-Only Memories to drive a character display and a normal output simultaneously.

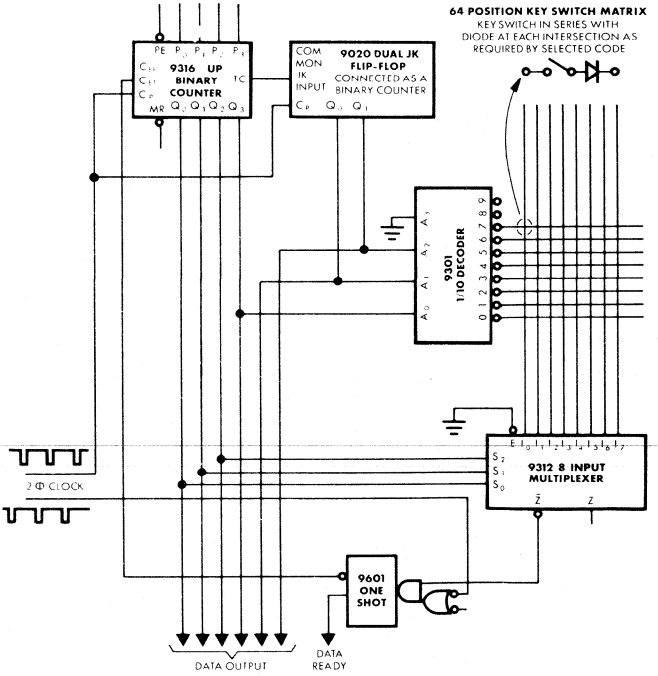
Operation

The two major elements of the design are a 64-position matrix and a six-bit synchronous counter. (The counter is composed of a 9316 four-bit binary counter and a 9020 dual JK flip-flop.) The three Most Significant Bits of the counter output address the 1-of-8 decoder (9301) forming one side of the matrix, sequentially driving its outputs "low." The three Least Significant Bits address the 9312 scanning multiplexer (the other side of the matrix), sequentially looking at its eight inputs. With this arrangement, all multiplexer inputs are scanned once for every change in the decoder output.

When a key is depressed a high is transmitted to the *complementary* output of the multiplexer. This triggers the one-shot which stops the counter and provides a "data ready" signal. The duration of the one-shot is set to cover any possible contact bounce. The output of the counter can now be used as the encoded signal, and the matrix can be arranged so that any key closure provides any binary code from 000 000 to 111 111.

The code that appears corresponds to the first key depressed. As long as that key remains down, the retriggerable one-shot continues to receive reset pulses that hold the counter at the count independently of any other switch closures on the board. Once that key is released, the counter resumes its scanning after the one-shot time period has run out.

Scanning Keyboard Encoder



General Description

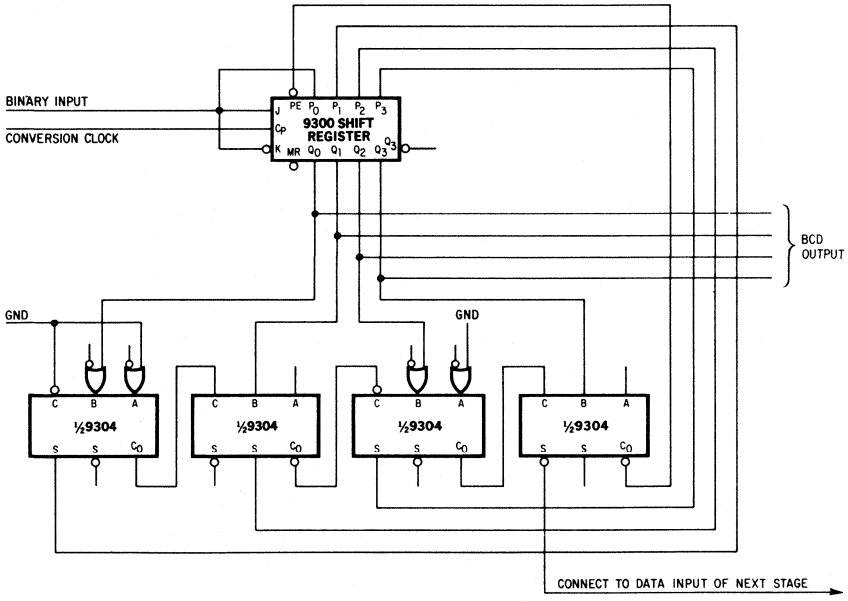
Only three (3) MSI packages are needed for a complete Binary-to-BCD converter. The fast carry generation (8 nsec. per stage) of the 9304 (full adder) allows high speed conversion.

These same three packages can be used to form a BCD-to-Binary Converter, and the addition of a small number of external gates would allow other code conversions (i.e., excess three, etc.)

Operation

Four bits are shifted into the 9300. If the value of the register is five or greater, the mode of the register is converted to parallel enable and, on the next clock, three is added to the present contents of the register. The results are then shifted one place, which provides a one input to the next more significant stage. After the fourth clock pulse, the register contains the BCD equivalent of the serial binary input.

Binary-To-BCD Conversion



General Description

This D/A converter technique, with a select matrix of only three MSI packages, is capable of *simultaneously* converting ten channels of 8-bit digital words to analog. The PDM (pulse duration modulation) output of each channel can either be stored in digital form for later translation or it can be immediately translated to analog through a low pass filter.

Again, a voltage reference can be used for shaping of the PDM levels to attain more precise analog translation.

Operation

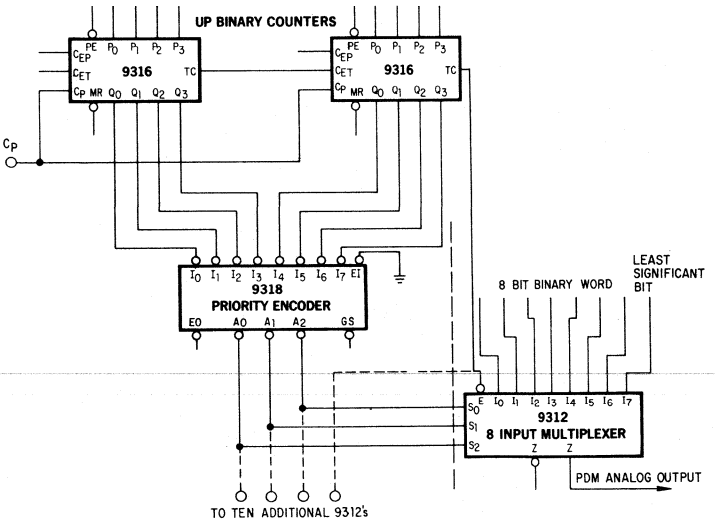
The 9316's (presettable hexidecimal counters) are fed into the 9318 (priority encoder) — the Q_0 output routed to the LSB encoder input — to give a code sequence on the multiplexer select logic inputs that will guarantee that the I_0 input of each multiplexer is seen at the output for 128/256th of the count cycle, the I_7 input is seen at the output for 64/256th of the count cycle, etc.

This weighted PDM output can then be integrated, or in many cases such as panel meter or audio speakers, fed directly to the analog output device.

NOTE:

The 9316's should be clocked at 1 MHz minimum clock rate.

A Multiple Channel Digital-To-Analog Conversion Technique



General Description

A simple method for selecting TV channels by using the 9300 as a presettable feed back shift counter is illustrated. Since a 9300 costs much less than presettable sequential counters, a significant cost reduction is achieved using the MSI packages VS alternate designs.

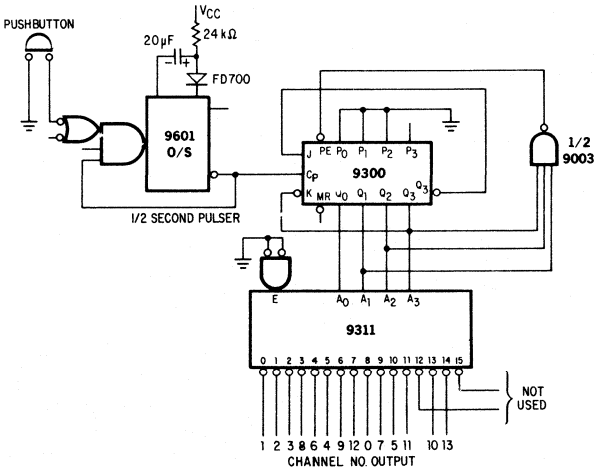
Operation

The retriggerable one-shot (9601) is connected as an oscillator. As long as the push button switch is closed, the 9601 will produce output pulses at the rate of approximately two per second. These pulses will cause the 9300 to count (connected as a presettable feedback shift counter).

The count sequence is determined by hand-wiring the start count into the synchronous parallel entry of the register and sensing the terminal count through the single T^2L NAND gate.

The channel select decoder (9311) provides a logic flow for the channel selected.

TV Tuner Switch Control Technique



APPLICATIONS OF THE CCSL 9304 DUAL ADDER

INTRODUCTION

The Fairchild CCSL 9304 Dual Adder is a multifunctional, complex, integrated circuit for use in high-speed digital systems. The 9304 Dual Adder consists of two separate full adders with carry, and both polarities of the sum as outputs. The device uses TTμL (Transistor-Transistor Logic) technology and has active pullup outputs, thus providing high speed and excellent noise margins with reasonable power consumption. Like other high-speed TTμL devices, the dual adder incorporates input diodes to ground, thereby minimizing line reflection effects. It is compatible with all other Fairchild CCSL (Compatible Current Sinking Logic) integrated circuits and is particularly attractive for use with other Fairchild complex function devices. The two adders are unconnected, thereby enabling them to be used in the widest variety of applications. They are suitable for high-speed ripple-carry addition, carry-save arithmetic, and parity generating or checking. In a large number of applications the use of the 9304 Dual Adder reduces considerably the number of required integrated circuits, associated interconnections, and packaging.

LOGIC DESCRIPTION

The logic diagram, pin layout, and loading rules of the Dual Adder are shown in Fig. 1. AND-OR-INVERT gates are used to produce a carry-dependent sum adder. This adder design has the advantage of being particularly suitable for TTμL circuitry, and it also has a propagation delay of a single AND-OR-INVERT gate - typically 8 ns with reasonable loading. This single gate delay design produces the low active carry out which can generally be used directly without need for inversion. Therefore, no additional inverter is provided to generate the active high carry output.

Consider the sum and carry equations for Full Adder 1.

$$S = A \oplus B \oplus C$$

$$\overline{C_0} = \overline{AB + BC + AC}$$

If active low inputs are used, the adder produces the outputs at the sum and carry terminals:

$$\overline{A} \oplus \overline{B} \oplus \overline{C}$$

$$\overline{\overline{A}\overline{B} + \overline{B}\overline{C} + \overline{A}\overline{C}}$$

These two Boolean expressions can be manipulated to give:

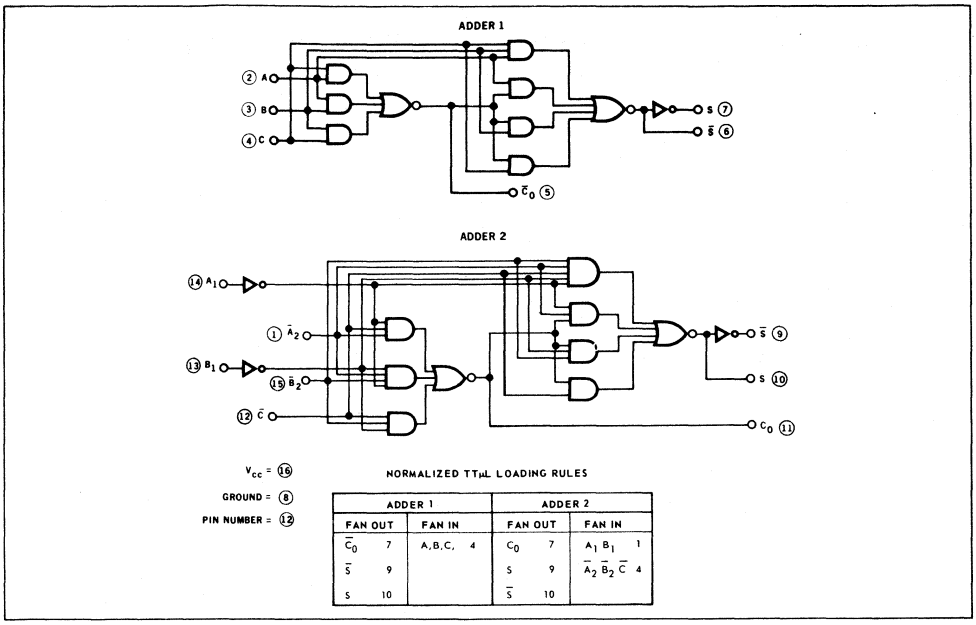
$$\overline{A \oplus B \oplus C}$$

$$AB + BC + AC$$

These expressions are the active low sum and active high carry, respectively. Therefore, Adder 1 provides an active low carry out using active high inputs, and an active high carry out using active low inputs.

Adder 2 is identical to Adder 1 except that provision is also made for active low inputs by providing inverters at the non-carry input terminals. Therefore, the two adders can be cascaded, the carry output of Adder 1 connected to the carry input of Adder 2, and the correct sums and carry result. In a great many applications, the inverter at the non-carry inputs causes an extra delay which can be avoided. Adder 2 has two extra terminals for provision of non-carry active high inputs. If the inputs to the inverters are grounded (pins 13 and 14) the two full adders become logically identical.

FAIRCHILD
SEMICONDUCTOR



ADDER 1			ADDER 2		
FAN OUT		FAN IN	FAN OUT		FAN IN
$\bar{C}_0$	7	A,B,C, 4	C_0	7	A_1 B_1 1
$\bar{S}$	9		S	9	$\bar{A}_2$ $\bar{B}_2$ $\bar{C}$ 4
S	10		$\bar{S}$	10	

Fig. 1. CFSL 9304 dual adder logic diagram.

The logic block diagram of the Dual Adder is shown in Fig. 2. The principle of duality is used to show how the adders respond to both active-high and active-low inputs. This dual method of logically describing the function of the adder facilitates logic design and enables a greater understanding of the capabilities of the device. Examples of both representations are given in the following applications. It should be noted that variables A, B, and C acting as inputs to the adders can be interchanged at will and the correct sum and carry will result, since the sum and carry functions are symmetrical. This may be of advantage when laying out printed circuits.

Unused inputs on the adders may be left open. However, with the exception of inputs B_2, A_2, on pins 13 and 14, (Fig. 1) maximum speed through the adder will occur, if unused inputs are tied to a positive voltage in order to minimize the effect of shunt capacitance. Unused inputs may be directly connected to V_{CC} if the supply voltage high limit is restricted to 5.5 volts, or they may be tied to V_{CC} through a 2-KΩ current-limiting resistor. Another method is to connect unused inputs to another logic signal ensuring that the fanout of the driving device is not exceeded and that logic operation is not affected. If an unused gate is available, an input can be grounded and the output conveniently used as a positive voltage source.

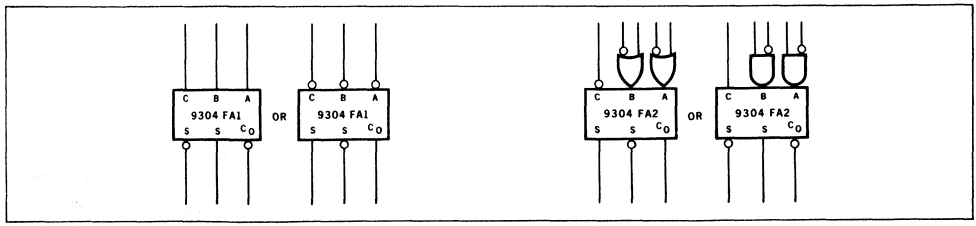


Fig. 2. Dual adder functional block representation.

APPLICATIONS

A few of the uses for the 9304 Dual Adder are described below.

Adder

The Fairchild 9304 Dual Adder is very attractive for use as a high-speed binary ripple-carry adder. The single AND-OR INVERT gate carry delay per adder stage often obviates the necessity for carry lookahead circuitry in a large number of digital computation applications. Figure 3 shows the method previously outlined, where the active low output carry of Adder 1 is fed into the active low carry input of Adder 2, and the active high carry output of Adder 2 is fed into the active high carry input of Adder 1 and so on. The scheme provides high addition speed with low integrated circuit package count. Figure 4 shows the resulting propagation delay to the final sum and the integrated package count against word length.

The propagation delay for an N-stage parallel adder using this ripple-carry technique is typically $[(N + 1) \cdot 8 + 5]$ns. Therefore, parallel addition of two 24-bit binary numbers can be performed in approximately 200 ns. The adder design shown in Fig. 3 uses an active high carry input, and the input carry terminal should be grounded if not used. If an active low input carry is desired, the second adder in the 9304 should be used at the first adder stage followed by Adder 1 at the second adder stage. Active low X, Y inputs to the adder can be used with the same adder scheme. From reference to the duality principle shown in Fig. 2 it can be seen that the active low and active high sum outputs will be reversed. The ripple-carry scheme can also be used for subtraction as shown in Fig. 5. Although the complement of the Y variable is required at each stage, an additional inverter is required only at every other adder stage since the remaining inverters can be supplied by Adder 2. The propagation delay to the final difference is identical to that of the ripple-carry adder.

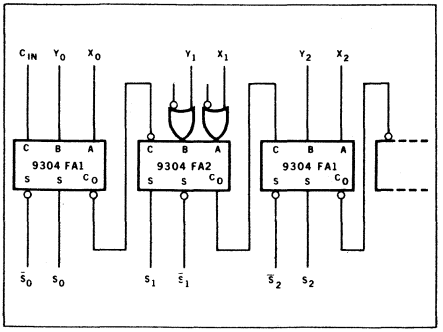


Fig. 3. Ripple-carry parallel addition.

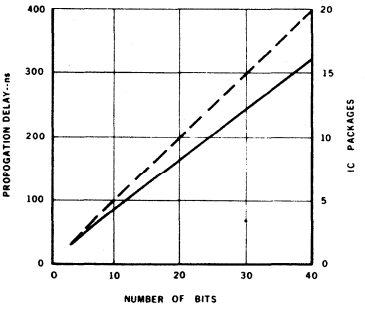


Fig. 4. Propagation delay and package count against word length for ripple-carry addition.

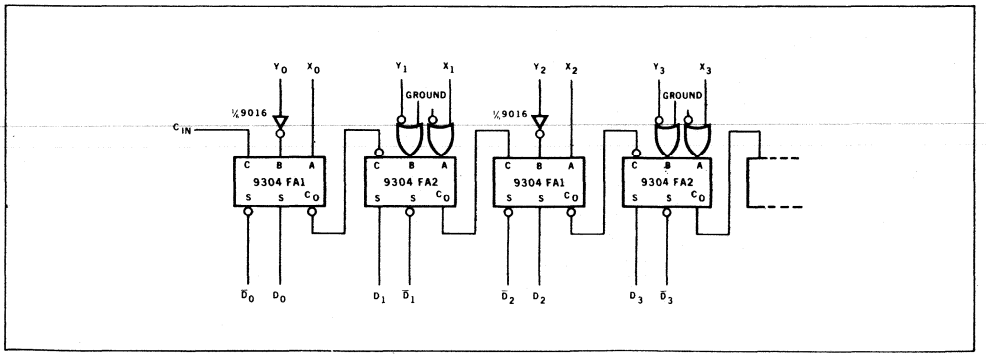


Fig. 5. Ripple-carry parallel subtraction.

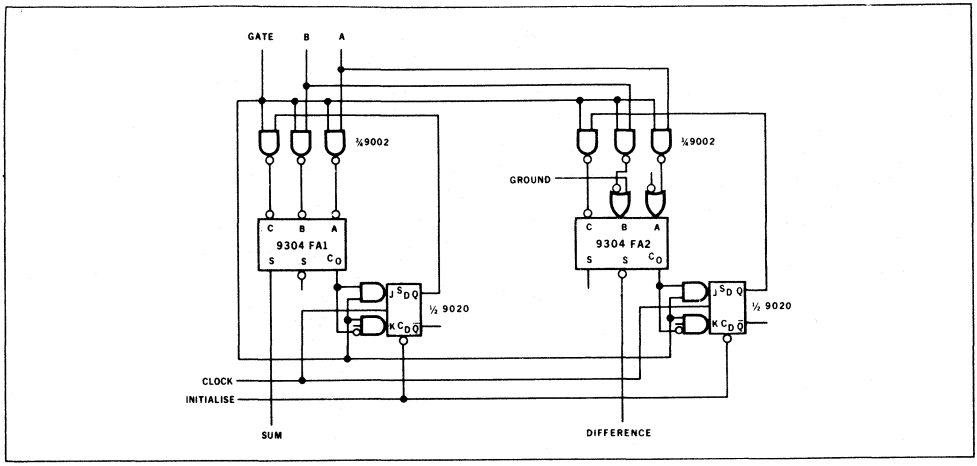


Fig. 6. Serial sum and difference generator.

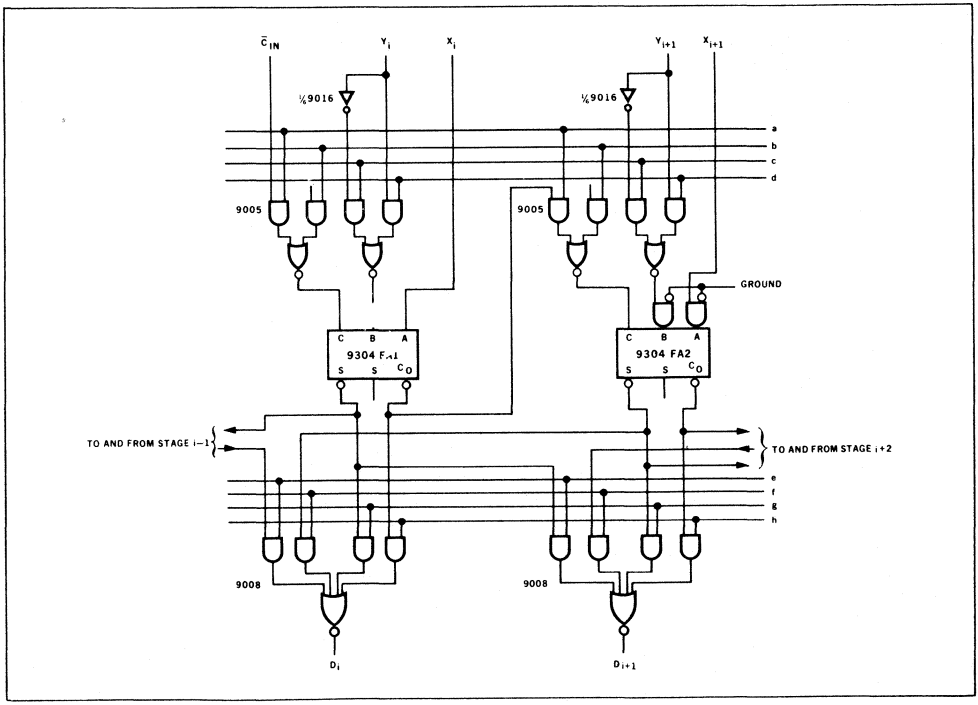


Fig. 7. Arithmetic logic unit.

TABLE I.

ARITHMETIC AND LOGIC OPERATIONS.

Function	Description	Time (ns)	a	b	c	d	e	f	g	h
X + Y	X added to Y	16N + 21	1	0	1	0	0	0	1	0
X − Y	Y subtracted from X	16N + 16	1	0	0	1	0	0	1	0
$(X+Y)2^{1}$	X added to Y and shifted up one place	16N + 21	1	0	1	0	1	0	0	0
$(X+Y)2^{-1}$	X added to Y and shifted one place down	16N + 21	1	0	1	0	0	1	0	0
X AND Y	X logical AND with Y	29	*	1	1	0	0	0	0	1
X OR Y	X logical OR with Y	37	0	0	1	0	0	0	0	1
X EX. OR Y	X logical EXCLUSIVE OR with Y	37	*	1	1	0	0	0	1	0
X EQU. Y	X logical EQUIVALENCE with Y	37	0	0	1	0	0	0	1	0
	N = Number of bits in binary word.		* = Indicates "Don't Care" condition.							

In Fig. 6 the adders are shown used in a serial mode to provide the sum and difference of two variables which are presented serially at the inputs A and B. The two carry storage flip-flops should be initialised at the start of a computation to ensure correct results. Given their sum and difference, the same design can be used to generate two variables. If the sum and difference are added, the resulting sum out is one variable multiplied by 2, or shifted one-bit position in time, and the difference would produce twice the other variable.

Figure 7 shows how the 9304 can be used in an arithmetic logic unit for a binary machine. The unit can perform the operations given in Table I at high speed on the input variables X and Y. The configuration of the control lines a, b, c, d, e, f, g, and h to achieve the various possible operations is also given in Table I. Addition and subtraction is not as fast in this arithmetic logic unit as in the ripple-carry adder because of the necessity of placing an AND-OR INVERT gate at the output of each carry stage. However, the addition and subtraction speed is still fast enough for a large number of process control computers.

The 9304 Dual Adder is very suitable for use as a building block in parallel-serial or parallel-parallel decimal computers or desk calculators. Figure 8 shows an addition scheme in the 8421 BCD code. This design produces an active low carry out for an active high carry in. This is no problem when parallel-serial operation is performed, since both outputs of the carry storage flip-flop will be normally available.

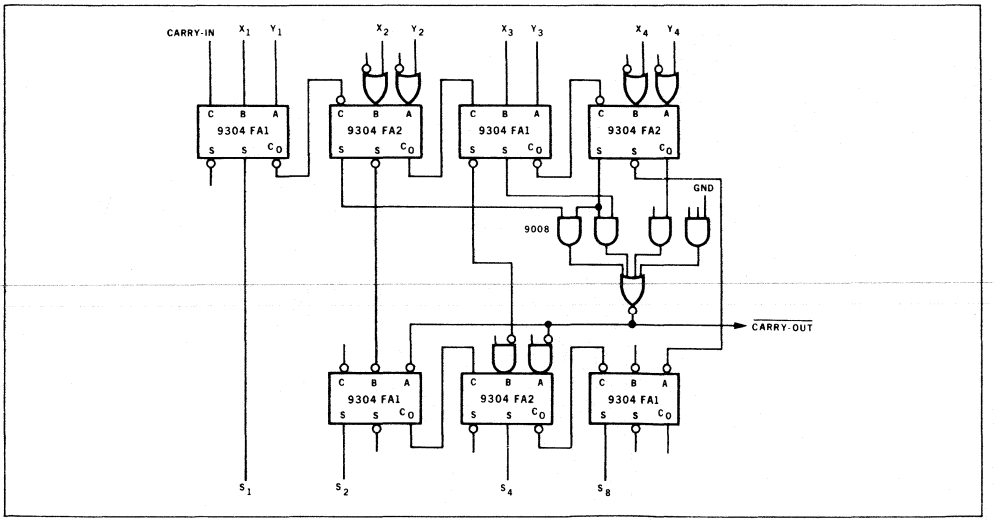


Fig. 8. BCD adder 8421 code positive carry in negative carry out.

Q

If parallel BCD arithmetic is used, advantage can be made of the flexibility of the Dual Adder and the 8421 BCD Code Adder of Fig. 9 which produces an active high carry out for an active low carry in can be used alternatively with the adder of Figure 8. The delay to the final sum in both designs is typically 85 ns, with a carry delay to the next decade of 60 ns.

The BCD adder of Fig. 8 works as follows: The inputs to the adder (X_1, X_2, X_4, X_8, and Y_1, Y_2, Y_4, Y_8) are weighted accordingly in the 8421 BCD code. If the two decimal numbers, XY, are added in a 4-bit binary adder and the resulting decimal sum is less than 9, then the sum produced by the binary adder is correct. However, if the sum is greater than 9, then a carry to the next decade should be produced and a correction to the sum applied. A carry to the next decade can be produced in three ways: (1) A carry from the output of the ripple 4-bit binary adder indicating that the sum is greater than or equal to 16. (2) A sum from the last adder stage and a sum from the next-to-last adder stage indicating that the sum is greater than or equal to 12. (3) A sum from the second adder stage together with a sum from the final stage, indicating that the sum is greater than or equal to 10. The Boolean function for the carry-to-the-next decade is therefore

$$C = C_8 + S_8S_4 + S_8S_2$$

In Fig. 8, the active low carry is produced by a TTμL 9008 device and can be used directly without inversion to correct the sum by the addition of 6 whenever a carry occurs. This addition of 6 is performed using additional adders.

Various other BCD code adders can be designed around the 9304 Dual Adder. Figures 10 and 11 show adders using the 5421 BCD code. The design in Fig. 10 produces an active low carry out for an active high carry in. The adder in Fig. 11 requires an active low carry in and produces an active high carry out, thereby enabling the designs of Figs. 10 and 11 to be cascaded for parallel BCD code addition. A BCD adder using the excess-3 code is shown in Fig. 12. The excess-3 code has the advantage of producing a carry to the next decade under identical conditions to a 4-bit binary adder. If a carry is present, the sum must be corrected by adding 3 to the binary sum; if a carry is not present, 3 must be subtracted from the binary sum. The design requires only a single inverter, due to loading conditions, in addition to the adders.

Carry Save Arithmetic

Since the adders are logically separate, they can be used in a variety of applications which do not make use of the ripple-carry concept. One such application is carry-save arithmetic. This technique of multi-variable addition uses

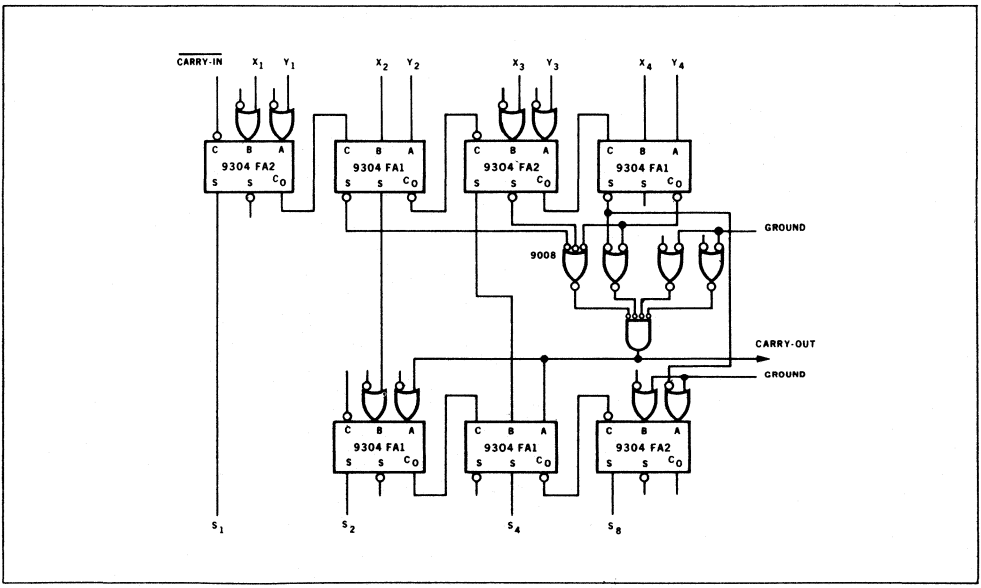


Fig. 9. BCD adder 8421 code negative carry in positive carry out.

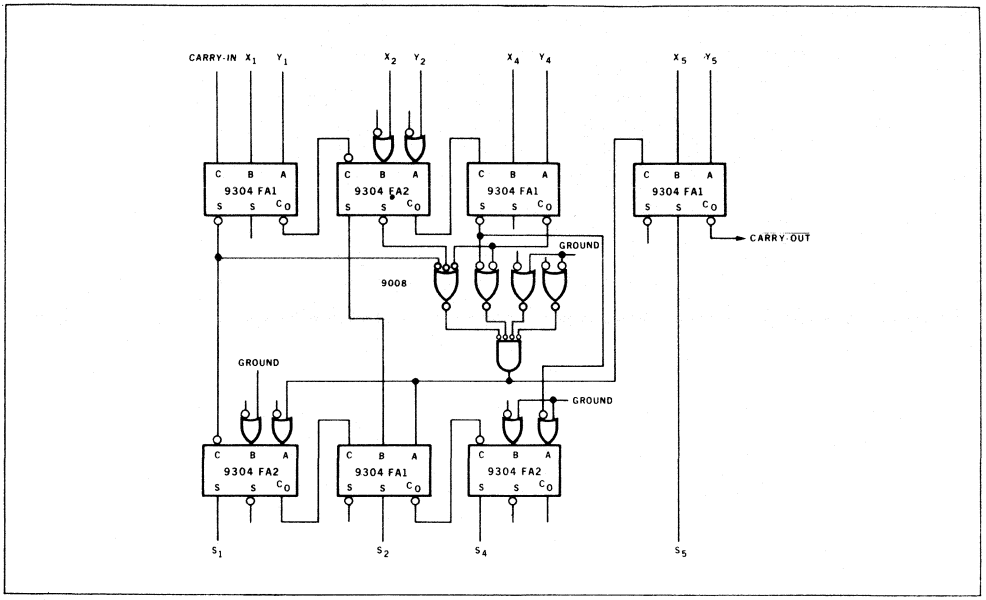


Fig. 10. BCD adder 5421 code positive carry in negative carry out.

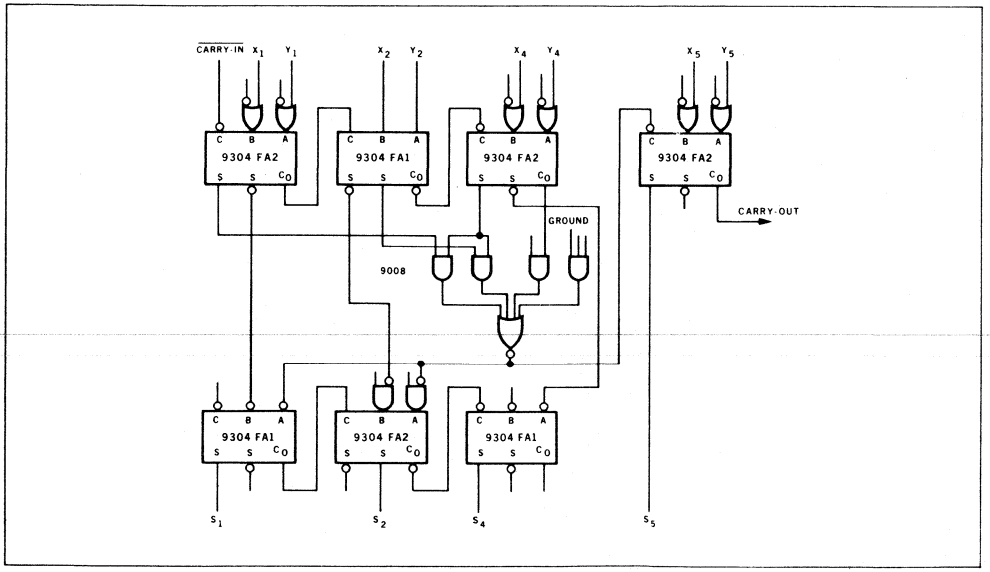


Fig. 11. BCD adder 5421 code negative carry in positive carry out.

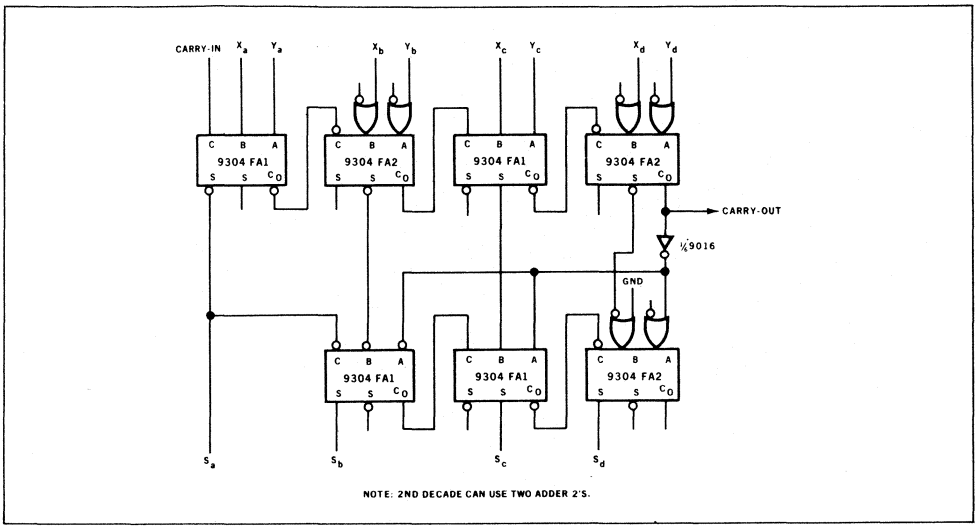


Fig. 12. BCD adder excess 3 code.

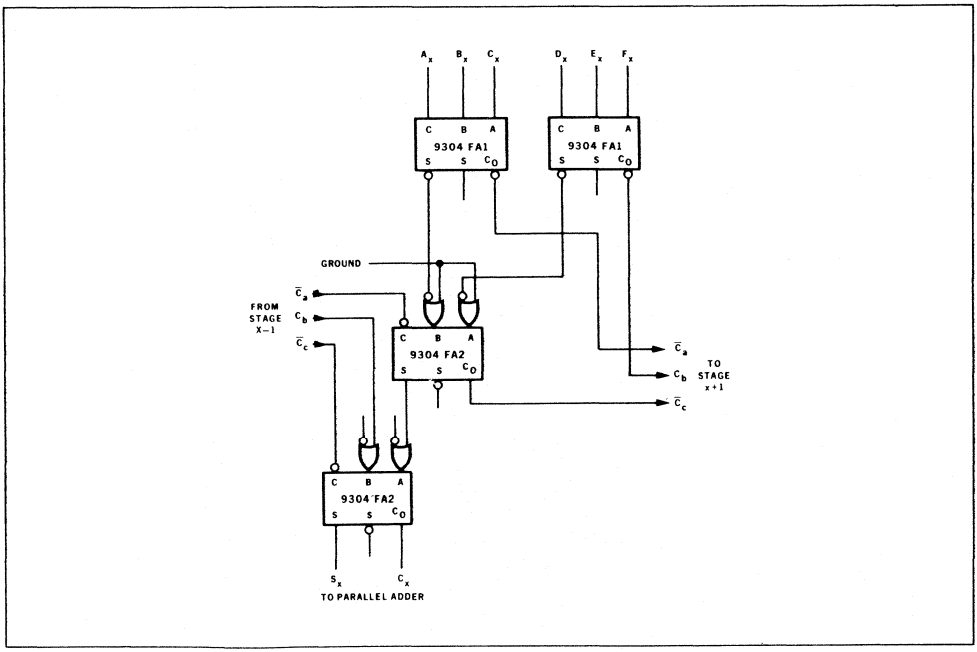


Fig. 13. Addition of six variables.

full adders which have three inputs to give two outputs (a partial sum and carry) which can then be combined with other partial sums and carries which can be added at a lower level using other full adders. Each carry is forwarded to the next upper stage, and carries from the next lower stage are incorporated with sums to produce further partial sums and carries. At each level three variables are reduced to two. Figure 13 shows a typical carry-save addition scheme for the addition of six variables at high speed. Four full adders per bit are used to produce a final sum and carry which can then be added using a high-speed parallel adder. For short word lengths, the 9304 Dual Adder using the ripple-carry technique may be suitable for this final parallel adder since the carry delay will be tolerable. However, for high-speed multivariable addition with large word lengths, a parallel adder with carry lookahead would be more suitable. The design shown in Fig. 13 takes advantage of the shortest path through the adders to produce the final sum and carry in approximately 53 ns. Active low inputs would produce active low final sum and carry. Other designs could produce active low final carry and sum for active high input variables and vice versa. The scheme can be extended to include additional input variables; however, as the number of input variables increases the propagation, delay and hardware required increases. For large word lengths and a large number of inputs, some intermediate storage scheme may have to be used to limit the integrated circuit package count to a reasonable level.

The carry-save method of adding several variables can be used to perform high-speed parallel multiplication.

Figure 14 shows the twelfth bit of a binary parallel multiplier for two 12-bit numbers. The TTμL 9002 quad two-input gates are used to switch the appropriate multiplicand

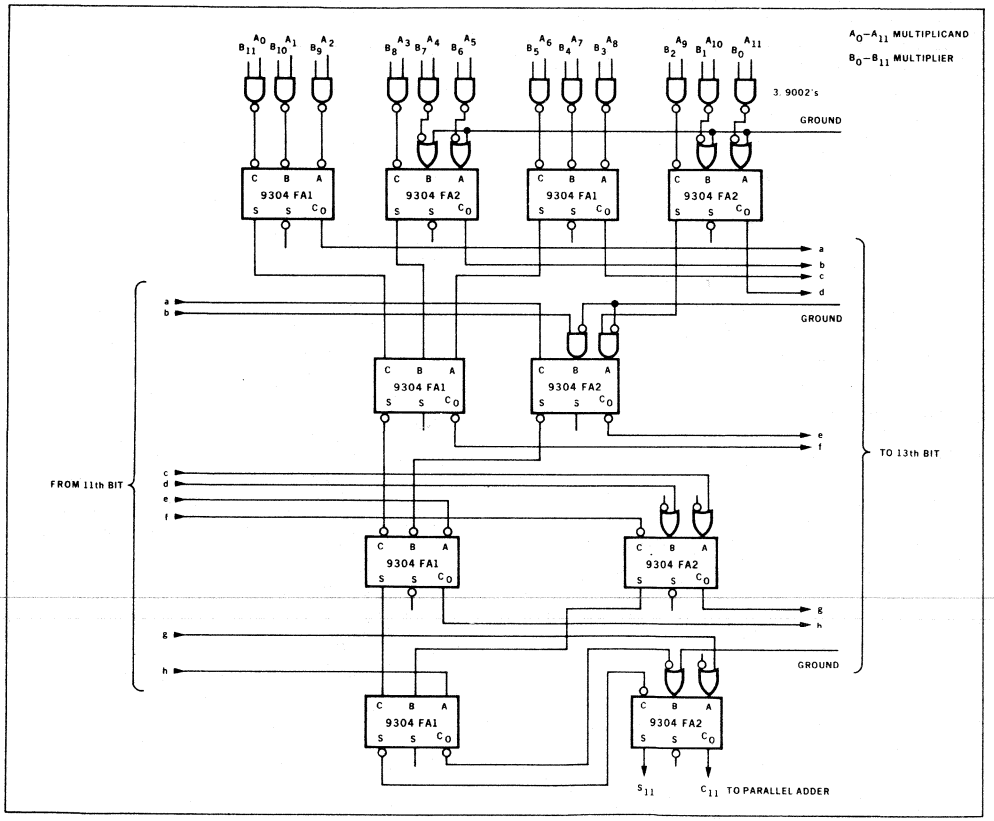


Fig. 14. Twelfth stage of multiplication using 12-bit multiplier and multiplicand.

digit selected by the correct multiplier digit. At stage 12 of the multiplier, the following additions are required:

$$A_{11} \times B_0 + A_{10} \times B_1 + A_9 \times B_2 + \ldots \ldots + A_0 \times B_{11},$$

where A is the multiplicand and B the multiplier.

The number of input variables varies at each stage, being maximum at the nth stage for an n-bit multiplier. The final sum and carry can be added in a high-speed parallel adder with carry lookahead which can neglect lower order terms if a single length product is required. The amount of hardware required for large word length multiplications can be limited by using the carry-save net in time sequence. Several passes through the carry-save net would increase the time taken for multiplication, but would hold down the integrated circuit package count to reasonable levels.

The carry-save scheme can also be used for division either by generating multiples of the divisor or by a reciprocal evaluation technique. The division process can be extended to produce high-speed square-root evaluation. The 9304 is extremely useful in special-purpose computers such as real time computation of Fourier constants by the Cooley-Tukey algorithm, thus providing real time digital evaluation of electromagnetic spectra.

Parity Checking and Generation

The remaining main use of the dual adder is in parity checking or generation. The sum output of the adder is

$$S = A \oplus B \oplus C .$$

This function is basic to parity checking. Figure 15 is a design of a 9-bit byte parity checker or generator using two dual adders to produce odd parity in approximately 32 ns.

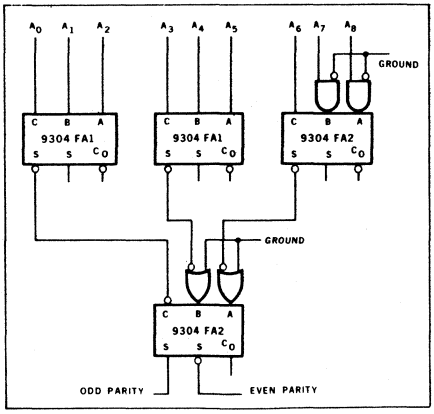


Fig. 15. Byte parity generation or checking.

An 81-bit version would produce odd parity in 64 ns. This high-speed method of parity checking will often be fast enough to stop incorrect data from being processed. The adders can also be used for Hamming code generation and checking. Figure 16 shows a design using three adders to generate the three parity check digits in a single error correcting Hamming code having four data bits. The corresponding Hamming code checker is shown in Fig. 17, where the 9304 is used

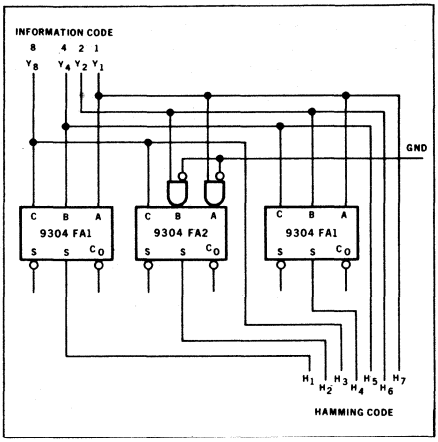


Fig. 16. Single error correction hamming code generation.

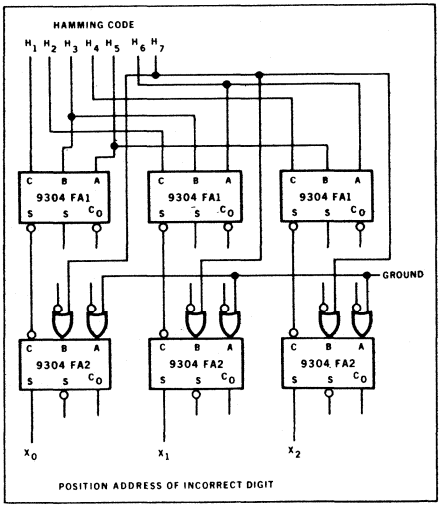


Fig. 17. Single error correction hamming code checking.

to generate the address of any existing single error in the 7-bit word. If, for example, the digit H_6 is in error, the output X will be 011, indicating that the sixth digit is in error and should be complemented.

Other Applications

The 9304 Dual Adder can be used for a variety of further applications. Figure 18 shows the device being used as a limit detector. The design is a ripple-through carry subtractor where only the carry out line is of interest. If the input carry is high, the output carry is high, if the input variable, A, is less than or equal to the other variable, B. This scheme is of interest for application in test equipment, integrated circuit tester and process control systems. A digital window can be established by using the same subtractor in time sequence and setting a flip-flop if variable B is outside the two ranges, A and C. The active low equivalence function can also be obtained by using an additional gate to determine when all the sum outputs are zero.

Figure 19 shows the 9304 being used to generate the address of the least significant "1" in a binary word. This leading "1" detector would be useful for priority gating systems in interrupt logic or for establishing program priorities in real-time digital computations. The design could be incorporated in the arithmetic logic unit of a computer. The outputs from the TTμL gates provide the active low outputs:

$$X_0$$
$$\overline{X}_0 X_1$$
$$\overline{X}_0 \overline{X}_1 X_2$$
$$\overline{X}_0 \overline{X}_1 \overline{X}_2 X_3$$

These outputs can be considered as inputs to TTμL gates acting as low active input OR gates to provide the appropriate address of the least significant "1" in the input word. The design can be extended for larger word lengths and it conveniently gives address "0" if no "1" is present in the word.

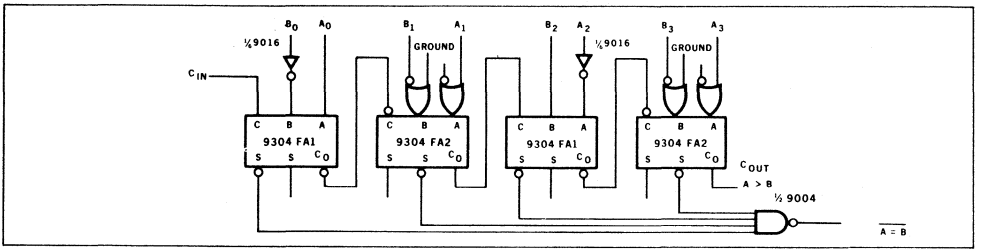


Fig. 18. Limit detector.

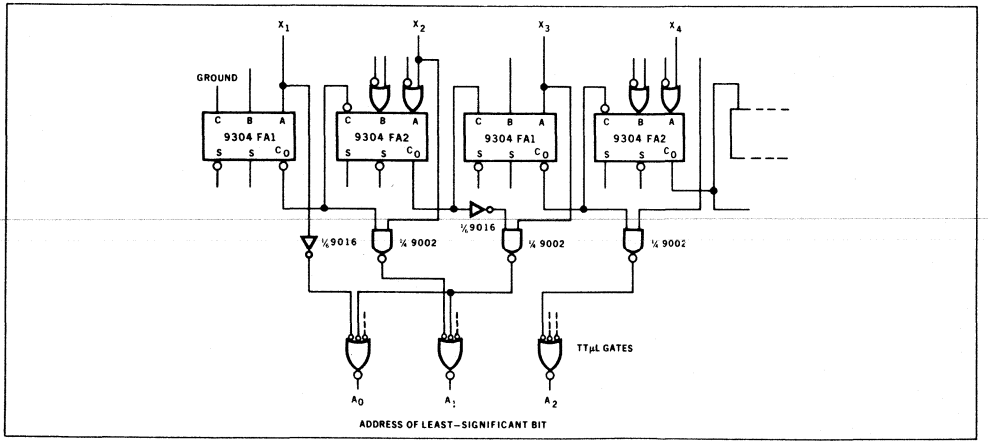


Fig. 19. Priority gating system.

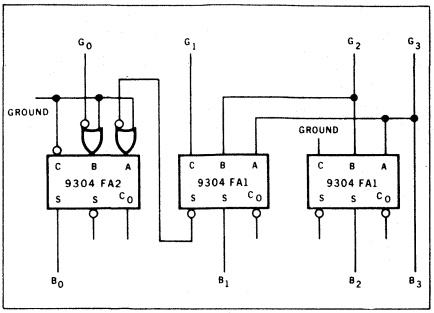


Fig. 20. Four-bit parallel gray to binary conversion.

Figure 20 shows the 9304 used as a code converter. Four digits in Gray code are converted to binary in parallel. The adders can be used for other code conversion schemes, particularly conversion of cyclic codes.

SUMMARY

This note has described the Fairchild 9304 Dual Adder and has shown how it may be used in a wide variety of applications. The device typifies the Fairchild complex integrated circuit approach to provide high-speed digital circuits with maximum functional capability. The 9304 Dual Adder is particularly attractive for use with other Fairchild CCSL complex function integrated circuits to reduce integrated circuit package count, interconnections, and packaging requirements, and to increase system reliability. Designers are encouraged to investigate the capabilities of the other Fairchild complex function integrated circuits for use in conjunction with the 9304 to produce a reliable, high-speed and more economical system than has been previously possible.

PHILOSOPHY AND DESIGN OF MSI

INTRODUCTION

As integrated circuits increase in logic complexity, there is a growing tendency toward custom logic design. On the other hand, considerations such as cost, system design time, circuit design, and inventory strongly suggest that if a set of complex standard digital building blocks were established, it would offer considerable advantages over a custom logic approach to system design.

This article discusses the philosophy, the logic design, and the semiconductor processing and packaging constraints of such a set of standard MSI (medium scale integration) circuits. The specific group under consideration (the 9300 family) consists of some 30 digital functions which can efficiently implement most logic in digital systems. The gate complexity ranges from about 20 to 100 gates.

REASONS FOR STANDARD MSI (MEDIUM SCALE INTEGRATION)

From both a performance and cost standpoint, it is highly desirable to maximize the packing density of components in a system. The simplest way to do this is to put as many components as possible on each silicon chip. In fact, as processing techniques have improved, manufacturers have done just that. The result has been lower function cost and increased system reliability.

There is, however, a limit to the number of components that can be placed on a chip, and this limit is determined by the yield and the selling cost. Beyond a certain component density, the yield begins to decline, and the selling price begins to rise. It turns out that for any IC there exists an optimum number of components that will minimize the *manufacturing* cost per component. This optimum number depends on the technology employed and keeps increasing each year.‡

‡It is possible to relate this optimum component count to the number of gates. This is done in Figure 1 where the relationship between manufacturing cost and number of gates is plotted for the years 1966 and 1968 and predicted for the year 1970. Note that these curves represent *manufacturing* costs and do not include the engineering cost of developing the IC.

As the complexity of an IC is increased to optimize the packing density, and hence minimize the manufacturing cost per component, two other factors come into play that may actually increase the total cost of the device: (1) the engineering development costs tend to rise; and (2) the number of IC's needed to implement a system decreases, the IC becomes more specialized, and the possibility of savings due to large-volume production goes down. Thus if one wishes to optimize packing density of complex IC's and at the same time minimize the total system cost, one must either

- reduce engineering development cost, or
- increase the volume of production.

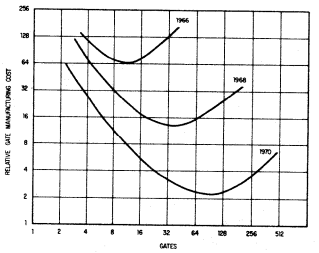


FIGURE 1 — The manufacturing cost of an I C is a minimum at a certain complexity. Each year this minimum occurs at higher complexities — indicating a learning process. Curves are shown for simple DTL gates; more sophisticated logic forms would compress the curves towards the y ordinate.

To reduce engineering development cost of complex IC's, many manufacturers have devised relatively inexpensive custom design techniques. Fairchild uses two such techniques: one involves a fixed array of gates (MICROMATRIX™), and the other a composition from a library of cellular building blocks (MICROMOSAIC™). Most of these custom techniques achieve cost savings by means of automation and computer-aided design. They have, however, one major drawback: they tend to sacrifice component packing density on the chip in order to provide logic flexibility.

FAIRCHILD
SEMICONDUCTOR

To increase the volume of production of complex IC's, it is necessary to design standard complex building blocks that can be used either (a) as general-purpose devices in a wide variety of applications, or (b) as specialized devices in specific high-volume applications. *These building blocks are called MSI (medium scale integration) integrated circuits.* As a group, the specialized MSI circuits are fairly easy to define; they include code converters, display decoders, etc. The general-purpose MSI circuits, however, are not so readily defined, and often a great deal of effort is required to determine what devices are needed to give a set of flexible, high-volume logic blocks.

TECHNOLOGICAL CONSTRAINTS IN STANDARD MSI

In practice several technological constraints limit the choice of standard MSI products, but even with these constraints, the number of possible logic configurations is still large. These constraints are: component count, the package, power dissipation, and crossunders.

Component Count

As described earlier, for a given process and technology at a specific time, there is some optimum number of components that should be placed on a chip. If this value is exceeded, then the design may be uneconomical.

Package

As a constraining factor, the package is perhaps second only to the component count. In order to keep costs low, one limits the number of different types of packages in a system. This in turn places a constraint on the number of package leads and, consequently, on the design of the product.

Power

The amount of power that can be dissipated in an IC is determined to a large extent by the package and the method of chip attachment. For high-speed IC's, both switching currents and power dissipation are high. Since device outputs must be able to drive high-capacitance loads, inputs are preferable to outputs when one is trying to increase logic capability without excessively increasing power consumption.

Crossunders

The majority of MSI devices now built use single-layer metal. The result is a yield loss due to: (1) the large amount of chip area required for crossunders, and (2) extraneous voltage drops caused by these crossunders. Although careful layout and circuit wizardry can reduce the number of these resistive connections, it might be preferable to design circuits that have a small number of crossunders to begin with or to use two-layer metal fabrication. The latter technique has no resistive connections and is easier to lay out, but because of the extra process required, it gives a higher yield loss.

MSI PHILOSOPHY

In order to make best use of the silicon chip area, a standard complex circuit should have a small number of inputs and outputs. If the number of pads on the chip is unduly large, then not only is the chip area being inefficiently utilized, but the package and circuit assembly costs are high, and the cost advantage of placing more circuitry on the chip is lost.

To make full use of IC technology, it is necessary to make the gate-to-pin ratio high. Functional blocks, such as adders and registers, are examples of logic circuits with high gate-to-pin ratios. Figure 2 shows the gate-to-pin ratio plotted against the number of pins for several logic circuits. As can be seen in the diagram, a single two-input gate gives a gate-to-pin ratio of 1/3, while an interconnected four-bit adder gives a ratio of 32/12 — an eightfold increase.

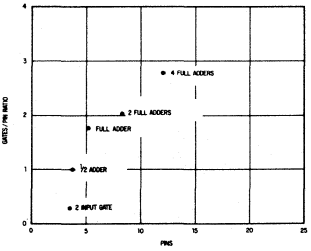


FIGURE 2 — As logic circuit becomes more functional, the gate-to-pin ratio increases, thus allowing considerable circuit complexity with a minimum number of pins.

The following groupings of functional devices are used to build digital systems:

(1) Stores — Storage of some form is essential for computation and for digital systems, and can take the form of registers, latches, and memory cells.

(2) Multiplexers — A multiplexer moves data from a series of lines to an output line or set of output lines.

(3) Demultiplexers — A demultiplexer, the converse of a multiplexer, moves data from a line or lines to a greater number of lines.

(4) Decoders — A decoder takes coded information and converts it to an uncoded form. Some decoders act as demultiplexers.

(5) Encoders — An encoder takes information and converts it to a coded form.

(6) Counters — A counter is a sequential circuit that controls the timing and the flow of data in a digital system.

(7) Operators and Decision Makers — This is possibly the most obscure area in the design of a set of logic building blocks. An operator or a decision maker operates on data in some way, such as addition, subtraction, or comparison.

The number of package types used for a set of functional building blocks should be limited to allow some form of standardization in printed circuit board and assembly. Once these package standards are chosen to give a low package, low assembly cost, and high reliability, a constraint has been placed on the function that can be designed. Since the ultimate objective is low system costs and maximum functional capability, all the package pins should be used. To increase the circuit's versatility, the pins left over after the basic function has been performed should be used to expand the functional capability as much as possible.

Since the MSI family has been designed as a set of building blocks, it is important to produce the function so that it can be self-extending. Thus, a 4-bit comparator should be designed so that an 8-bit or multiple-bit comparator can be produced

by combining two or more 4-bit comparators, preferably without extra discrete gates; this also places a constraint on the form of the device produced and on the logic configuration. Sequential circuits such as registers and counters should be made synchronous; although this uses additional active circuitry and increases chip area, the advantages of high operating speed, ease of logic, and system design are extremely significant.

As a logic set, the products must interface with a minimum of discrete gates. The logic circuits should be designed as a compatible set, and the polarity of enables, clocks, and other inputs and outputs must be chosen for maximum performance. Buffers should be used on the silicon chip to lower the loading on the gating, clock, enabling, and other control inputs. At first, this might seem an extravagant use of active chip area, but several advantages are gained by using on-chip buffers. First, the fan-in is reduced, thereby decreasing the number of discrete gate buffers in a system. Second, the on-chip buffers do not drastically increase the chip size, and since the buffers must be provided somewhere in a system, it is better to place them on the chip where they have high speed and low power and can be designed to drive the known fan-out. (A discrete gate buffer must be designed for a worst-case fan-out, noise margin, etc., and is therefore slow.) This scheme of incorporating high speed on-chip buffers can be extended to the placing of complete decoders on the chip. Again, the chip area used for this purpose is generally only a small percentage of the overall chip area, but the advantages of more function and packaging more than offset the extra chip size. Placing decoders on the chip has important system consequences: it substantially increases the logic power of circuits, and it results in a greater logic flexibility.

If the complex logic blocks are built using an optimized circuit approach, a minimum-area circuit results. Since a large amount of circuitry in these complex devices does not have to drive off the chip, the circuitry may consist of low-level circuits that are buffered from external noise and therefore do not require the large d-c noise margins that are required of circuits used as inputs or outputs (Figure 3). These low-level circuits have fewer components and consume less power than high-level circuits. They allow more circuits to be placed on a chip, they are faster, and they permit the building of functional blocks. Active pullup outputs should be used where necessary for high speed. OR tie capability should be provided where speed is not essential or where the use of the wire OR significantly increases logic capability.

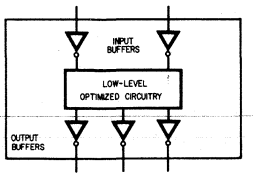


FIGURE 3 – Standard MSI circuits allow digital function to be built around a low-level optimized circuit concept and permit the use of buffers to reestablish input and output logic levels.

MSI PRODUCT DESCRIPTION

Now that we have outlined the philosophy of standard MSI and discussed the constraints imposed by the process and packaging, let us see how to go about defining an MSI circuit.

A common element in many systems is a shift register. Shift registers are used for serial storage in computation, encoding, checking, etc. If a shift register is to be built in a standard package (say 16 pins), two pins are taken by the power supply and 14 pins remain as input and output to and from the chip. The number of stages in the shift register is undefined. Three pins must be used initially to provide for clock, data-in, and data-out (Figure 4A). If a high-speed device is required and it is decided to make the circuit more useful by bringing out the outputs of intermediate stages in the shift register, then the power constraint comes into play and effectively limits the number of stages that can be placed in the 16-pin DIP package to four or five. Rather than make a five-stage register, it would seem more suitable (1) to build a four-stage shift register (since four is a more useful modular block) and (2) to bring out the negation of the last stage in addition to the four assertion outputs. Bringing out the negation of the last stage allows greater functional use and often saves an inverter. For this reason, the design illustrated in Figure 4B has been developed. Note that there are still free pins available. Since inputs do not take up as much power as outputs, one should try to find input configurations that would be useful and would add to the shifting function of the register. An obvious extension is to incorporate a parallel load facility over the four register stages. This means five additional pins – four for the four parallel inputs and one for the mode control. The design is shown in Figure 4c. The circuit of Figure 4d illustrates another advantageous facility – an asynchronous reset capability with the last free pin providing a $J\overline{K}$ shift input configuration. Such a facility enables (1) a single-line D input by tying the $J\overline{K}$ inputs together, and (2) a toggle action by making J high and $\overline{K}$ low.

The shift register described above is the MSI 9300, a 4-bit device that is used in numerous digital systems for a multitude of applications. In order to facilitate system design, the register parallel load facility is synchronous. Many of the MSI sequential building blocks in the 9300 series have this synchronous parallel load capability which enables them to avoid race conditions and reduces the number of extra flip-flops needed in complex control systems. Another important point is the polarity of enables, inputs, and outputs. For example, the fact that the polarity of the parallel enable control on the 4-bit shift register is active low means that the device will require fewer extra gates or inverters when used in conjunction with discrete inverting gates or with the other MSI 9300 series devices.

When all the stages are brought out for logic use, the constraint of power fixes the number of stages in the 9300 shift register to four. If, however, all the outputs are not brought out to pins, then a longer shift register can be produced. The 9328 dual 8-bit shift register is such a circuit. Its main constraints are component count and chip size. If more than four shift register stages were placed on the chip and only a small number of stages brought to the outside world, the shift register would be useful as a serial store. For serial storage a reasonable register size is 16 bits. Thus since two 8-bit shift registers offer more design flexibility, the 9328 was designed as a dual 8-bit shift register. The assertion and negation of the last stage of each register are brought out, and the remaining pins extend the functional capability of the device. A 2-input multiplexer is incorporated at the input of each 8-bit shift register, allowing data to be entered from two different sources under control of a separate source control for each register. In addition, the registers have provisions for a shift enable control and a common master reset. In the 9328, as in the 9300, all package pins have been used to give the maximum logic flexibility and function capability consistent with the integrated circuit constraints imposed.

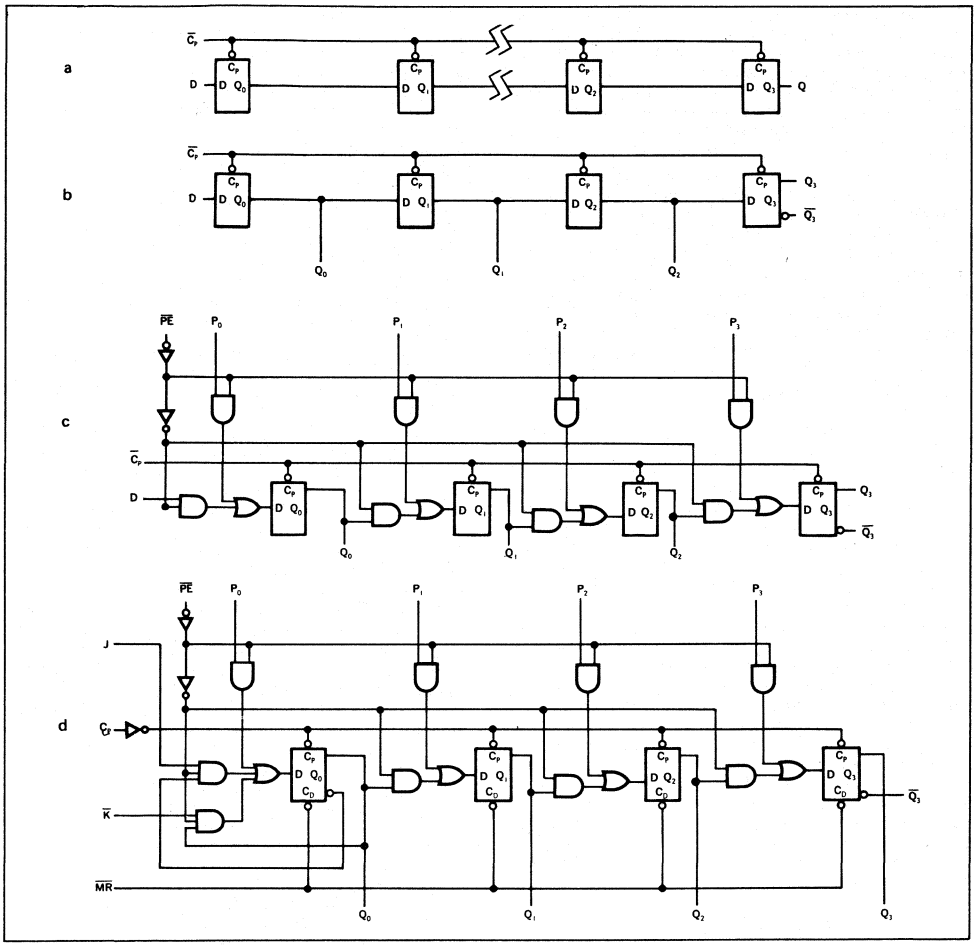


FIGURE 4 — The figures show the logic development in the design of a typical MSI circuit from the basic minimum function to final form. Maximum function capability is achieved by using all package pins.

THE 9300 FAMILY

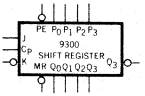
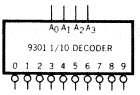
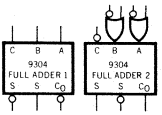
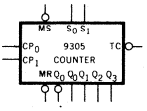
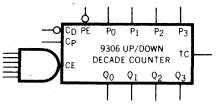
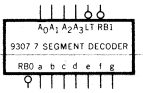
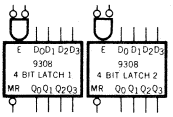
The 9300 set of logic elements, their logic block symbols, and a simple description of each element are given in Table I. The symbology follows for the most part the MIL-STD-806B representation of logic blocks as an extension of the usual gate symbols. As in the gates, active low inputs and outputs are designated by a small circle indicating that the logic block performs the given function when that input, in conjunction with others, is active low (that is, at the algebraic lowest voltage of the two used in the system to express the two logic states). In all but one instance, inputs enter the block from the top and left, and outputs leave from the right and bottom. The only exception is in the sequential circuits where the master reset input is at the bottom left corner of the block. These logic symbols assist logic design, make it easier to understand how these devices are used with one another, force the designer to think at the functional building block level, and greatly reduce design and engineering support time.

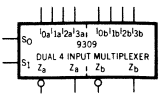
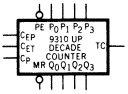
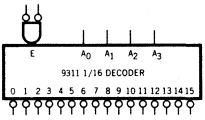
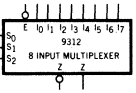
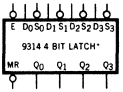
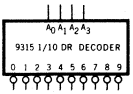
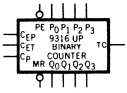
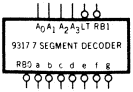
Each logic block, e.g., the AND gate, has at least one logic equivalent. Figure 5 shows logic equivalents of the 9312 multiplexer block. All diagrams describe the functional capability of the device. Normally, the active high inputs are used, but the active low input configuration can also be used to advantage.

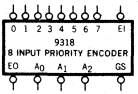
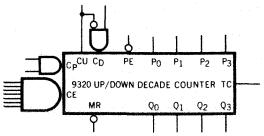
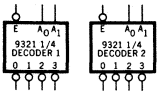
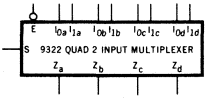
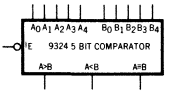
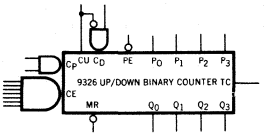
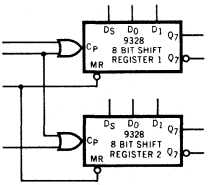
Note in Figure 5D how altering the polarity of one of the select inputs changes the order of selection of data inputs. For the 8-input multiplexer, there are 16 logic equivalents, all of which could prove useful. In these logic equivalents the circuit is the same but the logic form is different. For example, if a 3-stage binary counter controls input selection and only the

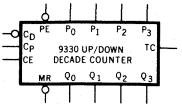
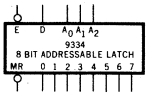
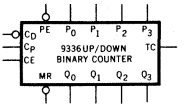
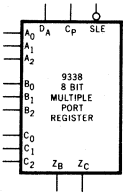
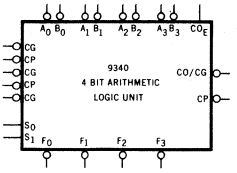
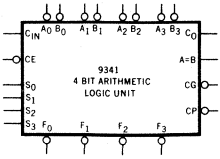
TABLE I MSI LOGIC BLOCK SYMBOLS

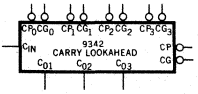
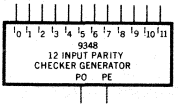
The symbols used to express the logic function of the MSI blocks are shown below together with a short description of each element. The symbology uses small circles to denote polarity of active levels and appends gate symbols to the block where required for clarity.

	9300	4-Bit Shift Register having all assertion outputs and complement output of last stage; master reset facility; $\overline{JK}$ input configuration and synchronous parallel load facility.
	9301	1-out-of-10 Decoder accepting four BCD 8421 code inputs and providing mutually exclusive active low output corresponding to input code.
	9304	Dual Full Adder, two full adders having sum and its complement and carry output; second adder has provision for active low or high operant inputs.
	9305	Universal Counter which can be connected to provide division by 2 x 4, 5, 6, 7 or 8. Counter is split into two parts, a divide by 2 and a synchronous programmable divide by 5, 6, 7 and 8 which is under control of S_0, S_1 inputs. Device can be used either in a binary or 50% duty cycle mode. Overriding master set and reset signals are provided. An active low terminal count output allows cascading of counters without extra gates.
	9306	Up/Down Decade Counter, a synchronous up/down BCD 8421 code counter; single line up/down mode control and six input wide count enable AND gate and single line terminal count; synchronous parallel load facility.
	9307	7-Segment Decoder accepting BCD 8421 code input and producing corresponding outputs for driving 7-segment display for numerical display; lamp test input and provision for suppression of insignificant zeros automatically; outputs for segments are active high.
	9308	Dual 4-Bit Latch with two separate 4-bit latches having assertion outputs, asynchronous reset facility and two-input active low AND enable.

	**9309** Dual 4-Input Multiplexer switching two bits of data in parallel from two 4-bit data sources to the appropriate outputs in parallel, both polarities of outputs available with internal decoding for bits in common.
	**9310** Up Decade Counter, synchronous decade BCD 8421 code counter having two count enable inputs giving lookahead facility over several decades without extra gates; terminal count output, asynchronous reset, and synchronous parallel load facility.
	**9311** 1-out-of-16 Decoder accepting binary input and providing active low output at appropriate output. Also has two-input active low enable AND gate.
	**9312** 8-Input Multiplexer with facility to switch any of eight data sources to output; complementary outputs available; active low enable input and internal decoding.
	**9314** 4-Bit Latch having D and S inputs on each latch. Latches have active high outputs, a common active low enable and master reset. Each latch can be used as an active-low, set-reset latch with reset override.
	**9315** 1-out-of-10 Driver Decoder used for driving cold cathode tubes directly; unused code gives blanking capability.
	**9316** Up Binary Counter, binary version of 9310 up decade counter.
	**9317** 7-Segment Display Converter, active low output version similar to 9307.

	9318	8-Input Priority Encoder producing three address outputs; inputs are weighted in priority when two or more inputs are active; highest numbered input takes priority; facility is made by input and output enables for expansion.
	9320	Up/Down Decade Counter, synchronous decade counter having up/down facility; seven-input-wide count enable, AND gate, single line terminal count, synchronous parallel load facility and asynchronous master reset input.
	9321	Dual 1/4 Decoder having low outputs and active low enable on each decoder. Device can also be used as a dual 4-output demultiplexer by using enable line as data input.
	9322	Quad-2 Input Multiplexer with active high outputs, active low common enable and common select line.
	9324	5-Bit Comparator compares two 5-bit parallel words to give outputs A < B, A > B, A ≡ B; device can also be used as 4-bit comparator with extension inputs.
	9326	Up/Down Binary Counter, binary version of 9320.
	9328	Dual 8-Bit Shift Register having assertion and negation of last stages as outputs; 2-input multiplexer at the input of each register with input select control, active low shift enable, common clock and master reset facility.

	9330	Up/Down Decade Counter, a synchronous decade counter having single line up/down control, synchronous parallel load facility, count enable input, single line terminal count, and asynchronous load facility. Counters can be cascaded by connecting terminal count to next counter enable.
	9334	8-Bit Addressable Latch which stores single line data in the addressed latch. Device has active low enable and common master reset. When master reset and enable are both active device acts as a demultiplexer.
	9336	Up/Down Binary Counter version of 9330.
	9338	8-Bit Multiple Port Register which stores single line data in the register bit addressed by the A field on receipt of a clock pulse. The B and C fields give two independent outputs from the eight register bits. The device can be used either as a master slave flip-flop register or as a multiple port latch block by continually enabling the slaves.
	9340	4-Bit Arithmetic Logic Unit having subtraction, addition, AND and EXOR capability under control of inputs S_0S_1, plus a built-in internal carry lookahead; carry in and carry out networks give maximum speed without additional gate packages; the device has only seven gate delays for subtraction for word lengths of up to 16 bits and requires only two additional gate delays for each additional 12 bit increment in word length.
	9341	4-Bit Arithmetic Logic Unit controlled by CE, S_0, S_1, S_2 and S_3. When carry is disabled,unit generates any function of two variables on two 4-bit parallel words A, B. When carry is enabled, unit performs operations such as Add, Subtract and Double A. Unit has built in carry lookahead and carry out, carry generate and carry propogate as outputs. For high speed,arithmetic device is used in conjunction with 9342 Carry lookahead. For slow speed operation, carry out signal allows unit to be employed in ripple carry mode. Provision is made for comparison of the two 4-bit parallel words A, B by A = B output.

	9342	Carry lookahead logic used in conjunction with 9340 or 9341 arithmetic logic unit. Device accepts active low carry generate, propogate signals and active high carry in and provides the necessary carry outputs for four 9341 devices. Active low carry propogate and generate output signals for next higher level or lookahead are also provided allowing 9340 and 9341 to be used together with 9342 to form extremely fast large word length adder/subtractors.
	9348	12-Input Parity Checker/Generator having even and odd parity over the 12 inputs as outputs.

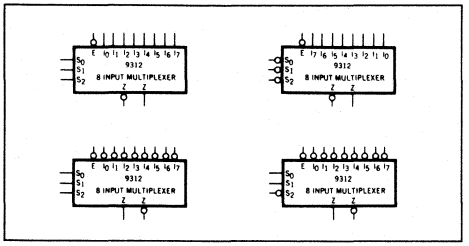


FIGURE 5 – MSI functional blocks often have several logic equivalents. The multiplexer performs the same function with active high or low inputs and any combination of active high or low select input combinations.

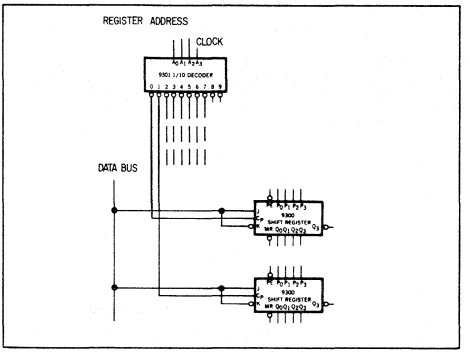


FIGURE 6 – MSI functions are designed as a compatible set, thereby minimizing the number of discrete gates required in a system. The figure shows the decoder switching the clock to the appropriate register in a bank of registers. Active low outputs of the decoder are compatible with clock requirements of all MSI sequential circuits.

negation outputs are available, there is no need to place inverters between the counter outputs and select inputs; rearrangement of the input wires will accomplish the same purpose. This can be seen most clearly by considering the device from a functional viewpoint as opposed to examining the detailed logic diagram. When an input with a circle is connected to an output with a circle, the two circles logically cancel. This actually is an active low output driving an active low input, which is logically identical to an active high output driving an active high input.

The design of the 9300 MSI family is based on the philosophy outlined earlier. For example, the 9301 and 9311 decoders have active low outputs for speed and power considerations, and the polarity of clock inputs on the sequential logic circuits have been chosen so that the decoders can act as a clock demultiplexer (Figure 6). The polarity of enable and control inputs allows a logic block to be selected via the decoder's active low outputs without the use of additional gates (Figure 7).

At first it is not apparent that MSI offers any advantages in areas of control and non-standard logic. It turns out, however, that several of the MSI building blocks are powerful universal logic circuits.[2] Consider half of the 9309 dual 4-input multiplexer: If the two select lines are regarded as inputs for two variables and the multiplexer input configuration as a function of a third variable, the output can be any one of the possible $2^8 = 256$ configurations of three variables, allowing half of the 9309 to implement any Karnaugh map of three variables. Any

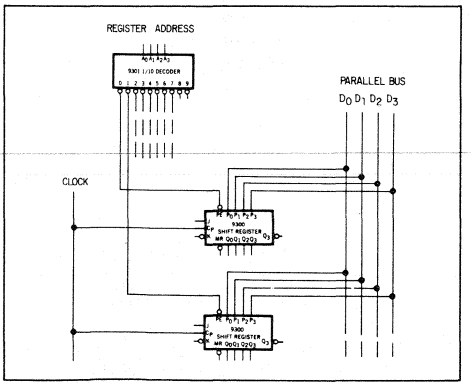


FIGURE 7 – Another example of logic compatibility. The decoder is used as a select control for the parallel loading of a register from a bank of registers.

logic function of variables can be expanded with respect to any "n−1" of the "n" variables. In the three-variable case: $f(x, y, z) = \bar{x}\,\bar{y}\,f(0, 0, z) + \bar{x}\,y\,f(0, 1, z) + x\,\bar{y}\,f(1, 0, z) + x\,y\,f(1, 1, z)$. The functions (0, 0, z, etc.) are functions only of the values z, $\bar{z}$, 0 or 1. Figure 8 shows a truth table, the three-variable Karnaugh map and its realization with 1/2 of a 9309 dual 4-input multiplexer. The 9312 8-input multiplexer can implement any Karnaugh map of four variables, and several multiplexers can be interconnected to extend the capability to a large number of variables. The 9301, 9311 decoders can also be used as general-purpose circuits since they are effective Minterm generators, and different Minterms can be summed using an active low OR gate[3] (Figure 9). The advantage of the decoder over the multiplexer is that it is often more efficient, when considering multiple outputs, to produce Minterms that are then summed rather than to devote one complete multiplexer or more to each output. A mixture of decoders and multiplexers that produce a Boolean function with "m" inputs and "n" outputs is frequently more economical than a circuit that has only decoders or only multiplexers.

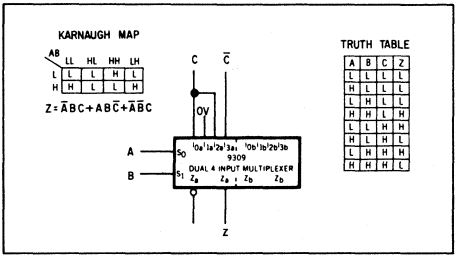


FIGURE 8 — Multiplexers can act as universal function generators generating random logic functions by connecting inputs to additional variable or appropriate logic level. The 9309 multiplexer can generate any two logic functions of three variables with two variables common to the two functions. The 9312 multiplexer can generate any logic function of four variables.

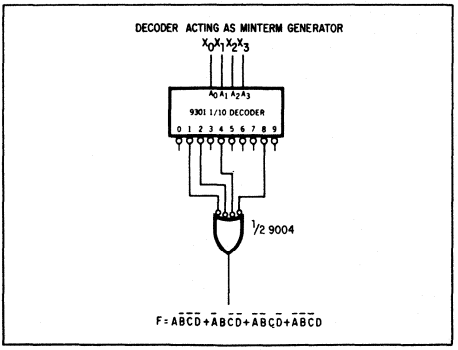


FIGURE 9 — A decoder can also act as universal function generator by summing appropriate minterms (outputs) with active low input OR-gate.

SYSTEM DESIGN USING MSI

The MSI building blocks are ideal for building systems where there is a large amount of standard logic format such as storage and multiplexing. In such systems MSI can be used efficiently and constitutes most of the IC package count. MSI building blocks will not show their full capability if retrofitted into existing systems or incorporated into systems designed around present discrete gate logic circuits. Systems built in this manner will have a lower package count and fewer economic advantages, but for best results, the system design should be built around the MSI building blocks themselves. When this is done, the true value of MSI will become apparent: system design will become easier, faster, and more modular; system design will be similar to a block diagram design; and new avenues of approach to problems will be apparent. The designer should think about minimizing the number and cost of the logic blocks used in the system — he should not think in discrete gate terms. Some logic designers may feel that MSI is in competition with their occupation. In reality, it raises their design capability and thinking to a higher plane.

Although MSI can provide all the logic circuits required in a system, the control (a non-modular, non-standard section) can often be more economically performed with discrete gates, read-only memories, or a customized array approach. The array approach is very useful when a circle can be drawn around a section of non-standard logic that has (1) a reasonable gate-to-pin ratio and (2) a number of gates equal to or less than that available on an array. The most economical system will often employ all the various types of integrated circuits: MSI, custom arrays, and discrete gates. All these circuits are logically and electrically compatible. In the future, instead of packing the individual chips in separate packages, one will be able to connect them on a ceramic substrate having multilayer connections to form a hybrid circuit. In fact, bipolar LSI of several hundred gates will probably be implemented in this hybrid form long before a true monolithic version is available. The one big advantage of this technique is that (apart from the few purely custom chips) the chips are produced in high volume and are therefore low-cost items. Consequently low-cost custom subsystems with high performance can be built within a relatively short turn-around time.

ADVANTAGES OF MSI

The advantages of an MSI system design, compared with a discrete gate version are similar to the advantages of an IC system compared to a discrete component version: (1) lower system cost, (2) higher packing density, (3) fewer interconnections, PC cards, connectors, wire wrap, and soldered joints, (4) lower IC package count, and (5) greatly increased reliability. Easier system extension is possible since extensive use of MSI forces the designer to build a more modular digital system. Design time, check-out, supporting effort, and maintenance are reduced considerably. More system functions that are traditionally performed by analog methods can now be economically performed digitally with a consequent increase in stability, ease of control, and system performance. If only a few systems are to be built, then a straightforward, direct implementation with MSI can be designed quickly and easily. If on the other hand a large number of systems are to be built, and cost considerations become important, then expert logic designers can be called upon to produce an extremely efficient design.

APPLICATIONS OF MSI

The best way to illustrate the power of a logic set of building blocks is to use them to build a variety of systems. The design problem now centers on a logic functional approach rather than a gate approach. Figure 10 shows a logic diagram of a 4-bit parallel high-speed computing unit incorporating MSI blocks. Owing to the modular form of the desired function, the design has no requirement for discrete gates. The unit can perform at

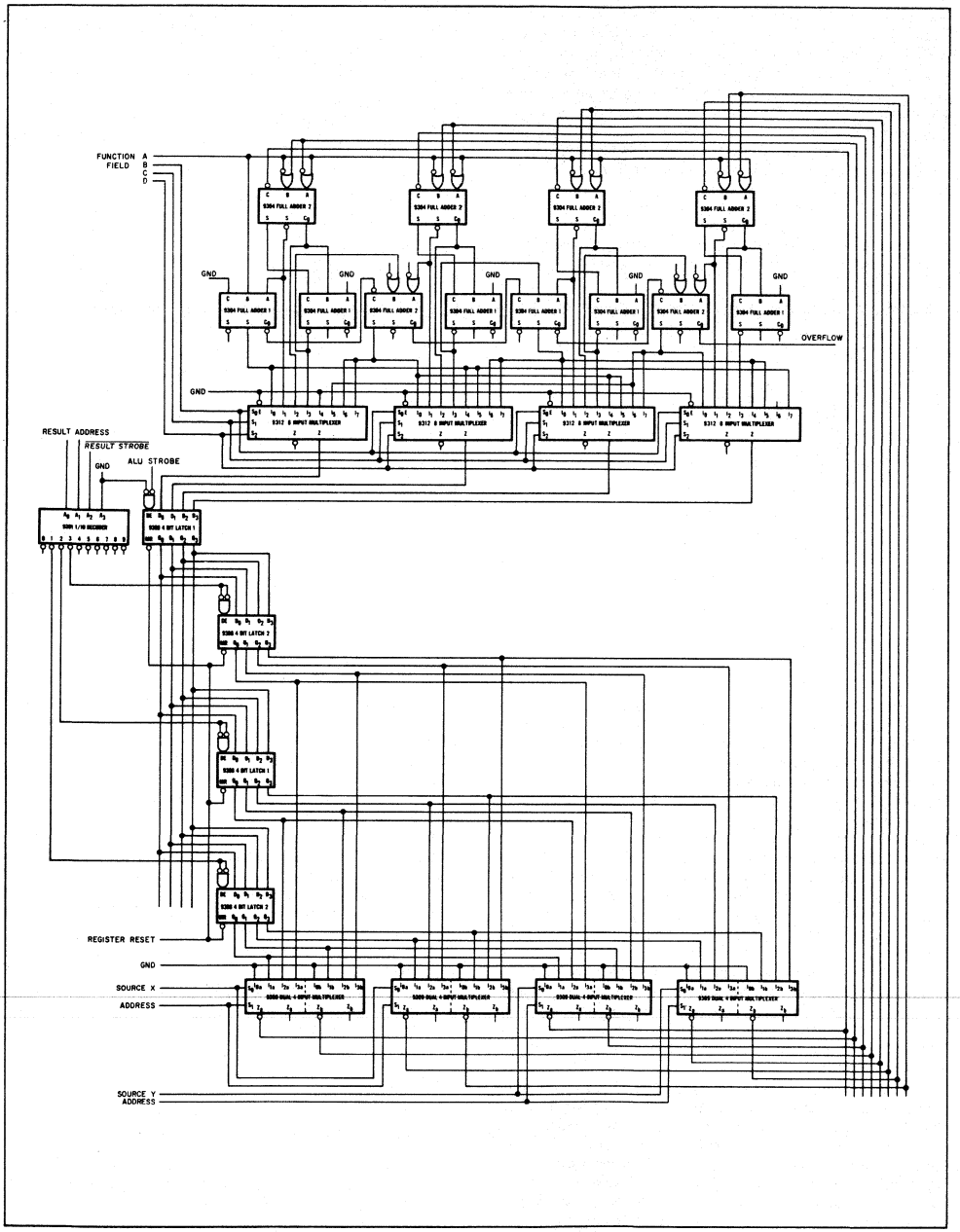


FIGURE 10 — The above design is a four-bit arithmetic logic register unit using MSI. Instructions are obeyed in a three-address format, any two registers being operated on the result sent to any register. Functions which are shown in Table II include add, subtract, AND, OR, shift, etc.

high speed the 16 arithmetic and logic functions (as given by Table II) on data selected from any two of three working registers, and send the result to any one of the working registers. Only 17 integrated circuits are required for this 4-bit parallel block, and only an additional 16 MSI IC's are required for each additional 4-bit clock. Arithmetic operation execution times are dependent on the word length, but the design, even though incorporating a ripple carry adder, is fairly fast, giving typical arithmetic cycle operation times of 3 MHz with a 24-bit parallel word.

TABLE II.

This table gives the function code required to implement the various arithmetic and logic operations possible using the ALU design of Figure 10.

Function Field A B C D	Operation
L L L L	x ADD y
H L L L	x SUBTRACT y
L H L L	$x \oplus y$
H H L L	$x \oplus \bar{y}$
L L H L	$x + y$
H L H L	$x + \bar{y}$
L H H L	$x \cdot y$
H H H L	$x \cdot \bar{y}$
L L L H	(x ADD y) 2 arithmetic
H L L H	(x SUBTRACT y) 2 arithmetic
L H L H	(x ADD y) 2 logical end around
H H L H	(x SUBTRACT y) 2 logical end around
L L H H	(x ADD y) 2^{-1} arithmetic
H L H H	(x SUBTRACT y) 2^{-1} arithmetic
L H H H	(x ADD y) 2^{-1} logical end around
H H H H	(x SUBTRACT y) 2^{-1} logical end around

In this processing unit design, it can be seen that efficient use of MSI forces a straightforward modular design whose control functions are performed via a set of encoded lines and not via a single line that controls each individual function. The design also shows how apparently difficult problems are solved by manipulation of the MSI blocks. The first-level adder in the processor forms a partial sum and carry; the control wire A determines whether the input operant B is either active high or low; and the partial sums and carry are added at the third level in a ripple carry adder to produce the sum or difference under control of this A input of the functional field. Various other logic functions are provided by means of combinations of the sum and carry functions, e.g., the second level adder acts as an exclusive OR circuit from which the OR function is produced. The shifting capability is produced by multiplexing the appropriate sum signals on the output bus with an 8-input multiplexer. For storage, the dual 4-bit latches act as a single master/multiple slave flip-flop scheme where the slave latch receiving the information is activated by using a decoder as a strobe demultiplexer.

The second application shown in Figure 11 is a time-sharing display scheme featuring MSI circuits. In this design the eight decade counters count up for the required time period, and then the count value is shifted in decades (using the parallel load facility on the counter) into two shift registers arranged in eight parallel BCD 4-bit words. The information is displayed by driving a single 7-segment display decoder at the output of the shift registers. While the information is being displayed by multiplying and recirculating, the counters can count up for another time period. Control of the multiplexing can be performed with an additional counter and decoder. This entire scheme requires far fewer IC's than a design using discrete IC's.

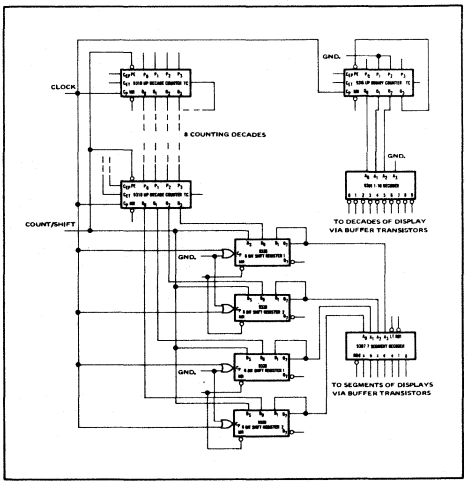


FIGURE 11 – In a typical display application, the diagram shows MSI used in a display scheme where eight digits of BCD informations are time multiplexed through a display decoder. Control of the sequence is performed by a 9301 1/10 decoder.

CONCLUSION

As new applications are found for digital integrated circuits and processing improvements are made, the number and complexity of standard MSI building blocks will continue to grow. It is essential to design these larger logic blocks not only for electrical compatibility, but also for logic compatibility, using the natural advantages of IC technology and avoiding as much as possible the disadvantages of IC design. This can only be realized with a very close liaison between system and logic designers and the corresponding IC engineers. As subsystems increase in complexity, there is a tendency to design custom circuits. These may well be more efficiently implemented with a mixture of MSI standard and custom circuits than with one very large expensive LSI circuit. As IC technology improves, and as larger chips capable of incorporating large numbers of gates with reasonable yield can be produced, standard subsystems will be devised to allow further cost reductions and to extend MSI into LSI, and existing MSI and gates will be used to glue these larger subsystems together.

REFERENCES

1. Earle, J., "The Impact of Microelectronics – Special Report," *Electronic Design*, December, 1964.
2. Tang, C. K., and Yan, S. S., "Universal Logic Circuits and Their Modular Realizations," Proceedings of the 1968 Spring Joint Computer Conference.
3. Ghest, R. C., "Applications of the CCSL 9301 Decoder," Fairchild Application Bulletin, December, 1967.

AN MSI APPROACH TO MULTIPLEXING MODE OPERATION OF A LOW-VOLTAGE VACUUM TUBE 7-SEGMENTED NUMERIC DISPLAY

INTRODUCTION

The display industry has been searching constantly for reliable and inexpensive display devices. This is especially true in the numeric display field. The most familiar device in the market so far has been the Nixie* type tube which for years has been monopolizing the numeric display application. Recently a new low voltage, vacuum tube type display device has been introduced. In this device the digit is built up of seven phosphorescent bars arranged in a figure eight pattern. Each bar is an anode that will glow when 10 to 60 volts d.c. is applied to it. The cathodes are two almost invisible wires strung vertically between the segments and the viewers. Tubes of this type are available at present from Tung-Sol (Digivac), NEC and Itron.

Generally one decoder plus the associated drivers are required for each digit to be displayed. For a multiple digit display, this constitutes an appreciable circuit cost. One solution is to multiplex (time share) one decoder and one set of drivers, switching at a sufficiently high speed to provide flicker-free operation of all the digits.

This time sharing technique is commonly used in multi-digit displays with Nixie tubes.

This paper describes how multiplexed operation of 8 Tung-sol, or NEC tubes can be implemented with MSI devices. Multiplexing of a different number of digits is also discussed.

* Registered Trademark of Burroughs Corporation

CIRCUIT DESCRIPTION

The scheme consists of the six function blocks shown in Figure 1;

1. input registers 2. input multiplexers 3. decoder 4. drivers 5. multiplexing timing and control 6. display tubes. Each of the functional blocks is described in the following sections.

1. INPUT REGISTER

Four dual 4-bit latch MSI 9308's are used to store 8 x 4 bit BCD inputs D_0, D_1, D_2, and D_3. Data is entered into the latches when a load command (low) is applied to the enable inputs. As long as this logic condition exists, the outputs if each latch, Q_0, Q_1,Q_2, Q_3 will follow the inputs D_0,D_1,D_2, and D_3. All Q_0 outputs are connected to the inputs I_0, I_1, ..., I_7 of the first 931 multiplexer; all Q_1's to the second; and all Q_2's to the third multiplexer, and so on.

2. INPUT MULTIPLEXER

Four 9312's connected to the input register as described make up the input multiplexer. The 9312 is a logical implementation of a single pole 8-position switch with the switch position

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controlled by the state of three select inputs S_0, S_1, S_2. Both assertion and negation outputs are available. The enable input (E) is active low. The logic function provided at the outputs is shown in the truth table (Table 1), and with the Boolean equation:

$$Z = \bar{E}\,(I_o\bar{S}_0\bar{S}_1\bar{S}_2 + I_1S_0\bar{S}_1\bar{S}_2 + I_2\bar{S}_0S_1\bar{S}_2 + I_3S_0S_1\bar{S}_2 + I_4\bar{S}_0\bar{S}_1S_2 + I_5S_0\bar{S}_1S_2 + I_6\bar{S}_0S_1S_2 + I_7S_0S_1S_2)$$

By applying all $S_0S_1S_2$ logic combinations in sequence the output of each multiplexer will represent sequentially the binary bits corresponding to the decimal digits stored in each of the eight input latches.

3. DECODER

The 9307 is a decoder designed to convert 4 line BCD inputs into seven line outputs suitable for seven-segment display devices. It has an active low input lamp test which overrides all other inputs and lights up all 7 segments to enable a check of possible display malfunctions.

4. DRIVERS

72N4945 transistors, common base connected, as shown in Figure 4 and Figure 4A provide the high voltage (60V) drive required without inversion.

5. MULTIPLEXING TIMING AND CONTROL

A 9601 one shot, connected as a free-running multivibrator, 9310 decade counter, and 9301, 1 of 10 decoder are used for multiplexing timing and control. A minimum of 1 kHz refreshing frequency is desirable to avoid flicker, in view of the rather short decay time of the P15 phosphor. The multivibrator therefore must operate at 1 kHz or higher frequency. Its output is used as clock for the 9310 decade counter which is programmed to count up to 7 and recycle. This is achieved by providing feedback to the parallel enable (PE) input from a NAND gate which has as inputs the Q_0, Q_1, Q_2 counter outputs. Whenever the 9310 counts from 0000 to 0111 (from 0, to 7 in decimal digits), the NAND gate output goes low, energizing the parallel enable and 0000 is loaded into the counter during the next clock pulse since the parallel inputs P_0, P_1, P_2, P_3 are connected to ground. The Q_0, Q_1, and Q_2 outputs of the counter are applied respectively to the A_0, A_1, and A_2 inputs of the 9301 decoder and to the S_0, S_1, S_2 select inputs of the 9312 multiplexers.

The 9301 decoder outputs 0 through 7 are thus successively energized (set to "low"). These outputs are then connected through 8 transistor drivers (Figure 4A) to the filament transformer secondaries for each Tung-sol tube or to the control grid of each NEC tube.

As a result, the input data for each decimal digit is sequentially applied to the 7 segment decoder and the corresponding display tubes are sequentially enabled.

6. DISPLAY TUBES

These require 1.6 V at 45 ma (a.c. or d.c.) for their cathode filaments. The anode supply for DC operation is +25 V. For multiplexing operation using 8 tubes (12.5% duty cycle) +60 V is required to provide adequate brightness. The current per segment is then approximately 1 ma. The NEC tubes are enabled by the control grid. The Tung-sol tubes are enabled by connecting their cathodes to ground. To accomplish this a filament transformer with 8 secondary windings is used, each energizing one tube. Each winding (and therefore each tube cathode) is at +60 V i.e. reverse-biased unless enabled. (A suitable miniature transformer in a 1" x 1" x 1/2" package is available from Tranex Co.).

OPERATION DESCRIPTION

Refer to the overall logic circuit diagram and timing diagram Figure 2. To start with, assume the 9310 decade counter is in the $Q_3Q_2Q_1Q_0$=0000 state (t_o). The 9301 1 of 10 decoder, activates outputs pin 0 which in turn enables the T_o tube. Meanwhile the 9312 input multiplexer, through select control $S_0S_1S_2$=000, applies the four

bit BCD data for decimal digit #0 (most significant digit) from the 9308 input register #0 to the 9307 decoder, and the decoder output lights up the appropriate segments of Tube T_0. During clock period t=1 the BCD data for decimal digit #1 is decoded and tube T1 is enabled, and so on until digit #7 is decoded and tube T7 enabled. The cycle of operation then repeats itself.

OTHER MULTIDIGIT DISPLAYS

The same system can be easily adapted to multiplex 5, 6 or 7 digits by changing the reset decoding for the 9310 counter as shown in the system diagram. The number of 9308 input register packages may be reduced to suit the required number of digits but four 9312 multiplexers are still required.

Four-digit multiplexing still proves economically attractive because a dual JK F.F. (9020) used as mod 4 counter, associated decoder using two quad 2-input gates (946), and two 9309 dual 4 input multiplexers can be used in place of four 9312 multiplexers. Figure 3 shows the simple system which results.

For display of more than 8 digits it becomes increasingly difficult to obtain adequate brightness because of the low duty cycle, and therefore a better approach is to divide the system into two parallel multiplexing sub-systems, sharing the same timing and control logic. This approach is feasible even with unequal number of digits in each sub-system by allowing one clock period to be unused in the smaller block. Figure 5 shows a block diagram of a 15-digit system using this technique.

CONCLUSION

A straightforward multiplexing scheme has been described utilizing available MSI devices. The additional cost of the multiplexing control logic is more than offset by the reduction in decoding hardware (one over straightforward DC operation decoder and seven drivers for each additional tube) when a display system of 4 or more tubes is required.

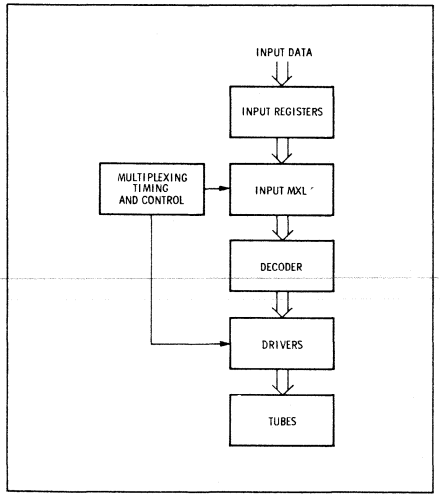

Fig. 1. Functional block diagram.

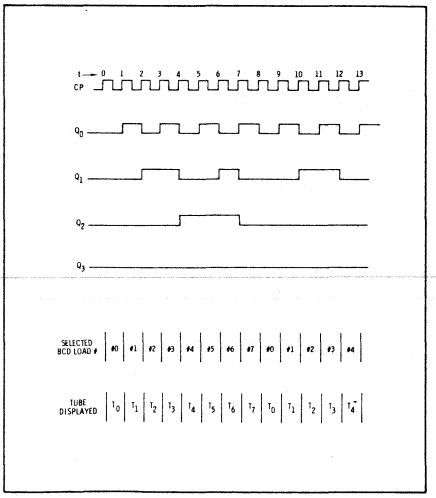

Fig. 2.

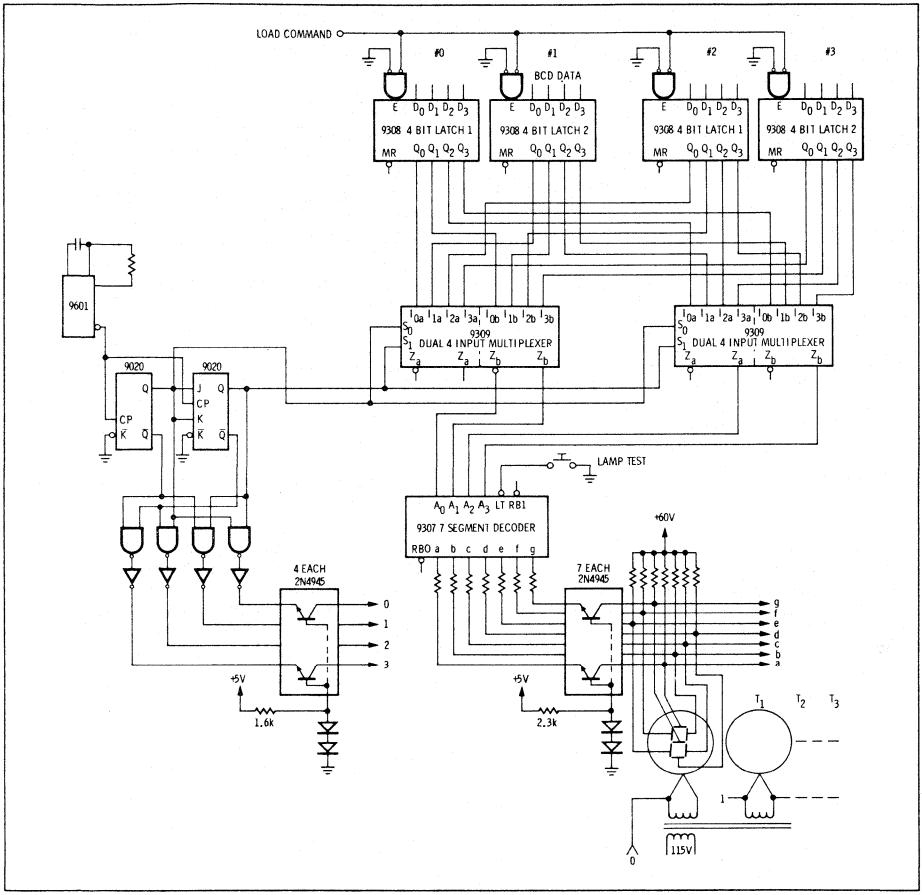

Fig. 3.

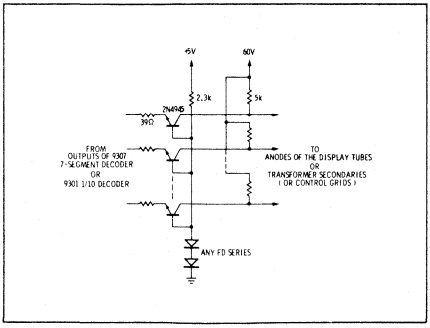

Fig. 4. Discrete version of driver stage.

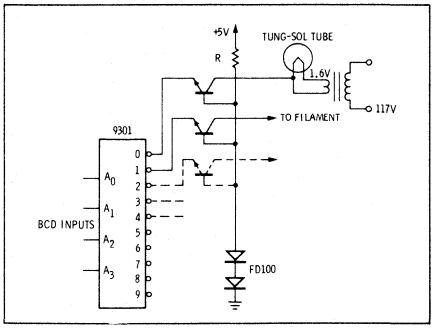

Fig. 4a.

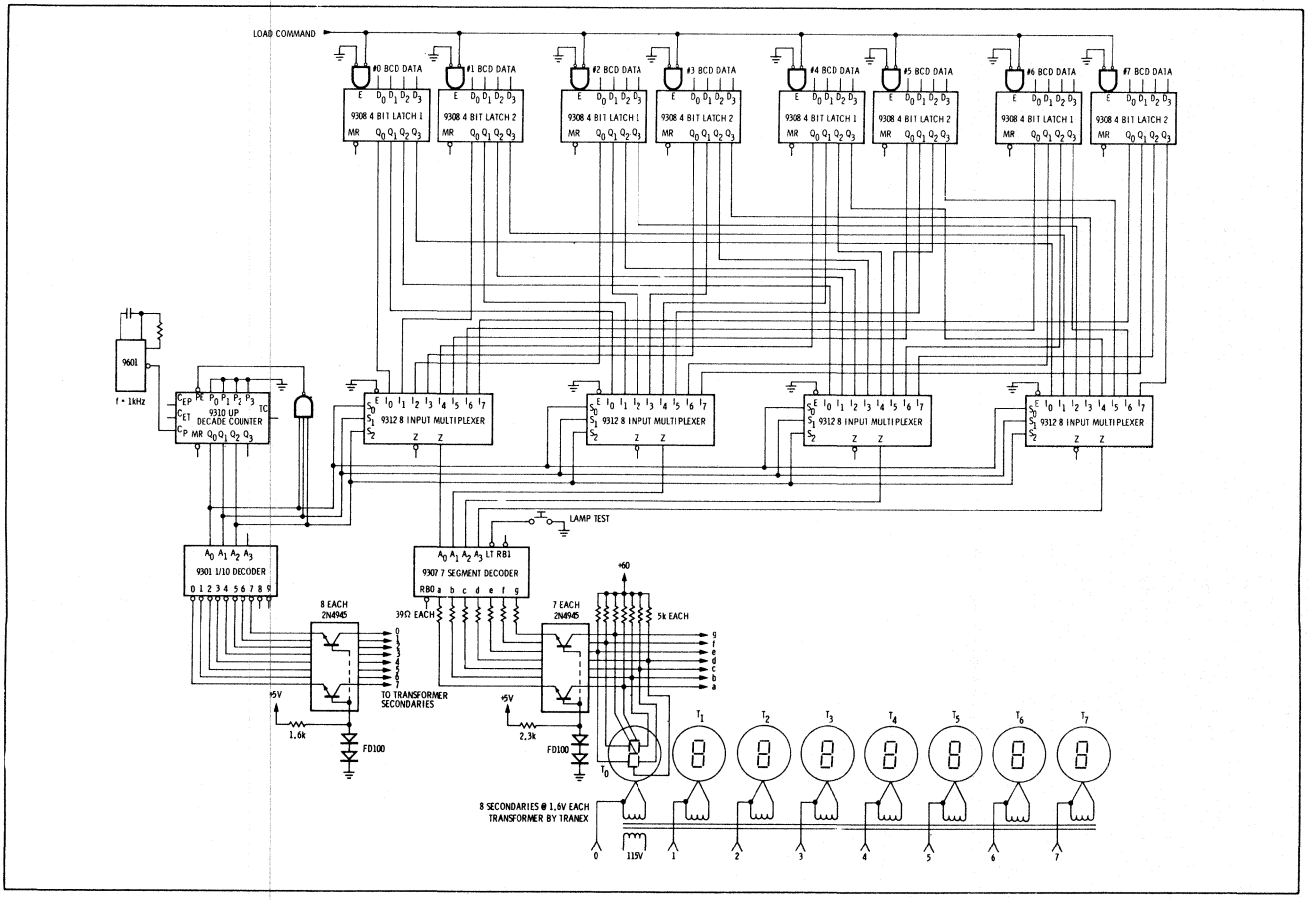

Fig. 6. Multiplexing mode operation of TUNG-SOL Digivac 7-segment readout.

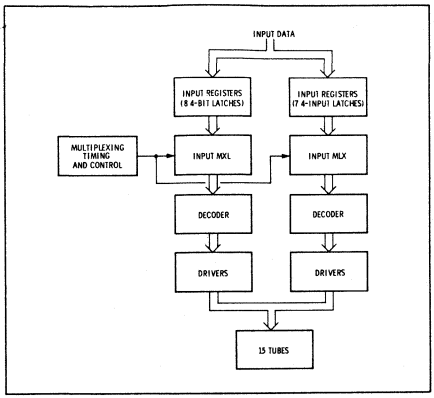

Fig. 5. Block diagram

TABLE I. Truth Table

$\overline{E}$	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	Z	$\overline{Z}$
H	X	X	X	X	X	X	X	X	X	X	X	L	H
L	L	L	L	L	X	X	X	X	X	X	X	L	H
L	L	L	L	H	X	X	X	X	X	X	X	H	L
L	L	L	H	X	L	X	X	X	X	X	X	L	H
L	L	L	H	X	H	X	X	X	X	X	X	H	L
L	L	H	L	X	X	L	X	X	X	X	X	L	H
L	L	H	L	X	X	H	X	X	X	X	X	H	L
L	L	H	H	X	X	X	L	X	X	X	X	L	H
L	L	H	H	X	X	X	H	X	X	X	X	H	L
L	H	L	L	X	X	X	X	L	X	X	X	L	H
L	H	L	L	X	X	X	X	H	X	X	X	H	L
L	H	L	H	X	X	X	X	X	L	X	X	L	H
L	H	L	H	X	X	X	X	X	H	X	X	H	L
L	H	H	L	X	X	X	X	X	X	L	X	L	H
L	H	H	L	X	X	X	X	X	X	H	X	H	L
L	H	H	H	X	X	X	X	X	X	X	L	L	H
L	H	H	H	X	X	X	X	X	X	X	H	H	L

H = HIGH VOLTAGE LEVEL
L = LOW VOLTAGE LEVEL
X = DON'T CARE, EITHER HIGH OR LOW VOLTAGE LEVEL

SERIAL NUMERIC DISPLAY SYSTEM

DESCRIPTION

The display system described here consists of eight 7-segment numeric readout modules, being pulsed one at a time in sequence from least significant to most significant digit. The advantage to this method of driving the display is that less circuitry is needed per digit than with conventionally parallel driven displays. The system is shown in Figure 1.

The display driver is made up of one 9307 7-segment decoder, eight character buss drivers, a module strobe circuit, and eight high current module drivers. The display modules are wired in a matrix network, the eight character buss drivers forming one side of the matrix and the eight module drivers forming the other side (see Figure 2).

OPERATION

In operation, a 4-bit BCD signal representing the value of the least significant digit is applied to the input of the 9307 decoder. The 7-segment decoder then activates, through the character buss drivers, the proper segments of the display modules needed to form a visual representation of the decimal number. At the same time, the digit strobing circuit activates, through the module drivers, the proper digit to be illuminated; in this case the least significant digit. The next least significant digit is then applied to the 7-segment decoder, and simultaneously, the digit strobing circuit activates the next least significant display module. When the most significant digit has been reached, the digit strobe circuit then reselects the least significant digit and the process is repeated.

In this manner each of the eight display modules is actually on for only 12.5% of the time; however, the repetition rate of the strobe circuit is fast enough to cause the display modules to appear continuously illuminated. To cause the bulbs of the display to achieve full brilliance with only the 12.5% duty cycle pulses being applied, the pulse voltage is approximately 2.8 times the normal voltage rating of the bulb. Since power dissipation of a constant load is proportional to the square of the voltage, this causes the bulbs to dissipate eight times their normal wattage, but for only one-eighth of the time. In order to eliminate a possible reduction of bulb life caused by the constant heating and cooling of the filaments, a much higher pulse frequency than that required to eliminate flickering is used, thus keeping the bulbs at a more constant temperature by taking advantage of the slowness of their heat dissipation. In this respect, the higher the pulse frequency the better; however, a limit is imposed

due to the delay time of the high current drivers. Pulse frequency used in this circuit is approximately 30 kHz.

The module strobe circuit is shown in simplified form in Figure 3. It is made up of a variable duty cycle pulse generator, a pluse shaper, a modulo eight shift counter and a one-out-of-ten decoder. The pulse generator provides a constant frequency, adjustable duty cycle pulse signal which is used for intensity modulation of the display bulbs. The signal is applied to a shaper circuit which changes the variable duty cycle pulse into a constant high duty cycle pulse signal which is used in the remainder of the circuitry as a clock signal. The high duty cycle clock signal is advantageous in increasing the noise immunity of the system. The clock pulse is applied to an external recirculating storage system and to the modulo eight shift counter. The three output lines of the counter are applied to the one-out-of-ten decoder. The decoder activates one of its eight lowest valued output lines for each of the eight possible recurring states of the counter and these eight output lines are, in turn, applied to the eight high current module drivers.

The variable duty cycle pulse generator is made from two 9601 single-shot multivibrators. The active high output of each single shot is applied to an active low input of the other. In operation, one of the single-shots is in its active state and the other is in the reset state. When the active single-shot times out, its output drops, thus triggering the second single-shot. Similarly, when the second single-shot times out it retriggers the first single-shot. The pulse widths of the two single-shots are controlled by capacitors C_1 and C_2, and resistors R_1, R_2 and R_3 (Figure 3). R_3 is placed in the circuit in such a way that adjustment of the resistor increases the pulse time of one of the single-shots and decreases the pulse time of the other. In this way the duty cycle of the generator can be controlled without affecting the frequency

The pulse shaping circuit consists of diode D_1, resistor R_4, capacitor C_3, and one of the four two-input gates of a 9002. The two complementary outputs of one of the 9601's of the generator are applied to the inputs of the 9002 gate, one directly and the other through the delay circuits D_1, R_4, and C_3. Because of the delay circuit the high voltage states of the complementary 9601 outputs, as seen at the gate, overlap for a short period of time for each cycle of the pulse generator. During this high voltage overlap period the NAND function of the gate is satisfied to produce a low going pulse. This pulse is of relatively short duration in order to produce an overall high duty cycle clock signal.

The module eight counter is made from a 9300 4-bit shift register and two additional gates of the 9002. Eight possible logic states can appear on the three output lines of the counter. These states change with every clock pulse applied to the counter; however, the eight states do not appear in binary numerical sequence. The actual count sequence is shown in Table I.

Since the highest numeric state from the three output lines of the counter is a binary seven, only the lowest eight outputs of the 9301 corresponding to a zero-through-seven binary input would be normally activated and these eight output lines are used to sequentially activate the appropriate display modules. If, however, a high voltage is placed on the A_3, most significant input of the 9301, the decoder sees a higher numerical input than seven, no matter which state the counter is in and, therefore, none of the display modules will be activated. This most significant input is used to provide two additional functions of the digit strobe circuit. One is to provide, in conjunction with the 9307, a method of controlling the brightness of the display. The second function is to provide a safety control to prevent the bulbs of any one of the modules from burning out in case the counter should hang up in one state for any reason and thus present a continuous voltage to one of the modules.

The safety control consists of a 9601 single-shot multivibrator. The input of the multivibrator is connected to one of the output lines of the counter. The pulse time width is set to where it remains in its triggered state as long as the multivibrator receives pulses from the counter. Should the counter stop, the multivibrator is allowed to time out and return to its reset state. The active high output of the 9601 is coupled through a two input NOR gate to the A_3 input of the 9301, so that if the counter stops, the A_3 input goes high and inhibits the zero-through-seven output lines of the 9301.

The other input of the NOR gate is used for lamp intensity control. Since each clock pulse produced by the pulse generator causes a change of state in the shift counter, the maximum length of time that each display module can be activated is equal to the time between consecutive clock pulses. With the modulo eight counter this pulse width corresponds to a 12.5% duty cycle, which, as explained above, will illuminate the lamps to full brilliance. This duty cycle can be reduced by inhibiting the outputs of the 9301 for a portion of the time between each clock pulse. To do this the variable duty cycle signal from the pulse generator is applied through the NOR gate to the A_3 input of the 9301. The duty cycle of this pulse can be varied from 10% to 55%, thus reducing the time that each module strobe line is activated per cycle by that amount. This causes a corresponding reduction in the lamp intensity of each display module. The variable duty cycle pulse is also coupled through a diode to the ripple blanking output of the 9307 decoder. The ripple blanking output of the 9307, when connected in this manner, performs the same functions as the A_3 input of the 9301, so that the intensity modulation is applied to both sides of the matrix.

Three outputs, a clock output and two sync outputs are provided by the serial driver to accommodate synchronization of the recirculating storage used in conjunction with the display system. The complete logic diagram for the serial display system, excluding the module and character drivers, is shown in Figure 4.

ADAPTION OF A KEYBOARD TO THE SERIAL DISPLAY

Complete data storage for the serial display can be provided by two 9328 dual eight bit shift registers. An additional 9328 is used to store decimal point information and leading edge zero blanking information.

The three 9328's, a 9020 dual JKK flip-flop, and two 9002 quad two input gates make up the entire keyboard-to-display storage system described here. The system is shown in logic form in Figure 5.

The 9328 registers are used as recirculating storage registers by connecting the output of the 8-bit position of each register to the D_1 input of the first bit position of the register. The D_0 inputs of the registers are used to feed data into the system from an external source. The effective input, i.e., D_0, or D_1, is determined by the condition of the D_S line to each register. If the D_2 line is at a low logic level the data which shifts into the first stages of the registers is taken from the external input lines; however, if the D_S line is at a high logic level the data which shifts out of the last bit position of each register is put back into the first bit position and allowed to recirculate through the register.

The clock pulse which produces the shifting action of the registers is the same clock which activates a change of the module strobe circuit in the serial display system. Because there are eight bit positions in each register, the data in each position of the registers reappears at the outputs once every eight clock pulses.

Identically, the module strobe circuit in the serial display system re-strobes each display module once every eight clock pulses so that the phase between the information flowing through the recirculating registers remains con-

stant in relation to the phase of the strobe circuit. As long as this constant phase relationship is maintained, the numbers appearing on the display hold a fixed position; however, if the storage registers were prevented from shifting during one clock pulse without affecting the operation of the strobe circuit, the numbers on the display would appear to shift one position to the left.

A circuit is built into the storage system which causes this to happen each time a numeric key on the keyboard is pressed. This resynchronizing circuit is made with a 9020 dual flip-flop with the CD asynchronous reset inputs of both 9020 stages connected to the keyboard strobe line. This line remains at a low logic level until a key is pressed, at which time the line goes high. Until a key is pressed the two flip-flops are held in the reset condition. The JK inputs of the first flip-flop stage are tied together and connected to the $\bar{Q}$ output of the second flip-flop. The JK inputs of the second flip-flop are also tied together and are connected to the Q output of the first flip-flop. Whenever a keyboard numeric key is pressed the reset conditions of the two flip-flop stages are removed.

On the first clock pulse which appears after the key is pressed the JK inputs of the first flip-flop stage, which see the high logic level of the $\bar{Q}$ output of the second stage, allow the first flip-flop to toggle into the set condition. The JK inputs of the second flip-flop, however, see a low logic level from the first stage Q output and, thus, the second stage is inhibited from toggling and remains in the reset condition. On the next clock pulse the first stage still sees the high level output of the second stage Q output and toggles again to the reset position. At the same time the second stage sees the high output of the first stage Q output and toggles to the set condition. After the second clock pulse the first flip-flop is in the reset state. The second flip flop is in the set state and the JK inputs of both stages see logic low voltage levels and no further change of state takes place until the activated key on the keyboard is released.

When the activated key is released the strobe line again goes low, resetting both flip-flop stages. The Q output of the first stage is connected to the clock gate of each 9328 register, so that, when the Q output of the first stage flip-flop goes high it inhibits the clock inputs of the storage registers. Since this Q output goes high for one clock period each time a key is pressed, one clock pulse is in turn inhibited from activating a shift in the storage system, causing the numbers on the display to shift one place to the left. The second clock pulse received after a key is pressed causes the Q output of the second stage flip-flop to go high. This output then remains high until the activated key is released.

The second stage Q output is coupled to an AND gate along with the sync signal from the display system and the output of this gate is, in turn, connected to the D_S input control lines of the registers. The sync line goes high every time the module strobe circuit is strobing the least significant digit of the display. When the second stage Q output goes high, indicating that the re-synchronization has taken place, and when the sync signal goes high, indicating the strobing of the least significant digit, the output of the AND gate goes low, causing the D_S register inputs to strobe the BCD information from the keyboard into the storage register. The sync signal causes the new data to be strobed into the proper bit position of the four data registers to cause the new number to appear in the least significant digit position of the display.

The blanking shift register is used to blank leading edge zeros of the displayed number. The output of this register is connected to the ripple blanking input of the 9307 seven-segment decoder in the serial display system.

This input inhibits all output lines of the decoder whenever a BCD zero is seen on the four data input lines. When this input is at a low logic level the zero output condition of the 9307 is blanked. When the blanking input is high the zero condition is allowed to be displayed.

When the reset line of the storage system is momentarily activated, all information in the six registers is removed. Thus, a zero condition exists in each position of the four data registers and all zeros exist in the positions of the blanking register. Since the blanking register output is connected to the ripple blanking input of the 9307, this input sees a constant low voltage. The four data inputs of the 9307 see a BCD zero condition and, therefore, the display is blanked. Whenever a number is punched into the storage system, a logic one is placed in the corresponding position of the blanking register to remove the blanking signal whenever the data is at the output stages of the four data registers. Thus, if a zero is punched into the system, although nothing goes into the data registers, a one is placed in the blanking register and the zero will be displayed.

Decimal point information is placed in the decimal point register by means of a special input line. Whenever a low logic level is seen on this line a logic one is placed in the bit position of the decimal point storage register which corresponds to the strobing of the least significant display digit. Since the strobe input line is not activated along with the decimal point input line the 9020 re-sync circuit is not activated and the numbers on the display do not change position. However, a decimal point will appear on the display behind the least significant digit. If additional numeric data is then punched into the system the decimal point register is re-synced along with the other registers and the decimal point being displayed shifts across the display screen along with the numbers. A keyboard suitable for use with this system is shown in Figure 6.

8 STAGE DECIMAL COUNTER FOR SERIAL DISPLAY SYSTEM

A logic diagram of a decimal counter designed to be used in conjunction with the serial display system is shown in Figure 7. The counter uses separate recirculating storage so that while the counter is in a count cycle, the result of the previous count cycle can be held on the display screen.

The basic counter is made up of eight 9310 up decade counter packages wired in a high speed counting arrangement. Each 9310 package is a four stage binary counter which resets itself and produces a terminal count pulse whenever it reaches a binary nine state and receives an additional clock pulse. The terminal count output of each 9310, with the exception of the least significant counting package, is wired to the count enable trickle input of the next higher significant package. This causes the state of any particular 9310 package to advance only when all previous 9310 packages have reached binary nine states. The terminal count output of the least significant 9310 package is wired through two inverters serving as drivers to the count enable parallel inputs of all the following stages. This increases the high frequency limitation of the counter in that the carry pulse of the least significant stage has less circuitry to go through to reach the most significant package when all the intermediate stages are in their binary nine states. At the end of a count sequence, the resulting 4-bit binary number in each 9310 package represents the BCD equivalent of a decimal digit to be displayed.

In order to transfer the result of a count cycle from the eight stage counter to the recirculating storage register, the parallel enable inputs activate the parallel output-to-input interconnections between the 9310 packages so that, with each clock pulse applied to the counter circuit, the BCD digits in each stage of the counter shift to the next least significant stage and finally are applied to the inputs of the storage register through the four parallel output lines of the least significant 9310. This shift

sequence must be synchronized with the shift action of the 9328 recirculating registers so that the clock pulse applied to the counting circuit during the transfer cycle is the same clock pulse which is causing the recirculating shifting action in the storage circuit.

To control the mode of operation of the counter, a stepper circuit is made from a 9020 dual $J\bar{K}K$ flip-flop and a 9309 dual four input multiplexer. The controlling sequence of the stepper circuit is shown in Table II. The 9020 is wired as a two digit control counter. Three possible input pulses can change the state of the control counter; however, only one of these pulses will have an effect on the counter for any one state, i.e. when the counter is in the 0, 0 state, only the start count pulse is applied through one side of the 9309 multiplexer to the 9020 control counter. In the 0, 1 state only the stop count control pulse can advance the control counter and in the 1, 1 and 1, 0 states only the sync pulse coming from the serial display system will advance the counter.

For the control circuit description, assume the control counter to be initially in the 0, 0 state. During this time the negation outputs of both stages of the control counter are at a high logic level and are applied to the two inputs of a 9002 NAND gate. The NAND gate responds to the two high level inputs with a low level output which is applied to the active low master reset terminals of the eight decade counter stages. This ensures that the main counter circuit will be completely clear prior to the count cycle. At this time no clock pulses are applied to the main counter. When the start count pulse is received at the system it is gated through side A of the multiplexer to the control counter to cause it to shift to the 0, 1 state. In this state the active low signal is removed from the master reset terminals and the pulse to be counted is applied through side B of the multiplexer to the main counter.

The stop count line is now connected to the control counter through the multiplexer and the main counter is in the count mode and will continue counting until the stop count pulse is received at the system. The stop count pulse sets the shift counter to the 1, 1 state. In this state all clock pulses are removed from the main counter and the sync line from the serial display system is coupled to the control counter through the multiplexer. Also, the parallel enable terminals of the main counter stages are activated to shift the counter from the counting mode into the serial transfer mode. When the sync pulse is received from the display system, the control counter advances to the 1, 0 state. Clock pulses from the display system are now coupled to the main counter and the information in the counter is shifted out of the least significant stage of the counter into the 9328 storage registers. Eight display clock pulses appear between each sync pulse so that eight shifts of the information take place in the main counter which is the exact number of shifts needed to transfer the eight BCD coded digits from the counter to the recirculating register. When the second sync pulse appears at the system the control counter changes back to the original 0, 0 condition. The display clock pulses are removed from the main counter and the parallel enable terminals of the counter are deactivated. The master reset terminals are again activated and the start count line is coupled to the control counter. The counter circuit is now ready to start another count cycle with another count start pulse.

The recirculating storage register for this system is made from two 9328 dual 8-bit shift registers and is similar to that used for the keyboard display system, but without the re-sync circuitry. Like the keyboard storage system, these 9328 registers can be made to either recirculate their internal information by maintaining the strobe input, D_S lines of the register at a high logic level; or information from an external source,

in this case the decimal counting circuit, can be made to shift into the counter by applying a logically low voltage level to the strobe input lines. The strobe line of each 9328 register is applied to the common parallel enable line of the decimal counter so that whenever the counter is in the transfer mode, the storage register is in the external input mode and whenever the counter is in the count mode, the storage register is in its recirculation mode of operation.

Figure 8 illustrates a similar counter without separate storage. In this circuit the parallel outputs of the least significant 9310 are coupled to the parallel inputs of the most significant 9310, so that the counter itself acts as a recirculating register during the transfer cycle. The transfer cycle in this case is used for display and a separate "stop display" pulse, rather than the sync pulse is used to advance the control counter out of this condition.

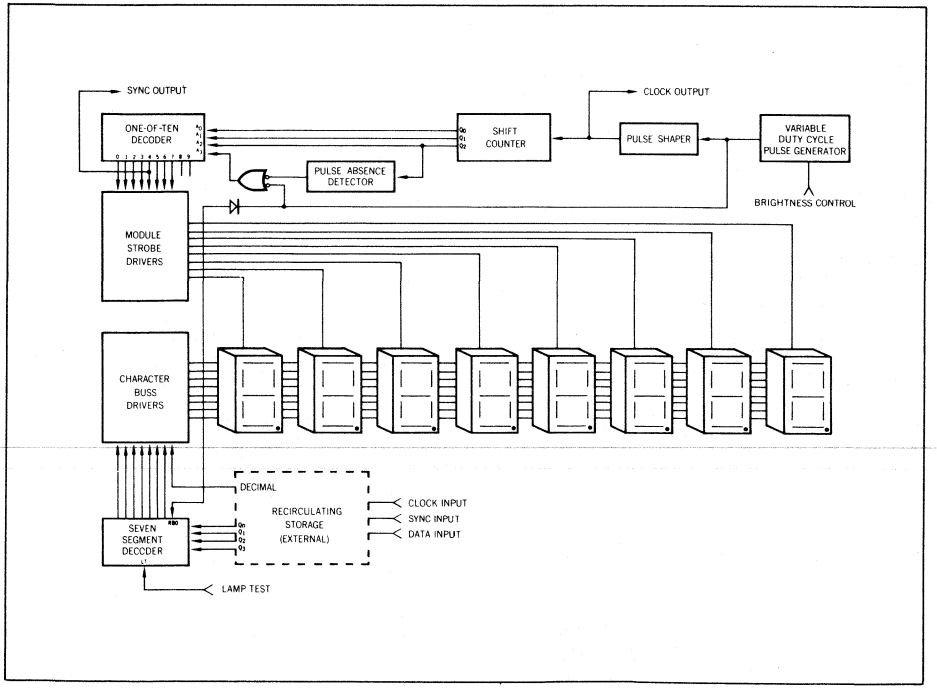

Fig. 1 Block Diagram of Serial Display System.

R

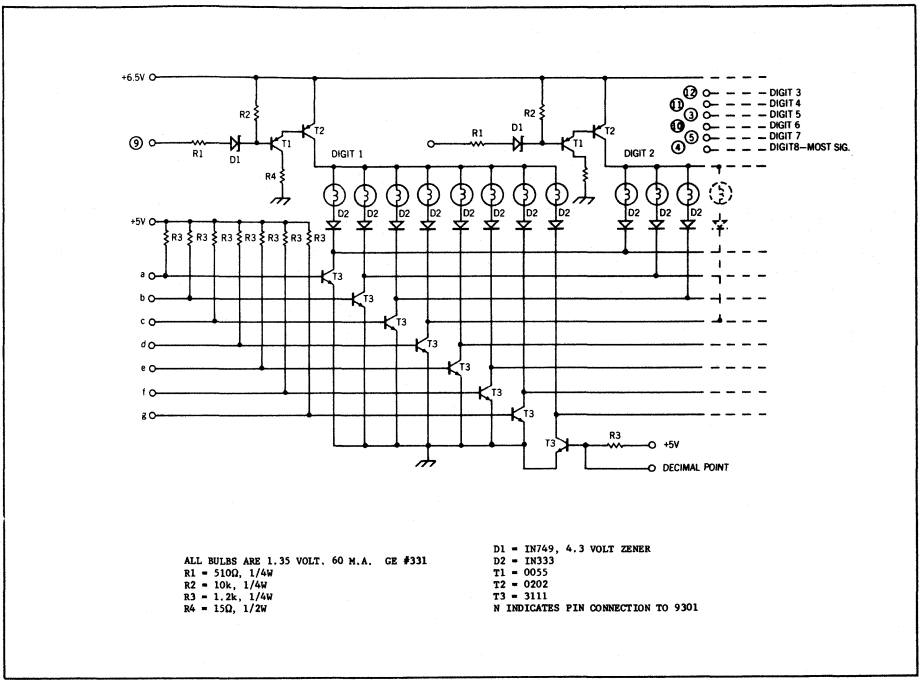

Fig. 2 Matrix Switching Circuit.

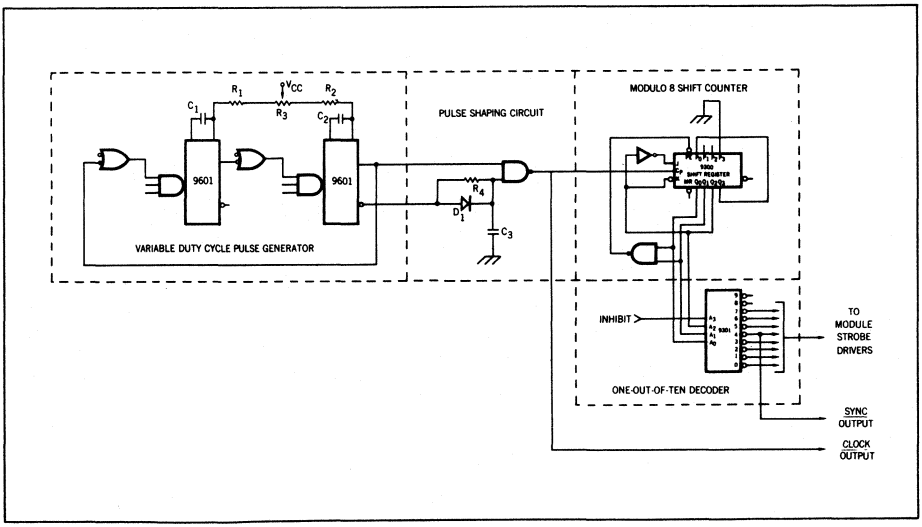

Fig. 3 Basic Module Strobe Circuit.

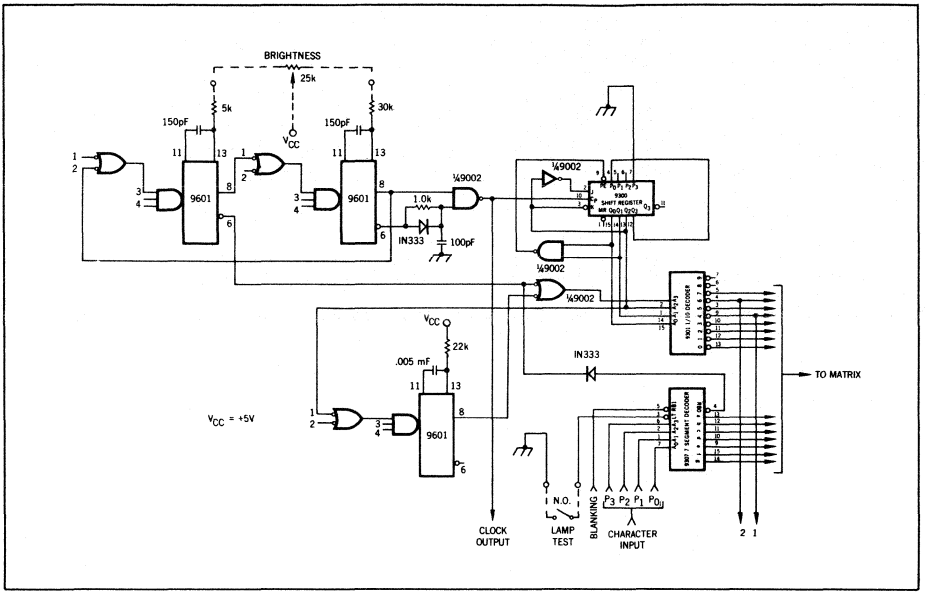

Fig. 4 Serial Display Driver.

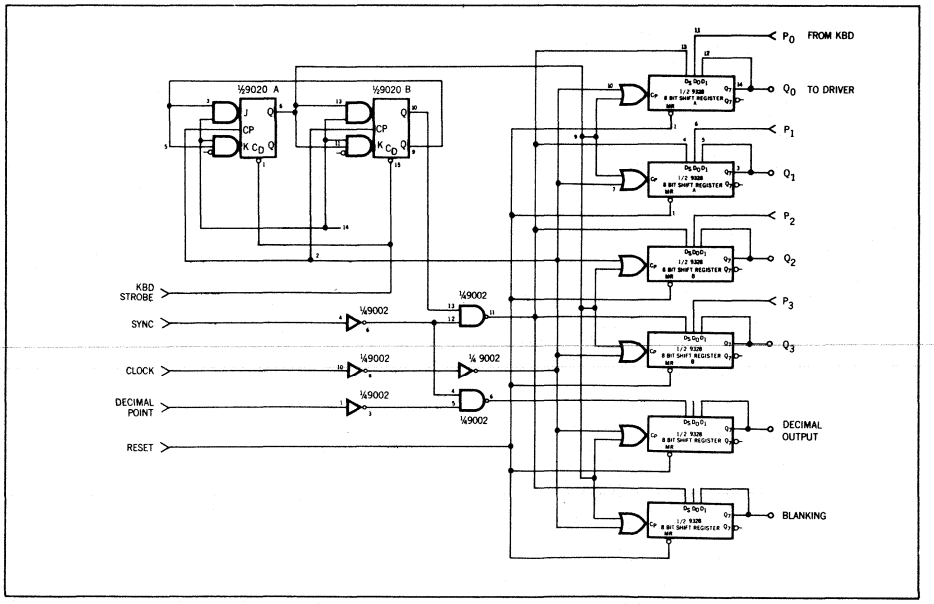

Fig. 5 Keyboard to Display Storage.

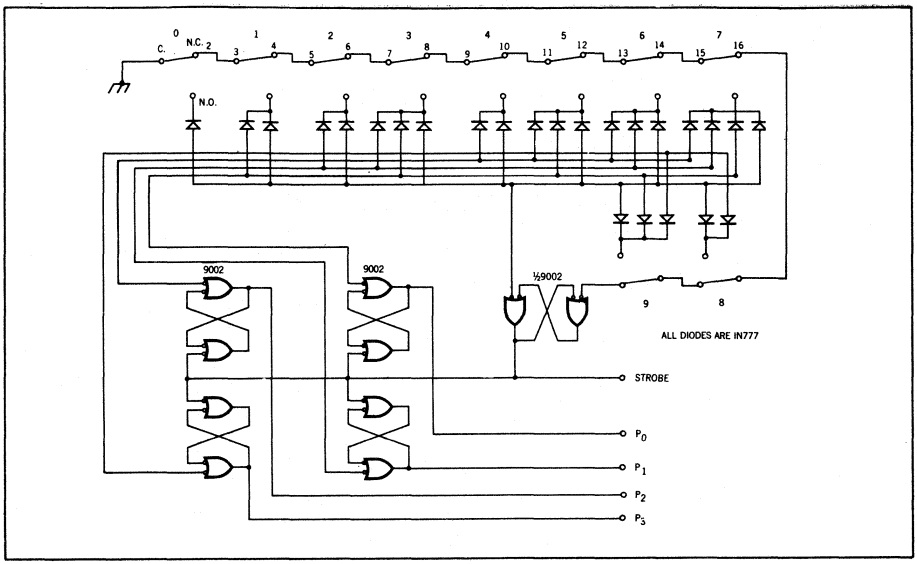

Fig. 6 Keyboard Used With Serial Display System.

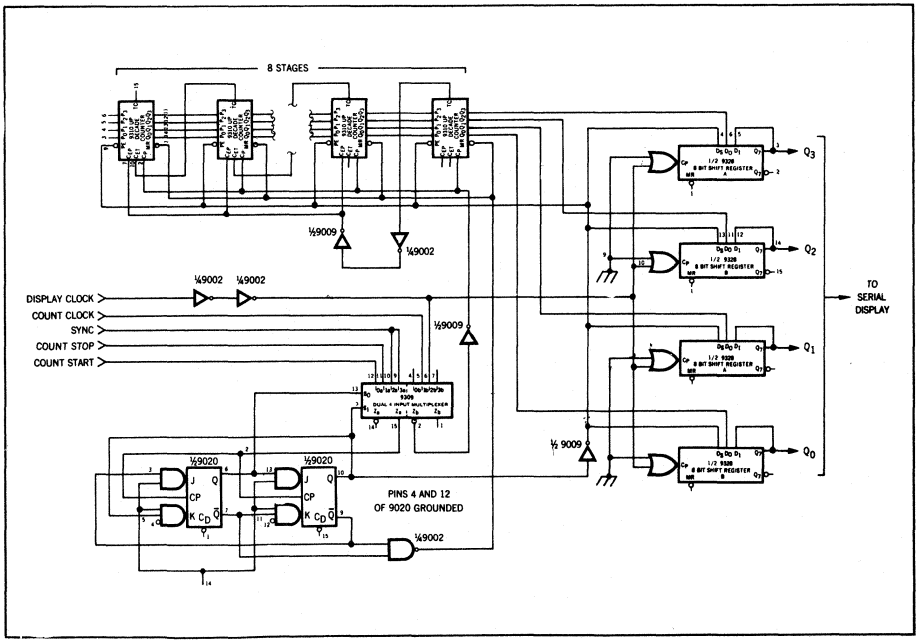

Fig. 7 Eight Decimal Counter.

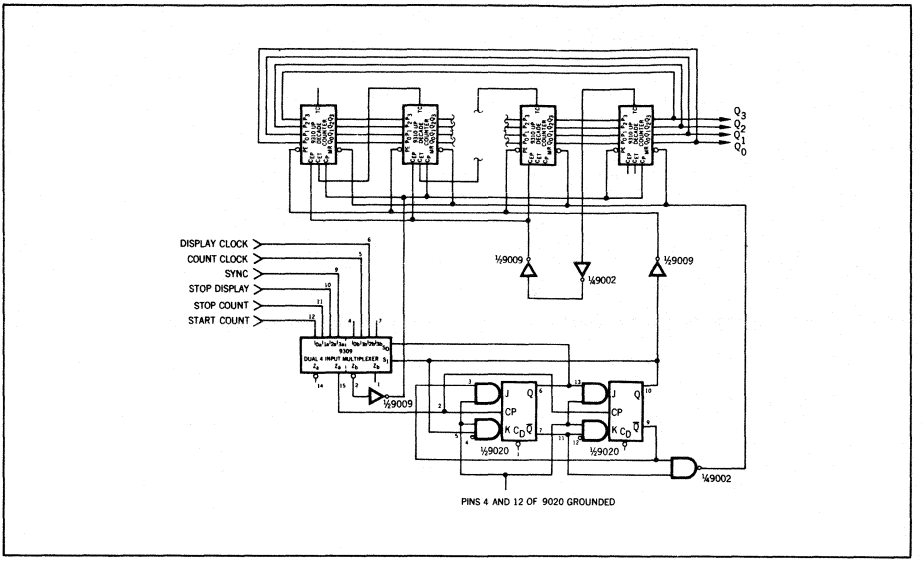

Fig. 8 Eight Stage Non-Storing Decimal Counter

TABLE I

COUNT ORDER OF MOD. 8 COUNTER		
COUNT Q_3 Q_2 Q_1 Q_0	9301 OUTPUT	DIGIT STROBED
1100	4	1
1000	0	2
0001	1	3
0010	2	4
0101	5	5
1011	3	6
0111	7	7
0110	6	8

TABLE II

COUNTER CONTROL SEQUENCE

STATE OF CONTROL COUNTER	MODE OF OPERATION	CONDITION FOR TRANSFER	PARALLEL ENABLE	CLOCK	STORAGE
S_1, S_0 0, 0	MASTER RESET	START COUNT PULSE	DEACTIVATED	NO CLOCK	RE-CIRCULATING
0, 1	COUNT	STOP COUNT PULSE	DEACTIVATED	COUNT CLOCK	RE-CIRCULATING
1, 1	WAIT	SYNC PULSE	ACTIVATED	NO CLOCK	EXTERNAL INPUT
1, 0	TRANSFER	SYNC PULSE	ACTIVATED	DISPLAY CLOCK	EXTERNAL INPUT

THE 9300 AS A 2-INPUT SHIFT REGISTER

The MSI 9300 4-bit shift register is a versatile storage register with both shifting and synchronous load capabilities. Use of the synchronous load facility offers the advantage of considerably reducing the number of gates in a system. With suitable connections, the 9300 shift register can have two shift inputs under control of the parallel enable signal. These two inputs and the select control can then generate any function of two variables shifting the result of the operation into the register.

Figure 1 shows the necessary connections for two inputs to the 9300 shift register D_0 and D_1. Each output of the register is connected to the next higher stage input. P_0 acts as the D_0 shift input. The J and K inputs are connected together to form the second shift input D_1, and the parallel enable D_S determines which input is active.

One obvious use of the 2-input shift register is to use one input for new data and the other for recirculation with the parallel enable input acting as an enter/circulate control--see Figure 2. Another not-so-obvious application is manipulating D_0, D_1 and D_S for operation on the two data streams A and B. A function of the two variables can then be generated with a suitable interconnection prior to inserting data into the shift register. The dual-entry register can be considered as a single-input shift register with a 2-input multiplexer at the front end of the register. Any function of two variables can be generated by suitable connection of the input variables and logic "0" and "1" to the D_0, D, D_S inputs. Table 1 is a multiple output truth table of the two variables A and B. Each of the 16 possible outputs are shown with corresponding connections to D_0, D_1 and D_S. An example of this use of the 9300 shift register is shown in Figure 3.

In a bank of eight shift registers, the 9301 decoder with active low outputs, controls which shift register that data will enter. The first three address lines on the 9301 act as a shift enable address, and the A_3 terminal acts as an overall inhibit signal. All unselected shift registers shift in logic zeros on each clock pulse.

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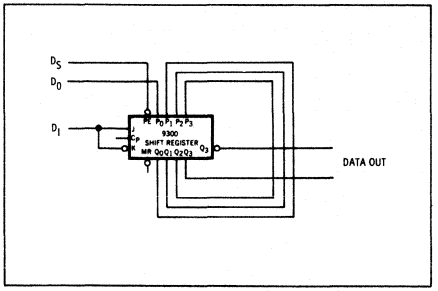

Fig. 1. 2-Input Shift Register

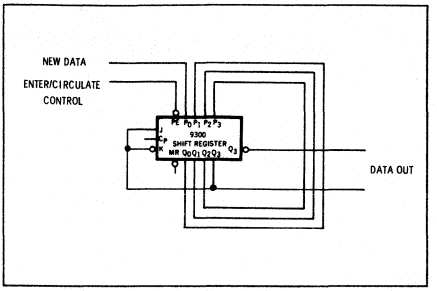

Fig. 2. Recirculation and Enter Capability

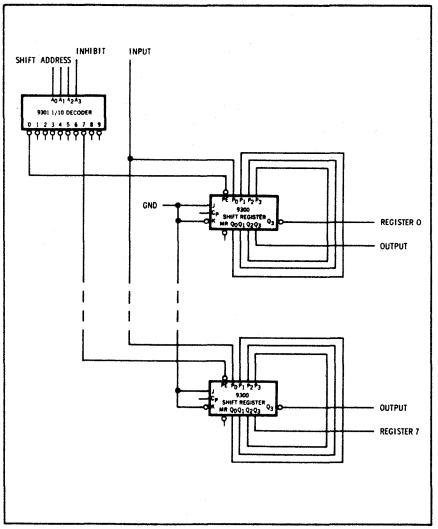

Fig. 3. 9301 Enabling Shift Register

TABLE 1
Minimum Input Pattern For Output of Any of 16 Possible Functions of Inputs A, B

FUNCTION NAME	CONNECTION TO D_S	D_0	D_1	A / B	L H L H / L L H H / OUTPUT
All Zeros	X	L	L	0	L L L L
Not A and Not B	A	B	L	1	H L L L
A and Not B	B	A	L	2	L H L L
Invert B	B	H	L	3	H H L L
Not A and B	A	B	L	4	L L H L
Invert A	A	H	L	5	H L H L
A Not Equivalent B	A	B	$\bar{B}$	6	L H H L
Not A or Not B	A	H	$\bar{B}$	7	H H H L
A and B	A	L	B	8	L L L H
A Equivalent B	A	$\bar{B}$	B	9	H L L H
Data A	A	L	H	10	L H L H
A or Not B	B	H	A	11	H H L H
Data B	B	L	H	12	L L H H
Not A or B	A	H	B	13	H L H H
A or B	A	B	H	14	L H H H
All Ones	X	H	H	15	H H H H

X = Don't Care Condition

9338 EIGHT-BIT MULTIPLE-PORT REGISTER

INTRODUCTION

The 9338 eight-bit multiple-port register may be considered as a one-bit slice of eight high speed working registers. Data may be written into any one of eight storage locations and read out from any two of the eight storage locations simultaneously. Master-slave operation eliminates all race problems associated with simultaneous writing in and reading from the same location.

The timing of this data transfer is similar to that of a standard master-slave flip-flop. While the clock is low the slaves are held steady, but the information on the D (data) input is permitted to enter the selected master. The next clock transition from low to high locks the masters in their present states making them insensitive to the D input and write address inputs. This rising clock edge also connects each of the two slaves to the selected masters causing their contents to be reflected on the outputs. Outputs change, therefore, following the low-to-high transition of the clock as on almost all Fairchild TTL/MSI devices and TTL flip-flops.

The $\overline{\text{slave enable}}$ ($\overline{\text{SLE}}$) input may be used to defeat the master-slave operation. If the slave enable (SLE) line is held low, the slaves are continuously enabled, allowing immediate transfer of information from the selected masters to the outputs.

The features of this member of the Fairchild TTL/MSI product line are:

- Master-slave operation permitting simultaneous write/read without race problems.
- Readily expandable to allow for larger word sizes and word count.
- Two output lines allow two words to be read out simultaneously. This means both inputs to an arithmetic or logical operation may be provided from one register bank composed of 9338's.
- Typical power dissipation of 265 mW.

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Other characteristics which are typical of all members of the Fairchild 9300 MSI line are:

- High speed--typical delay from clock pulse to output of 35 nanoseconds.
- Available in 16-pin DIP or Flatpack.
- TTL integrated circuitry with active pull-ups to provide high speed with reasonable power consumption and excellent noise margins.
- Input clamp diodes to ground to minimize the effects of line reflections.
- Input/output characteristics that provide easy interfacing with all Fairchild TTL and DTL devices.

Figure 1 is a pin location and loading chart, and the logic diagram for the 9338 is shown in Figure 2. When the clock input (Cp) is low, the data applied to the data input line (D_A) enters the selected master. This selection is accomplished by coding the three write input select lines (A_0, A_1, A_2) appropriately. The data is stored synchronously with the rising edge of the clock pulse.

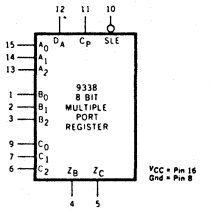
The information for each of the two slaved (output) latches is selected by two sets of read address inputs (B_0, B_1, B_2, and C_0, C_1, C_2). The information enters the slave while the clock is high and is stored while the clock is low. If $\overline{SLE}$ is low, the slave latches are continuously enabled. The signals are available on the output (Z_b and Z_c) pins. The input bit selection and the two output bit selections may be accomplished independently and simultaneously.

The data flows into the device, is demultiplexed according to the state of the write address lines, and is clocked into the selected latch, Figure 3. These eight latches function as masters and store the input data. The two output latches are slaves and hold the data during the read operation. The state of each slave is determined by the state of the master selected by its associated set of read address inputs.

The functional equivalent of this device can be shown using other members of the 9300 MSI family, Figure 4. Fourteen packages are required to implement the function of four 9338's.

Parallel Expansion Capabilities

One 9338 is needed for each bit of the required word length. The read and write and write input lines should be connected in common on all of the devices. This register configuration provides two words of n bits each at one time, as is illustrated in Figure 5 where n devices are connected in parallel.



PIN NAMES		LOADING
A_0, A_1, A_2	Write Address Inputs	2/3 UL
D_A	Data Input	2/3 UL
B_0, B_1, B_2	B Read Address Inputs	2/3 UL
Z_B	B Output	10 UL
C_0, C_1, C_2	C Read Address Inputs	2/3 UL
Z_C	C Output	10 UL
C_P	Clock Active High Going Edge Input	2/3 UL
$\overline{SLE}$	Slave Enable (Active Low) Input	2/3 UL

Figure 1. Pin Location and Loading Chart.

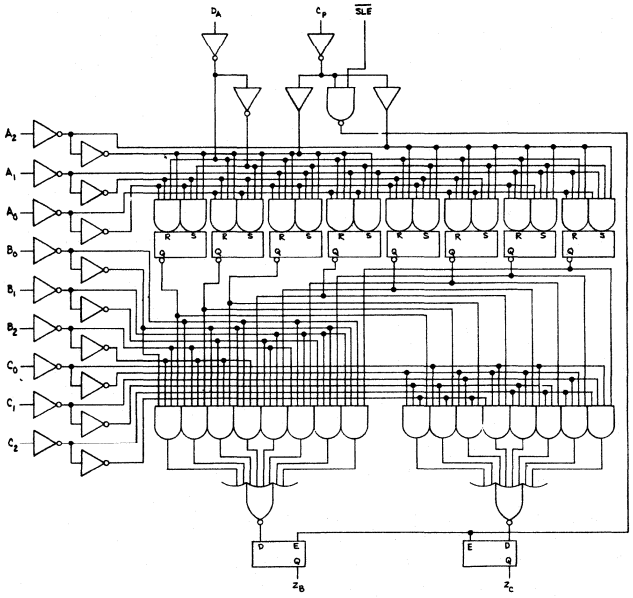


Figure 2. 9338 Logic Diagram.

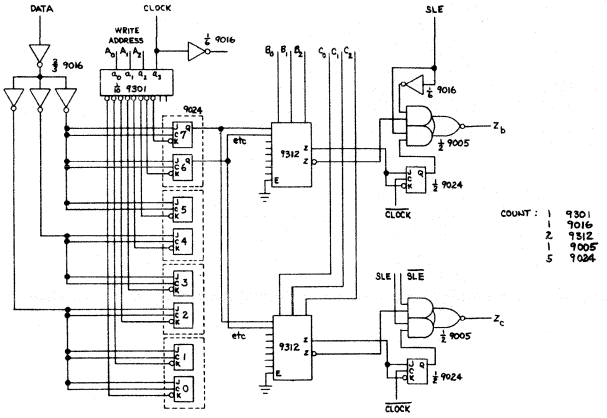


Figure 3. Functional Equivalent of the 9338.

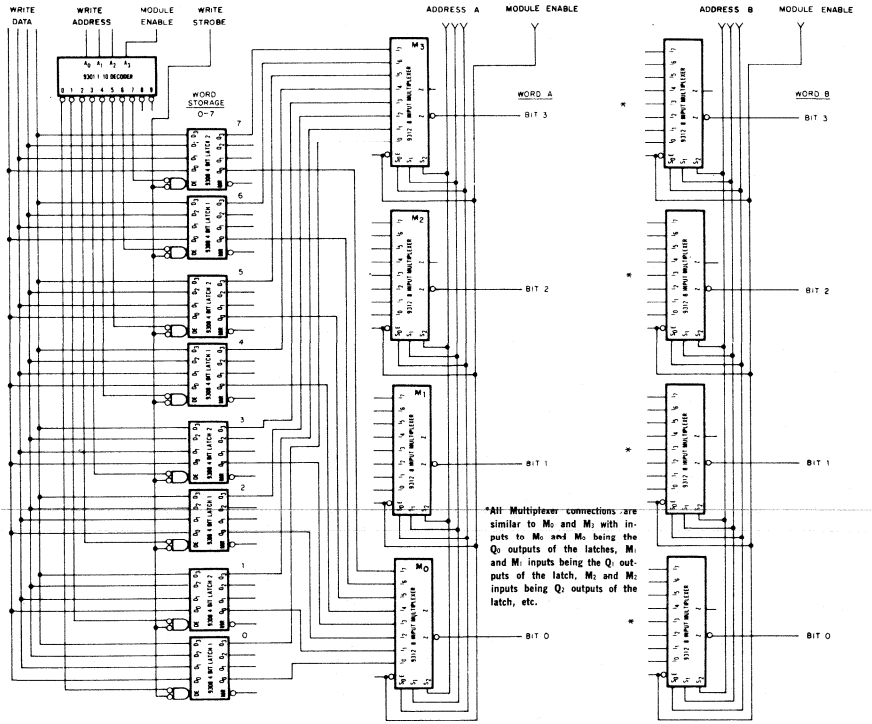


Figure 4. Equivalent TTL/MSI Implementation of Four 9338's.

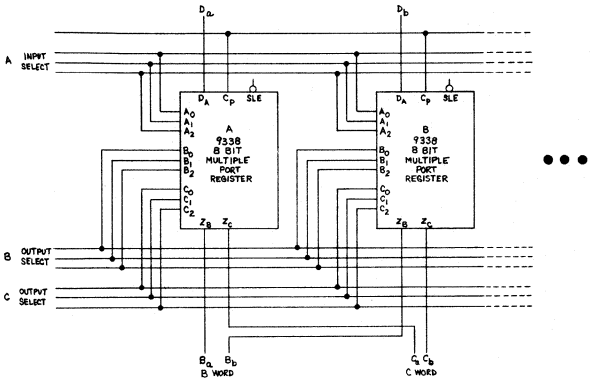


Figure 5. Parallel Expansion of the 9338.

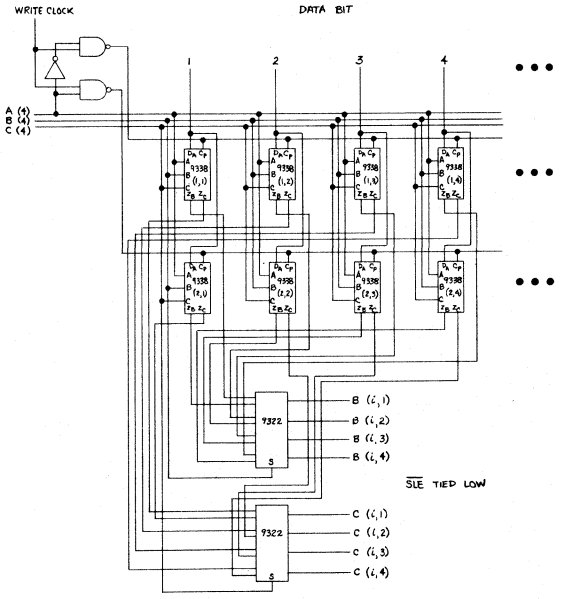


Figure 6. Serial Expansion of the 9338.

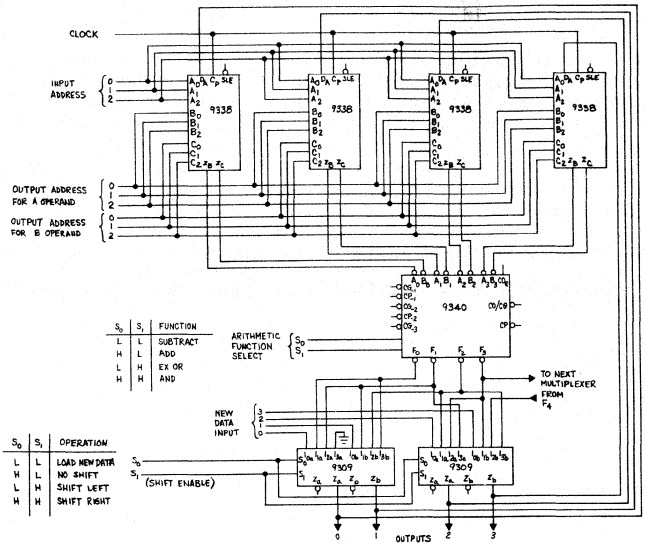


Figure 7. Three-Address Arithmetic Unit with Eight Registers.

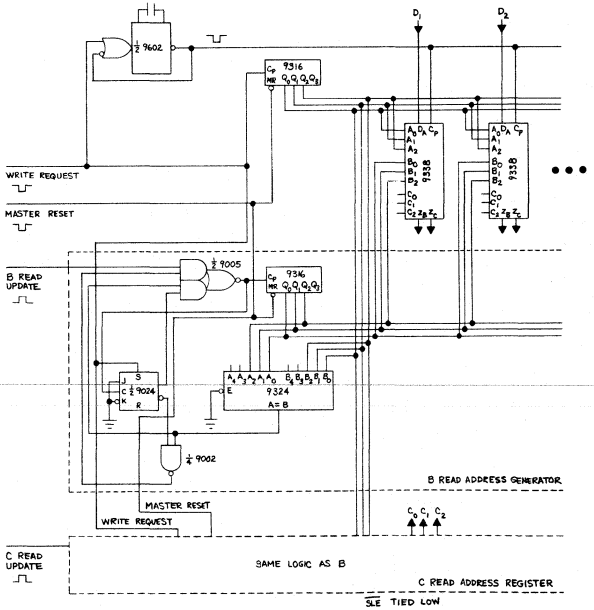


Figure 8. First-In First-Out Memory.

Serial Expansion Capabilities

9338's may be extended serially to get m banks of n bits each by designing several n-stage registers and multiplexing the outputs. Figure 6 shows the case where m = 2, i.e., 16 registers. More banks could be added by extending the addressing scheme, using larger multiplexers and a decoder to drive the clock inputs. The information is written into the required register bank by pulsing the clock line. The master/slave arrangement functions properly with this clocking scheme but may be defeated by tying $\overline{SLE}$ low, of course.

The A, B and C address lines consist of four lines each. The three low-order bits (A_{0-2}, B_{0-2}, C_{0-2}) are common to all 9338's and are organized as in Figure 6. The high-order bit (A_3, B_3, C_3) defines which bank is to be operated on. Bit A_3 is used to gate the clock pulse to one of the banks. This pulse will load all of the data bits into the bank defined by A_3 and the position defined by A_{0-2}. Bits B_3 and C_3 are used to select which bank's information is passed through the multiplexers.

Three-Address Arithmetic Unit with Eight Registers

The primary intended usage for the 9338 is as a one-bit slice of eight registers/accumulators to be used with an arithmetic logic unit. A four-bit section of such a system is shown in Figure 7. This is easily expandable to a larger word length.

The section uses four 9338 eight-bit multiple port registers and two 9309 dual 4-input multiplexers in conjunction with a 9340 four-bit arithmetic unit. The system provides eight storage registers, any of which may be used as accumulators, data registers, or scratch pad memory.

Because of the manifold capabilities of the 9340, this design results in a flexible arithmetic unit. One or two words can be written into the 9340 and operated on according to the two select lines. The output can be fed back to the registers into the same or a new location, and it may be shifted left or right by the multiplexers before being reloaded. New data is also entered through the multiplexers. Two words may be operated on by the 9340 at the same time new data is being loaded for increased speed.

This configuration results in an arithmetic unit capable of operating by itself, without additional access to the main memory. The unit can execute short subroutines extremely rapidly by using the eight registers provided by the 9338. The shifting capability provided by the multiplexers permits multiplication and division to be performed.

With additional gating this section could be part of a BCD arithmetic unit instead of the hexadecimal (binary) mode described here.

First-In First-Out Memory

Figure 8 shows a first-in first-out memory using 9338's. The memory

is capable of storing eight words in the order they are received and reading them out in this order. The writing and reading out by two different requesters is completely asynchronous, permitting the memory to act as a buffer between two systems operating at different speeds. Only the B read is used, but the C outputs may be used to provide a second independent readout.

A write clock causes a data word to be written and causes the next address code in order to be generated in a 9316 up binary counter (used as a modulo 8 counter) with address Ø following address 7. A new data word appears on the outputs of the 9338's whenever the read clock line is pulsed. Since the $\overline{SLE}$ line is high the outputs are isolated from the inputs and will only change following a read clock.

Problems occur when the address of the read 9316 counter is the same as that of the write 9316 counter. This situation is monitored and signaled by the 9324 comparator. There are two ways this can come about. If the read counter catches up to the write, the memory is empty and everything has been read out. Therefore, read clock pulses are inhibited. If the write counter catches up to the read, the memory is full and additional write pulses will cause data to be written into places which have not been read out. Since write requests must be honored, the data words are written and the read counter pulsed. This maintains the requirement that the first (oldest) word be the one available to be read out. The status of who caught up to whom is known in the 9003 latch by knowing which line was pulsed last, the read clock or write clock.

The first-in first-out memory is initiated by pulsing the master reset line, setting both counters to zero and the latch as if the read caught up to write. Now the read counter is inhibited until data is written into the memory. When data is written it is immediately available to the subsequent processors in the order it was written.

Uprated design features include a 16-word memory formed by adding another bank of 9338's. The control circuitry will handle this bank without additional hardware by utilizing the Q_3 outputs of the 9316 counters and the A_3 and B_3 inputs to the 9324 comparator. The write Q_3 output can be used to gate the clock line to the proper bank for writing and the outputs can be multiplexed by 9322's as in Figure 6.

Also, by using one 9366 up/down binary counter for both read and write address, a last-in first-out memory can be designed. A write clock increments the counter following a write into the memory. A read clock causes the counter to decrement. The current address would be the most current word written into the 9338 bank. If two words are to be read without a write, then the latest and the next latest word would be read. The terminal count output from the 9366 can be used to prevent the counter from overflowing or underflowing.

APPLICATIONS OF THE CCSL 9301 DECODER

INTRODUCTION

The Fairchild CCSL 9301 1-out-of-10 Decoder is a high-speed complex function integrated circuit suitable for use in high-speed digital equipment. This decoder has four inputs which act as an address to produce an output at the corresponding output terminal. It employs TTμL (Transistor-Transistor Logic) circuitry for high speed and has excellent noise margins with reasonable power consumption. The device has an input clamp diode at each input terminal to limit the negative swing of an input waveform and to considerably reduce adverse line reflection effects. The decoder is compatible with all other Fairchild CCSL (Compatible Current Sinking Logic) integrated circuits and is particularly suitable for use with other Fairchild complex-function integrated circuits. This decoder has applications in a large number of areas and considerably reduces the integrated circuit package count of a system, thereby simplifying packaging and increasing system reliability.

LOGIC DESCRIPTION

The logic diagram which includes pin layout and loading rules for the 9301 Decoder is shown in Figure 1. Input buffers are used to reduce input loading to that of a single TTμL gate input; the buffered signals are then decoded. The "A_0" terminal of the decoder is considered least significant so that an input configuration such as $A_0A_1A_2A_3$ would select output 1. The outputs from the decoder are active low level, which keeps power dissipation on the chip to a reasonable level and allows an inverting driver to be used between the decoder and other circuitry. Input configurations producing an address in excess of 9 will inhibit all outputs. The first three inputs (A_0, A_1, A_2,) can be interchanged and the device will still produce the correct outputs by relabeling the output pins. This may be convenient for layout of printed circuit boards.

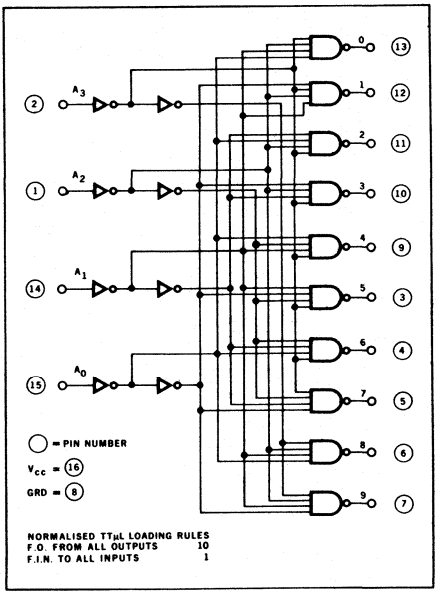


Fig. 1. CCSL 9301 1/10 Decoder logic diagram.

The propagation delay of the decoder will depend upon the output selected, but the longest path passes through two inverting buffers and a single gate to give a typical delay of 20 ns. Since the inputs of the decoder are buffered, it is not necessary to connect unused inputs to V_{CC}. Unused pins may be left open and no speed penalty is incurred.

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APPLICATIONS

For the following applications, the decoder is illustrated as a logic block in order to simplify the designs.

Address Decoding

The 9301 is a high-speed general-purpose decoder for use in decoding networks for all types of address selection. It is particularly suitable as an address decoder in high-speed ferrite-core, thin-film, and semiconductor memories. The device can be a 1-out-of-10 decoder, or a 1-out-of-8 decoder with inhibit by using the A_3 input as a control line. This active high inhibit facility allows more than three variables to be decoded by a combination of several 9301 decoders.

Figure 2 shows one method of decoding four binary digits (using two 9301 decoders) to produce 16 outputs. The register holding the input variables is a Fairchild 9300 Shift Register with the most significant digit of the binary word on the right. The shift register has active high outputs from all stages as well as an active low output from the last stage. The first three outputs of the register are inputs to the $A_0A_1A_2$ terminals of the decoders, and the active high output of the last stage of the register is the A_3 input to the first decoder and the active low output is the A_3 input to the second decoder. The design shows the outputs of the decoders driving inverting power gates which supply the fairly high currents required for addressing a memory of reasonable size. Alternate outputs (0, 1, 8, and 9) are available from the unused decimal outputs of the decoders.

An alternate method of 1-out-of-16 decoding is illustrated in Figure 3. The address, or source, register is comprised of TTμL 9020 Dual JK Flip-Flops. The active high outputs of the flip-flops are inputs to the first decoder to produce outputs 0 through 7, and the active low outputs of the flip-flops are inputs to the second decoder to produce the remaining eight decodes by relabeling the output pins. This scheme gives alternate outputs (6, 7, 8, and 9) and also loads each side of the address register equally. Other methods of decoding four variables using various input configurations to produce 16 outputs are possible.

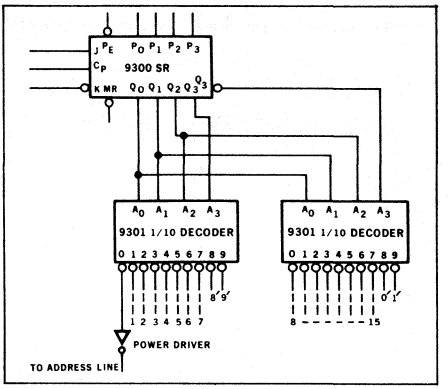


Fig. 2. 1-out-of-16 decode, method 1.

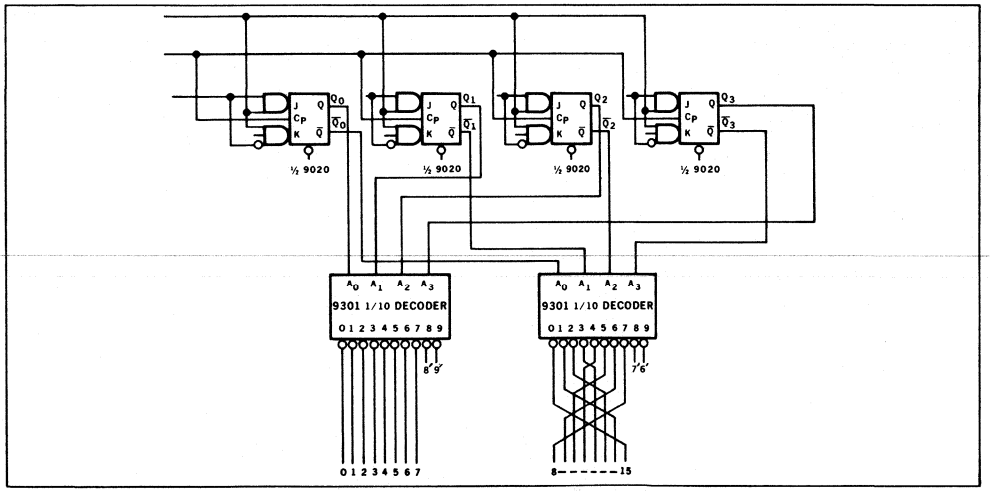


Fig. 3. 1-out-of-16 decode, method 2.

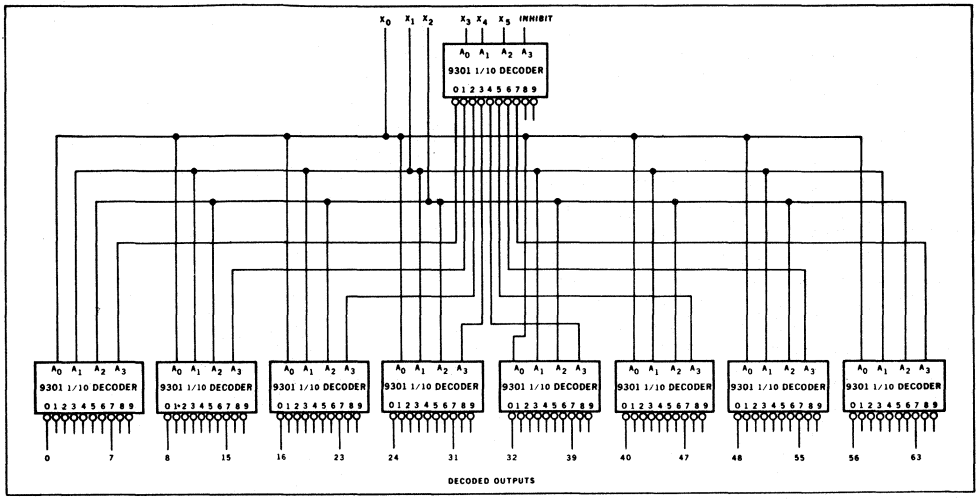
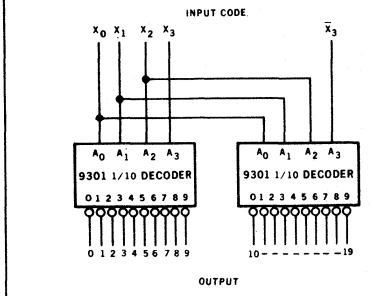


Fig. 4. 1-out-of-64 decode.

Figure 4 describes how a 1-out-of-64 decoder can be made using several decoders. The three most significant bits of the input address are decoded in the first decoder to produce eight outputs which are then used as gating signals. The three least significant address bits are inputs to the $A_0A_1A_2$ terminals of a bank of eight decoders. Each decoder in the bank is selected by the appropriate output of the first, or gating, decoder via the A_3 input terminal. The design in Figure 4 can be directly extended to produce a 1-out-of-80 decoder by having four most significant address bits and by using the two outputs, 8 and 9, from the gating decoder to control two additional decoders. The basic idea of using one or more decoders to select other decoders can be used to decode large address words. The propagation delay and loading of the lower significant address bits increase with word length.

Code Decoding

The 9301 Decoder can be used to decode codes other than binary. Figure 5 shows examples of decoding, commonly used weighted and unweighted 4-bit codes. Two decoders



DATA	OUTPUT SELECTION				
	8421	5421	4221	EXC. 3	4-BIT GRAY
0	0, 18	0, 18	0, 18	3	0, 18
1	1, 19	1, 19	1, 19	4	1, 19
2	2	2	2	5	3
3	3	3	3	6	2
4	4	4	6	7	6
5	5	8, 10	9, 11	8, 10	7
6	6	9, 11	14	9, 11	5
7	7	10	15	12	4
8	8, 10	11	16	13	14
9	9, 11	12	17	14	15
10					17
11					16
12					12
13					13
14					9, 11
15					8, 10

Fig. 5. Decode 4-bit codes.

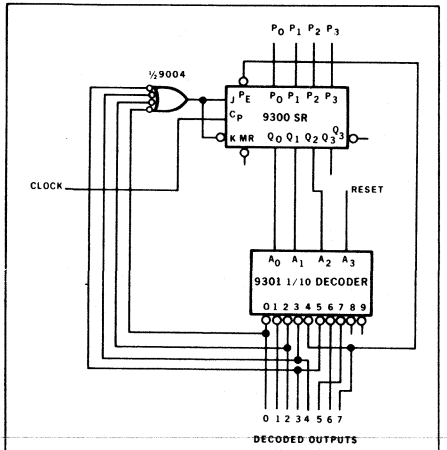
are required and the decoding scheme of Figure 2 is used. The outputs of the decoders are rearranged to produce the output decodes in the correct order. The table in Figure 5 gives the output selection with an alternate choice of outputs for some decodes.

The decoded outputs could be used to drive some form of display, such as a Nixie tube, via a high-voltage driver. Generally, the high speed of the 9301 decoder is not required for display applications. However, in a time-sharing display system, the high speed of the decoder will allow one decoder to service a great many display characters and could offer substantial cost savings.

Decoder in Counting Applications

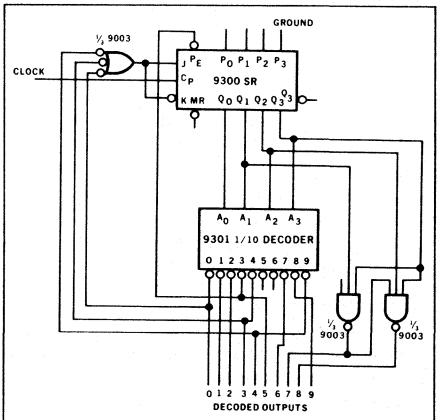
The 9301 Decoder can be used directly with a BCD 8421 Code Counter to produce ten decoded output signals. It may also be used for decoding and controlling nonweighted code counters. Figure 6 shows the 9301 Decoder, the 9300 Shift Register, and a 4-input TTμL gate forming a programmable decoded counter. Modulo counts from 1 to 8 can be selected by altering the configuration on the parallel inputs to the shift register according to the accompanying table. The first three stages of the shift register are inputs to the $A_0A_1A_2$ terminals of the decoder, and the A_3 terminal of the decoder is used as a reset. The shift counter counts through a sequence of states which can all be decoded by the decoder. Decoder outputs 0, 2, 3, and 5 are low active inputs to the 4-input low active OR gate and load a logic "1" in the shift register on the receipt of a clock pulse, thus enabling the counter to proceed through the chosen count sequence. State 001X of the counter is taken as the terminal state and when it occurs, the Parallel Enable facility is used to load the shift register to the configuration specified for desired modulo count. The counter has no persistent or "lock up" state and may be initiated by the A_3 active high inhibit terminal on the decoder. Since only the first three stages of the shift register are decoded, either a logical "1" or "0" can be loaded into the last register stage. This counter design can be extended to produce programmable counters with longer count sequences.

A similar scheme is illustrated in Figure 7 where a 9300 Shift Register is employed as a modulo-10 counter.



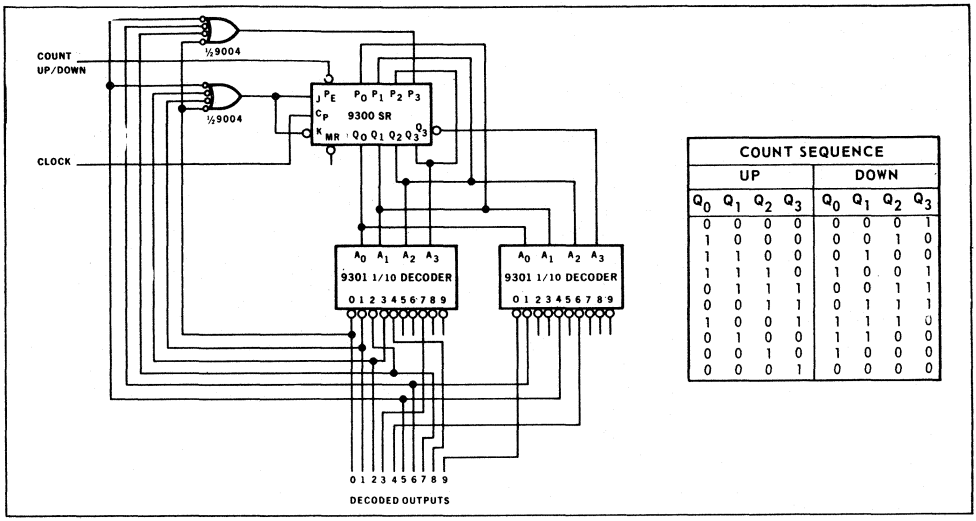
COUNT SEQUENCE				MODULO	PARALLEL INPUTS			
Q_0	Q_1	Q_2	Q_3		P_0	P_1	P_2	P_3
0	0	0	1	8	0	0	0	X
1	0	0	0	7	1	0	0	X
0	1	0	0	6	0	1	0	X
1	0	1	0	5	1	0	1	X
1	1	0	1	4	1	1	0	X
1	1	1	0	3	1	1	1	X
0	1	1	1	2	0	1	1	X
0	0	1	1	1	0	0	1	X

Fig. 6. Modulo-N counter with decode N = 1 to 8.



STATE	COUNT SEQUENCE				DECODE
	Q_0	Q_1	Q_2	Q_3	
0	0	0	0	0	0
1	1	0	0	0	1
2	0	1	0	0	2
3	0	0	1	0	4
4	1	0	0	1	9
5	1	1	0	0	3 PE
6	1	1	1	0	7
7	0	1	1	1	$Q_1 Q_3$
8	0	0	1	1	$Q_2 Q_3 \overline{7}$
9	0	0	0	1	8

Fig. 7. Decade counter with decode.



COUNT SEQUENCE							
UP				DOWN			
Q_0	Q_1	Q_2	Q_3	Q_0	Q_1	Q_2	Q_3
0	0	0	0	0	0	0	1
1	0	0	0	0	0	1	0
1	1	0	0	0	1	0	0
1	1	1	0	1	0	0	1
0	1	1	1	0	0	1	1
0	0	1	1	0	1	1	1
1	0	0	1	1	1	1	0
0	1	0	0	1	1	0	0
0	0	1	0	1	0	0	0
0	0	0	1	0	0	0	0

Fig. 8. Up-down decoded decade counter.

The outputs from the decoder are used to insert a logical "1" in the first stage of the shift register at the appropriate count via a three-input OR gate. The remaining logical "1" required for counting modulo-10 is inserted into the register by the parallel load facility of the shift register. The 9301 Decoder can decode only 8 of the 10 states of the shift register; the remaining 2 are decoded by auxiliary gates.

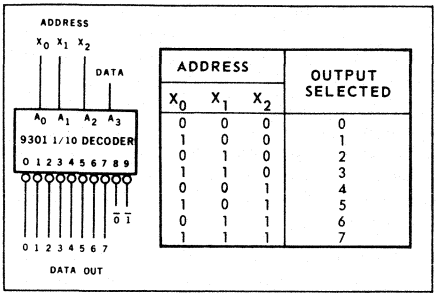
Figure 8 shows an up/down decoded decade counter. The parallel load facility is used to make the shift register effectively shift down by connecting each output of the register to the corresponding lower stage input. Two TTμL 9004 Gates are used to inject the logical "1's" in the shift register at the correct state to produce the two modulo-10 counts. Two 9301 Decoders decode the 10 states and also provide the required feedback waveforms.

Demultiplexing

Figure 9 illustrates the decoder used as an 8-output demultiplexer. The following truth table is arranged to show the effect of keeping the three inputs, $A_0A_1A_2$, constant while varying the polarity of the signal on the A_3 input.

The first three inputs select the appropriate output, and the logic level of the signal on the A_3 terminal determines its polarity. Therefore, data on the A_3 input is switched to the output terminal selected by the address, $A_0A_1A_2$. The last two outputs, 8 and 9, are the complement of the first two outputs, 0, 1. It should be noted that data does not suffer inversion when switched from the A_3 terminal to the selected output. The A_2 input of the decoder can also be used as a data input. In this mode, the A_3 terminal becomes an active high inhibit and inputs A_0 and A_1, a 2-bit address. Outputs 0, 1, 2, and 3 of the decoder are the assertion outputs of the demultiplexer and decoder outputs 4, 5, 6, and 7, their corresponding complements.

Inputs				Outputs									
A_0	A_1	A_2	A_3	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	1	1	1	1	1	1	1	1	1
0	0	0	1	1	1	1	1	1	1	1	1	0	1
1	1	0	0	1	0	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	0
0	0	1	0	1	1	0	1	1	1	1	1	1	1
0	0	1	1	1	1	1	1	1	1	1	1	1	1
1	1	1	0	1	1	1	0	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1
0	0	0	0	1	1	1	1	0	1	1	1	1	1
0	0	0	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	1	1	1	1	1	0	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1
0	0	1	0	1	1	1	1	1	1	0	1	1	1
0	0	1	1	1	1	1	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1	0	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1



ADDRESS			OUTPUT SELECTED
X_0	X_1	X_2	
0	0	0	0
1	0	0	1
0	1	0	2
1	1	0	3
0	0	1	4
1	0	1	5
0	1	1	6
1	1	1	7

Fig. 9. Decoder acting as 8-output demultiplexer.

The multistage decoding scheme can also be used for demultiplexers requiring a large number of output channels. Figure 10 shows a design of a 31-output demultiplexer. One decoder has two inputs to produce four active low outputs, which are then used to select one of four other decoders. The remaining inputs of the first decoder are used for input of data and gating.

Minterm Generator

The 9301 Decoder can function as a low active output minterm generator which produces the first 10 minterms of the possible 16 from four variables. The appropriate minterms can be summed with the use of a low active input OR gate. Figure 11 shows this method of producing a sum of minterms. The resulting Boolean function gives an active high output whenever the input word contains a single "1".

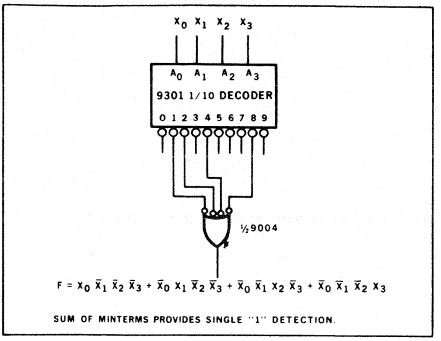


Fig. 11. Decoder acting as minterm generator to produce single "1" detection.

The design in Figure 12 is a gated full subtractor with two OR gates used to sum appropriate minterms, producing the required borrow and difference signals. Several decoders can be combined to generate minterms of additional variables. This technique is suitable for all kinds of control, sequencing, and decoding logic, and should simplify considerably the problem of generating a required sequence of outputs on a set of lines.

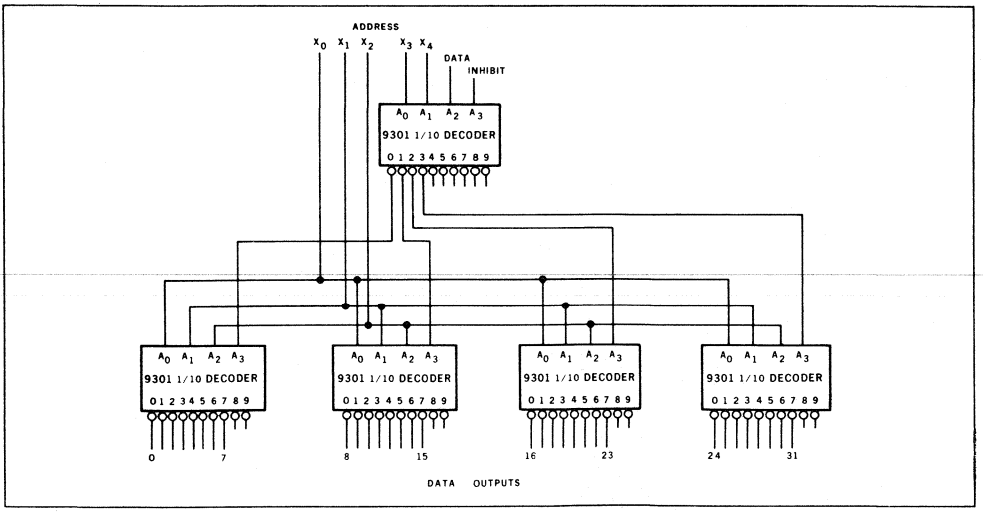


Fig. 10. Decoders used to form 31-output demultiplexer with inhibit.

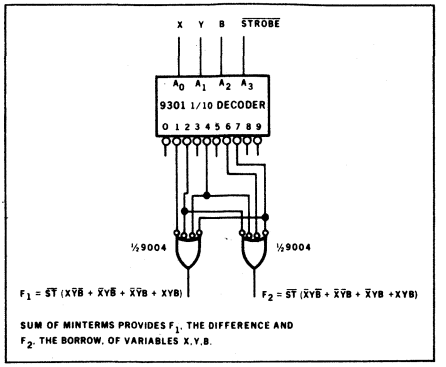


Fig. 12. Decoder acting as minterm generator to produce full subtractor.

SUMMARY

This Application Bulletin has described the operation of the 9301 1-out-of-10 Decoder and, by the applications illustrated, has shown the versatility of the device. This decoder is one of a number of standard high-speed digital logic blocks manufactured by Fairchild. The use of these complex logic blocks will have a large impact on the way future digital systems are designed and manufactured. In the past, the emphasis was on a minimum gate design; in the future, the effort will be to minimize the number of logic blocks and interconnections. Discrete integrated circuits will be used to "glue" larger digital blocks together. In the future, logic designers will specify logic black boxes and the main problem will be to interface one logic block with another, both logically and electrically.

The use of standard logic blocks enables a digital system to be implemented in a direct and simple manner. The logic design becomes similar to a system design, each block of logic being easily identifiable and directly implemented with one or more complex functions IC's. Circuit design complexity on the integrated circuit chip may be increased to improve functional use and representation. These standard logic blocks can be used to limit interconnections at the printed circuit level and, with duplicity of function, at a higher level. The advantages are a more modular, easily recognizable, and reliable digital system which is easier to design, commission, understand, and repair. Due to the smaller number of circuit and backboard connections, the noise and speed problems are considerably reduced compared to a conventional high-speed design.

9321 DUAL ONE-OF-FOUR DECODER/DEMULTIPLEXER

INTRODUCTION

The 9321 is a TTL/MSI one-of-four decoder consisting of two independent multipurpose decoders each designed to accept two inputs and provide four mutually exclusive active low outputs. These outputs are logically compatible with other Fairchild MSI products, permitting such functions as logic control and clock demultiplexing. Additional logic flexibility is provided by separate active low enables on each decoder. This device complements Fairchild's 9300 MSI line, providing demultiplexing, decoding, logic control, function generation and other decoding functions.

The 9321 uses TTL technology and is compatible with Fairchild's TTL family. It features high speed (22-ns typical delay), excellent noise margins, and input clamps to ground, which minimize the effects of line reflections.

The loading, pin names, and logic symbol chosen to represent the 9321 are shown in Figure 1.

DESCRIPTION

The truth table and logic diagram for the 9321 are shown in Figures 2a and 2b. Each decoder accepts two inputs and produces one low output corresponding to the logic combinations on the inputs. However, before any output can go low, the enable of the decoder must be low. The enable therefore can perform gating and control functions, framing data changes on the A_0A_1 inputs and determining the time that the outputs become active. Each enable can also be considered as an active high inhibit, disabling the decoder when a high logic level is present. If the enable is not used it should be tied to ground.

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SEMICONDUCTOR

All inputs of the 9321 are buffered, presenting only one TTL unit load to the driving circuitry, and the outputs offer a drive capability of ten TTL loads.

The number of gate delays in the longest path from the address inputs to outputs varies depending on the output selected. The worst-case selection is through the equivalent of three gate delays resulting in a typical propagation delay of 22 ns. The propagation delay for the enable is typically 15 ns, reflecting the fact that only two gate delays are present between the enable and outputs.

APPLICATIONS

The 9321 one-of-four decoder can satisfy many decoding, demultiplexing, and function generation requirements in digital systems. It is electrically and logically compatible with other Fairchild TTL/MSI functions. The 9321 is logically compatible because its active low outputs match the active low enable controls used on 9300 series devices. This makes the logic control and selection of other logic units possible without extra gates or inverters and their subsequent additional delay.

DECODING

The major uses of the 9321 are decoding for logic control and selection and for memory address decoding. To perform these decoding functions the 9321 can, of course, be used alone to provide one-of-four decoding. As shown in Figure 3, the decoder supplies the extra decoding necessary to address a word in a 64-word semiconductor memory. One 1/4-decoder is used to decode the two most significant bits of memory address and enable the appropriate memory units. The four least significant bits are decoded on the 4102. The high fanout capability of the 9321 would allow it to drive ten 4103 memory units with a word length of 40 bits without any additional buffers.

When larger decoding arrays are required, such as the one illustrated in Figure 4, the 9321 can be utilized. In this one-of-64 decoder each of the four 9311's is selected by one of the 9321 decoder outputs. Again, the two most significant bits are decoded by the one-of-four decoder and used to select the appropriate 9311 decoder. The dual AND-enable of the 9311 permits the use of one enable for selection and the other for strobing. It is preferable to frame decoder address changes at the last level to give higher enable switching speeds.

Even larger decoder arrays are possible by arranging both decoders in the 9321 and 16 9311 decoders in a 4 by 4, X-Y matrix to produce a 256-output decoder. Each of the one-of-four decoders, decoding two bits of the address, would enable the one-of-16 decoder when both decoders' low outputs coincide. The four address inputs of the 9311 decoder would again be connected in parallel.

Figure 5 illustrates an example of a special purpose decoder configuration possible with the 9321. Two independent decimal one-of-ten decoders, each with an active low enable, are formed with three 9321's. To provide this function with other logic elements would require four or more packages.

DEMULTIPLEXING

The 9321 can act as a demultiplexer, routing data from a single source to a destination chosen by the applied address. The data is applied through the enable and routed without inversion to the output determined by the address inputs (A_0, A_1). As before, all unselected outputs remain high. For example, with both address inputs high, output 3 will follow the state of the enable input, low when the enable is low and high when the enable is high. Demultiplexing can be employed for either data routing or clock distribution.

A two-bit data demultiplexer is shown in Figure 6. Two bits of active low data are routed to the outputs selected by the applied address, as shown in the table.

Clock demultiplexing for clock distribution and generation is readily accomplished with the 9321. Figure 6 shows a four-phase clock generator that will produce non-overlapping clock pulses for TTL or will drive MOS circuitry through interfaces. When driving TTL counters or registers, the usual clock input loading is two unit loads per four counter bits, allowing the 9321 to drive up to 20 bits of registers or counters. Note that the enable is tied to the clock input, eliminating glitches by framing address changes which occur when the flip-flops change state on the rising edge. Also the high state of an inactive output insures better TTL register and counter noise immunity by locking out the master flip-flops a majority of the time.

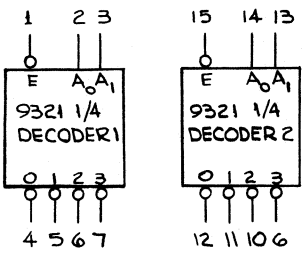
FUNCTION GENERATION

The 9321 can be considered to produce the minterms of two variables. These four minterms can be useful in some special applications replacing logic functions and thereby reducing the number of packages required in a logic network. The gate functions the 9321 can replace are shown in Figure 8a. Figure 8b illustrates a 9's complementor which utilizes these gate functions.

MSI DECODERS

There is a wide variety of decoders in the Fairchild TTL/MSI family. They can be divided into two groups, logic decoders/demultiplexers and decoder/drivers or decoders for display. The 9321 falls into the former category, offering dual one-of-four decoding for logic systems. The 9321 can be used for display purposes, but for most applications it would require drivers on its outputs. The other logic decoders/demultiplexers, the 9301 one-of-ten decoder and 9311 one-of-16 decoder, supply the decoding requirements for the rest of a digital system. The 9301 offers one-of-ten decoding and one-of-eight

demultiplexing or decoding with an enable control. The 9311 offers one-of-16 decoding and demultiplexing and features a dual enable, which is valuable when extending decoding arrays. These three decoders, used together or singly, will supply the decoding functions needed in any system.



LOGIC SYMBOL

PIN NAMES		LOADING
DECODER 1 AND 2		
$\overline{E}$	ENABLE (ACTIVE LOW) INPUTS	1 UNIT LOAD
A_0, A_1	ADDRESS INPUTS	1 UNIT LOAD
$\overline{0}, \overline{1}, \overline{2}, \overline{3}$	(ACTIVE LOW) OUTPUTS	10 UNIT LOADS

FIG. 1

TRUTH TABLE

$\overline{E}$	A_0	A_1	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

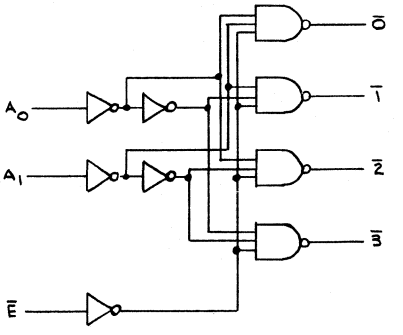
H = HIGH VOLTAGE LEVEL

L = LOW VOLTAGE LEVEL

X = DON'T CARE CONDITION

FIG. 2a

LOGIC DIAGRAM



*NOTE: ONLY ONE DECODER SHOWN

FIG. 2b

64-WORD SEMICONDUCTOR MEMORY

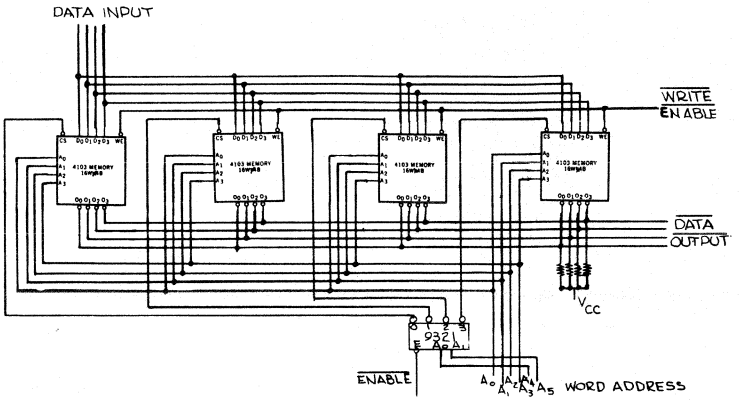


FIG. 3

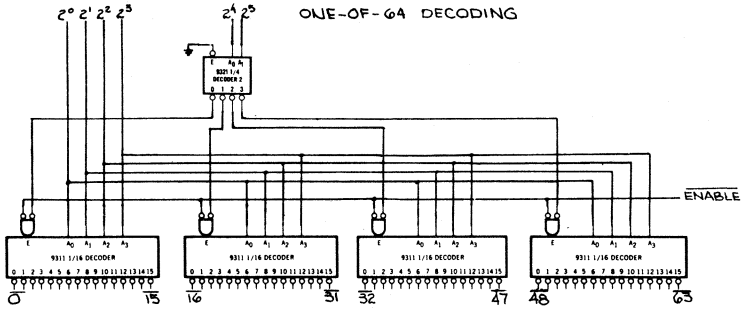
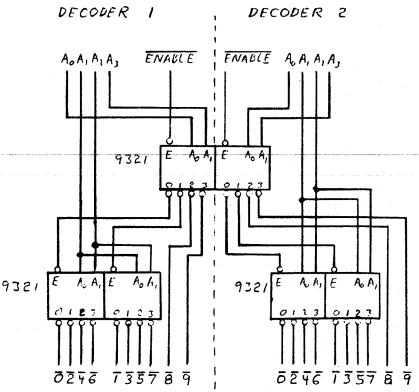


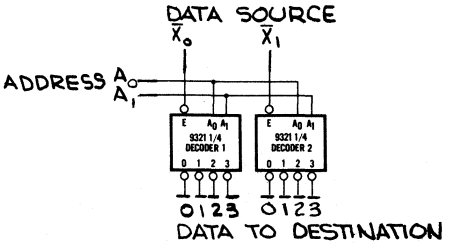
FIG. 4

FIG. 5



DUAL ONE-OF-TEN DECODER WITH ENABLES

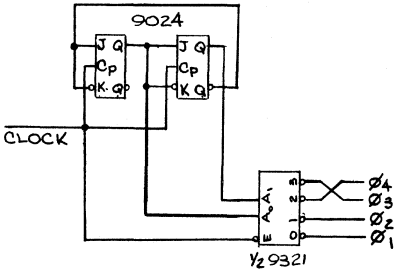
DATA DEMULTIPLEXER



A_0	A_1	OUTPUT SELECT
0	0	0
0	1	1
1	0	2
1	1	3

FIG. 6

4 ϕ CLOCK GENERATOR



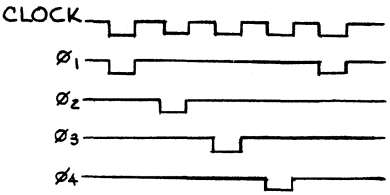


FIG. 7

FIG. 8a

GATE EQUIVALENTS OF 9321

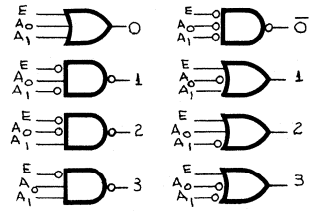
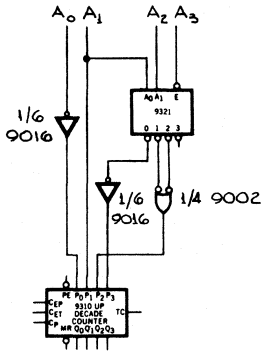


FIG. 8b

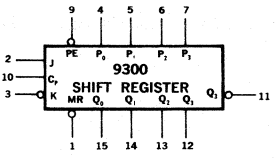


BCD NINE'S COMPLEMENTOR

CCSL 9300 SHIFT REGISTER

INTRODUCTION

The CCSL 9300 4-Bit Shift Register is a general-purpose, sequential, medium-scale integrated circuit which can be used in a wide range of digital applications. This application bulletin will provide information on the logical operation of this element, and, by the use of examples, show techniques for using the 9300 Shift Register as a general-purpose sequential element. The symbol used to represent the element along with pin connections and loading constants is shown in Fig. 1.



LOADING RULES (1 U L = 1 TTμL Gate Input Unit Load)

INPUTS	LOADING
J, $\overline{K}$, MR, P_0, P_1, P_2, & P_3	1 UL
PE	2.3 UL
C_P	4 UL
OUTPUTS	**FANOUT**
Q_0, Q_1, Q_2, Q_3, & $\overline{Q_3}$	6 UL

Fig. 1. Symbol for CCSL 4-bit shift register.

DESCRIPTION OF OPERATION

The logical operation of the CCSL 9300 Shift Register is indicated by the logic diagrams shown in Fig. 2. The element is composed of four clocked master-slave flip-flops

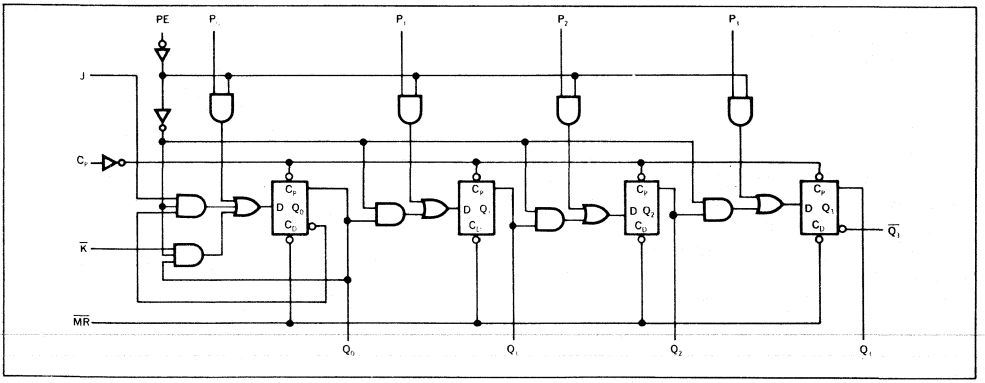


Fig. 2. Functional representation of the operation of the CCSL 9300 4-bit shift register.

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with D inputs. The D input of every stage can be switched between two logical sources by the Parallel Enable (PE) input. When the PE input is low, the D inputs of the four stages (Q_0, Q_1, Q_2, and Q_3) are logically connected to the parallel inputs (P_0, P_1, P_2, and P_3). When the PE input is high, the D inputs of stages Q_1, Q_2, and Q_3 are connected to the outputs of Q_0, Q_1, and Q_2, respectively, thus forming a 4-bit shift register. The D input to stage Q_0 with PE high is obtained from the J and $\overline{K}$ inputs via gating elements to produce the action of the first stage as shown in the truth table of Fig. 3. All stages are set to zero when the master-reset (MR) input is low, overriding the effect of any other input.

J	$\overline{K}$	Q_{n+1}
L	L	L
L	H	Q_n
H	L	$\overline{Q_n}$
H	H	H

Fig. 3. Truth table for J$\overline{K}$ input.

Special Features

The operation of the 9300 Shift Register includes several special logic features which enhance its usefulness in register and counter applications and reduce or eliminate discrete IC gates used in these applications.

The J$\overline{K}$ Input

The truth table for the J$\overline{K}$ input is shown in Fig. 3. This input is the same as the more common JK input except that the low-voltage level activates the $\overline{K}$ input (as is indicated by the circle at the $\overline{K}$ input shown in Fig. 1). The high voltage level activates the J input so that connecting the J and $\overline{K}$ inputs together results in a D input. The truth table in Fig. 4 shows the comparison between the inputs required to control a J$\overline{K}$ flip-flop and a RS flip-flop. Notice there are twice as many "Don't Care" conditions (indicated by X's) for the J$\overline{K}$ input. This results in a reduction of the number of gates required to implement most input functions.

CHANGE		INPUT REQUIRED			
Q_n	Q_{n+1}	J	$\overline{K}$	S	R
L	L	L	X	L	X
L	H	H	X	H	L
H	L	X	L	L	H
H	H	X	H	X	L

The X's indicate that a specific high or low input is not required.

Fig. 4. J$\overline{K}$ and RS input requirements chart.

Synchronous Operation

Except in response to the master-reset input, the outputs of the 9300 Shift Register change only on the low-to-high transition of the clock input signal. As a result of this synchronous operation, much less external logic is required in most applications.

Buffered Clock Input

As indicated by the logic diagram in Fig. 2, the clock input is buffered so that only four loads are presented to the external logic. In addition to load considerations, the logic level input requirement of this buffer permits clock gating with a single NAND gate.

Q_3 And $\overline{Q_3}$ Outputs

The assertion (active high) output is provided for all four stages and both assertion and negation outputs are provided for the last stage. This feature often reduces discrete IC gating in counter applications.

Master Reset

A master asynchronous clear input allows the setting to zero of all stages independent of the condition of any other inputs.

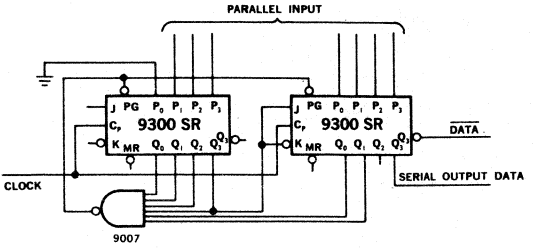
APPLICATIONS

The CCSL 9300 Shift Register is applicable to data handling, counting, and many other digital handling functions. A few examples are described on the following pages.

Data Handling

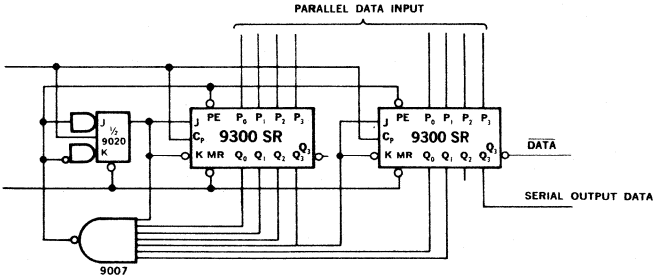
Parallel-to-Serial Conversion

Figure 5 shows two parallel-to-serial conversion circuits. The circuit in Fig. 5a is a 7-bit converter and illustrates the approach used when the number of bits to be converted is one less than an integral multiple of 4 bits. The circuit in Fig. 5b has an additional discrete flip-flop to produce an 8-bit converter. There is one additional flip-flop in both circuits to time the conversions, so that a marker bit



This converter uses a "0" marker bit to count the data bits shifted out. After the parallel load, which loads a "0" followed by 7 data bits, each shift brings in a "1". When the register contains six adjacent "1's", the output of the last stage is the last data bit from a previous load. At this time, the gate output becomes low, enabling a load on the next clock.

Fig. 5a. Seven-bit parallel-to-serial converter.



The 9-bit shift register shown is composed of two 9300 Shift Registers and one TTμL 9001 Flip-Flop. When the first 7 bits of this register are "1's", the TTμL 9007 Gate is enabled. The output of this gate enables the parallel load of the 9300's and supplies a "0" input to the flip-flop, so that on the next clock the register is loaded with a "0" followed by 8 bits of data. Seven clocks after the parallel load, the last bit of data is in the last position.

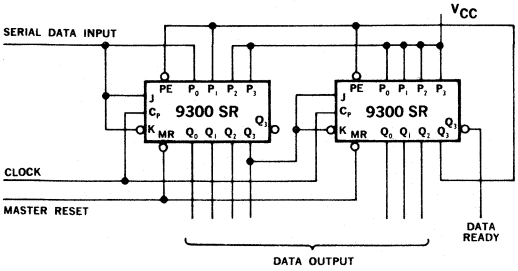
Fig. 5b. Eight-bit parallel-to-serial converter.

can be used to determine when the next parallel input must be loaded. The parallel load enable (PE) input to the shift register(s) is activated in both circuits when the shift register contains "1's" in all positions except the last two. At this time, the last position contains the last data bit for serial output from the previous parallel load, and the next-to-last bit contains a "0". Until this "0" was shifted into the next-to-last position, it held the PE input high during the shifting out of the data. The output of the gate driving the parallel load enable now goes low, so that on the next clock the next parallel data word will be loaded along with a new "0" marker bit.

Serial-to-Parallel Conversion

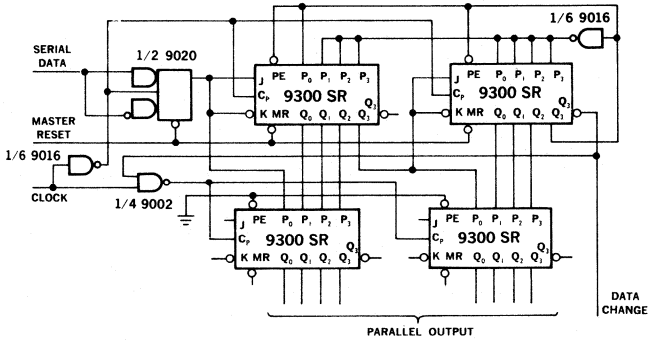
The 7-bit serial-to-parallel converter shown in Fig. 6 operates in a manner quite similar to the parallel-to-serial converter. When the register is full, a "0" marker bit has reached the last position of the register and provides a low signal to the PE, so that on the next clock a parallel load takes place. Loaded into the register will be the next data bit from the serial line plus the "0" marker bit followed by "1's" to fill the register. The $\overline{Q}_3$ output of the last bit in the register provides a signal to indicate when the register is full.

Figure 7 shows an 8-bit serial-to-parallel converter



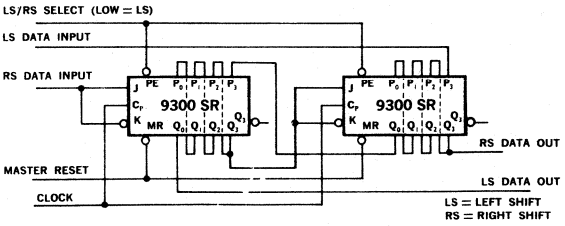
This converter counts the incoming data bits with a "0" marker so that a high signal results on the data-ready line when the next 7 bits of data are present on the seven data output lines.

Fig. 6. Seven-bit serial-to-parallel converter.



A high-to-low signal change on the data change output line indicates that the next 8 bits of data is present at the parallel output.

Fig. 7. Eight-bit serial-to-parallel converter with holding register.



This register shifts left or right on each shift clock. Shift direction is determined by the LS/RS select input.

Fig. 8. Eight-bit left-right shift register.

with two 9300's used as a holding register so that the parallel data will be available for more than one bit time. The $\overline{Q}_3$ output of the last bit position of the serial-to-parallel converter gates the clock into the holding register.

Left/Right Shift Register

The synchronous parallel inputs of the 9300 can be used to produce a register that will shift left or right on each clock. In Fig. 8 each 9300 has the Q_1, Q_2, and Q_3 outputs connected to the P_0, P_1, P_2 inputs, respectively, so that each element now shifts right when the parallel enable is high and left when it is low. For left shifting, Q_0 is the serial data output and P_3 is the serial data input.

Dual Input Shift Register

If data is to be shifted into a register from two sources, the synchronous parallel load capability of the 9300 can again be used to advantage. Figure 9 shows a 4-bit shift register where the P_1, P_2, and P_3 parallel inputs are connected to the Q_0, Q_1, and Q_2 outputs so that right shifting occurs independent of the condition of the PE input. The PE input now selects either the P_0 input or the $J\overline{K}$ inputs to the register.

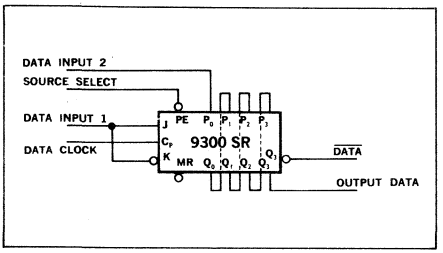


Fig. 9. Parallel-enable input is used to select serial-input source for shift register.

Counting

The 9300 may be used to produce a wide variety of counting circuits, including simple counters of different modulo, variable modulo counters, and up-down counters. The most economical approach to the design of a counter with the 9300 is the shift counter technique. Figure 10 shows the general state diagram of a 4-bit feedback shift register. Each state is identified by a decimal number which is the equivalent of the contents of the register taken as a binary number, and the first bit in the register taken in the least significant bit. Each state has two entrances and two exits. One exit results from shifting a "0" into the register, and the other from shifting in a "1".

A wide variety of loop sequences may be chosen from this state table (Fig. 10) by assigning "1" and "0" exits from successive states. Count sequences may be selected based on decode requirements, simplicity of feedback logic, or other system constraints.

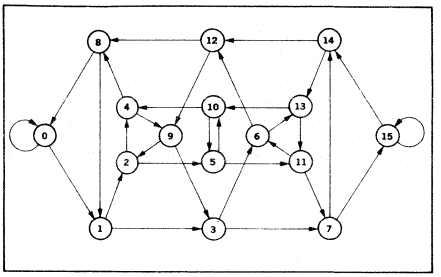


Fig. 10. General state diagram for a 4-bit shift register.

Feedback Shift Counting

The design of a feedback shift counter which uses the 9300 can be accomplished by several methods. One approach would be to select the desired sequence of states using the general state diagram shown in Fig. 10. Then, the necessary input functions would be developed to produce the selected sequence. On the first attempt to generate the input function, those states not appearing in the desired sequence (except the all "0's" and all "1's" states) can be considered as "Don't Care" conditions. However, it is necessary to check the states considered as Don't Care conditions against the generated input function to see that they do not form any unwanted loops. The all "1's" and all "0's" states are special cases since they may be persistent states (loops of one state). If an all "1's" or an all "0's" state is not wanted, this requirement can be taken into consideration on the initial development of the input function by supplying a "0" input for the all "1's" state and a "1" for the all "0's" state. If the unused states form a loop, it may be necessary to modify the input function to eliminate the secondary loop. Examination of the relationship between states in the desired and undesired loops will indicate which changes in the input function are required to eliminate the undesired loops. Except for the two-state (1010, 0101) loop, there are several distinct loops for all loop lengths. For example, there are 16 different loop sequences of length 16. The implementation of the necessary input function is much simpler for some loops than for others.

An example of this approach to the design of a feedback shift register is illustrated in Fig. 11. A 10-state loop is selected, and the Veitch diagrams for the J and $\overline{K}$ inputs are shown along with the resulting state diagram for the simplest gate implementation. With the simplest gate implementation

S

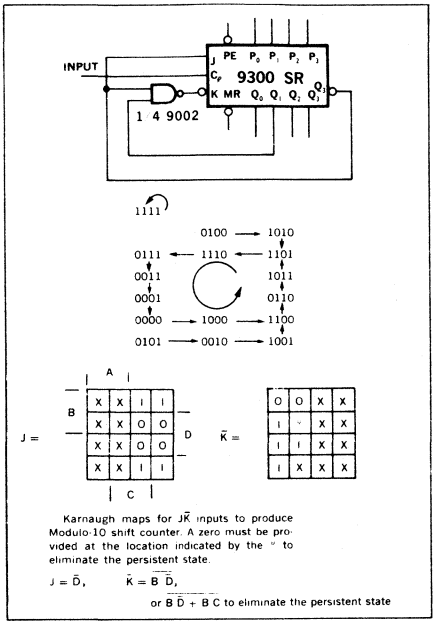


Fig. 11a. Modulo-10 counter with one loop and one persistent state (1111).

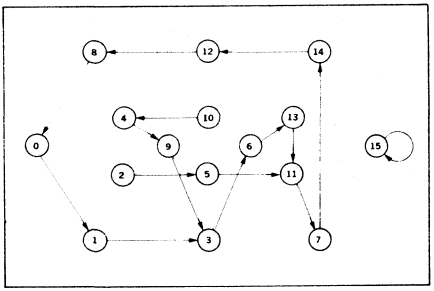


Fig. 11b. State diagram for a modulo-10 counter.

of the main loop, the all "1's" state is persistent. This condition can be relieved by several approaches. Figure 12 shows a new input function and its gate implementation which results in a "0" input for the all "1's" state. Another method of eliminating the all "1's" persistent state is to connect a 4-input gate as shown in Fig. 13 so that the all "1's" condition will produce a master-reset input. At least one stage will then be set to "0". Still a third approach will be discussed later under "Modulo-N Counters".

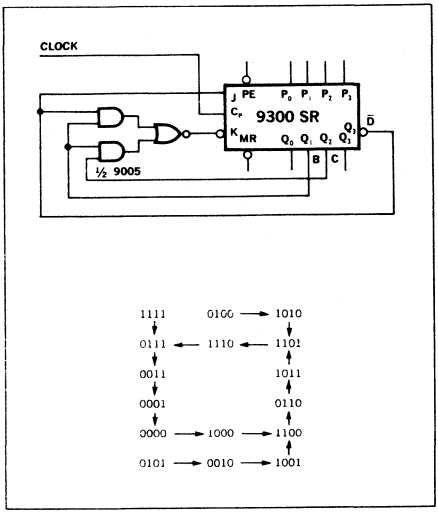


Fig. 12. Modulo-10 shift counter with one loop and no persistent states.

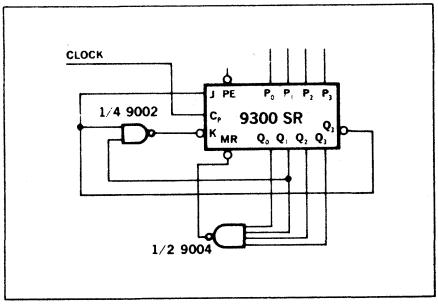
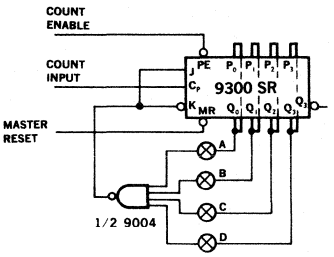


Fig. 13. Elimination of all "1's" persistent state by enabling Master Reset on the all "1's" condition. This will zero at least one stage.

Figure 14 shows a simple feedback consisting of a single NAND gate. The output of each stage is provided as an input to the NAND gate through a single-pole, single-throw switch. The accompanying chart shows the modulo and main loop sequence for various settings of the four switches. There are no persistent states and no other loops for all switch combinations shown (except for the second 8-state loop for the modulo-8 counter). Another possible use for the parallel load input is illustrated by the counter shown. The parallel inputs are connected to the corresponding stage outputs so that the counting action can be disabled by supplying a low signal to the PE input.



MODULO AS A FUNCTION OF SWITCH CLOSURES

SWITCH A	B	C	D	MODULO	SEQUENCE
C	Ø	Ø	Ø	2	5 10
C	C	Ø	Ø	3	6 13 11
C	C	C	Ø	4	7 14 13 11
C	C	C	C	5	7 15 14 13 11
Ø	C	C	C	6	7 15 14 12 9 3
Ø	Ø	C	C	7	7 15 14 12 8 1 3
Ø	Ø	Ø	C	8	7 15 14 12 8 0 1 3
					OR 6 13 10 4 9 2 5 11

C = CLOSED Ø = OPEN

STATES ARE DENOTED BY THE DECIMAL EQUIVALENT OF THE BINARY NUMBER OBTAINED BY CONSIDERING THE LEFTMOST BIT AS THE LEAST SIGNIFICANT.

This circuit counts in the sequence shown in the table as a function of the setting of the four SPST switches. All states not in the loop for each modulo lead into the indicated loop, except for the modulo-8 counter that has the 16 states divided into two 8-state loops. The four outputs of the shift register are provided as inputs to the parallel inputs so that the parallel-load enable may be used to enable the counting operation. When the parallel-enable input is low, the shift register will load its own contents on each clock, thus disabling the counting operation.

Fig. 14. Variable modulo counter.

Another approach to the generation of a count sequence with a feedback shift register is to first generate a simple sequence such as that which might be obtained by toggling the first stage whenever the last stage is "0". This simple function will produce a loop of $(2^n - 1)$ states and a single all "1's" persistent state for the values of n = 2, 3, 4, 6, 7, 15, and 22. Figure 15 shows a 9300 connected in this manner and the resulting sequence of states. Examination of this sequence will show that a 10-state counter will result if a jump is caused from the 1000 state to the 1100 state. It is only necessary to inhibit the reset of the first stage to obtain this jump. Further examination of the sequence will reveal that the inhibit function is simply the Q_2 output. This approach results in exactly the same counter as obtained by the previous methods.

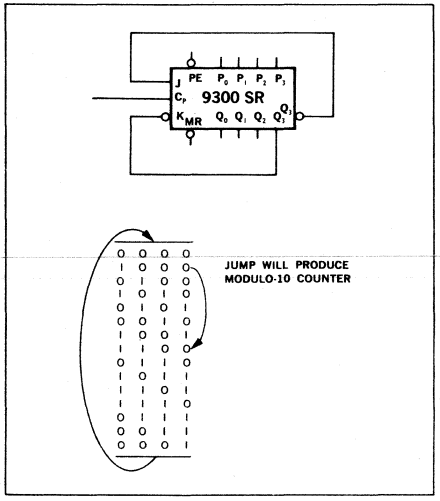


Fig. 15a. Simple feedback produces modulo-15 counter.

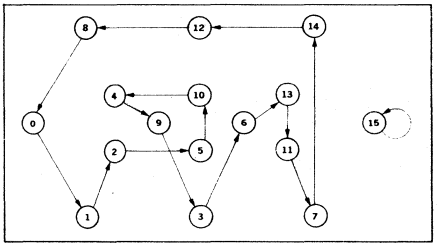
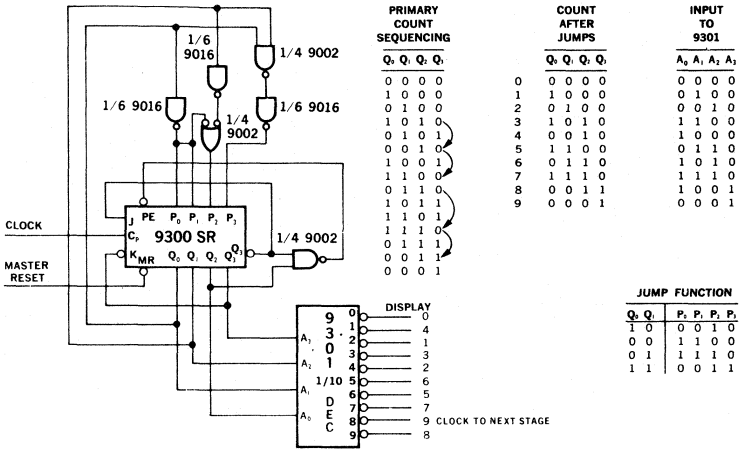


Fig. 15b. Fifteen-state loop that results from toggling the first stage when the last stage is "0".

The parallel load feature may also be used in the generation of count sequences. Figure 16 shows a 9300 shift register with the simple feedback used in the previous example, but this time the modification of the state sequence is accomplished in such a way that a parallel load is caused whenever the last two stages are "1, 0". The constant loaded at this time is generated as a function of the condition of the first two stages as is shown in the Jump Function table. The resulting 10-state sequence can be used as input to the 9301 1-out-of-10 Decoder to produce a 1-out-of-10 output if the output of the 9300 is connected to the inputs of the 9301 as shown.

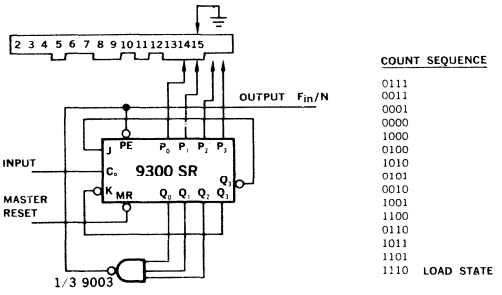


A simple-to-implement count sequence is modified by parallel-loading when the Q_2, Q_3 stages are "1", "0", respectively. The state loaded results in a jump in the sequence so that the outputs of the 9300 shift register may be used as inputs to a 9301 Decoder.

Fig. 16. Decade counter with 1-out-of-10 output.

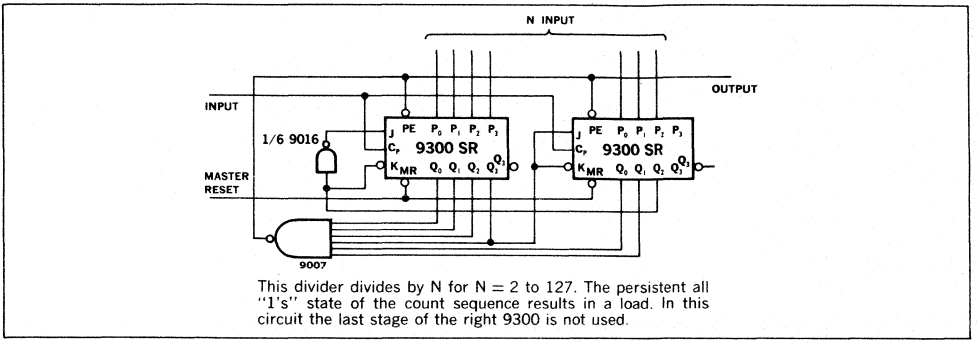
Variable Modulo Counters

Another use for the parallel input is illustrated by the variable modulo or divide-by-N counter shown in Fig. 17. Again, the simple feedback (toggle the first stage when the last stage is "0") is used. This time a single gate is used to produce the parallel load signal whenever the last three stages contain all "1's." The parallel input combination to be loaded into the register is determined by the slide switch. The arrow indicating the connection of the slide switch to ground also indicates the modulo of the count selected by that position of the slide switch. This simple slide switch



This circuit produces an output pulse for every N-input pulse. The number N is determined by the position of the slide switch shown. The persistent all '1's" state results in a load. (N = 15 is shown above.)

Fig. 17. Divide-by-N counter for N = 2 to 15.



This divider divides by N for N = 2 to 127. The persistent all "1's" state of the count sequence results in a load. In this circuit the last stage of the right 9300 is not used.

Fig. 18. Programmed divider.

0000000	0011100	1111000	0000110
1000000	1001110	0111100	1000011
0100000	0100111	1011110	1100001
1010000	0010011	0101111	1110000
0101000	0001001	0010111	0111000
1010100	0000100	0001011	1011100
0101010	1000010	0000101	0101110
1010101	0100001	0000010	1010111
1101010	0010000	1000001	1101011
0110101	1001000	1100000	1110101
0011010	0100100	0110000	1111010
1001101	1010010	1011000	0111101
1100110	0101001	0101100	0011110
0110011	0010100	1010110	1001111
0011001	1001010	0101011	1100111
0001100	0100101	0010101	1110011
1000110	0010010	0001010	1111001
0100011	1001001	1000101	1111100
0010001	1100100	1100010	0111110
0001000	0110010	0110001	1011111
1000100	1011001	0011000	1101111
0100010	1101100	1001100	1110111
1010001	0110110	0100110	1111011
1101000	1011011	1010011	1111101
0110100	1101101	1101001	1111110
1011010	1110110	1110100	0111111
0101101	0111011	0111010	0011111
0010110	0011101	1011101	0001111
1001011	0001110	1101110	0000111
1100101	1000111	0110111	0000011
1110010	1100011	0011011	0000001
0111001	1110001	0001101	

Sequence obtained by toggling the first stage when the last stage is "0".

Fig. 19. Count sequence for 7-bit feedback shift register.

input is another advantage of the shift counting method. Also note that the persistent all "1's" condition is interpreted as the parallel load condition and will result in a return of one of the loop states. The divide-by-N counter shown in Fig. 18 is simply an extension to 7 bits of the 4-bit divide-by-N counter just discussed. Figure 19 shows the count sequence for the 7-bit version.

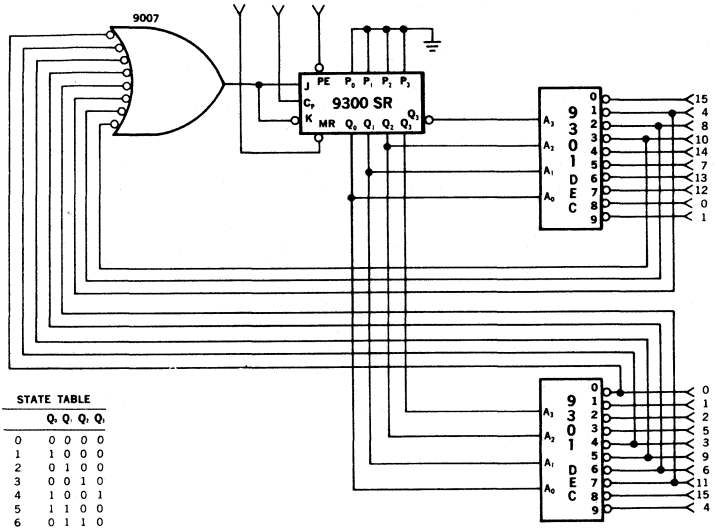
Figure 20 shows a divide-by-N counter for N = 2 to 16 with full decoding of all states. As shown, the counter counts from state "0" to a selected terminal state. A terminal state may be selected by feeding back that decoded state to the PE input.

Multi-Stage Program Divider

Divide-by-N counters are difficult to use in a large number of program divider applications due to the unwieldy nature of the N-input format when large values of a variable N input are required. This can be overcome by building the counter in stages. Since the decimal number system is most popular, the following examples are shown with decade stages, although most techniques discussed could be applied to other systems.

Figure 21 shows a simple, fully synchronous 2-stage decade counter. Each stage counts down modulo-10, with the first stage gating the clock to the second stage when it is in the zero condition. When both stages are in the zero condition, the parallel load is enabled, thus setting the value of N into the 2-decade stages. Since the decade count "00" is included in the sequence, the counter counts one more than the value of N loaded. Each additional decade stage using this approach requires either much more logic or a reduction in the operating speed.

A novel approach to the construction of a decade programmable counting stage is one that utilizes trickle-down clocking between stages and requires no additional logic or speed reduction even when a large number of stages are used is shown in Fig. 22. This counter uses states not within the main loop to solve two of the problems associated with this approach. The feedback to produce the modulo-10 count is the same as before and the 4-input NAND gate is added to eliminate the all "1's" persistent state. A clock (low-to-high transition) is provided to the next more significant stage when

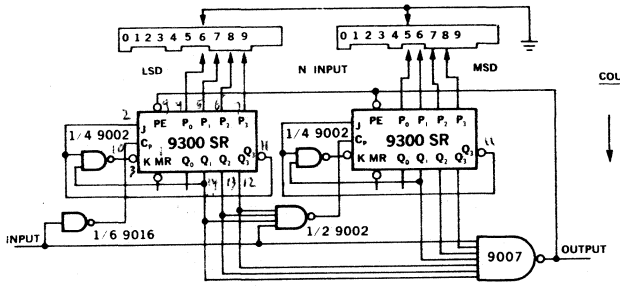


STATE TABLE

	Q_3	Q_2	Q_1	Q_0
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	0	0	1	0
4	1	0	0	1
5	1	1	0	0
6	0	1	1	0
7	1	0	1	1
8	0	1	0	1
9	1	0	1	0
10	1	1	0	1
11	1	1	1	0
12	1	1	1	1
13	0	1	1	1
14	0	0	1	1
15	0	0	0	1

The modulo of this counter may be controlled by providing PE with one of the decoded state. The skipped states (see state table) are those states between the decoded state to PE and state "0". Note that the decodes of states 0, 1, 8 and 9 are each available on two outputs.

Fig. 20. Divide-by-N counter with decoding for N = 2 to 16.



COUNTING STATES

9	0011
8	0001
7	0000
6	1000
5	1100
4	0110
3	1011
2	1101
1	1110
0	0111

This circuit divides by any number N from 1 to 100. The selected N is one greater than is shown on the slide switches. As an example, the switches show 56, therefore the circuit will divide by 57.

Fig. 21. Two-stage decade programmable divider.

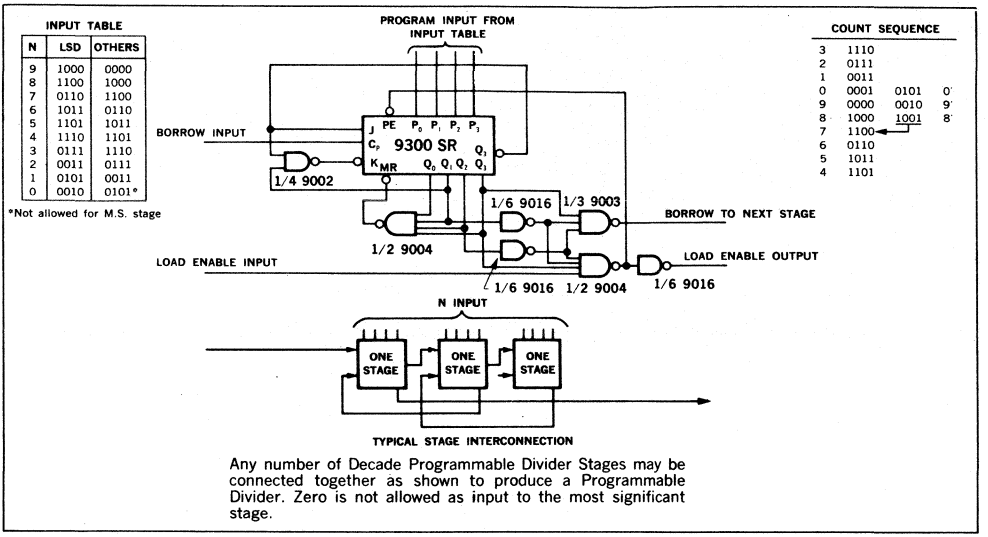


Fig. 22. Decade programmable divider stage.

the counter leaves a state that has 001 as the contents of the last three stages. The parallel load is enabled when a load enable is received indicating that all higher order stages contain a "0", and this stage contains a "0". The divider counts down from the previously loaded N-input until the all "0's" condition is achieved, at which time all generated clock outputs and parallel enables are low. The next clock into the least significant stage causes the loading of that stage from the least significant decade of the N-input. At this time the first problem presents itself. If a "0" is loaded as the least significant decade, there will be no clock produced to the next higher stage, and thus no action of the counter. All parallel enables and all clocks will remain low. The problem may be solved by not loading "0" as shown in the count sequence, but loading "0'". The transition from "0'" to "0" requires ten input pulses so the counting action is not changed. As usual, however, this produces another problem. If a "0'" was to have been loaded, the next clock after the clock that caused the load should result in a clock from the least significant stage to the next more significant stage. Since "0'" was selected because it will NOT provide a low clock output, this will not happen. The clock to the next stage is instead produced when leaving the "8'" state. Although a little late, the same result is accomplished as long as "0" is not allowed as the N-input for the most significant stage.

Now that the first problem is taken care of, the second problem must be solved. The counter will count by N + 1 again if the value N is loaded after the all "0's" condition. Since the "8'" condition produces a clock, it is only necessary to make a slight change in the loading table for the least significant decade. In effect, the state loaded in the least significant decade is the one which would result after the next input clock, except for the state "1" in which case "0'" is loaded in place of "0".

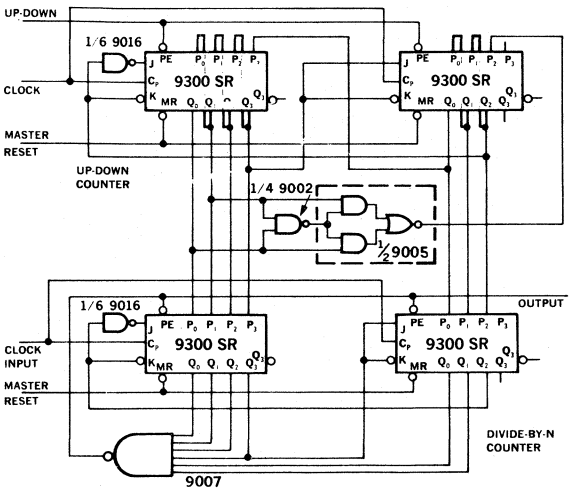
Miscellaneous Applications

One method of generating the inputs required by the 7-bit shift counter (Fig. 18) would be to supply the inputs from an up-down counter that counts in the same sequence. To reverse the count of the simple sequence shown in Fig. 19, it is only necessary to implement a left/right shift register as shown in Fig. 8 and supply a "0" to the left shift input when the first two stages are different. This follows the simple feedback rule of toggling the first stage whenever the last stage is "0". Putting all this together results in Fig. 23. The up-down input in some applications could be considered as a correction input to adjust the divide ratio to maintain a desired output clock frequency.

The binary-to-BCD converter shown in Fig. 24 is a simple implementation of a well-known conversion algorithm.

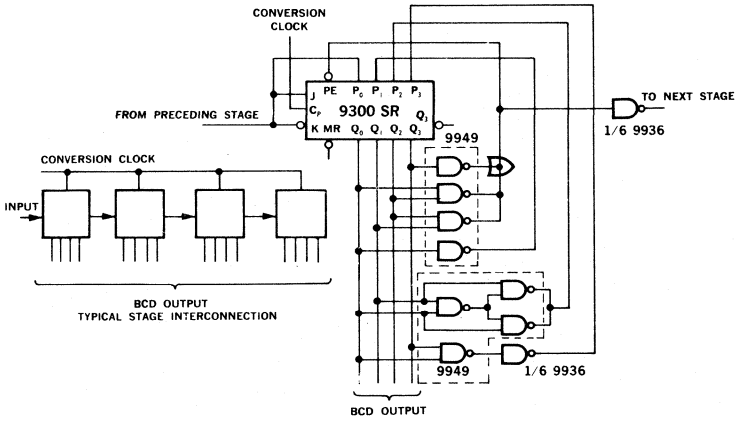
SUMMARY

The Fairchild CCSL 9300 4-Bit Shift Register is a general-purpose sequential building block which is not limited to the uses implied by its name, but is useful in a wide range of sequential digital applications.



The up-down counter counts in the same sequence as the divide-by-N counter. The frequency of the output can be incrementally changed by inputs to the up-down counter. This circuit could be used to generate a clock that would follow the frequency of an incoming signal.

Fig. 23. Divide-by-N counter with N-input from up-down counter.



A binary number shifted, most-significant bit first, into a number of stages large enough to hold the results, will be converted to BCD after the clock shifts the last bit into the converter.

Fig. 24. Binary-to-BCD converter.

TTL/MSI QUAD 2-INPUT MULTIPLEXER

The 9322 Quad 2-Input Multiplexer is another member of the Fairchild TTL/MSI family. It consists of four multiplexing circuits with common select and enable logic. Each circuit consists of two inputs and one output where the data on one of the inputs is allowed to appear on the output line according to the level of the select line. It is the logical implementation of a four-pole two-position switch, with the position of the switch being set by the logic level supplied to the one select input. The enable line can disconnect both inputs from the output, forcing the output low. The logic symbol and diagram are shown in Figure 1. The truth table for each section is given in Figure 2.

A common use of the 9322 would be for moving data from a group of registers to four common output busses. The particular source of the data would be determined by the state of the select input. A less obvious use is as a function generator. The 9322 can generate four functions of two variables if one variable is common to all four functions. This is useful for implementing gating functions.

This device features the following:

- Multifunction Capability
- 20-ns Through Delay
- On-Chip Select Logic Decoding
- Fully Buffered Outputs
- TTL Compatible Characteristics Provide Easy Interfacing with Fairchild DTL, LPTTL, TTL, and MSI Families.
- Input Clamp Diodes Limit High Speed Termination Effects

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Applications

This Applications Brief is intended to be a short description of the capabilities of the 9322 rather than a treatise on multiplexing. Additional information on multiplexing is available in Fairchild Application Note 181 (APP-181) which covers the 9312 8-input multiplexer and the 9309 dual 4-input multiplexer.

Data Routing

The obvious use of a multiplexer is to route data from one of several locations to one location. One application of this is shown in Figure 3. This system displays the contents of one of two counter register banks composed of Fairchild TTL/MSI 9310 decade counters.

Counter 1 is connected to the I_0 parallel inputs of the 9322's and counter 2 to the I_1 inputs. The choice of which information will appear at the output is controlled by the state of the counter select line. If it is low, the information from counter 1 will be the output of the multiplexer; if high, counter 2's information is the output. This is then stored in 9308 dual 4-bit latches. After storage it is decoded in 9317 seven-segment decoders which can drive directly a seven-segment incandescent lamp display. Notice that the four-unit-in-a-pack switching capability of the 9322 matches the capacities of the 9310 and 9308 units and means that no external gating, interfacing, or buffering is required. This is an example of the functional as well as the electrical compatibility of the TTL/MSI 9300 line.

Another data routing application is as part of a 10-input, BCD-addressed multiplexer, shown in Figure 4. One 9322 and two 9312 8-input multiplexers can be used to route two sets of 10 inputs to two output lines. Addresses can be generated under the control of a 9310 decade counter or a 9306 up/down decade counter. This configuration is the most efficient for BCD operation because there are no unused states or inputs.

Digital Function Generation

The two-input multiplexer described here can produce any four functions of two variables without additional elements if both the assertion and negation of one variable is available, and if the other variable is common to the four functions. To produce these functions apply one of the variables, X, to the select line; and apply the other variable, Y, with values Y, $\overline{Y}$, "0", or "1", to the input terminals, I_0 and I_1. The procedure for implementing this function generator is:

1) Draw truth table
2) Construct Karnaugh map
3) Map area allotted to each input (I_0 and I_1)
4) Determine signal for each input by comparing the two maps.

This procedure, incidentally, is equally valid for implementing any function of three variables from a 9309 4-input multiplexer or using a 9312 8-input multiplexer as a function generator of four variables.

The 9322 is especially useful for generating functions of this form:

$$f_1 = (f_A)X + (f_B)\ \overline{X}$$

$$f_2 = (f_C)X + (f_D)\ \overline{X}$$

$$f_3 = (f_E)X + (f_F)\ \overline{X}$$

$$f_4 = (f_G)X + (f_H)\ \overline{X}$$

Let us illustrate this procedure:

It is desired that one variable Z be compared with four other variables V, W, X, and Y. Signals are required to show that Z is the same as the first, V, different from the second, W, that Z and X are both one's and Z and Y are both zero's. The truth tables and Karnaugh maps are:

1. 0_1 (output) = $VZ + \overline{V\ Z}$ (exclusive NOR)

V	Z	0
0	0	1
0	1	0
1	0	0
1	1	1

	Z	$\overline{Z}$
V	1	0
$\overline{V}$	0	1

2. $0_2 = \overline{W}\ Z + W\ \overline{Z}$ (exclusive OR)

W	Z	0
0	0	0
0	1	1
1	0	1
1	1	0

	Z	$\overline{Z}$
W	0	1
$\overline{W}$	1	0

3. $O_3 = X\ Z$ (AND)

X	Z	0
0	0	0
0	1	0
1	0	0
1	1	1

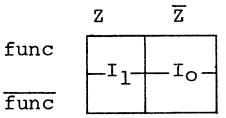
	Z	$\overline{Z}$
X	1	0
$\overline{X}$	0	0

4. $Q_4 = \overline{Y}\ \overline{Z}$ (NOR)

Y	Z	0
0	0	1
0	1	0
1	0	0
1	1	0

	Z	$\overline{Z}$
Y	0	0
$\overline{Y}$	0	1

The input area map will be for all cases:



Comparing the Karnaugh maps to the input area map yields the logic diagram shown in figure 5.

While it is true that these functions may be generated by standard NAND and NOR logic gates, the 9322 produces four different logic functions in the same module. If the configuration shown above were needed only once, then the designer would need portions of four different packages which would mean utilizing them in an inefficient manner.

Special Applications

Shift-Left, Shift-Right, Parallel-Load Register

As an example of a non-obvious use for a multiplexer, Figure 6 shows a shift-left, shift-right, parallel-load register. The 9300 shift register will right shift synchronously with the clock's low-to-high

transitions if the $\overline{PE}$ input is high. If $\overline{PE}$ is low, then the rising clock will enter the data on the P_0 thru P_3 inputs into the four stages of the shift register.

The multiplexer will feed to each parallel input either new data or the state of the stage to the right of each parallel input. This latter mode is the shift-left capability. The data on the Q_n output is multiplexed to be fed to the P_{n-1} input. On the next clock, the data is loaded into the n-1 stage and appears at Q_{n-1}, effectively shifted one stage to the left. The 9322 shifts the data or enters new data at the discretion of the process controller. Connections to preceding and following stages of a larger register are shown.

Using 9322's to provide shifting capability is useful in any unit which has parallel inputs and storage. The 9306 up/down decade counter, the 9310 decade counter, the 9316 binary counter, the 9338 multiple-port register and many more members of the Fairchild TTL/MSI line are all good candidates for this procedure to allow them to both shift and load using the 9322.

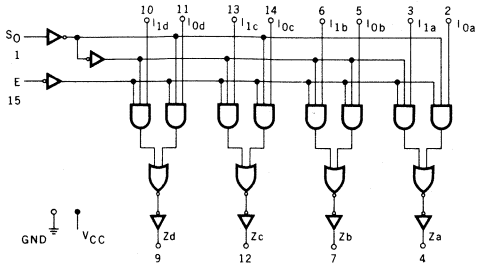
Four-Word Sorter

The configuration of 9322's and 9324 five-bit comparators shown in Figure 7 is used to compare and order four 4-bit words. The four words are applied as shown.

The result of the comparison of A and B in module 1 causes the larger of the two to appear at the outputs of module 2. Likewise the larger of C and D appears at the outputs of module 4 as a result of the decision of module 3. Module 5 compares these two larger words and causes the larger of these to appear at the output of module 6. Lines Z_0 and Z_1 indicate which of the four words appears here. If all of the words are identical Z_2 will be at a logic "0".

The operation is completely asynchronous. Therefore, when the result appears after worst-case propagation time, the resultant largest word can be stored and the word indicated by Z_0 and Z_1 can be set to all zero's. Now the new largest word will appear at the outputs of module 6. This procedure continues for a total of four storage operations. The words are now ordered and Z_2 should be at a logic "0".

This configuration may be extended to more bits or more words by the addition of more 9324's and 9322's.



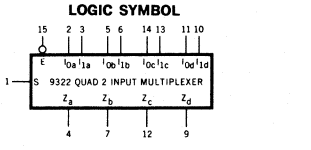


FIG. 1

TRUTH TABLE

ENABLE	SELECT INPUT	INPUTS		OUTPUT
$\overline{E}$	S	I_{0X}	I_{1X}	Z_X
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

Identical for Each Multiplexer

L = low voltage level
H = high voltage level
X = either high or low logic level

FIG. 2

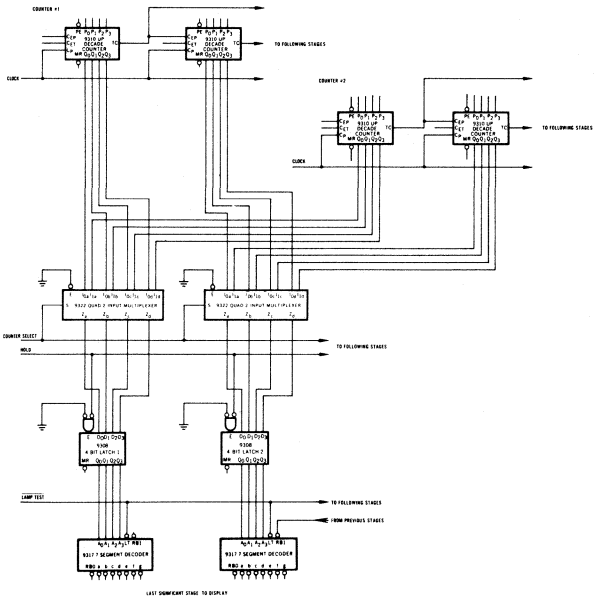


FIG. 3

DUAL 10 INPUT MULTIPLEXER

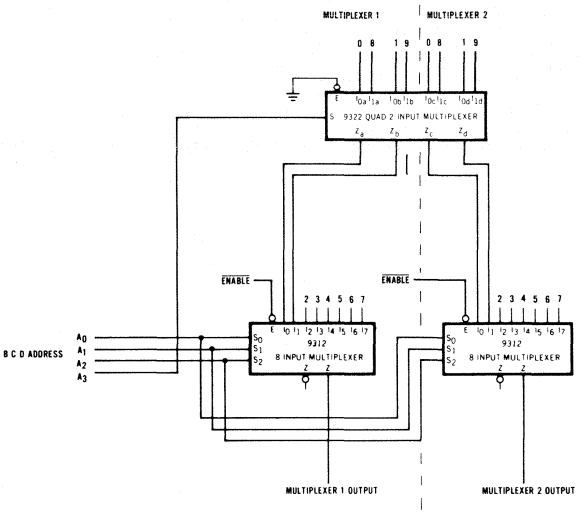


FIG. 4

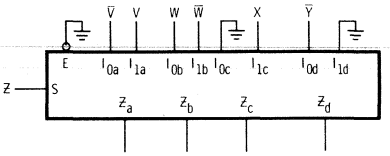
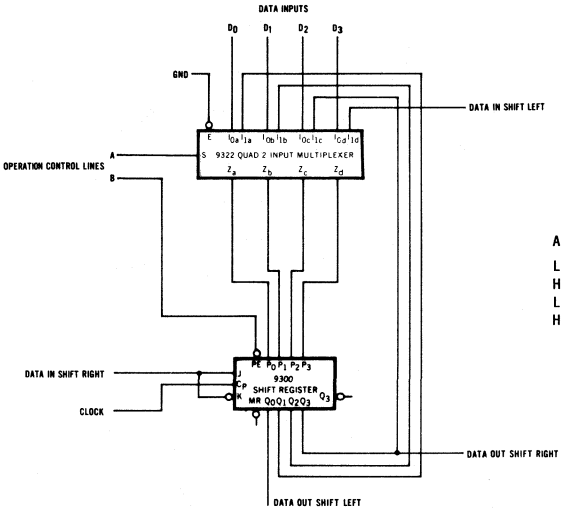


FIG. 5

SHIFT LEFT, SHIFT RIGHT, PARALLEL LOAD REGISTER



OPERATION CODE LIST

A	B	Operation
L	L	Parallel Load
H	L	Shift Left
L	H	Shift Right
H	H	Shift Right

This register will shift left, shift right, and load 4 bits of parallel data according to the operation code applied to A and B.

FIG. 6

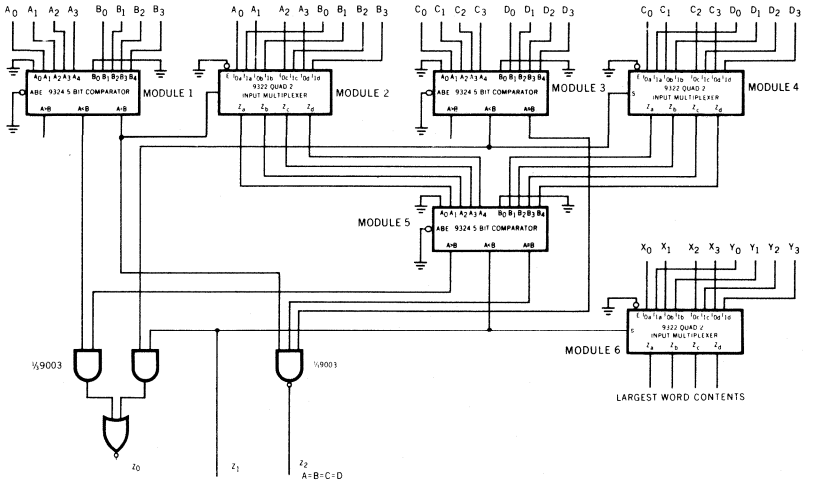


FIG. 7

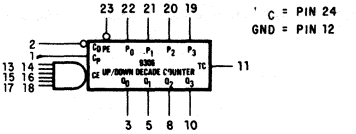
CCSL 9306 UP/DOWN BCD COUNTER

INTRODUCTION

The Fairchild CCSL 9306 Synchronous Up/Down Decade (1248) counter is an MSI circuit suitable for high speed operation. The device uses TTμL (Transistor-Transistor Micrologic) technology and has active pullup outputs which provide high speed and excellent noise margins with reasonable power consumption. Like other high speed TTμL and MSI devices, the 9306 incorporates input clamp diodes to ground to minimize adverse line reflection effects. Compatible with all other Fairchild CCSL integrated circuits, the 9306 is particularly attractive in combination with other Fairchild MSI 9300 series devices. The symbol used to represent the element, along with pin layout and loading constants, is given in Figure 1.

LOGIC DESCRIPTION

The logic operation of the CCSL 9306 Up/Down Counter is indicated by the logic diagram in Figure 2.



NORMALIZED $T^2\mu L$ LOADING RULES

INPUTS	
$C_D, CE_0, CE_1, CE_2, CE_3, CE_4, CE_5$	1 UNIT LOAD (U.L.)
C_P, PE	2 U.L.
P_0, P_1, P_2, P_3	$^2/_3$ U.L.
OUTPUTS	
Q_0, Q_1, Q_2, Q_3, TC	6 U.L.

Fig. 1. CCSL 9306 pin layout and loading constants.

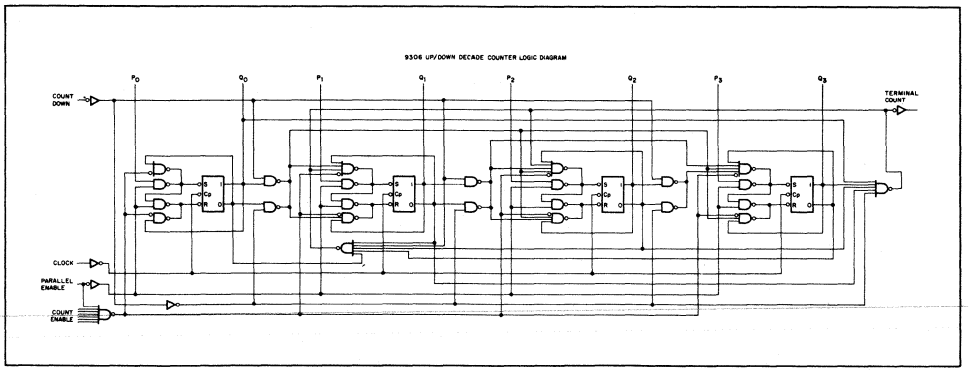


Fig. 2. CCSL 9306 logic diagram.

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CLOCKING

The element is composed of four clocked RS master-slave flip-flops and a number of gates. A clock buffer and inverter drive the four clock inputs of the flip-flops in parallel, insuring synchronous operation. When the clock input (CP) is low, the slave is quiescent, but data can enter the master via the R and S inputs. During the low-to-high transition of the clock, (1) the data inputs (R and S) are inhibited so that a later change in the input data will not affect the master; and (2) the information now trapped in the master is transferred to the slave and appears at the outputs. When the transfer is complete, both the master and the slave are steady (as long as the clock input remains high) regardless of the logic state at any other input to the device. During the high-to-low transition of the clock input, (1) the transfer path from master to slave is inhibited, leaving the slave steady in its present state; and (2) the data inputs (R and S) are enabled so that new data can enter the master. As a result of this synchronous operation, higher clock frequency is possible, and compared to an asynchronous counter, much less external logic is required in most applications.

MODE SELECTION

The control inputs--Parallel Enable (PE), Count Enable ($CE = CE_0 \cdot CE_1 \cdot CE_2 \cdot CE_3 \cdot CE_4 \cdot CE_5$) and Count Down Enable (CD)--select the mode of operation in accordance with the table in Figure 3. There are four different modes: count up, count down, preset, and no change. Any change in mode among these four must take place when the clock CP input is high. The one exception to this rule is a mode change to the preset mode.

PE	CD	CE	MODE
0	0	0	PRESETTING
0	0	1	
0	1	0	
0	1	1	
1	1	1	COUNT UP
1	0	1	COUNT DOWN
1	1	0	NO CHANGE, CLOCK INHIBITED.
1	0	0	

WHERE $CE = CE_0 \cdot CE_1 \cdot CE_2 \cdot CE_3 \cdot CE_4 \cdot CE_5$

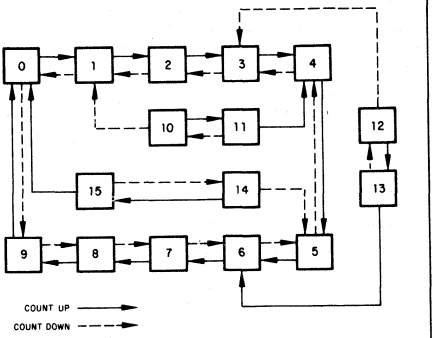
Fig. 3. Mode selection scheme.

PRESETTING MODE

The R and S inputs of each counter stage can be switched between two logical sources by the Parallel Enable (PE) input. When the PE input is low, the R and S input of the four stages-Q_0, Q_1, Q_2, and Q_3-are logically connected to form four clocked D-type flip-flops with the respective parallel input (P_0, P_1, P_2 and P_3) acting as type-D flip-flop inputs. The counter is in the presetting mode when the PE input is low, regardless of the logic state of any other input and can be preset to any number from 0 and 15. The counting sequence from codes greater than 9 is shown in Figure 4. The encoded number is applied to the parallel inputs (P_0, P_1, P_2 and P_3) and clocked in as explained in the section under CLOCKING.

COUNTING MODES

Two counting modes exist, one for count UP and one for count DOWN. The state diagram and the code table in Figure 4 describe the two modes in detail. The 9306 is a decade counter and has in its state diagram a loop with 10 stable states (0-9). When the counter is in one of 10 states in the loop, each clock pulse at the CP inputs changes the counter to the next state in the loop in forward or reverse direction, depending on the count mode selected. The state diagram also shows what happens when the counter is preset to a state outside the loop.



DECIMAL NUMBER	ENCODED NUMBER			
	Q_0(1)	Q_1(2)	Q_2(4)	Q_3(8)
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
10	0	1	0	1
11	1	1	0	1
12	0	0	1	1
13	1	0	1	1
14	0	1	1	1
15	1	1	1	1

Fig. 4. State diagram and code table.

MULTI-DECADE COUNTING

The CCSL 9306 decade counter has built-in carry/borrow circuitry for synchronous multi-decade counting, following the parallel carry/borrow scheme seen in Figure 5. The table in Figure 3 shows that the counting mode can exist only if CE is

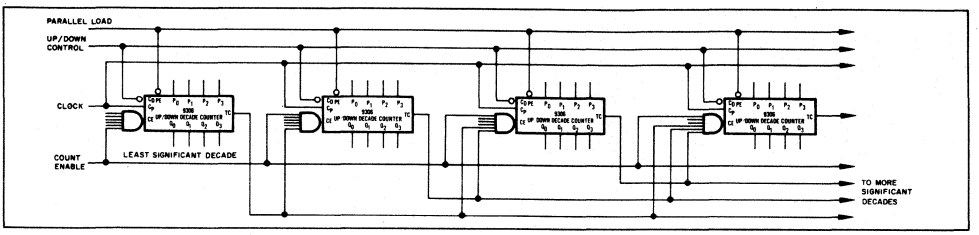


Fig. 5. Synchronous Multi-decade counting scheme.

high, where $CE = CE_0 \cdot CE_1 \cdot CE_2 \cdot CE_3 \cdot CE_4 \cdot CE_5$. Since each 9306 decade in Figure 5 has one of its CE inputs connected to the Terminal Count (TC) output of each of the less significant decades, the counting mode for a decade is first obtained when all less significant decades have active high TC signals. The Boolean expression for the TC signal is:

$$TC = CD \cdot Q_0 \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot Q_3 + \overline{CD} \cdot \overline{Q_0} \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot \overline{Q_3}$$

This means that TC is high when, and only when, the state of the counter is 9 and CD is high (counting UP) or the state of the counter is 0 and CD is low (counting DOWN). As can be seen from the Boolean expression, the state of TC is independent of the state of the PE and CE inputs. Since one CE input is needed for each less significant decade, a seven-decade synchronous counter is possible without any external logic.

The 9306 decade in itself is synchronous, but the scheme in Figure 5 insures that all seven decades are synchronized. The CE inputs can also be used to form a clock inhibit line for the counter. This is done by tying together a CE input from each decade (Figure 5) and using this line as a count enable control.

APPLICATIONS

The 9306 Up/Down Decade Counter can be used in a number of counting sequences. The counter is designed so that when the limit (0 if counting down and 9 if counting up) of the count is reached the device overflows on the next clock pulse. Therefore, if the device is counting up, it starts again at state 0; if it is counting down, it starts at state 9. This overflow action can be inhibited by a single inverter in a feedback path between the terminal count output and count enable input, as shown in Figure 6. If the CD and TC signals are high, with the counter in state 9, further clock pulses will not allow the counter to jump to state 0, and the count is disabled. Similarly, if the CD input is low and the counter is in state 0, further clock pulses will not allow the counter to jump to state 9.

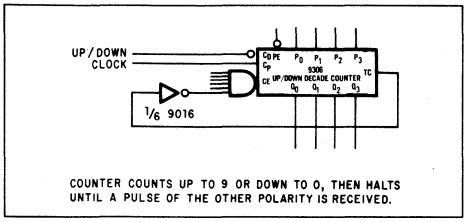


Fig. 6. Up/Down counting sequence 1.

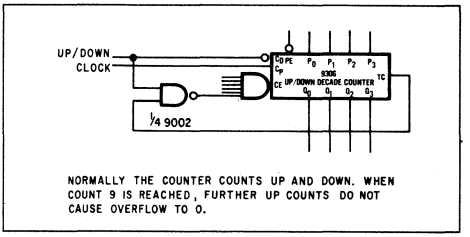


Fig. 7. Up/Down counting sequence 2.

This technique permits the counter to count only within the limits 0 to 9 and provides self-limiting at the terminal states 0 and 9. The concept of overflow inhibition can be extended to saturate the counter only when counting up (Figure 7) or only when counting down, and can be applied to multi-decades where the final decade terminal count is fed back to the initial decade input via an inverter or gate. Extensions of the above techniques allow the counter to circulate between state 0 and state 9 and then back to state 0 again, or to count up to 9, hold for a single clock pulse, count down to state 0, hold for a clock pulse, and so on (Figures 8 and 9).

These different counting schemes are useful in a variety of applications, such as waveform generation, pulse modulation and display sweep generation.

Synchronous Parallel Load Facility

The synchronous parallel load facility is a powerful logic tool in many applications. If a calculation is to be performed, the parallel load facility allows the counter to be started at a particular count before the computation begins. The parallel load can also be used for shifting information to the right or to the left by appropriate connection of the outputs of the device to the parallel inputs (Figure 10). This capability is useful in computations where the answer has to be sent in serial form to

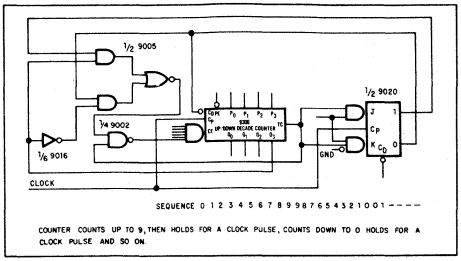


Fig. 8. Up/Down counting sequence 3.

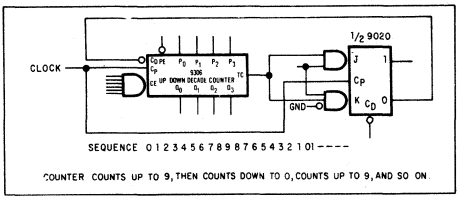


Fig. 9. Up/Down counting sequence 4.

some other logic. The information stored in the counter can also be shifted more than one place--up or down--again by appropriate input/output connections. One such connection permits the shifting of one decade of information to the next so as to present the decades in 8421 BCD parallel for display or for further processing in a parallel bit serial word configuration (Figure 11).

The parallel load facility can also serve as an additional count enable by connecting the outputs to the same weighted input. Such a connection loads the counter with the previous information when the parallel enable is low and allows the device to count only when the parallel enable is high. This extra count enable makes it possible to interconnect eight decades of information and to count synchronously without additional gates.

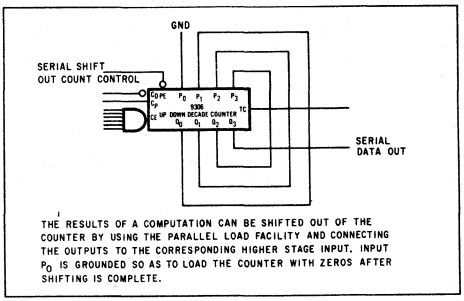


Fig. 10. Shifting out data serially.

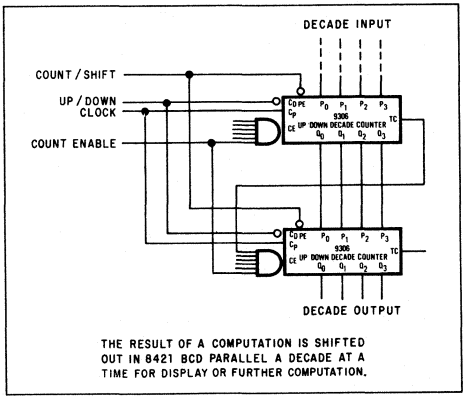


Fig. 11. Shifting data out in decades.

The 9306 Up/Down counter can function as a programmable divider by decoding the terminal count states of the decoder and

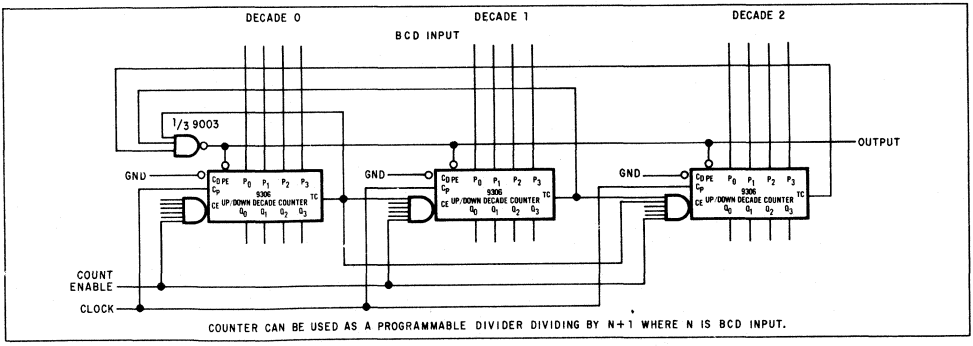


Fig. 12. Programmable divider.

using the parallel load facility to insert the division ratio. The design shown in Figure 12 divides by N + 1, where N is the input in decades, with the output going low for a clock period every N + 1 clock pulses.

Synchronizing Asynchronous Count Inputs

In many control systems requiring an up/down counter, the outputs from the system into the digital control and display portion are two asynchronous pulse trains. Pulses on one line indicate a count up and on the other a count down.

A typical system application might be the accurate measurement of length for an xy coordinate table using laser interferometers and De Moivre fringes. Pulses on one line would indicate that a table movement to the left is required, and pulses on the other that a movement to the right is necessary.

Figure 13 shows the logic that synchronizes the asynchronous up and down pulse trains to the synchronous 9306 and provides the correct control signals for the counter. A clock source is required whose frequency is at least twice as high as the asynchronous inputs so that pulses on either input line are not lost.

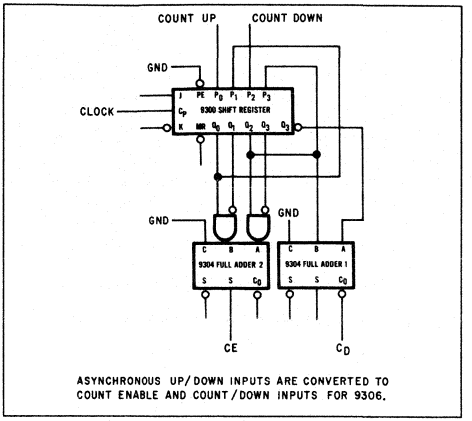
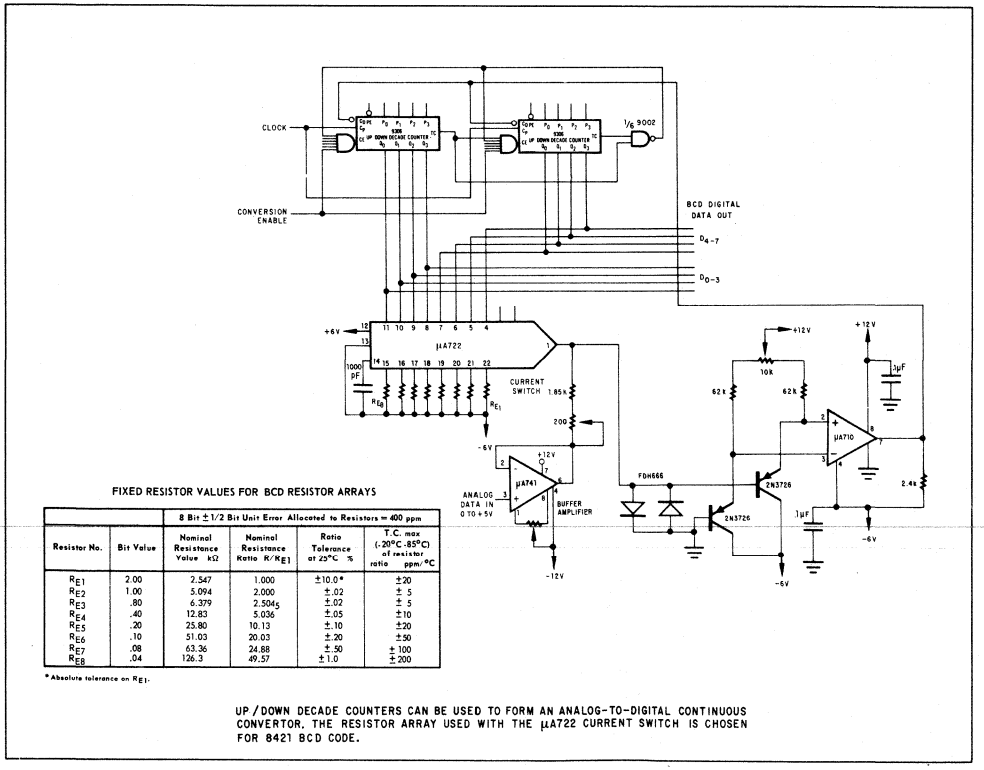


Fig. 13. Synchronization of asynchronous count up/down inputs.



FIXED RESISTOR VALUES FOR BCD RESISTOR ARRAYS

		8 Bit ±1/2 Bit Unit Error Allocated to Resistors = 400 ppm			
Resistor No.	Bit Value	Nominal Resistance Value kΩ	Nominal Resistance Ratio R/R_{E1}	Ratio Tolerance at 25°C %	T.C. max (-20°C -85°C) of resistor ratio ppm/°C
R_{E1}	2.00	2.547	1.000	±10.0*	±20
R_{E2}	1.00	5.094	2.000	±.02	± 5
R_{E3}	.80	6.379	2.504$_5$	±.02	± 5
R_{E4}	.40	12.83	5.036	±.05	±10
R_{E5}	.20	25.80	10.13	±.10	±20
R_{E6}	.10	51.03	20.03	±.20	±50
R_{E7}	.08	63.36	24.88	±.50	±100
R_{E8}	.04	126.3	49.57	±1.0	±200

*Absolute tolerance on R_{E1}.

UP/DOWN DECADE COUNTERS CAN BE USED TO FORM AN ANALOG-TO-DIGITAL CONTINUOUS CONVERTOR. THE RESISTOR ARRAY USED WITH THE μA722 CURRENT SWITCH IS CHOSEN FOR 8421 BCD CODE.

Fig. 14. Continuous analog-to-digital conversion.

When a clock pulse arrives, the two asynchronous inputs are loaded into two stages of a 9300 four-bit register via the parallel enable facility. The information held in these two stages is then shifted into the two remaining stages of the 9300. The stages Q_0Q_1 and Q_2Q_3 of the register hold two clock periods of information on the asynchronous input pulses. This information can be decoded to ascertain if either input has passed from a low level to a high level (which would indicate that a count was required). Since the 9306 has a count enable input and a single count up/down control, the count enable should be active whenever there has been a transition from low to high on one input line and not on the other. This function, which requires an exclusive OR circuit, is performed by the adder 2 on the 9304 adder. The count-down control should be active when a low-to-high transition has occurred on the down line, and this control can be generated using the remaining half of the 9304.

Other methods of synchronization are possible. However, these are more complicated and cannot easily account for simultaneous pulses on both lines. The method described above ignores simultaneous pulses and accurately provides up/down counting in excess of 10 MHz.

Analog-to-Digital Conversion

The 9306 Decade Up/Down Counter is a useful building block in the construction of analog-to-digital converters that work in 8421 BCD code for display or control purposes. The device can be used in a continuous conversion mode of operation where one or two decade counters count up and down in an attempt to follow the digital count value of the analog signal.

Figure 14 shows a typical analog-to-digital design using the 9306 in which the outputs of the counters are applied to a set of current switches (in this case the monolithic μA722). The ladder resistors are chosen to generate a weighted 8421 BCD code analog value of current at the output of the programmable current switch. The analog voltage whose digital equivalent is required is buffered off by a unity gain voltage follower. The voltage seen at the comparator input is the input voltage minus the current representation of the present count subtracted across the nominal 2k scaling resistor. If the comparison voltage is above ground, the digital value applied to the current switch is too small, and the output of the comparator goes high. Then the counter counts up until the input analog voltage exceeds the digital value derived from the network when the output of the comparator goes low, and the counter starts to count down. The output of the two 9306 counters is thereby a digital value in 8421 BCD code of the input analog voltage. In the feedback path between the final terminal count and the count enable inputs of both counters, there is a two-input gate that inhibits the counters from recirculating whenever the input analog voltage is greater than the specified value. The counters effectively saturate at states 00 or 99 if the maximum input level specified is exceeded.

The up/down counter can be used in a digital-to-analog converter for digitizing and transmitting analog signals. Figure 15 shows the 9306 counter in a delta modulator. The analog input is compared with the input from the 9306 counter and a resistive ladder network. If the analog input is at a higher potential than the output of the ladder, the output of the comparator is low and the counter counts down.

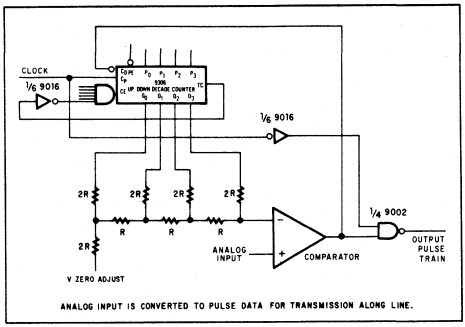


Fig. 15. Delta modulator.

Since the counter attempts to follow changes in the analog input equivalent, the comparator output is in effect a serial digital representation of the analog input; a high output during a clock period indicates a count up, and a low output indicates a count down.

This comparator output is gated with the clock to provide a pulse train suitable for transmission down a cable. If the analog input passes its prescribed limits and calls for more than nine consecutive count up or down pulses, the inverter that feeds back the terminal count output to the count enables stops the counter from overflowing.

The demodulator shown in Figure 16, with the equivalent resistance network and an integrating buffer amplifier, resembles the modulator just discussed. The incoming pulse train carries both the count up/down information and the clock frequency. The clock is extracted from the incoming pulse train by the 9601 single-shot, which has a time constant slightly shorter than the normal pulse period. If a pulse is present, the single-shot fires on the low-to-high transition of the pulse; if a pulse is not present in the time period, the single-shot reverts to its own natural frequency. This is the frequency produced by the feedback from output to input via the inverters, which lengthen the output pulse.

Therefore, a clock pulse is derived at the original clock frequency, independent of pulse transmission. This clock is then used at the clock input of the 9306 counter. If a pulse is transmitted, the generated clock is framed by the pulse (which is stretched by the second 9601) and forces the counter to count up if a pulse is not present, and down if it is present. As a result, the counter follows the equivalent counter in the modulator, and by means of the resistor network and integrating amplifier converts the digital equivalent in the counter to the desired analog signal.

Arithmetic Functions

Arithmetic functions can be generated by using counting techniques (as apart from direct addition, subtraction, multiplication or division). These techniques are based on the counter's ability to add and subtract unity each clock pulse. Two numbers can be added by placing the augend into a counter and allowing the counter to be counted up or down by the corresponding number of addend clock pulses.

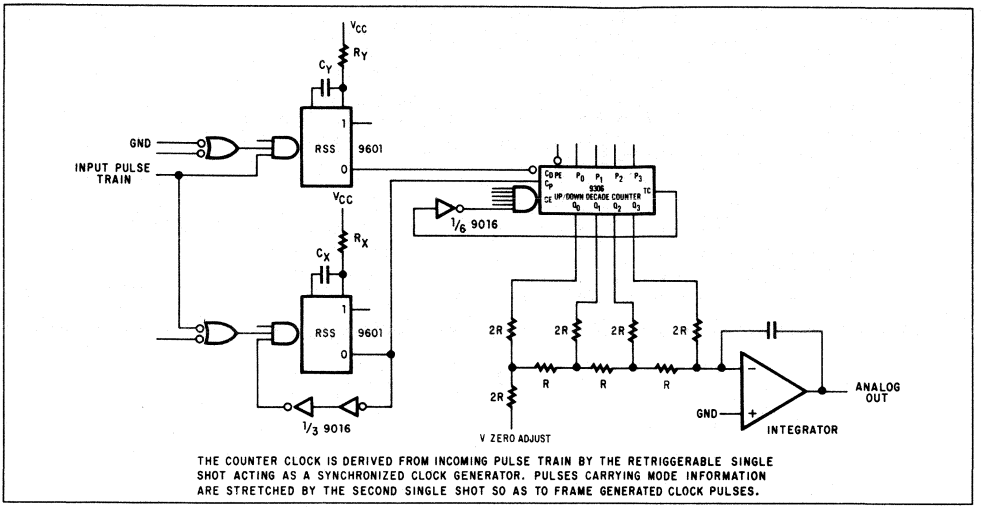


Fig. 16. Delta demodulator.

Figure 17 shows the 9306 used in this way to add or subtract two BCD numbers. The addend is loaded from the input busses in parallel under control of the parallel enable into the first 9306; the augend is then loaded into the second decade counter. The counter containing the augend is then counted down to 0 and at the same time the counter, which originally contained the augend, is counted up. A subtraction of unity from counter B is concurrent with an addition of unity in counter A. When counter B reaches 0, the terminal count goes high and inhibits both counters from further counting until another parallel load operation takes place.

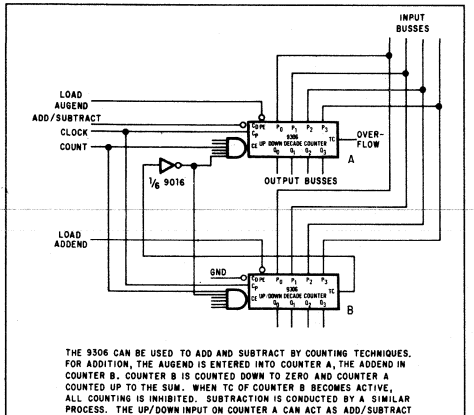


Fig. 17. Addition/subtraction.

Counter A now contains the sum of the two original numbers. If an overflow occurs, it can be stored in a discrete flip-flop or be passed on to another decade. Subtraction is a process similar to addition, except that counter A is operated in the count down mode. Counter B does not have to be an up/down counter. It can be either a counter having just a count down capability or an up counter which is loaded with the ten's complement of the second variable.

If several decades of operation are required, the addition/subtraction scheme can be extended by using more counters, but this would be costly in hardware and slow in operation. A better method would be to use the same logic and operate on the input variables a decade at a time. Such a method would require additional control logic, but the principles involved would be the same as those described above. The decades of the working variables could be stored in four shift registers, such as the 9328 dual eight-bit shift register or possibly MOS shift registers in parallel.

More complex arithmetic operations can be performed with counting techniques such as a square root calculation shown in Figure 18. This logic design calculates square roots by means of the formula:

$$n^2 = \sum_{1}^{n} (2n-1) \text{ or}$$

$$n^2 = 1 + 3 + 5 + 7 \ldots + (2n-1)$$

The operant whose square root is required is loaded into counter C by activating the START control line. The signal also loads decimal 1 into register A and clears flip-flop D allowing the contents of counter A to be transferred to counter B. On removal of the START signal, both counters B and C count down. When counter B reaches state 0, (which in this first instance happens after one clock pulse) the TC signal of counter B becomes active, inhibiting further counting of counters B and C and setting flip-flop E on the next clock pulse. As a result, counter A increases

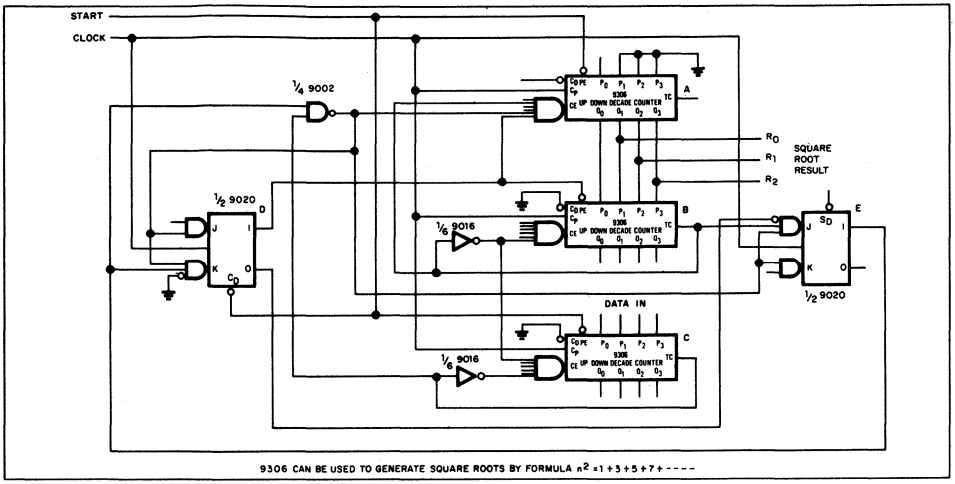


Fig. 18. Square root generator.

to decimal 2. On the next clock pulse, counter A increases to decimal 3. And finally a subsequent clock pulse resets flip-flop E, which resets flip-flop D (prohibiting counter A from increasing any further) and loads the contents of counter A into B where the complete process is repeated.

Each cycle reduces the contents of the counter C by the contents of counter B, which increase by 2 each time, thus subtracting 1, 3, 5, 7... from counter C. When counter C reaches 0, the counter is inhibited and when counter B reaches 0, counter A is allowed to increase by decimal 1. On the next clock pulse, flip-flop E is set and inhibits a further increase in counter A via the two-input gate on the count enable input. At the end of the computation counter A contains:

$$(2n-1) + 1 = 2n$$

The "2n-1" term is the last subtraction from counter C, and the "1" is a term added in the last stages of computation. The square root is obtained by taking the outputs of counter A one place to the right. This effectively divides the outputs of the counter by 2 to produce "n", the desired square root. For computation of operants having additional decades, the number of counters can be increased or computation can take place a decade at a time as indicated in addition and subtraction above.

Arithmetic operations may also be performed using the up/down counter as a digital servo. This technique uses rate multipliers for computation. A rate multiplier is a device in which the number of output pulses in a period is proportional to the input code. Figure 18 shows a decimal rate multiplier (DRM), with an input code in the 8421 BCD format, together with a timing diagram and logic symbol. Decimal rate multipliers can be connected together in conjunction with the 9306 Up/Down counter in a feedback arrangement for complex computation.

Figure 20 shows such a scheme where the first two DRM's produce an output proportional to the clock frequency C, and the parallel inputs A and B. The two lower DRM's produce an output

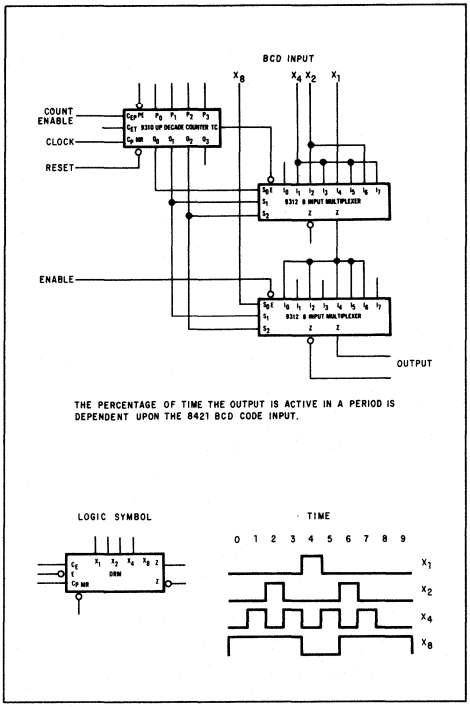


Fig. 19. 1248 BCD code decimal rate multiplier.

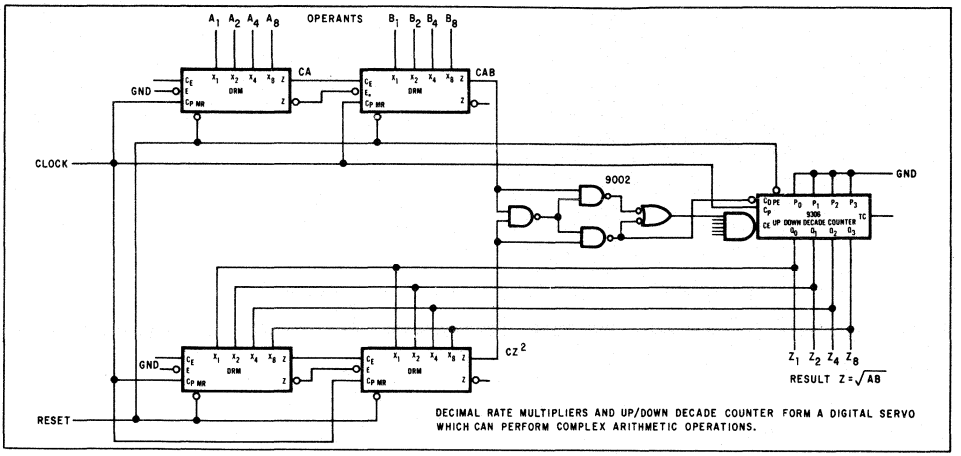


Fig. 20. Generation of arithmetic function $Z\sqrt{AB}$

proportional to the clock frequency multiplied by the squared output of the up/down counter. The two outputs, CAB and CZ^2, are then applied to the up/down counter in such a way that a count up is requested if the output CAB is high, and a count down is required if CZ^2 is high. The logic prior to the counter removes the possibility of CAB and CZ^2 both being active and asking for counts during the same clock period. Since the up/down counter acts as a servo, when the count inputs CAB and CZ^2 arrive at the same rate, the system is stable, CAB = CZ^2, and hence $Z = \sqrt{AB}$.

This technique is superior to others in the simplicity with which it generates very complex arithmetic calculations. It does, however, have two drawbacks. It is slow, and the weighted output pulses must be correctly interlaced or else stable oscillations will occur.

LIFO Memory Control

The 9306 up/down counter can be used as the control counter in a LIFO (last in/first out) memory. Such a memory could store link addresses, which point to the start of a subroutine in a digital computer program, or could control buffer memory dumps in peripheral equipment. Figure 21 shows an eight-word four-bit LIFO memory using the 9308 dual four-bit latch for storage and the 9312 and 9309 multiplexers for gating the stored information to the output busses. The up/down counter, acting as the control sequencer for the memory, is decoded with a 9301 decoder. The 9301's outputs select (1) the appropriate register in which to write information when the read/write control is active high and (2) the register to read from when this control line is low.

In the writing mode, the first information word present on the input busses is written into register 0, the second into register 1, and so on, up to 10 words, with the 10th information word being stored in register 9. In the reading mode, the order is reversed, the first information accessed being the last information written. Since only 10 information words can be stored, auxiliary control logic can be used to indicate overflow and inhibition of further writing if necessary. Only four-bit registers are shown in the logic diagram, but these could be extended to word length of 28 bits. For loading purposes, additional discrete gates are required only in the read/write control line. Various other memory configurations could be devised using the 9306 counter as the controlling element, and the logic shown in the figure could be extended to include additional memory words.

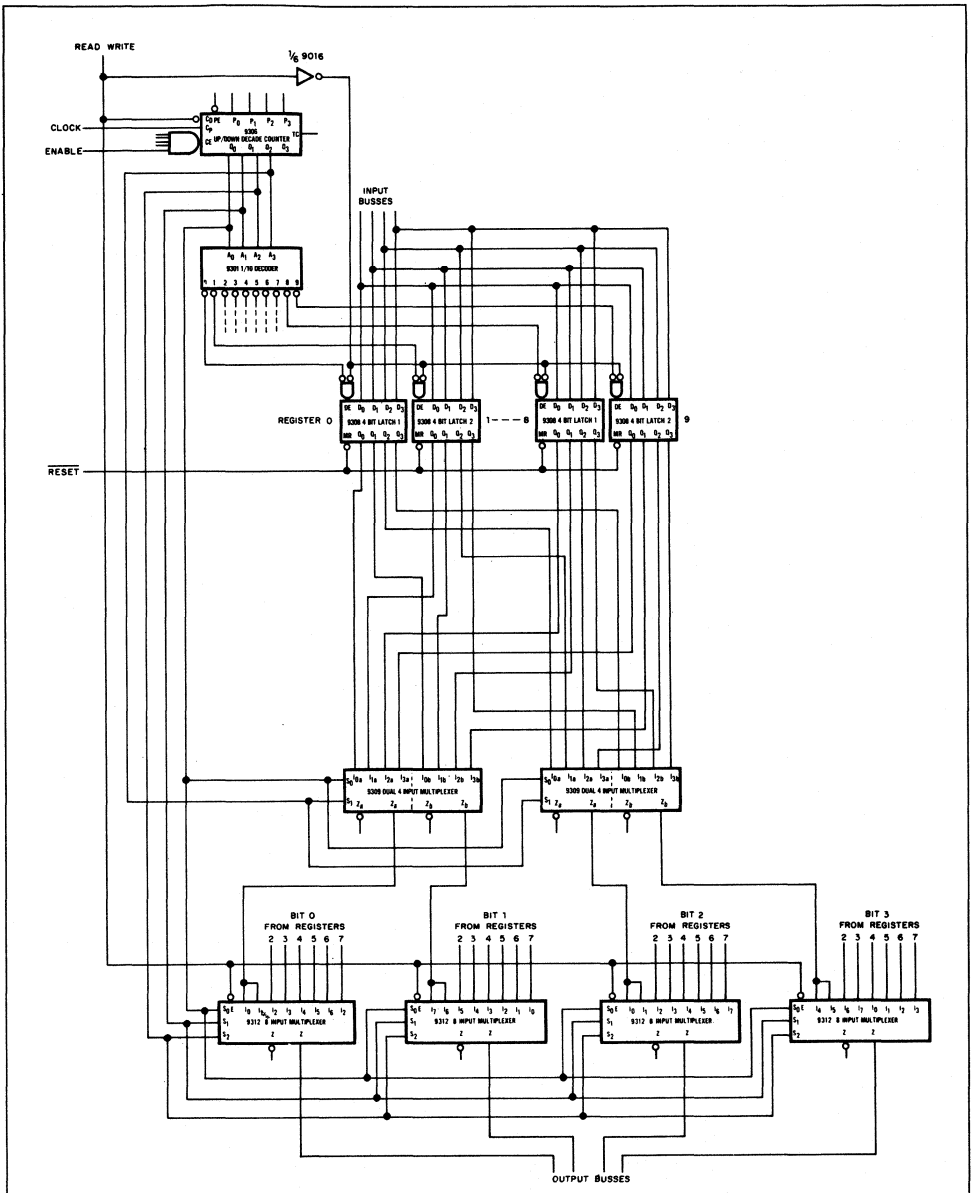
CONCLUSION

This application note has outlined the logic design and characteristics of the 9306 up/down counter and illustrated its use in a variety of systems. The logic designs give a general indication of the logic power of this MSI circuit. The device is one of the 9300 series MSI functional building blocks, which are designed as a compatible family.

System designs using these devices, in conjunction with discrete gates for the system glue, offer significant advantages over conventional methods of building designs with discrete gates and flip-flops. For example with discrete gates and dual flip-flops, approximately 50 gates or 12 discrete IC packages would be required to perform the same function as the 9306.

An MSI circuit such as the 9306 reduces the number of IC's needed and hence increases the reliability and the cost savings. Since the MSI circuits in the 9300 family are functional building blocks, they can often be directly inserted into a system at the block diagram level. The result is a substantial reduction in design time and supporting effort required.

Digital system design has now passed from the discrete gate level to the functional building block level. MSI circuits, such as the 9306 up/down synchronous BCD counter, will be the digital building blocks for the next generation of designs, and discrete gates will be the glue holding the larger building blocks together.



9306 UP/DOWN DECADE COUNTER CONTROLS INPUT AND OUTPUT OF INFORMATION TO AND FROM MEMORY.
A LIFO MEMORY COULD BE USED TO STORE INTERRUPT LINK ADDRESSES.

Fig. 21. LIFO-last in first out memory.

MSI 9308 DUAL 4-BIT LATCH

INTRODUCTION

The Fairchild 9308 dual 4-bit latch is a monolithic medium-scale integrated circuit designed for general purpose storage applications in high-speed digital systems. The device uses TTμL technology and is compatible with all other members of the CCSL group of Fairchild integrated circuits. The 9308 has been designed to work electrically and logically with all other Fairchild MSI circuits and forms one of the elements of the 9300 logic family.

The 9308 gives designers of digital systems a high-speed storage building block that is versatile and economical. Active pull-up output circuits are provided on latch outputs, ensuring high speed and good capacitance drive capability with excellent noise margins at both logic levels. All inputs incorporate diode clamps to ground to limit the effects of transient signals caused by reflections in unmatched lines. The device is especially suitable for use with the 9301 1-out-of-10 decoder, the 9311 1-out-of-16 decoder, and the 9309 and 9312 multiplexers to form high-speed storage systems.

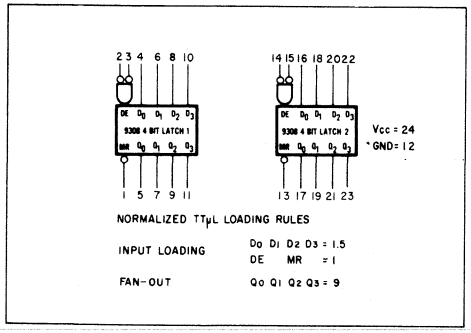


Fig. 1. 9308 Block diagram.

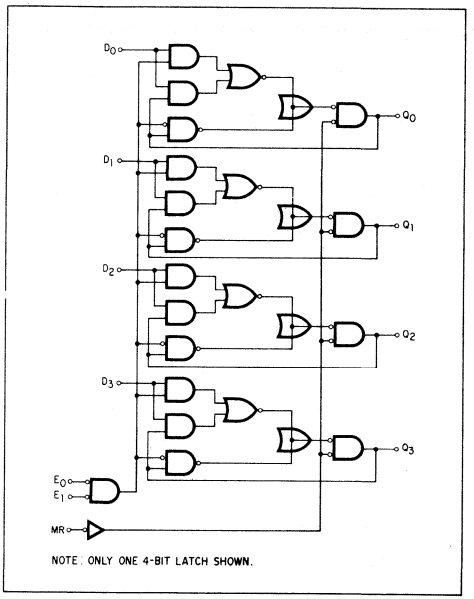


Fig. 2. 9308 logic diagram.

FUNCTIONAL DESCRIPTION

The symbolic block diagram of the 9308 is shown in Figure 1 along with pin numbers and loading rules. The logic diagram for one block of four latches is shown in Figure 2. Data is en-

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SEMICONDUCTOR

tered single-line in parallel into the four latches when the active low AND gate enable inputs are both at the low logic level. The information typically appears at the outputs within 25 nsec of the receipt of the enable pulse and is held in each latch by the feedback logic. Each latch having the output of the latch and data as inputs incorporates an additional AND gate to ensure that no glitches or logic spikes occur when the enable inputs are removed. A common reset which overrides all other input conditions is provided for the four latches, holding their outputs low while it is active. The master reset and enable inputs are buffered, thus presenting a TTμL input load of one. Generally, one active low input enable is used to select the latch block, and the other is used for the clock or strobe input.

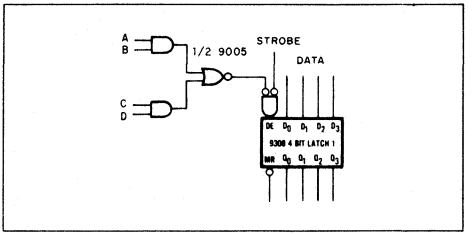


Fig. 4. AND-OR ENABLE.

APPLICATIONS

Register Selection

Figure 3 shows a block of four latches used with a 3-input NAND gate feeding into one input on the active low enable and a strobe signal on the remaining low active enable. This logic allows data entry into the latch block for an AND condition. Figure 4 shows the logic for several AND conditions using an AND-OR-NOT gate. These examples indicate the logic power of the active low inputs on the AND enable gate.

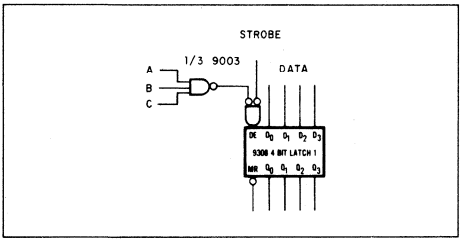


Fig. 3. AND ENABLE.

The 9308 was specifically designed to work with the other members of the 9300 MSI logic set and, again, the active low enable AND inputs prove useful for logic designs in conjunction with the 9301 1-out-of-10 and 9311 1-out-of-16 decoders. Figure 5 shows a register selection scheme in which information is presented on parallel busses, and the register to which data is to be sent is selected by a 9301 decoder. The only condition necessary for correct entry is that the register address inputs to the decoder be present before the registers are strobed. Since only a single unit load is presented by a 9308 enable input, one 9301 decoder can control 10 registers having a 40 bit word length. A similar scheme which might be used for a display or special storage is shown in Figure 6. Here, two decoders select which register should receive information from a set of common bus lines. The matrix shown consists of 64 registers arranged in an 8 x 8 matrix. Outputs 0 - 7 of each decoder are used in a coincident enable enable select scheme in which one decoder's outputs are common in the x direction and the other's in the y direction. The 8 and 9 outputs of the 9301 decoders are not used, and therefore the most significant A_3 input on the decoders can be employed as a strobe input. The low level fan-out of the decoder is 10 unit-loads, and the high level is 20 unit-loads. Therefore, in an extension of the scheme shown, two 9301 decoders can drive two 4-bit latches at each word. For systems having larger word length, either buffers should be provided, (which necessitates passing through two extra logic levels), or the more economical method of duplicating the decoding scheme should be used. The size of the matrix can be extended to 10 x 10 words by using the A_3 input of the decoders and an external 2-input gate for the input address and strobe. The 9311 1-out-of-16 decoder can also be used in a matrix format; however, since the fan-out at the low logic level is 10, a 256-

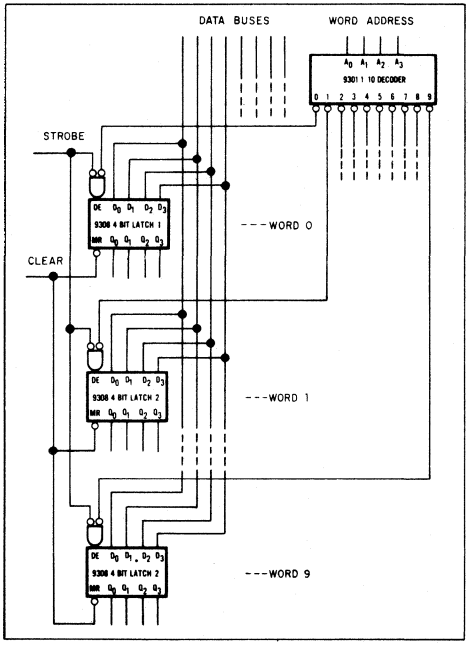


Fig. 5. Register selection. 9308 dual latches selected by 9301 decoder.

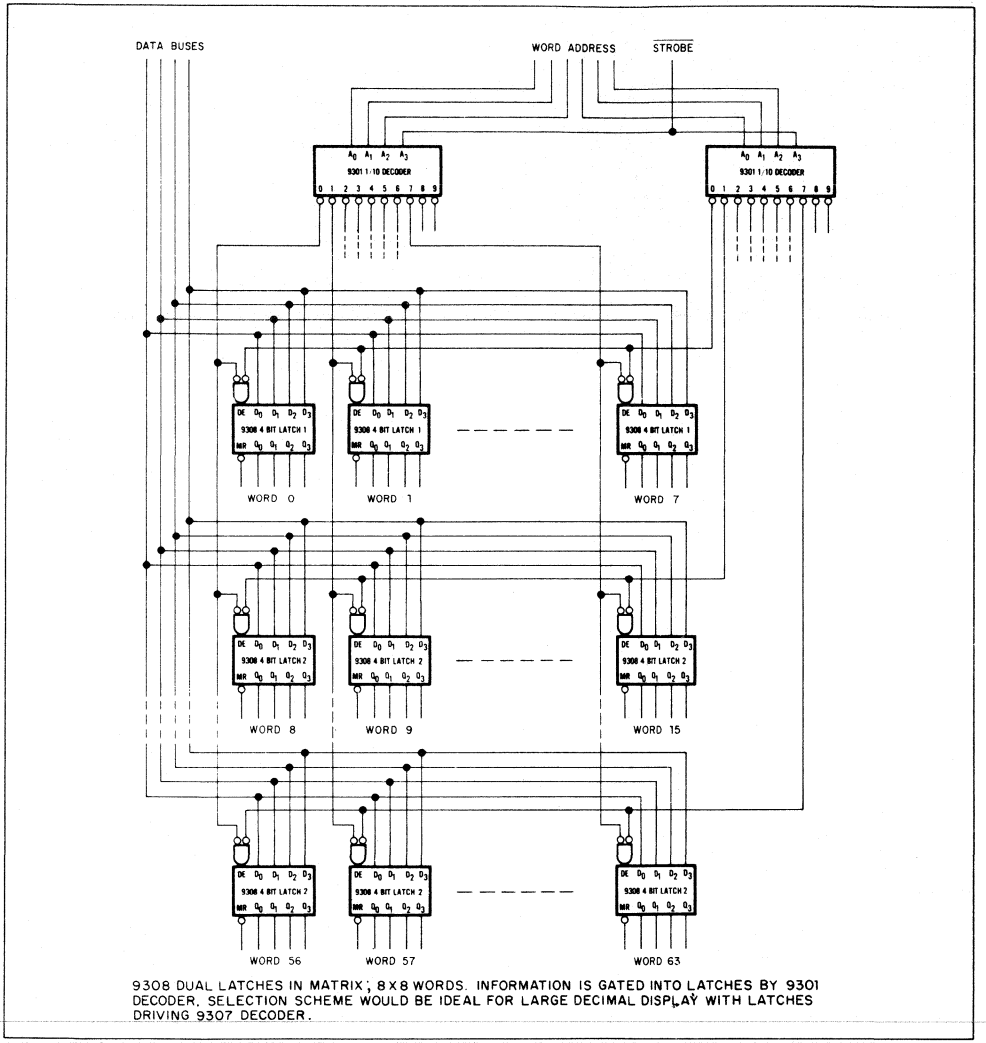


Fig. 6. Matrix register selection.

word matrix must share the load between two 9311 decoders. Various other decoding methods to select a single register from a group of registers can also be used with the 9301 and 9311 decoders.

Two-Phase Clock System

The 9308 can be used as a bank of four master-slave flip-flops by providing two clock or enable signals, one for the latch block acting as a master, and another for the slave. A single inverting gate can be used to generate these two clock phases from a single clock input. Figure 7 shows the dual latch as a 4-bit shift register using this two-phase clock system. The advantage of this method over 4-bit shift registers such as the 9300 is that four more possible combinations of signal phases are available from the outputs of the two blocks of latches. This scheme can be extended so that there is one master latch and several slave latches. A single master drives all slaves, and

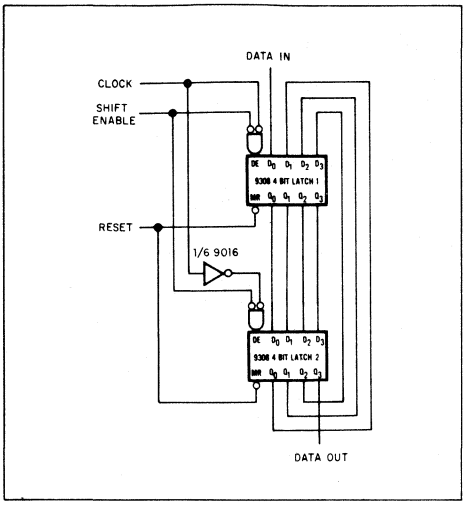


Fig. 7. 4-bit shift register using latches as master-slave flip-flops.

a decoder selects which slave receives the information from the master. This method is very economical in terms of hardware, and offers considerable savings over a multiple flip-flop register approach. Figure 8 shows one 4-bit latch acting as the master driving seven 4-bit latches acting as slaves. Which slave the information in the master is transferred to is determined by the 9301 decoder acting as a demultiplexer for the strobe or clock signal.

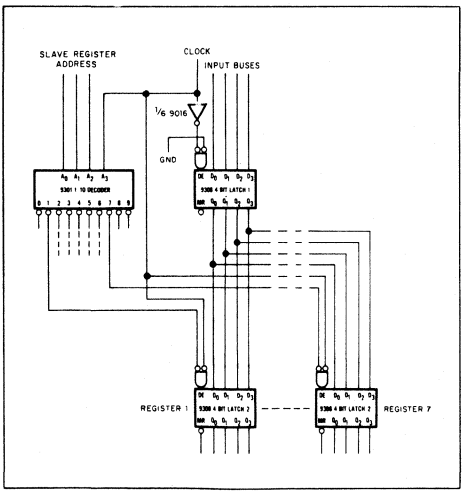


Fig. 8. Single master multiple slave flip-flop scheme.

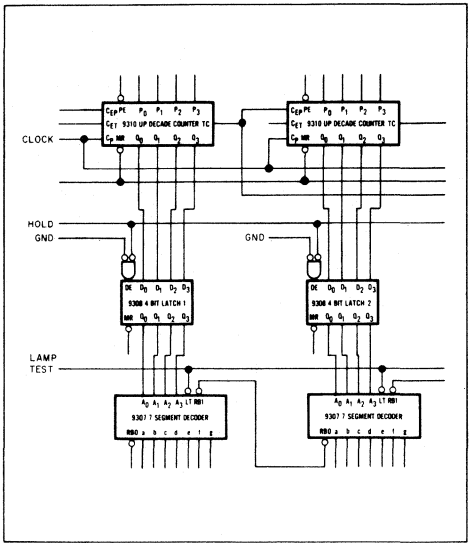


Fig. 9. Latch as holding register in counting and display application.

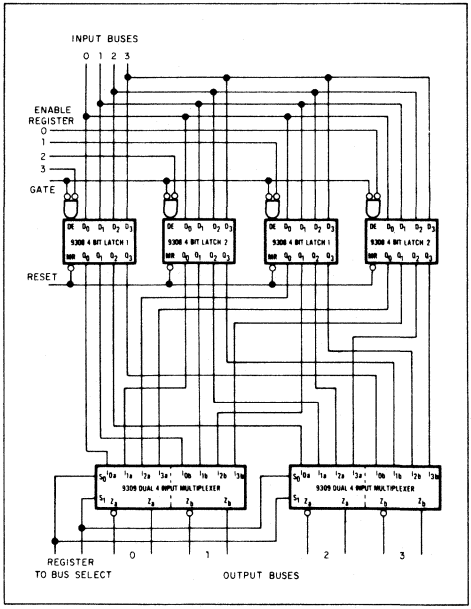


Fig. 10. Multiplexing. Dual 4-bit multiplexer used to gate selected register to bus.

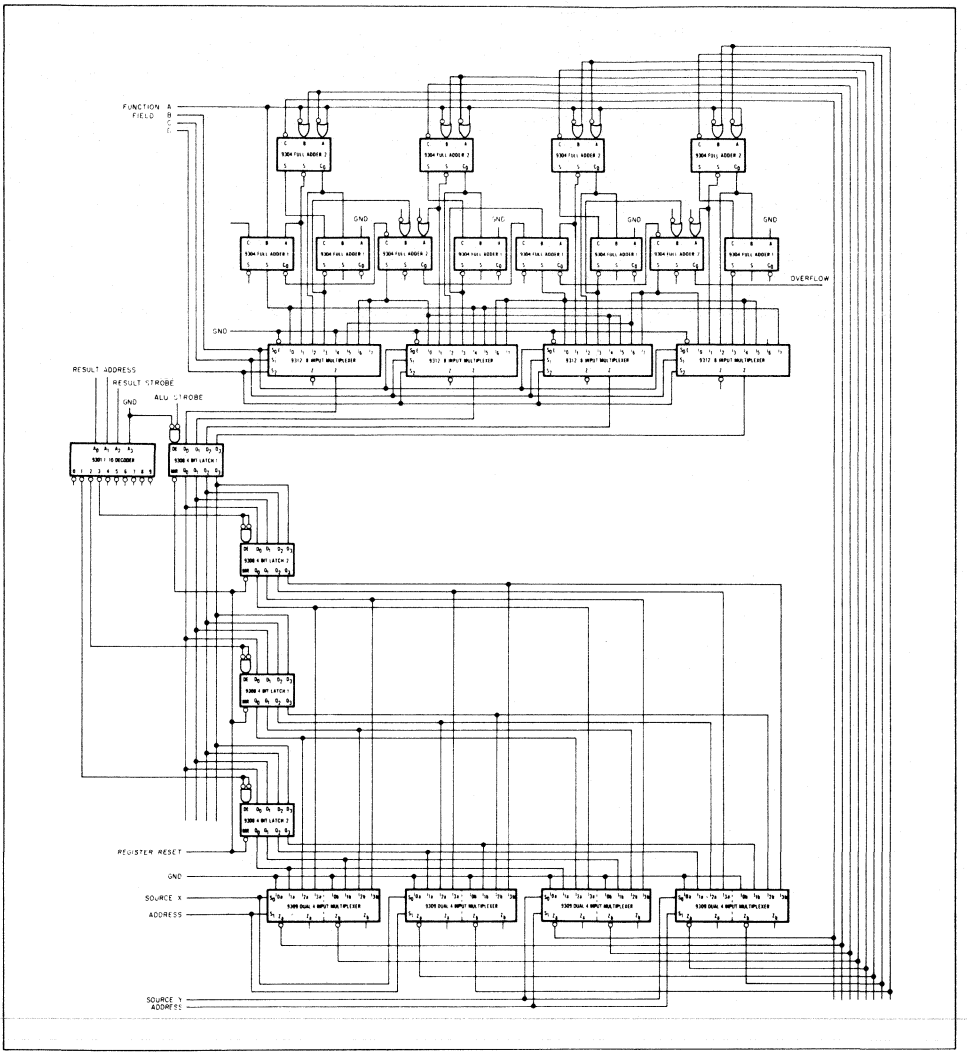


Fig. 11. MSI 4-bit arithmetic logic register slice.

TYPICAL APPLICATIONS WITH OTHER 9300 MSI CIRCUITS

The dual 4-bit latch is an ideal circuit for use as a holding register in counting operations. Figure 9 shows two 9310 synchronous decade counters in a typical counter design. At a specified time, the information from the counters is latched into the holding register, where it is held and displayed via the 9307 7-segment decoders until the next sample time.

In addition to selecting a particular register consisting of latches, there is often the need to multiplex the information from several latch registers onto a bus system. The 9309 and 9312 digital multiplexers are ideal building blocks for this purpose. Figure 10 shows four 4-bit registers being switched to the appropriate busses under control of the S_0, S_1 inputs of the multiplexer. This design, together with decoder selection, shows how

the MSI products are logically compatible in logic designs. It also shows that they use few or no discrete gates in modular areas of a machine design, resulting in improved reliability, higher speed and easier, faster design.

Figure 11 shows how the MSI 9300 series products can be used to form a 4-bit register arithmetic logic slice of a digital computer. Here, the 9308 is used for the high-speed registers needed to hold the variables used in computation. These registers are the slaves of a latch which supplies the result of a computation to the resultant register.

Only four registers are used in this design, with one of the slaves, or working registers, non-existent. Grounding appropriate inputs on the 9309 multiplexers results in the equivalent of a register containing nothing but logic zeros. The design is a 4-bit slice where information from any of the four working registers is sent to one or both of the two sets of four parallel busses via the multiplexers under control of the two source addresses. The information on the parallel busses is operated on by the arithmetic logic unit and the result is sent in parallel to the 9308 acting as a master latch. The result is then passed on to the appropriate slave register under control of the 9301 decoder. No discrete gates are used in this design, and the scheme can be extended to use up to seven working registers plus the zero register. The instruction set for this arithmetic logic unit can be split into two parts:

(1) Register selection
(2) Operation selection

The two source address fields select the information to be operated upon. If x signifies the contents of register X, y the contents of register Y, and r the contents of register R, we can symbolize an instruction as:

$$x \text{ operation } y \longrightarrow r$$

where X, Y, R are any one of the four working registers 0-3. Register 0 obviously cannot be a result register and if treated as such will act as a "do nothing" instruction. The operation field functions (shown in Table I) have ADD, SUBTRACT, AND, OR, EXCLUSIVE OR, and SHIFT operation capability. The scheme uses just 17 IC packages and no discrete IC gates. The typical delay time for the longest path in an operation of 100 + N x 8ns, where N is the number of bits in the parallel word, allowing cycle times of less than 500ns to be achieved for operation on parallel words of 24 bits.

SUMMARY

The Fairchild 9308 dual 4-bit latch is a high-speed sequential logic block which can be used throughout digital systems. An important feature of the device is its logic compatibility and use with the rest of the 9300 series of MSI building blocks. The 9300 family of high-speed elements provides maximum logic function per unit cost, great application flexibility, and a considerable reduction in the number of connections in a digital system. All logic pins on these products are generally used, thereby allowing the designer of digital systems to reduce the number of discrete gates required to interconnect the large MSI building blocks. High speed inverting buffers are provided where necessary to minimize input loading requirements and considerably reduce the number of discrete buffers necessary in the digital system.

Compared to conventional approaches, systems design with MSI building blocks such as the 9308 greatly reduces the amount of time needed for design, checkout, and supporting effort, while increasing overall reliability and maintainability.

TABLE I.

Operational Field				Function
A	B	C	D	
L	L	L	L	x ADD y
H	L	L	L	x SUBTRACT y
L	H	L	L	$x \oplus y$
H	H	L	L	$x \oplus \bar{y}$
L	L	H	L	$x + y$
H	L	H	L	$x + \bar{y}$
L	H	H	L	$x \cdot y$
H	H	H	L	$x \cdot \bar{y}$
L	L	L	H	(x ADD y) 2 arithmetic
H	L	L	H	(x SUBTRACT y) 2 arithmetic
L	H	L	H	(x ADD y) 2 logical end around
H	H	L	H	(x SUBTRACT y) 2 logical end around
L	L	H	H	(x ADD y) 2^{-1} arithmetic
H	L	H	H	(x SUBTRACT y) 2^{-1} arithmetic
L	H	H	H	(x ADD y) 2^{-1} logical end around
H	H	H	H	(x SUBTRACT y) 2^{-1} logical end around

APPLICATIONS OF THE 9311 1-OUT-OF-16 DECODER

INTRODUCTION

The Fairchild 9311 1-out-of-16 decoder is an MSI (Medium Scale Integrated) circuit in the 9300 CCSL compatible family of functional building blocks. The device uses $T^2\mu L$ technology for high speed and for large capacitance drive and gives normal CCSL d-c noise margins and excellent a-c noise margins at both logic levels. The 9311 is an extended version of the 9301 1-out-of-10 decoder and is packaged in a 24-pin dual in-line package with all the pins used to give maximum flexibility and function capability. Input clamping diodes are incorporated at all inputs to reduce the adverse effects of transmission line reflections. The device can be used in all areas of digital systems and is particularly suitable for control, demultiplexing, and memory selection.

LOGIC DESCRIPTION

Figure 1 shows the logic diagram, including the pin layout and loading rules, for the 9311 Decoder. The device has buffered inputs to reduce input loading and a decoding network that uses active low output AND gates to produce the 16 possible outputs from four Boolean inputs. The output "0" goes low when the inputs A_0, A_1, A_2, A_3 are all low, A_0 being the least significant address input and A_3 the most significant address input.

An active low two-input AND gate controls the outputs of the decoder. These low level enable inputs allow the decoder to be controlled by additional decoders and also by other members of the CCSL group of integrated circuits. The low level outputs keep the power dissipation at a reasonable level, permit inverting buffers to be placed between the decoder outputs and other circuitry, and are logically compatible for controlling other 9300 MSI series products.

The propagation delay through the decoder depends on the output selected. The longest path is through three high speed inverting buffers and gives a typical delay of 25ns. For operation, both enable inputs must be at the low logic level, and if the outputs are not being strobed, the enable inputs should be connected to ground.

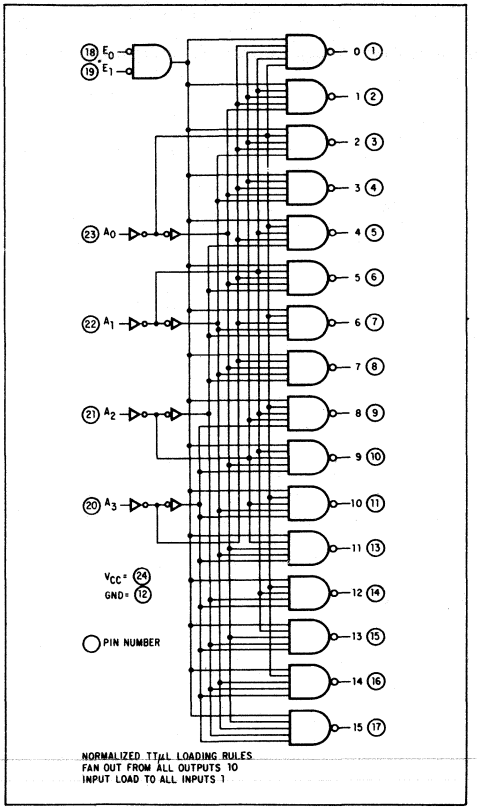


Fig. 1. 9311 Logic diagram.

FAIRCHILD
SEMICONDUCTOR

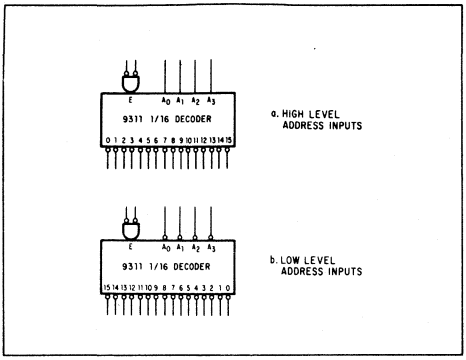


Fig. 2. 9311 Logic symbols.

Figure 2a shows the normal logic symbol for the 9311 decoder. In this symbology, a block represents the main logic function. Simple logic functions associated with inputs are shown by means of the normal AND, OR etc. symbol and are appended to the main block. Low level active states are represented by small circles at the input or output line. This method of drawing complex logic functions makes it easier to understand a complicated device and helps prevent continual drafting of complex interconnected gate configurations.

Using circles at both inputs and outputs facilitates logic interface and design with (1) other MSI functional blocks and with (2) existing discrete gates in the CCSL group of circuits. If active low address inputs are used, the symbol can be changed as in Figure 2b, with the outputs being rearranged as shown. Output "0" takes the place of output "15" and vice-versa. This concept of logic equivalence provides flexibility and ease of logic design. Since there are four inputs, there are 16 possible configurations of inputs producing the correct sequence of outputs by rearrangement of the output wires. The active low input AND enable gate may also be regarded as an active high input inhibit OR gate.

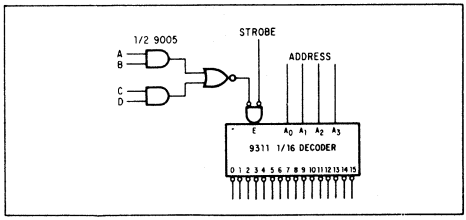


Fig. 3. Complex AND-OR enable.

Figure 3 demonstrates the logic power of the active low level AND enable gate. For example, in the circuit shown, the decoder is enabled only during an AND-OR condition. The remaining input on the AND enable gate can then serve as a strobe signal.

APPLICATIONS

Address Decoding

Address decoding is one of the prime applications of the 9311 decoder, which can be used for decoding in core, thin film, and semiconductor memory systems. The decoder does not normally have enough drive capability to drive memory elements directly, and therefore, some form of buffer is often inserted between the decoder outputs and the memory cells. Since the buffers used are generally inverting units, the active low level outputs of the decoder are an advantage. In the address decoder shown in Figure 4, a 9316 four-bit binary counter acts as a holding register.

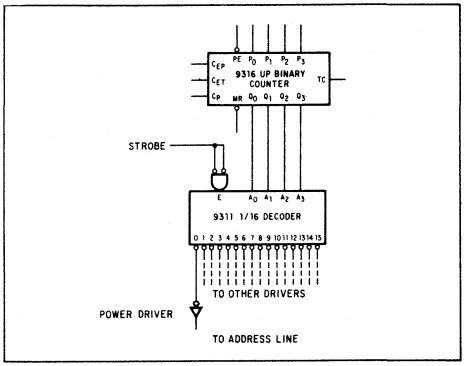


Fig. 4. Address decoding.

Several 9311 decoders will operate together to decode words of greater than four bits as illustrated in Figure 5 where two 9311 decoders decode five binary digits. In an extension of this technique, the low input enable gate of one decoder selects a decoder

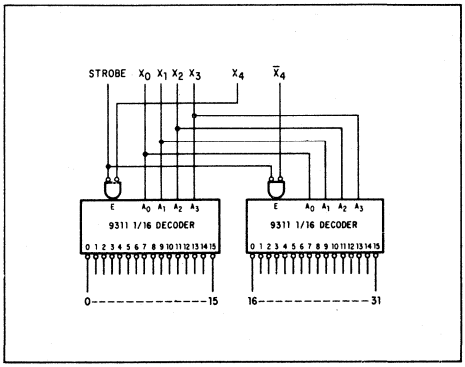


Fig. 5. 1-out-of-32 Decoder.

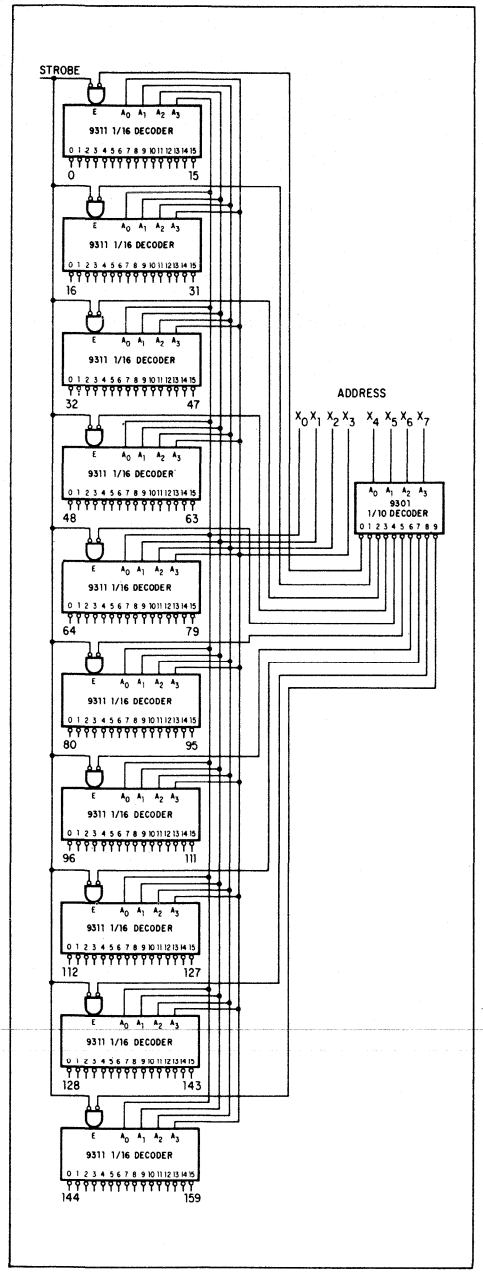


Fig. 6. 1-out-of-160 Decoding.

from a group of decoders (Figure 6). This decoding scheme uses a 9301 1-out-of-10 decoder to choose a particular 9311 with the address inputs of the 9301 representing the four most significant address bits and the address inputs of the 9311 decoders common representing the four least significant address bits. In Figure 6, a seven-bit binary address is decoded to 160 output lines, and the second AND enable input is used for a strobe. Larger decoders can be built in a variety of ways. One way is by using the XY matrix principle shown in Figure 7.

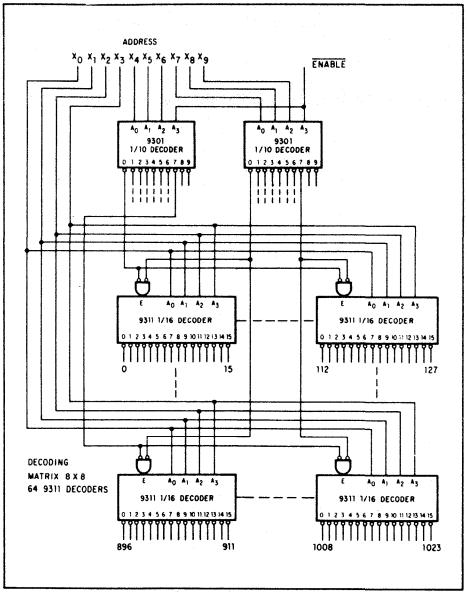


Fig. 7. 1-out-of-1024 Decoding.

The decoder is extremely useful in decoding and controlling semiconductor memory stacks. Figure 8 shows a 9311 decoder selecting a particular bipolar read-only memory from a group of 9034 memories comprising a complete stack. A single 9311 can control a group of 16 of these memories. Each memory contains 256 bits arranged in a 32 word x 8 bit format with the outputs of common digits being OR tied. An output from the 9311 can drive up to ten 9034 memories thereby allowing control of a 912 word x 80 bit or 72,960 bits of information with a single decoder.

Another memory configuration, which can incorporate the 9311 decoder, is built around the 9035 16 word x 4 bit read-write memory. Figure 9 shows the design of a typical semiconductor stack of 160 words x 40 bits. The 9035 is a linear select device requiring both active high inputs and inverting buffers between the decoders and memory cells as shown in the diagram. Since the decoder outputs can drive several inverters, and each of these can drive ten 9035 memories, a single 9311 and a 9301 can control a fairly large semiconductor random access read-write memory.

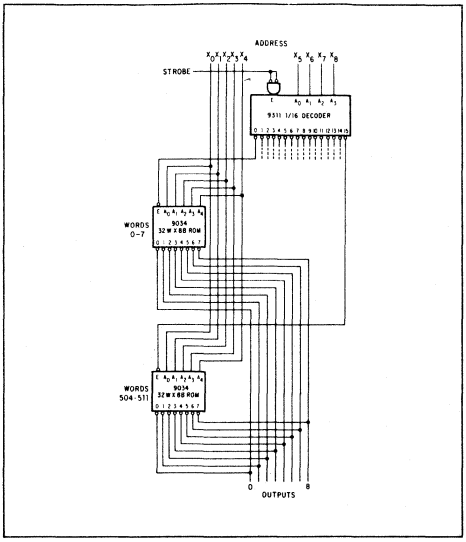
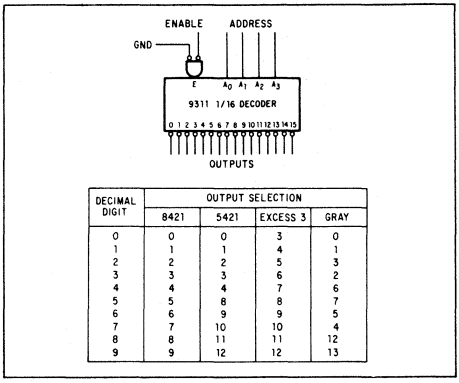


Fig. 8. 9311 Controlling read-only memory.

Code Decoding and Encoding

The 9311 decoder can be made to decode any four-bit weighted or unweighted code simply by selecting the appropriate outputs in the desired sequence. The table given in Figure 10 shows decoding for several well known four-bit codes.



DECIMAL DIGIT	OUTPUT SELECTION			
	8421	5421	EXCESS 3	GRAY
0	0	0	3	0
1	1	1	4	1
2	2	2	5	3
3	3	3	6	2
4	4	4	7	6
5	5	8	8	7
6	6	9	9	5
7	7	10	10	4
8	8	11	11	12
9	9	12	12	13

Fig. 10. Decode any 4-bit code.

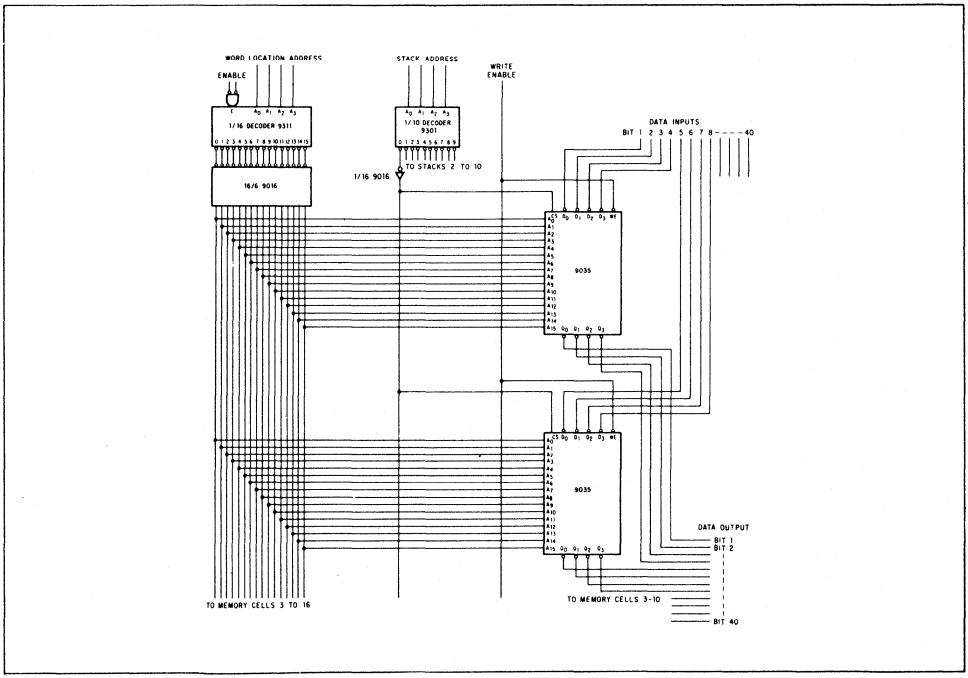


Fig. 9. Memory stack, 160 words of 40 bits.

A switch encoding scheme using the 9311 decoder is shown in Figure 11. A 9316 binary counter drives the decoder whose outputs pass through the switches. Only one switch may be selected at any one time. If a switch is selected, the flip-flop formed by the cross-coupled gates is set when the output line associated with that switch goes low. The counter counts through its sequence until it reaches the appropriate state for the selected output line to go low. Then the flip-flop is set and inhibits the counter from continuing. The state of the counter is now the encoded version of that switch which has been closed. When another switch is to be encoded, the flip-flop must be reset. This resetting can be performed by an additional switch. The 16 switches to be encoded and the reset switch can be mechanically arranged so that the operation takes place in the required sequence.

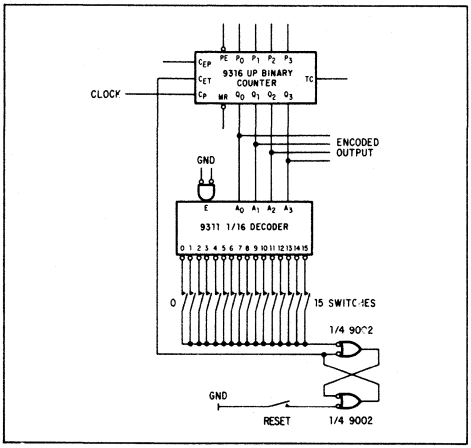


Fig. 11. Switch encoding using 9311 decoder.

Demultiplexing

The 9311 decoder can choose a particular output under the control of an address. Since the decoder has an enable control, this input enable can effectively switch data from a line to a specified output under control of the address input. If the address configuration selects output "0", then this output goes low if the AND enable function is active and high if it is inactive. Therefore, when data are inserted into one input of the active low AND enable gate, they are switched to the output under control of a strobe present on the other AND input. Hence, the decoder can act as a demultiplexer.

Many applications are possible using this demultiplexing principle. Figure 12 shows the decoder serving as a clock demultiplexer. The clock, under control of the address, switches to the appropriate register or counter. For correct operation the clock signal need only be framed by the address inputs, with the address set up prior to applying the clock. Since an output of the decoder can drive 10 TTμL input loads, and the load at the clock input of the 9300 MSI sequential circuits is generally two equivalent loads, a decoder is able to control 16 registers of up to 20 bits.

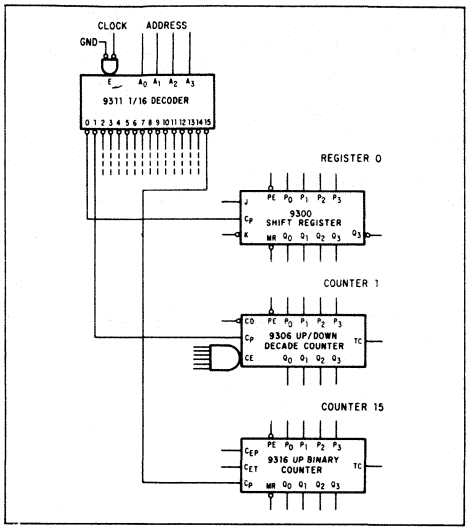


Fig. 12. Clock demultiplexing.

Another demultiplexing application is shown in Figure 13. In this application the decoder controls a group of latches working as a single master multiple slave flip-flop. When the clock line is high, information from a parallel set of busses is entered into

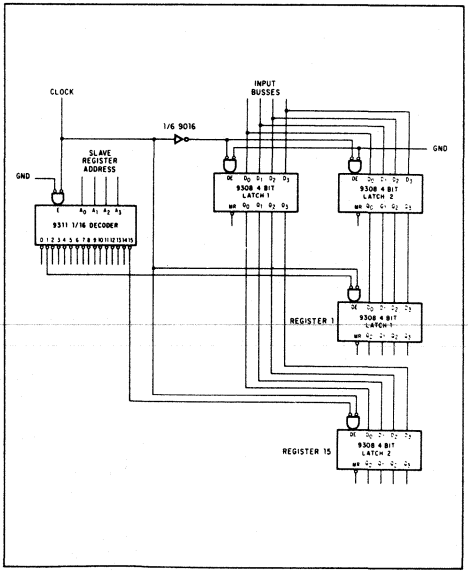


Fig. 13. Single master multiple slave flip-flop scheme.

the master latches. When the clock line goes low, this information is then transferred to the appropriate slave latch addressed by the decoder. Two dual latch blocks function as masters to share the load in order to drive the 16 slave registers. Alternatively, inverting buffers could be placed between the master and slave for loading purposes, but this would result in additional delay. Since each decoder outputs can drive ten latch blocks, the scheme shown can be extended to 40-bit words. This method of multiple slaves offers considerable hardware savings compared to a register approach where each register contains its own individual master slave latches.

Analog-to-Digital Conversion

A high speed successive approximation A/D converter can be designed using the 9311 decoder. The diagram in Figure 14 shows two such decoders in a 12-bit A/D converter. This converter actually produces a conversion in 13 clock periods, although for design convenience, a 16-clock conversion period is used. The two decoders are addressed from a 9316 binary counter, which is reset before each conversion.

At time period "0", decoder B (during the time the input clock is high) resets all stages of the 12-bit register that drive the current switches feeding to the resistance ladder network. At time period 1, output "1" from decoder B sets the first flip-flop, which contains the most significant bit in the register. The comparator then decides whether this binary value is greater or less than its analog equivalent. If it is greater, the comparator resets that latch via decoder A when the clock goes low. At time period 2, decoder B sets flip-flop 2 in the register, and again the comparator determines whether to leave this bit set or to reset it via decoder A. In this manner the various stages in the holding register are set and reset, or left set, until conversion is complete after 13 clock periods. The counter then continues until the terminal count is reached, whereupon an inverter in a feedback path inhibits further counting until another conversion is required. The terminal count output from the counter may be conveniently used as a conversion complete signal.

This method of analog to digital conversion is extremely fast. However if a higher speed is needed, it can be achieved by decoding the 13th state of the counter and using the decoded output to inhibit further counting, thus allowing conversion in 13 clock periods. The same scheme can be extended by using the extra time periods for conversion to a 14-bit or a 15-bit accuracy.

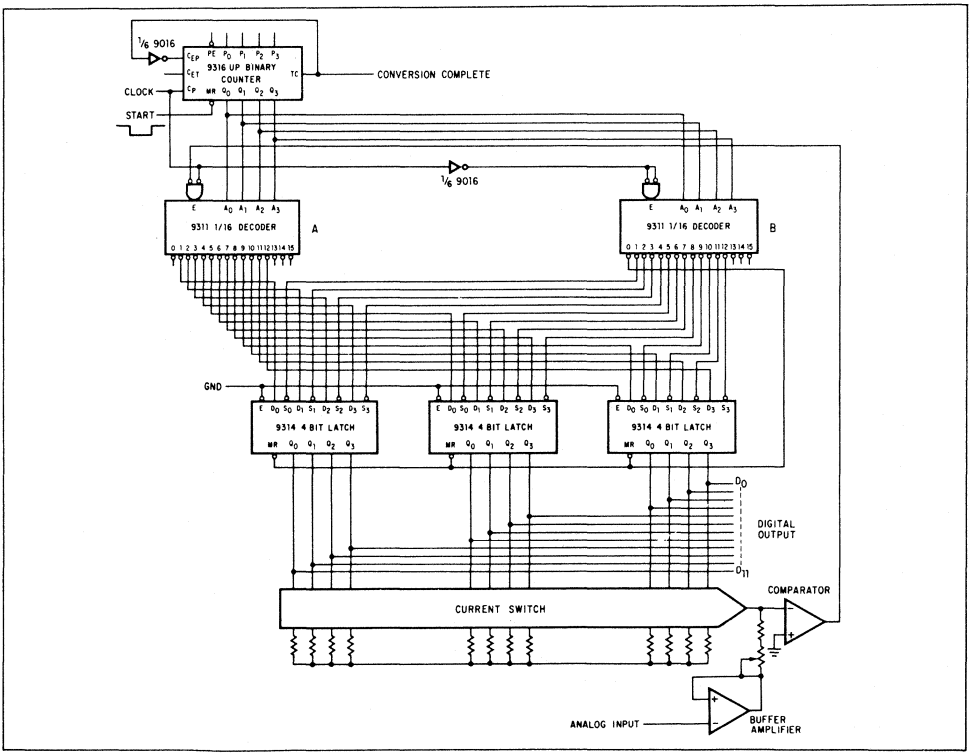


Fig. 14. 12-bit analog-to-digital conversion.

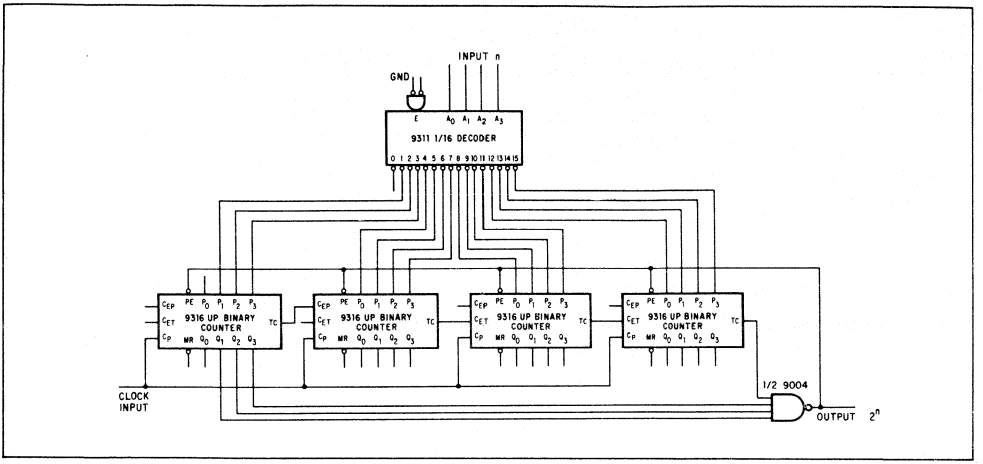


Fig. 15. Programmable divider ÷ 2^n.

Counter Applications

A programmable counter can be designed using a decoder that counts in modulo 2^n where n is the programmable input. Figure 15 shows such a design. It consists of a 9311 decoder and four 9316 binary counters capable of counting up to 2^{15}. The input n drives the selected output low so that when a parallel load occurs, all highs are written into the register except at the stage represented by the address n. The counter counts pulses and reaches the condition 0000111111111 at which point the terminal count of the last stage goes high. This process depends solely on the first three counting blocks since the terminal count of a stage enters a counter's CET input only after the first block. After 14 additional pulses bring the total to 2^n, the three remaining inputs to the 9004 gate are high, and a parallel load takes place resetting the counter to its original condition. The design therefore performs as a 2^n programmable divider.

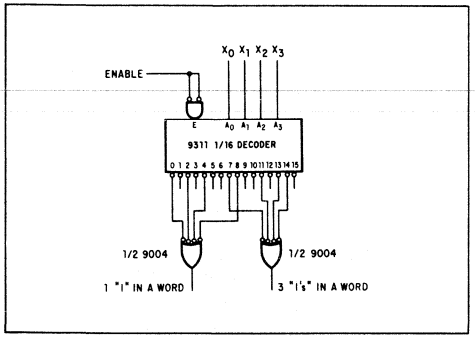


Fig. 16. Sum of minterms.

Minterm Generation

Since it produces the 16 possible minterms from 4 variables, the 9311 decoder may be regarded as a minterm generator and can therefore be used in control or random logic areas. This is done by summing appropriate minterms with an active low OR gate to produce the desired complex function. In Figure 16, appropriate minterms are summed to provide a detector for just a single "1" in a word and for three "1"s in a word. When used in conjunction with the 9301 decoder and 9309/9312 multiplexers for generating logic functions, the 9311 becomes a powerful logic tool for the design of complex control systems.

Summary

This Application Note has described the operation and some of the applications of the 9311 1-out-of-16 MSI decoder. The device is particularly suitable for memory decoding and provides functional building block design capability when used with other MSI circuits in the 9300 family.

These 9300 MSI devices offer significant system advantages over discrete gates and flip-flops in a digital system. Design time is shorter, design is simpler, and systems are easier to build and understand. There are fewer wires and soldered joints since more component interconnections are now on-chip connections. Consequently, the systems are more reliable and easier to maintain. The modern trend toward functional building blocks such as the 9311 decoder has resulted in smaller, faster, more dependable, and more economical digital systems.

TTL/MSI 9305
VARIABLE MODULO COUNTER

INTRODUCTION

The TTL/MSI 9305 variable module counter is designed to serve in many counting and division applications in a digital system. The 9305 is an extremely versatile device, offering standard binary counter modulos such as tabulated below without additional logic. In addition the TTL/MSI 9305 allows the logic designer to implement difficult divide functions and regular divide/count functions economically both in terms of cost and logic required.

WITH JUST ONE 9305 COUNTER

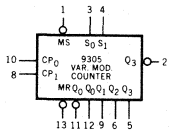
THE FOLLOWING CAN BE DONE

BINARY COUNTING MODES Without Additional Logic	FREQUENCY DIVISION MODES With 50% Duty Cycle Without Additional Logic	ODD DIVISION Modes With Additional Logic
Modulo 2	Modulo 8	Modulo 11
4	10	13
5	12	15
6	14	
7	16	
8		
10 (8421 BCD)		
12		
14		
16		

The logic symbol chosen to represent the 9305 along with a table of pin functions, loading and pin layout are shown in Figure 1.

FAIRCHILD
SEMICONDUCTOR

LOGIC SYMBOL



V_{CC} = Pin 14
Gnd = Pin 7

PIN FUNCTIONS

S_0, S_1	Select Inputs
CP_0	First Stage Clock Active High Going Edge Input
CP_1	Three Stage Clock Active High Going Edge Input
$\overline{MS}$	Master Set (Active Low) Input
$\overline{MR}$	Master Reset (Active Low) Input
Q_0	First Stage Output
$\bar{Q}_0$	Complementary First Stage Output
Q_1, Q_2, Q_3	Three Stage Counter Outputs
$\bar{Q}_3$	Complementary Last Stage Output

LOADING RULES

INPUTS	LOADINGS
CP_0, CP_1 $\overline{MS}$, $\overline{MR}$ S_0, S_1	1 U.L.

OUTPUTS	FANOUT AT LOGIC LEVEL	
	HIGH	LOW
Q_0, $\bar{Q}_0$, Q_1, Q_2, Q_3	16 U.L.	8 U.L.
$\bar{Q}_3$	20 U.L.	10 U.L.

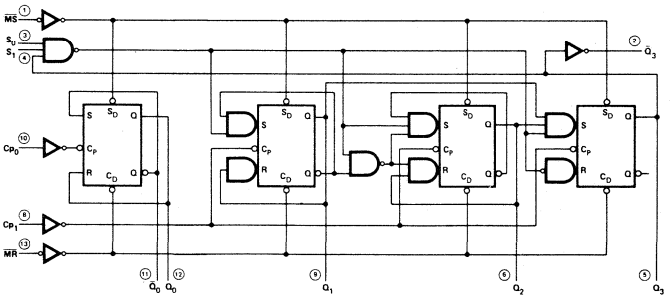
(1 U.L. = 1 TTμL gate input load)

Fig. 1

LOGIC DESCRIPTION

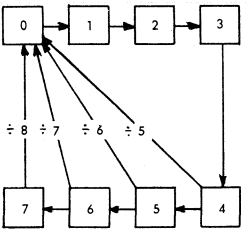
The logic diagram for the 9305 is illustrated in Figure 2. It shows that the 9305 consists of four R/S master slave flip-flops. The four flip-flops are separated into two functional units, a single toggle (first flip-flop) stage and a three stage programmable synchronous binary counter (2nd, 3rd, 4th flip-flops). A clock buffer drives the first R/S flip-flop toggle stage and a second clock buffer drives the three S/R flip-flops in parallel to obtain three-stage synchronous operation.

LOGIC DIAGRAM



V_{CC} = Pin 14
Gnd = Pin 7

STATE TABLE FOR PROGRAMMABLE THREE-STAGE COUTER



DECIMAL NUMBER	ENCODED NUMBER		
	Q_1	Q_2	Q_3
0	0	0	0
1	1	0	0
2	0	1	0
3	1	1	0
4	0	0	1
5	1	0	1
6	0	1	1
7	1	1	1

Fig. 2

The following sequence of events defines the operation of the master slave flip-flops relative to the clock input.

When the clock input (CP) is low, the slave is steady, but data can enter the master via the R and the S inputs. During the low-to-high transition of the CP, (1) the data inputs (R and S) are inhibited, so that a later change in the input data will not affect the master, and (2) the information now trapped in the master is transferred to the slave and appears at the outputs. When the transfer is completed, both the master and the slave are steady as long as the clock input remains high, regardless of any other logic input, except Master Reset ($\overline{MR}$) and Master Set ($\overline{MS}$).

During the high-to-low transition of the clock, (1) the transfer path from master to slave is inhibited, leaving the slave steady in its present state, and (2) the data inputs (R and S) are enabled permitting new data to enter the master.

The first stage R/S flip-flop is cross-coupled to provide a toggle stage. The R/S flip-flops of the three-stage counter are connected for synchronous binary counting. The synchronous "AND" reset with inputs S_0, S_1 and output Q_3, control the modulo of the three-stage counter by synchronously resetting all three flip-flops to zero when all the inputs are high. One input of this gate is returned internally from the last counter output (Q_3) and prevents the counter from being synchronously reset before five binary states have occurred. Therefore the reset state between five and eight, and correspondingly the count modulo, depends on the programming connections made to these two inputs (S_0, S_1). For example, if the S_0 input is connected to the Q_2 output and the S_1 input is connected to the Q_1 output, the counter will count until Q_1, Q_2, Q_3 are all high and then reset to zero synchronously with the clock to produce a modulo eight binary counter.

The complement output as well as the true output is available on the first toggle stage and last stage of the three-stage counter. These complement outputs allow binary ripple clocking on the correct transition when the first toggle stage and three-stage counter are connected together and/or stages are cascaded.

The synchronous set and reset are connected through noninverting buffers to the appropriate set direct and clear direct input of all four flip-flops.

As can be seen from the loading table in Figure 1, all inputs are buffered presenting only one unit load to the driving logic. Also all the outputs have a high drive capability of at least eight unit loads. Both the low fan-in and high fan-out of the 9305 reduce the package count of a digital system since fewer external buffers are required and improve the performance by eliminating their corresponding delay.

MODES OF OPERATION

Basic Configuration

The three-stage counter is programmed with external connections, as shown in Table 1, to provide synchronous binary count modulos of either 5, 6, 7, or 8. The programming of the three stages is independent of the toggle stage and the basic configuration allows synchronous binary counting by the last three stages and modulo 2 operation by the first stage.

PROGRAMMING CONNECTIONS FOR LAST THREE STAGES

TABLE 1

S_0	S_1	MODULO
Q_3	Q_3	5
Q_1	Q_1	6
Q_2	Q_2	7
Q_1	Q_2	8
Q_2	Q_1	8

These connections are equivalent to those given on the data sheet. They provide the most convenient and most appropriate method of terminating unused select inputs.

Simultaneous frequency divisions of 2, 4 and 8 are available from the three-stage counter when programmed to divide by eight.

Four Stage Configurations

The single-stage and three-stage counters are connected together without additional logic to form modulo 10 (8421 BCD), 12, 14 and 16 binary counters or 50% output duty cycle dividers. The connections for these four bit dividers and counters are summarized in Table 2.

CONNECTIONS FOR MODULO 10, 12, 14, 16 BINARY COUNTERS AND 50% DUTY CYCLE DIVIDERS

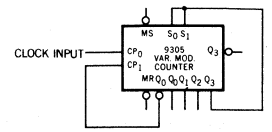
For Binary Counting $\overline{Q}_0$ connected to CP_1 Incoming clock to CP_0
For 50% Duty Cycle Output $\overline{Q}_3$ connected to CP_0 Incoming clock to CP_1

TABLE 2

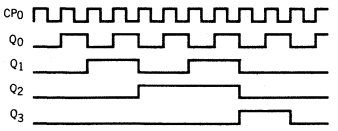
Table 2 shows that a four-stage binary counter with a modulo of 10, 12, 14 or 16 is obtained by applying the incoming clock to the single toggle stage and feeding its negation output to the clock input of the three-stage counter.

Figure 3 shows most of these counter configurations as well as their count sequences.

MODULO 10 COUNTER (BCD 8421 DECADE)

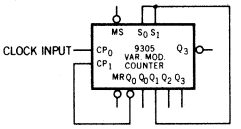


WAVEFORMS

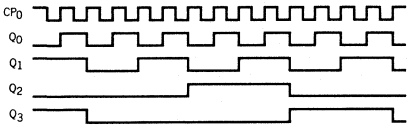


Count Sequence			
Q_0	Q_1	Q_2	Q_3
0	0	0	0
1	0	0	0
0	1	0	0
1	1	0	0
0	0	1	0
1	0	1	0
0	1	1	0
1	1	1	0
0	0	0	1
1	0	0	1

MODULO 12 COUNTER

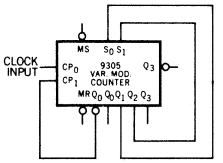


WAVEFORMS

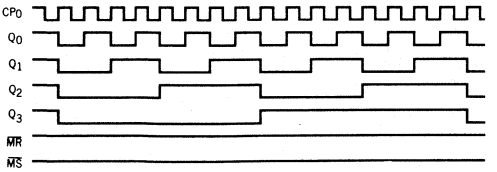


Count Sequence			
Q_0	Q_1	Q_2	Q_3
0	0	0	0
1	0	0	0
0	1	0	0
1	1	0	0
0	0	1	0
1	0	1	0
0	1	1	0
1	1	1	0
0	0	0	1
1	0	0	1
0	1	0	1
1	1	0	1

MODULO 16 COUNTER (4 BIT BINARY COUNTER)



WAVEFORMS



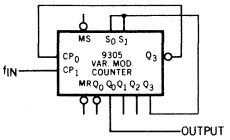
Count Sequence			
Q_0	Q_1	Q_2	Q_3
0	0	0	0
1	0	0	0
0	1	0	0
1	1	0	0
0	0	1	0
1	0	1	0
0	1	1	0
1	1	1	0
0	0	0	1
1	0	0	1
0	1	0	1
1	1	0	1
0	0	1	1
1	0	1	1
0	1	1	1
1	1	1	1

FIG. 3 STANDARD 4-BIT COUNTER CONFIGURATIONS

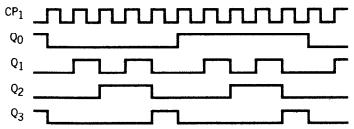
A four-stage divider with 50% duty cycle output is produced by feeding the incoming clock to the three-stage counter and clocking the single toggle stage with the $\overline{Q_3}$ output. Figure 4 illustrates divider configurations of modulo 10 and 12. Modulo 16 division with 50% duty cycle is obtained from the Q_3 output of the MOD 16 binary counter. In either the binary or 50% division mode the modulo (10, 12, 14, 16) is determined only by the external programming connections for the three-stage counter. These four-stage counters or dividers are not fully synchronous (semisynchronous) but have only one flip-flop ripple delay in any of these configurations. This flip-flop delay compares favorably with the more typical ripple delay of three in other counters, thus allowing higher operating speeds, typically where counter states must be decoded.

FIG. 4 50% DUTY CYCLE OUTPUT DIVIDERS

MOD 10 DIVIDER, 50% DUTY CYCLE OUTPUT

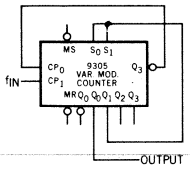


WAVEFORMS

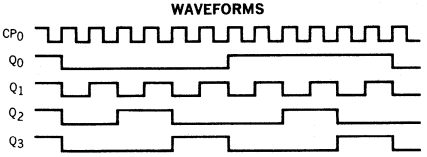


Count Sequence			
Q_0	Q_1	Q_2	Q_3
0	0	0	0
0	1	0	0
0	0	1	0
0	1	1	0
0	0	0	1
1	0	0	0
1	1	0	0
1	0	1	0
1	1	1	0
1	0	0	1

MOD 12 DIVIDER, 50% DUTY CYCLE OUTPUT



WAVEFORMS



Count Sequence			
Q_0	Q_1	Q_2	Q_3
0	0	0	0
0	1	0	0
0	0	1	0
0	1	1	0
0	0	0	1
0	1	0	1
1	0	0	0
1	1	0	0
1	0	1	0
1	1	1	0
1	0	0	1
1	1	0	1

Four-Bit dividers with odd divide modulos can be formed with a few extra gates as illustrated in the application section.

Asynchronous Reset and Set Modes

The master set and reset will asynchronously set or reset all four stages when activated. The active low reset input when low will clear the counter, overriding the clock and forcing the outputs Q_{0-3} low and outputs $\overline{Q_0}$, $\overline{Q_3}$ high. The active low set input when low will preset the counter, overriding the clock and forcing the outputs Q_{0-3} high and outputs Q_0, $\overline{Q_3}$ low. The master set provides a synchronous clear, since the first clock pulse following the asynchronous master set will reset all stages. This action is independent of the modulo programmed. Table 3 summarizes the asynchronous modes.

TABLE 3

ASYNCHRONOUS MODE

$\overline{MS}$	$\overline{MR}$	Q_0	$\overline{Q_0}$	Q_1	Q_2	Q_3	$\overline{Q_3}$
L	H	H	L	H	H	H	L
H	L	L	H	L	L	L	H
H	H	COUNT*					

*As Determined by Programming Connections

The table does not include the condition when both active low set and reset are activated. In the typical digital system there is no advantage or occasion where both are active. However, there are no restrictions on activating the two inputs as long as one remembers that both signals cannot be removed simultaneously and the state of the counter assured. When both set and reset are activated all outputs will be high except for the $\overline{Q_3}$ output which will be low.

APPLICATIONS

Multistage Counters/Dividers

Variable Modulo 9305 counters can be connected together without additional logic to form ripple type multistage counters or dividers. This is accomplished by connecting the active low $\overline{Q_3}$ or $\overline{Q_0}$ output of the less significant counter to the clock input of the following counter. As a result of these connections the more significant counter will be clocked when the less significant counter changes from its terminal count value to zero count value.

The connections required for a multistage ripple counter are shown in Figure 5. The 9305's are programmed in this case to form BCD decades, however, the same interconnections will permit multistage counting with the other counter modulos.

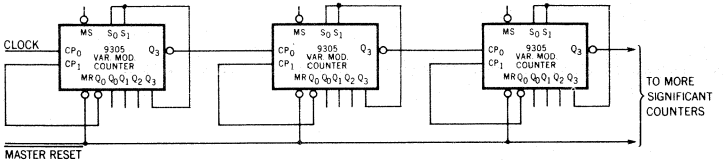


FIG. 5 - MULTISTAGE COUNTER

The ripple multistage counter formed with the 9305's has less ripple delay than the conventional ripple counter, since it has only one ripple delay per four bits. This means, for example, the number of ripple delays for a typical 16-bit ripple binary counter would be fifteen where a 16-bit counter composed of 9305's would have only seven ripple delays. In certain applications, the large ripple delay of conventional integrated 4-bit counters might dictate fully synchronous operation using relatively more expensive counters.

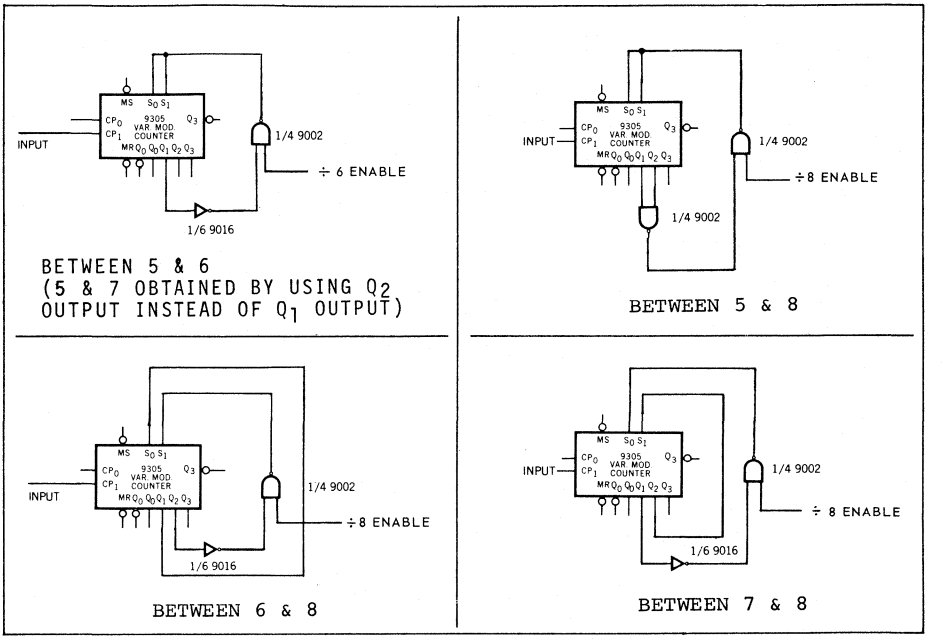
Variable Count Modulos

The count modulo of the 9305 can be logically controlled with additional gating logic. This logic is inserted between the appropriate counter output(s) and the select inputs. The logic then controls when the programmable three-stage counter is reset. The amount of logic required depends on the number of different count modulos desired. Control between two count modulos is all that most applications require, although control between three or four distinct count modulos would be possible with an increase of logic required.

Figure 6 illustrates the gating required for the programmable three-stage synchronous counter to logically control its modulo between 5 and 6, 5 and 7, 6 and 8, 7 and 8. To switch between modulo 5 and modulo 6, a representative case, a NAND gate and inverter are needed. When the enable line is low, the output of the NAND gate is high and accordingly allows the counter to only divide by five. With the control line high, the state of the Q_1 output is applied, without inversion through the inverter and NAND gate to the S_0 or S_1 input allowing modulo 6 operation.

In each case illustrated a high logic level will give the higher modulo.

FIG. 6 - CONTROLLABLE MODULO CONFIGURATIONS



These controllable modulo configurations can be used with the first stage and/or cascaded to produce counters and dividers with two or more modulos. These controllable configurations are the basis of the odd modulo and multistage dividers discussed next. They allow economical implementation of difficult divide functions.

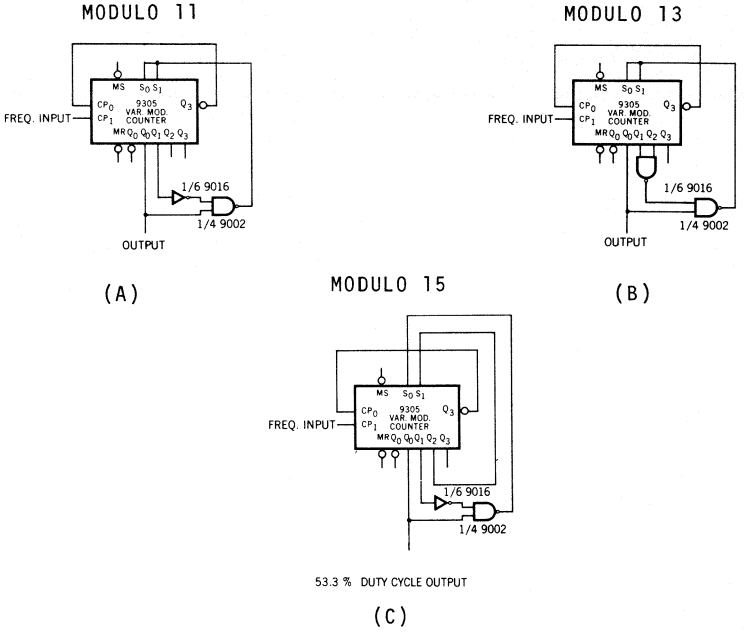
Dividers With Odd Modulos

Dividers with odd modulos can be built by utilizing one of the several logically controllable counter configurations. The single toggle stage, three-stage counter, or other combinations of other 9305 counters are used to control the modulo and simultaneously divide the output of the controllable counter.

Figure 7 illustrates some four-bit odd modulo dividers; modulo 11, modulo 13 and modulo 15. Each of these 4-bit dividers is easily implemented by adding two gates or one gate and inverter to a single 9305. The first single stage in all of these dividers is clocked by the three-stage counter and alternately switches the three-stage counter's modulo between the upper and lower modulo. The incoming clock is applied to the clock of the three-stage counter and the output taken from the first stage. The output obtained for these four-bit odd modulos is nearly 50% duty cycle.

In Figure 7a the three-stage programmable counter of the 9305 is alternately switched between modulo 5 and modulo 6 by the first stage flip-flop to obtain MOD 11, while controllable dividers of modulo 6 or 7 and modulo 8 or 8 are used in the modulos 13 and 15 dividers in Figure 7b and Figure 7c respectively.

FIG. 7 - 4-BIT ODD MODULO DIVIDERS



Full count speed is maintained since the control logic is not in a critical path. The first stage changes state (clocked) after the terminal state of the three-stage counter, which is at least four states before the inputs to the select gates need be present and stable. Dividers with large odd modulo divide ratios, such as 525 are discussed in the next section.

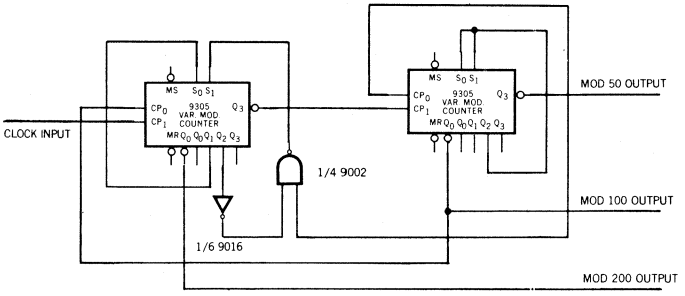
Multistage Fixed Modulo Dividers

Multistage dividers having large odd or even divide ratios can be implemented with very little additional logic and usually all the flip-flops in the 9305 can be utilized. These dividers can be formed in basically the same way as the four-bit odd modulo dividers just discussed. In these multistage dividers a multistage counter, as opposed to a single stage, controls and simultaneously divides the output of a

controllable modulo configuration. Of course conventional methods of cascading dividers to obtain large divide ratios can be used.

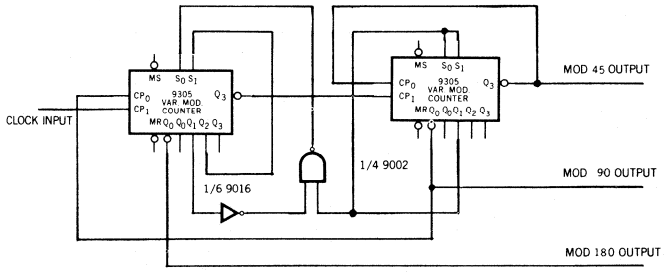
The 50/100/200 modulo divider shown in Figure 8a supplies these frequency divisions simultaneously. It uses a controllable modulo configuration of 6 and 8 (first 9305) that clocks a modulo 7 binary counter. The control for the modulo 6 or 8 counter is taken from the complement of the last stage of the modulo 7 counter, that directs the controllable modulo counter to divide by six three times and by eight four times. The modulo 50 output of the modulo 7 counter can be divided by the first stage of each 9305 used, to give modulo 100 and modulo 200 division. The two toggle stages could operate independently if modulo 100 or modulo 200 division were not needed.

FIG. 8a



MODULO 50/100/200 DIVIDER

FIG. 8b



MODULO 45/90/180 DIVIDER

The modulo 45/90/180 divider shown in Figure 8b is formed in a similar manner. In this divider the programmable three-stage counter of the first 9305 is set up to divide by seven and eight. This three-stage counter clocks the three-stage programmable counter of the second 9305 which is set up to divide by six. The first stage output of the second three-stage counter is used to control the seven/eight counter and directs it to divide by seven three times, and eight three times. The modulo 45 output occurs at the Q_3 output of the second three-stage counter. As before the first stages of each 9305 are used to divide the MOD 45 output further to obtain MOS 90 and MOD 180 division.

Figures 8c and 8d illustrate two basic TV sync generators. The 525 divider produces wave forms basic to the American EIA standard and the waveforms of the modulo 625 divider are basic to the European CCIR standard. Both the waveforms of the modulo 525 divider and modulo 625 divider are The Primary Timing waveforms. By gating the waveforms shown with appropriate equalizing, vertical serration, and blanking signals, standard sync waveforms can be generated.

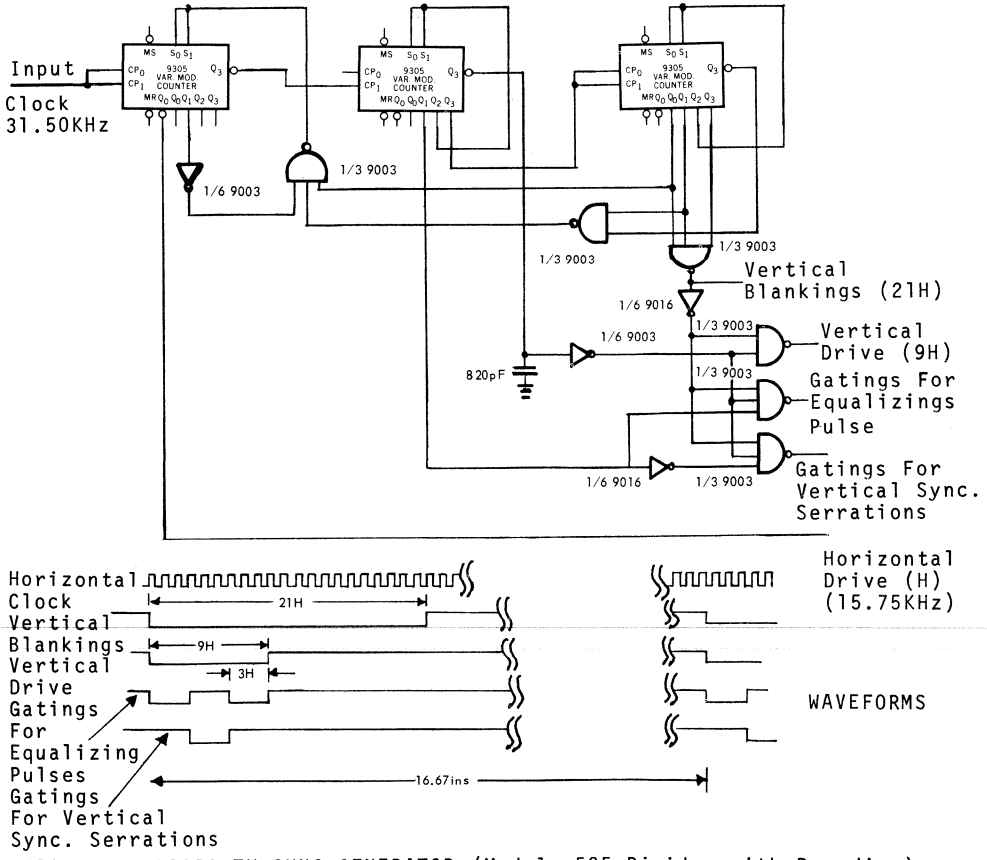


FIG. 8c - BASIC TV SYNC GENERATOR (Modulo 525 Divider with Decoding)

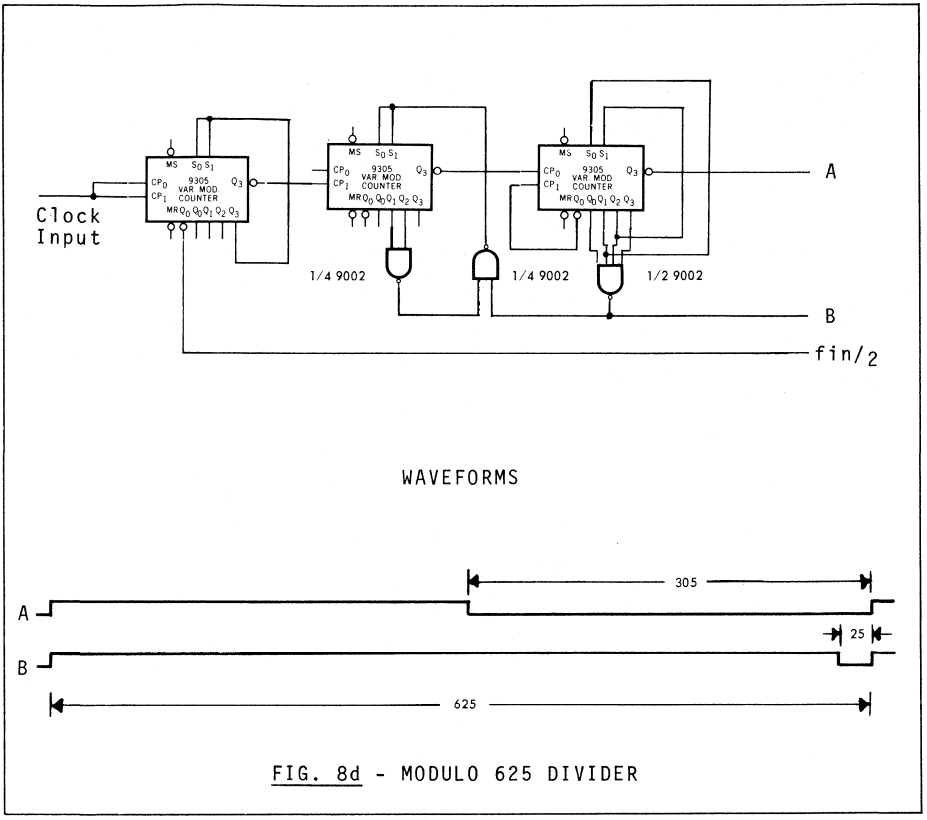


FIG. 8d - MODULO 625 DIVIDER

Multistage dividers that are semisynchronous or synchronous can be implemented by simultaneously clocking two or more 9305 counters that are relative prime (have no common factor). Since the counters are relatively prime, each state of the total counter is unique and any state can be decoded with gates to provide division. This method of implementing multistage dividers generally requires more gating logic than the cascaded divider configurations shown.

Sequencer

The one-of-ten sequencer shown in Figure 9 utilizes the 9305 as a modulo 10 counter for generation of the decoder address. The 9305 is connected synchronously to minimize the delay between counter outputs and the corresponding transients on the decoder outputs.

The synchronous operation is possible because the modulo of the first stage (2) and the modulo of the three-stage counter (5) are relative prime modulos. Thus ten unique states are produced by clocking the two counters simultaneously. The count sequence for this configuration is also shown in Figure 9.

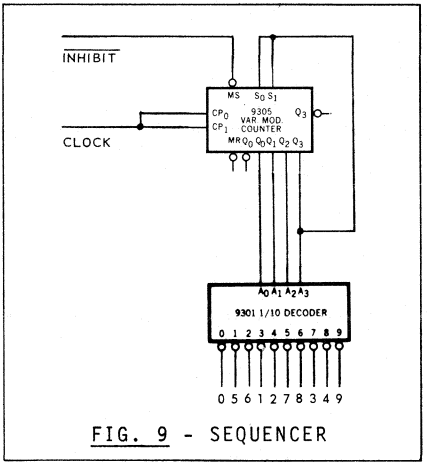


FIG. 9 - SEQUENCER

Count Sequence			
Q_0	Q_1	Q_2	Q_3
0	0	0	0
1	1	0	0
0	0	1	0
1	1	1	0
0	0	0	1
1	0	0	0
0	1	0	0
1	0	1	0
0	1	1	0
1	0	0	1

As can be seen in Figure 9, a BCD count sequence is not obtained. However, rearranging the order in which the decoder outputs are connected to the driven logic or driven devices can compensate for this.

The master set inhibits the sequencer by setting all counter outputs ($Q_{0,1,2,3}$) to one, thus blanking the 9301, which will not recognize codes above nine. When the master set is deactivated, the counter will sequence to zero synchronously with the next clock.

Counter with Enables

Single or multiple count enables can be added to the 9305 with an inverter and NAND as shown in Figure 10. The 9305 will not count if any of the count enables are low. Changes in the enables should only be made while the clock is high.

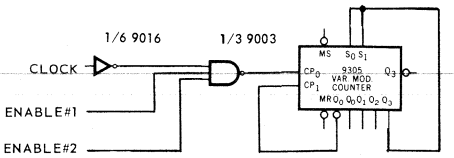


FIG. 10 - 9305 WITH COUNT ENABLES

Rate Multipliers

The 9305 counter is used as the master counter in the BCD rate multiplying scheme shown in Figure 11. The 9305's were connected synchronously because this count sequence as applied to the priority encoder produces a code which gives aninterlace sampling pattern for rate multiplying BCD 8421 numbers.

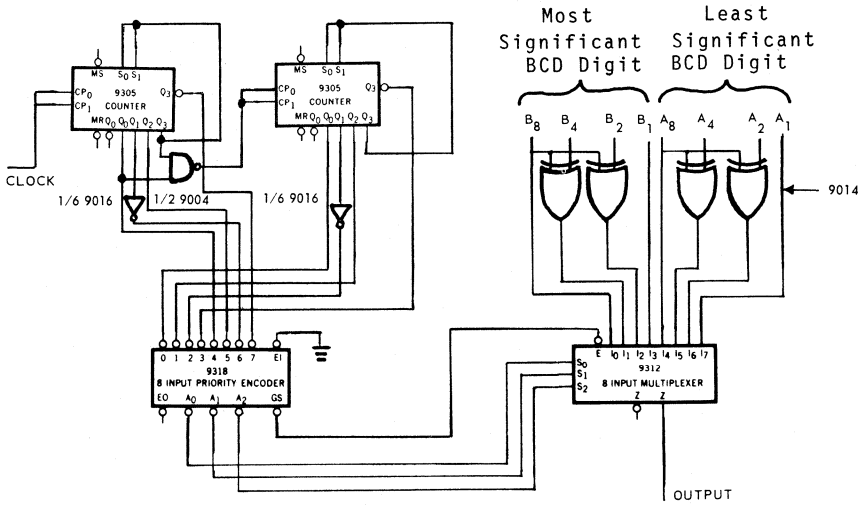


FIG. 11 - TWO DIGIT BCD RATE MULTIPLIER

THE 9601, A SECOND GENERATION RETRIGGERABLE ONE-SHOT

INTRODUCTION

A retriggerable monostable multivibrator is a one-shot that

- Has a maximum duty cycle as high as 100%
- Responds to input triggers while in an active timing state
- Completes one timing cycle after the last received input pulse.

The Fairchild 9601 is a retriggerable IC one-shot. It can serve as a pulse absence detector, digital low-pass filter, square wave generator, variable pulse delay generator, long delay timer and FM demodulator.

The 9601 has the following features:

(1) 100% maximum duty cycle
(2) CCSL compatibility with totem pole outputs
(3) Leading and trailing edge triggering
(4) Maximum repetition rate greater than 10 MHz
(5) D-C coupled inputs that are insensitive to transition times
(6) Input clamp diodes to ground
(7) Output pulse width insensitive to power supply variations.

CIRCUIT

A block diagram of the 9601 is shown in Figure 1. The trigger input gating is d-c coupled and hence independent of input transition times. Both true and complemented inputs are provided. The differentiator converts to a pulse the output transition of the input gating circuitry, and as a result, the output period and the input period are independent.

The discharge circuit receives a short pulse from the differentiator and discharges the timing capacitor to initiate a timing cycle. Since long delay periods use a large capacitance and require a long discharge time, the discharge circuit must continue to discharge the capacitor until the current drops to a fixed value. Thus the discharge circuit is similar in action to a silicon-controlled rectifier (SCR).

The timing components, R_x and C_x, are external RC timing components. Whenever an input trigger is received, capacitor C_x first discharges and then begins to charge toward V_{CC} through resistor R_x.

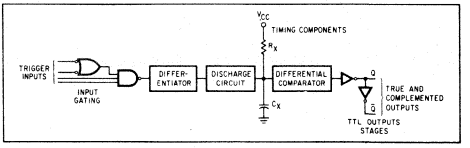


Fig. 1. Block diagram, 9601 retriggerable one-shot.

The differential comparator senses the voltage across C_x and holds the Q output high through TTL output stages while the voltage of C_x is below a differential threshold. The action is retriggerable since an input trigger will discharge C_x and begin a new delay cycle, independent of the Q output. When the voltage across C_x reaches a set fraction of V_{CC}, the differential comparator switches and drives the Q output through the TTL output stages. The Q output is also inverted and provided as the $\overline{Q}$ output.

IC IMPLEMENTATION

Owing to the component limitations inherent in standard TTL processes, the IC implementation of the block diagram of Figure 1 requires special treatment of the differentiator and discharge circuits. One method of IC implementation is shown in Figure 2a. The circuit uses an RC differentiator (R_1 - C_1) and a PNPN SCR (Q_2 - Q_3). If a negative-going pulse is applied to input T, Q_1 will cut off for a time approximately equal to $1/2\ R_1C_1$, thus triggering (through diode D_1) the SCR formed from transistors Q_2 and Q_3. The SCR is held in conduction by the C_x discharge current until the current drops to a minimum sustaining level. To retrigger, the input must first return to the high state to recharge C_1.

The circuit of Figure 2a has two serious drawbacks:

(1) Since R_1C_1 is the dominant factor in determining the minimum pulse width of the device, and since the tolerances on the IC components are loose, the minimum output pulse width varies greatly from device to device.

(2) PNP transistor Q_2 is impractical to fabricate using standard TTL IC processes.

FAIRCHILD SEMICONDUCTOR

To eliminate these two shortcomings, the circuit shown in Figure 2b was designed. This circuit is equivalent in operation to the circuit of Figure 2a and can be readily implemented using standard T^2 fabrication. It consists of a flip-flop and a monostable multivibrator interconnected through diodes. The lower flip-flop acts as the differentiator; the upper monostable multivibrator acts as an SCR.

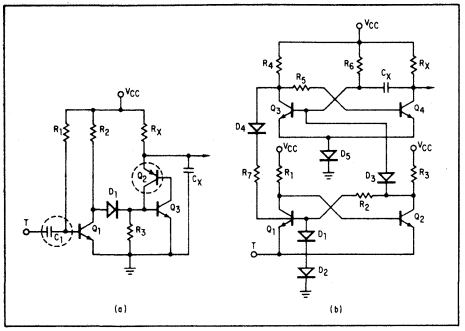


Fig. 2.

The upper flip-flop is in its stable state when Q_3 is ON and Q_4 is OFF. If T is high, D_3 is back-biased. When T drops to ground, Q_2 turns ON and sets the flip-flop. Diode clamp D_1 - D_2 ensures the correct state. The SCR-equivalent monostable then switches to its non-stable state, as Q_3 turns OFF through D_3, and remains there until C_x is discharged.

With Q_4 ON, the differentiator-equivalent flip-flop resets when Q_1 is driven on through D_4 and R_7. The resistance ratio R_7/R_2 is such that Q_4 is in saturation before Q_1 turns ON. The discharge path of C_x is through R_6, the collector of Q_4 and D_5. After C_x has lost sufficient charge, D_3 becomes again back-biased and the monostable returns to its stable state, allowing C_x to begin charging toward V_{CC}. Since R_6 is much smaller than R_x, the initial discharge period is only a small percentage of the total period. During the principal timing cycle, C_x charges through R_x, the base emitter of Q_3 and D_5. Retriggering occurs whenever T is brought high, then returned to ground. If no external timing capacitor C_x is present, the monostable returns to its stable mode as soon as the differentiator flip-flop resets.

The end result of this design is a differentiator that delivers a trigger pulse of optimum length and an SCR-equivalent discharge circuit that handles all values of C_x. Both SCR-equivalent circuit and differentiator are implemented with standard high-yield IC processes.

The differential comparator, shown in Figure 3, is an emitter-coupled Schmidt trigger. The trigger level, V_t, is given by the expression

$$V_t = \frac{(V_{CC} - V_d)\,R_4}{\frac{R_1 R_3}{R_1 + R_3} + R_4} + V_{BE}$$

where V_d is the V_{BE} of Q_3 and V_{d2} in parallel. Because Q_3 is saturated, the V_{CE} of Q_3 may be neglected. Q_1 and D_1 form a part of the monostable SCR multivibrator previously discussed.

The timing ramp equation is given as

$$V_t = (V_{CC} - V_{d1})\,(1 - e^{-t/RC}) + V_{d1} \quad \text{(neglecting } V_{CE}Q1\text{)}$$

Substituting for V_t

$$(V_{CC} - V_d)\,(.33) + V_{BE}\,Q_2 = (V_{CC} - V_d)\,(1 - e^{-t/RC}) + V_d$$

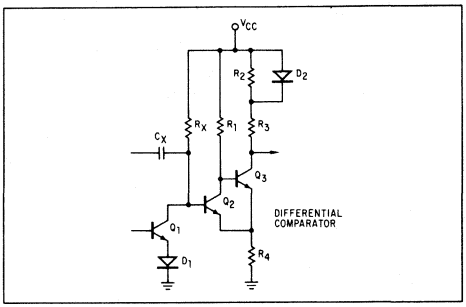


Fig. 3. Differential comparator.

If diode voltages are assumed equal, then it can be seen that the resistor ratio (.33 in this case) and the timing components, R_x-C_x, are the only factors in determining the output period. Therefore, pulse width stability over the voltage and temperature range depends on how well resistors and junction voltages track. In the integrated circuit, device sizes are tailored to current levels, and the ratio resistors are placed in the same plane and as closely together as possible in order to optimize the impedance match.

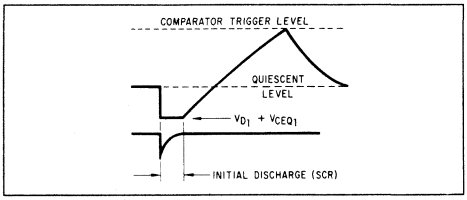


Fig. 4.

When the trigger level V_t is reached, Q_2 begins to turn ON and Q_3 cuts OFF, driving the output stage ON. Because R_x in parallel with R_1 cannot maintain across R_4 the voltage level that was previously maintained by R_1 in parallel with R_3, the turnover action is regenerative, with C_x discharging into the base of Q_2. The waveform appearing at the base of Q_2 is shown in Figure 4. Note that the impedances connected to the monostable are large enough to prevent false triggering from ground or power supply noise.

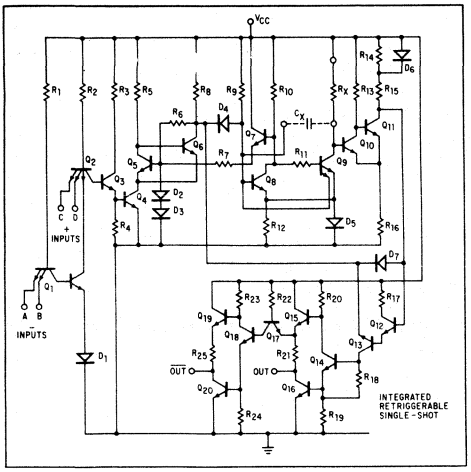


Fig. 5. Integrated retriggerable single-shot.

The complete circuit is shown in Figure 5. Input gating provides two inputs that will trigger on a positive transition and two that will trigger on a negative transition. Inputs are of the typical TTμL type and are CCSL compatible. Triggering takes place whenever Q_4 is driven ON. Q_5 and Q_6 form the differentiator-equivalent flip-flop. Q_8-Q_9 form the monostable, with feedback through Q_7 (emitter follower) and R_7. Note the extra emitter of Q_9.

Figure 3 shows that retriggering may take place at various voltage levels. In order to keep the initial discharge period more nearly constant, a fast discharge path is provided through the extra emitter of Q_9 when V_{cx} exceeds a certain value. Q_{10}, Q_{11}, and resistors R_{13}, R_{15}, and R_{16} make up the Schmidt trigger circuit. Q_{12}, Q_{13}, Q_{14} and Q_{16} form a four-diode hold-off for the true output. Q_{12} also acts as a current gain stage. Q_{13}, emitter, and D_7 connect directly to the differentiator output to substantially reduce through delay. Q_{13} base stored charge pulls the charge out of the base of Q_{14} (phase splitter). R_{14}, bypassing D_6, ensures sufficient output drive at low voltage and temperature. The complement output is a conventional TTL inverter with active pullup, driven by the true output.

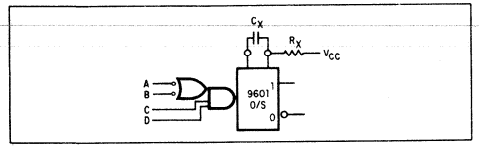


Fig. 6. Logic symbol.

The recommended logic symbol, compatible with MIL-STD-806B, is shown in Figure 6. The input combination required to trigger the 9601 is CD $(\overline{A} + \overline{B})$, i.e. both C and D must be high, and either A or B low to initiate an output pulse.

PERFORMANCE

Typical performance of the 9601 retriggerable one-shot is shown in Figures 7 through 10.

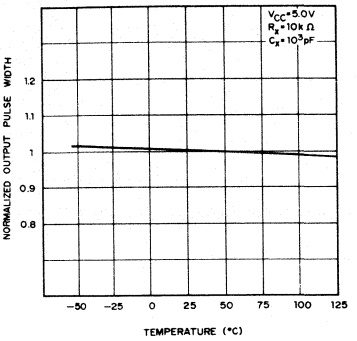


Fig. 7. Normalized output pulse width versus temperature.

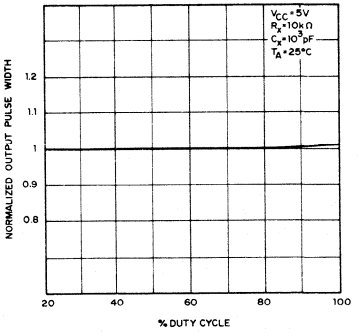


Fig. 8. Normalized output pulse width versus percent of duty cycle.

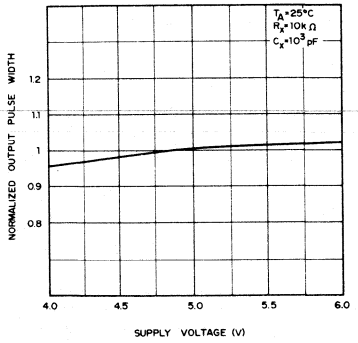


Fig. 9. Normalized output pulse width versus supply voltage.

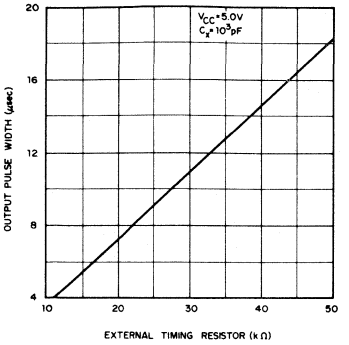


Fig 10 Output pulse width versus external timing resistor

APPLICATIONS

The 9601 may be used for virtually any application currently performed by an IC or discrete one-shot. It is particularly appropriate in systems where high noise levels are encountered. In addition, its nearly 100% duty cycle and retriggerable action open up new applications which, in the past, required multiple one-shots or synchronous techniques. Some typical applications are shown in the following paragraphs.

Non-retriggerable Operation

In situations where non-retriggerable operation is required, i. e., where input triggers are ignored during the output cycle, the input gating may be used to inhibit retriggerability, as illustrated in Figure 11. This connection may be used for frequency division of a fixed frequency input. By selection of appropriate values of R_x and C_x, the 9601 will retrigger on some multiple of input pulses.

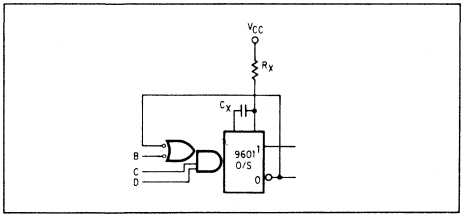


Fig 11 Connection for non-retriggerable operation

Astable Multivibrators

The most common astable configuration (Figure 12) is constructed by returning the normally high "0" output to the input AND gate to produce a retrigger (low-to-high transition) when the timing cycle has expired. This connection generates a typical positive pulse of 25 ns. For applications requiring longer positive pulses, various techniques are available to delay the retrigger pulse. Figure 13 illustrates two methods of extending pulse width.

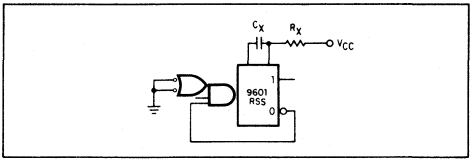


Fig. 12. Basic astable configuration.

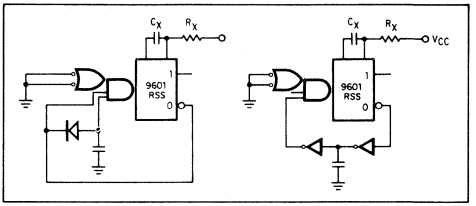


Fig. 13. Two methods of extending pulse width of 9601 astable.

To construct low frequency multivibrators without very large capacitors, the circuit of Figure 14 may be used. Resistor R_x is returned to the "1" output rather than to V_{CC}. With C_x = .47μF and R = 47kΩ, 100 Hz operation with 30 ms pulse width may be achieved.

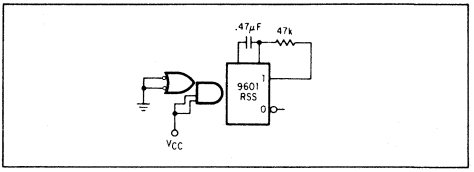


Fig. 14. 100 Hz multivibrator 2 ms pulse width.

A gated clock generator is shown in Figure 15. The output gating circuitry prevents transients from occurring when the

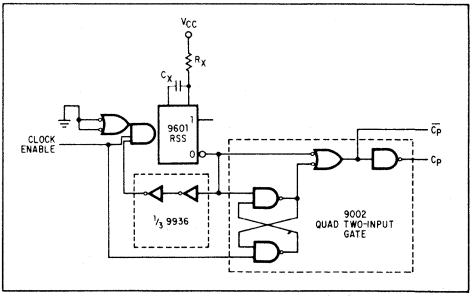


Fig. 15. Gated clock generator.

generator turns on following an enable signal. The DTL inverters in the feedback loop serve as delays to increase the output pulse width to a typical 80 ns.

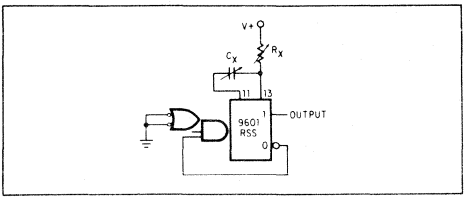


Fig. 16. Resistance-to-frequency converter.

One application of the astable connection is the analog-to-digital sensor shown in Figure 16. With the 9601 as a resistance-to-frequency converter, a change in the value of the R_X changes the timing cycle, thereby changing the frequency of operation. R_X can be any sensor that adjusts its resistance under the influence of some external parameter such as temperature, pressure, etc. In like manner, the resistance may be fixed and the capacitance altered.

A linear voltage-to-frequency converter particularly suitable for closed loop V_{CO} applications where a high frequency/voltage change ratio is required is shown in Figure 17. By this method, frequency changes of over 10 to 1 may be obtained.

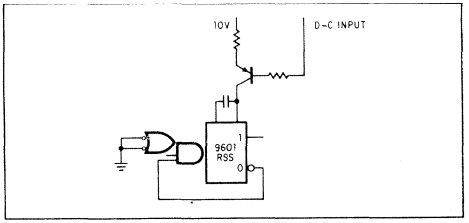


Fig. 17. Voltage-to-frequency converter.

Malfunction Indicator

A monitor which detects low speed malfunctions in a system may be constructed using the 9601 and gating circuitry shown in Figure 18. For a fixed R_X and C_X, the 9601 retriggers if the period of the triggering pulse is less than the timing cycle. The "1" output remains high as long as the 9601 continues to retrigger. A missed input pulse or a decrease in the input frequency allows the 9601 to time out, thereby setting the latch and indicating low speed malfunction. Possible applications are clock pulse and motor speed monitoring.

Delayed Pulse Generation

Two 9601's connected in tandem provide a means of delaying an input pulse and varying the pulse width (Figure 19). The 9601A determines the time T_1 before the initiation of the output pulse,

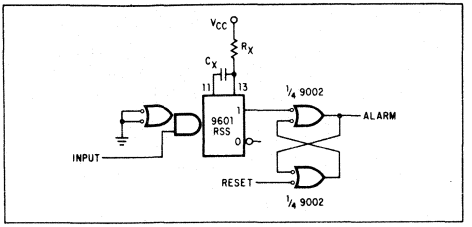


Fig. 18. Malfunction indicator.

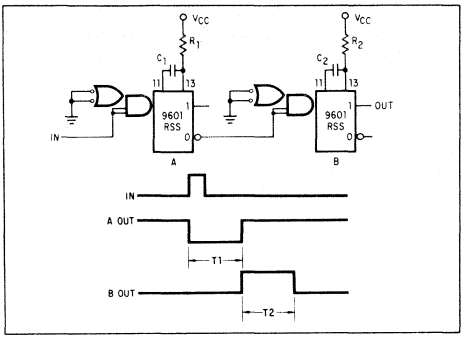


Fig. 19. Delayed pulse generation.

and the 9601B determines the output pulse width. While the timing cycle is active, the 9601's "0" output is low; the "1" output low-to-high transition at the end of the timing cycle triggers the 9601B. By returning the "0" output of the 9601B to the input of 9601A, a low frequency astable with variable duty cycle output may be achieved.

Frequency Discriminator

A simple resistor-capacitor integration network on the 9601 output may be used to produce a linear output voltage curve proportional to frequency over a limited range (Figure 20). For a given R_X and C_X, the output duty cycle will be directly proportional to input frequency. The duty cycle output is integrated by R_1 and C_1 to produce the voltage V_{out}.

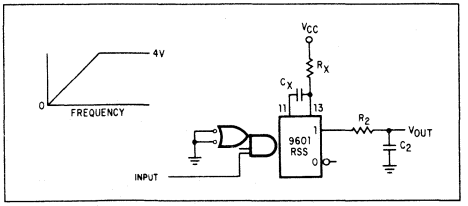


Fig. 20. Discriminator.

Pulse Duration Modulation and Detection

Pulse duration modulation allows both clock and information to be transmitted over a single line. The 9601 may be used as a PDM modulator by the circuit shown in Figure 21.

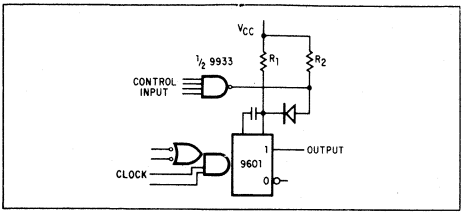


Fig. 21. PDM modulator.

Two current supplying resistors are used to provide timing cycle modulation. When R_2 is pulled to ground by the buffer, D_1 becomes reverse biased, thus making the timing cycle a function of R_1 alone and producing a long (logical 1) pulse. When R_2 is released, the effective resistance is lowered, and a shorter (logical 0) pulse is produced.

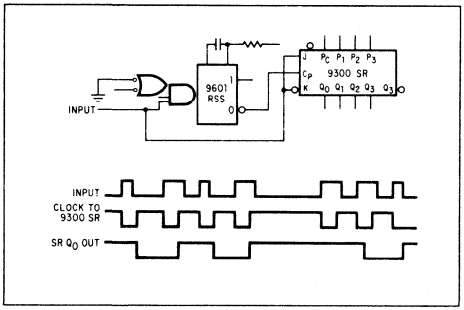


Fig. 22. PDM detection.

The decoding of PDM signals is shown in Figure 22. If the input data present a logical 0 (33% duty cycle) to the 9601 detector, the timing cycle will be longer than the input data pulse. The "0" output of the 9601 returning to its normally high state will clock a logical 0 into the 9300 four-bit shift register. A logical 1 signal (66% duty cycle) will still be high after the 9601 times out, thereby clocking a logical 1 into the shift register.

Early Termination of the Timing Cycle

The cycle timing can be terminated at any time using the circuit shown in Figure 23. If the stop input to the gate is high, a trigger input will cause the "1" output to rise, activating the gate cutting off D_2, and the one-shot will cycle normally. If the stop input to the gate is low, then R_2 and the 946 pullup resistor will terminate the cycle in approximately 100 ns, independent of R_x and C_x. With the "1" output dropped to its low inactive state, the 9601 is locked in its stable state until the next input trigger. The

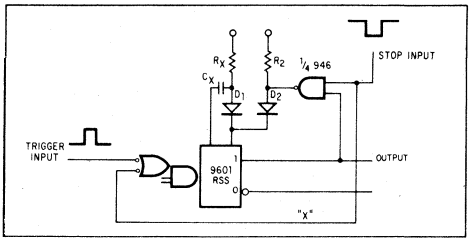


Fig. 23. Asynchronous termination of timing cycle.

length of the stop pulse must be equal to or greater than the termination delay. This delay may be shortened to about 50 ns if R_2 is reduced to 3kΩ. Connection "x" inhibits further triggering while the "stop" input is low.

Schmidt Trigger

Schmidt trigger operation is obtained by providing a triggering signal through R_x directly into the differential comparator section of the 9601 as shown in Figure 24. Input peak amplitude should be such as to supply ≥100 μamps at 2.5 volts to pin 13.

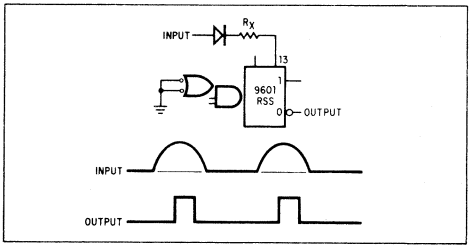


Fig. 24. 9601 used as a Schmidt trigger.

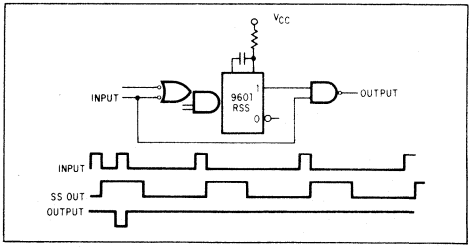


Fig. 25. Double pulse detector.

Indexing

The 9601 may be used to detect an index point on a rotating drum or disc. If a double pulse is recorded to indicate an index point, the circuit of Figure 25 will detect the index.

TTL/MSI 9360/74192 AND 9366/74193 UP/DOWN COUNTERS

INTRODUCTION

The TTL/MSI 9360/74192 is an up/down decade (8421) counter and the TTL/MSI 9366/74193 is an up/down four-bit binary counter. Both devices are synchronous, dual clock up/down counters with asynchronous parallel load, asynchronous overriding master reset, and internal terminal count logic which allows the counters to be easily cascaded without additional logic.

The 9360/74192 and 9366/74193 can be used in many up/down counting applications, particularly in those applications where the initial count value must be loaded into the counter and multistage counting is required.

These counters have active pullups for high speeds, input clamp diodes to minimize the effect of line reflections, excellent noise margins, and are compatible with all members of Fairchild's TTL Family.

DESCRIPTION

The logic diagrams for the 9360/74192 up/down decade and 9366/74193 up/down binary counters are shown in Figure 1 and Figure 2. Figure 3 shows logic symbols, pin names and loading rules.

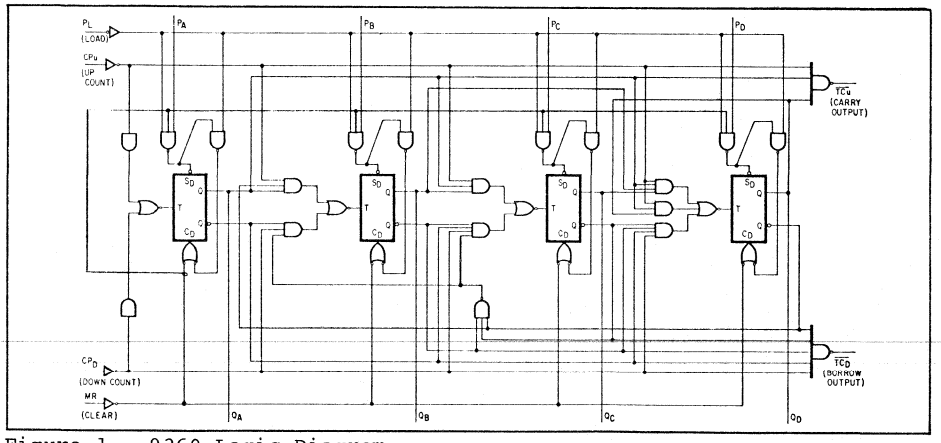


Figure 1. 9360 Logic Diagram

FAIRCHILD
SEMICONDUCTOR

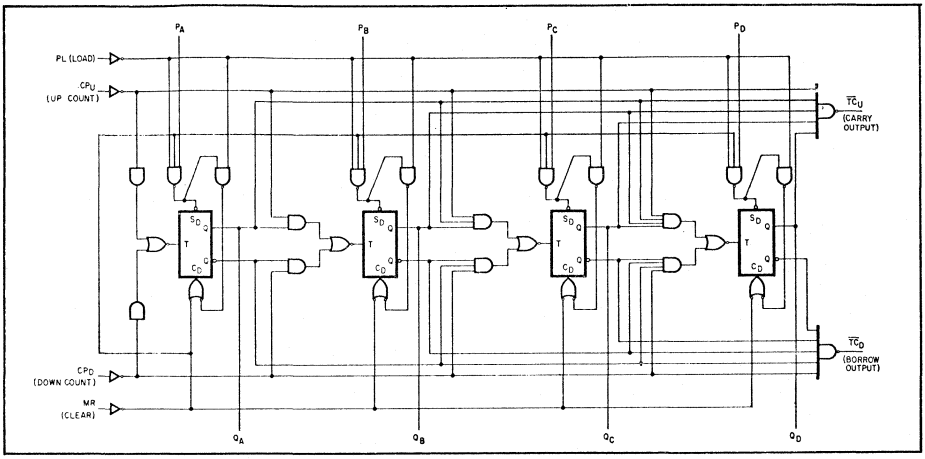


Figure 2. 9366 Logic Diagram

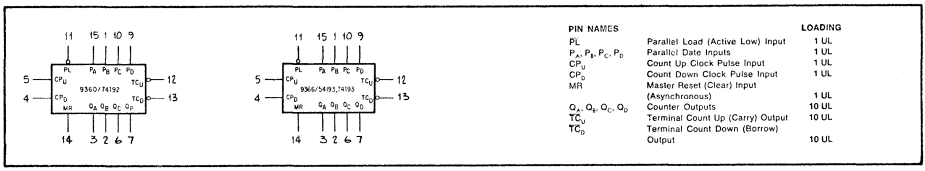


Figure 3. Logic Symbol, Pin Names, and Loading Rules

Both devices consist of four master slave flip-flops, plus steering, terminal count decoding, and preset logic. Each flip-flop is designed to toggle (change to opposite state) after each received clock pulse. Counting occurs by steering clock pulses from either the up or down clock input to the appropriate flip-flops. The clock pulse is applied simultaneously to the flip-flops and output changes are coincident, two gate delays after the rising clock edge.

The steering logic in the 9366/74192 up/down binary counter allows a particular flip-flop to receive an up clock pulse when all preceding stages are one and receive a down clock pulse when all preceding stages are zero. The first flip-flop toggles if a up or down clock is received. The 9360/74192 up/down decade counter incorporates slightly different steering logic to allow decade counting. Each flip-flop is a master slave toggle flip-flop which operates as follows: When the toggle clock input is low the slave is steady but the master is set to the opposite state of the slave. During the low to high transition of the clock the master is disabled, so that a later change in the slave outputs will not affect the master. Also the information now trapped in the master is transferred to the slave and is reflected at the output. When the transfer is completed the master and slave are steady as long as the clock input remains high. During the high to low transition of the clock, the transfer path from master to slave is inhibited, leaving the slave steady in its present stage and master enabled to be set to the opposite state of the slave.

The master slave operation of the flip-flops assures that any flip-flop change will occur while the master latch of the flip-flop is disabled and thus new data cannot affect the state of the slave.

Asynchronous set and clear inputs on each flip-flop allow the respective flip-flops to be set or cleared independently of the clock inputs.

All inputs are buffered and require only one unit load of drive. All outputs have drive capability of ten unit loads. The input loading and drive capability of this device are important in reducing the need for added external buffers in a digital system.

OPERATION

The 9360/74192 and 9366/74193 can be reset, preset and made to count up and down. The operating modes of the counters are tabulated in Figure 4, and are identical; the only difference being their count sequences (Figure 5).

MR	$\overline{PL}$	CP_U	CP_D	MODE
L	H	H	H	No Change
L	H	C_P	H	Count Up
L	H	H	C_P	Count Down
L	L	X	X	Preset (Asynchronous)
H	L	X	X	Reset (Asynchronous)
H	H	X	X	Reset (Asynchronous)

H = High Logic Level
L = Low Logic Level
X = Don't Care

Figure 4. Operating Modes

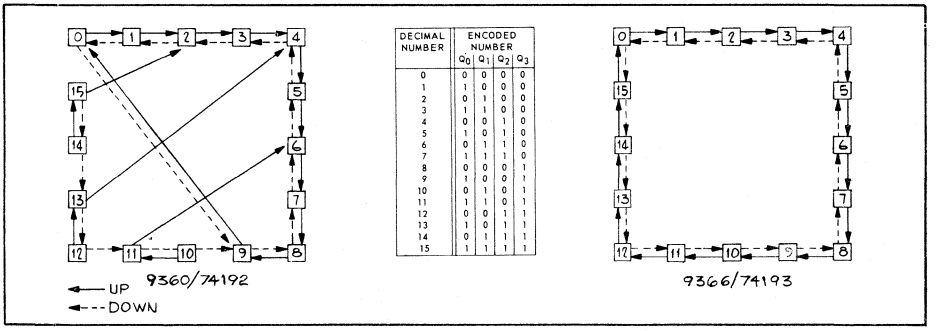


Figure 5. Count Sequences

COUNTING

Counting is synchronous with the outputs changing state after the low to high transition of either the count-up clock (CP_U) or count-down clock (CP_D). The direction of counting is determined by which clock input is pulsed while the other count input is high. Incorrect counting will occur if both the count-up clock and count-down clock inputs are low simultaneously. The counters will respond to a clock pulse on either input by changing to the next appropriate state of the sequences shown in Figure 5. (The state diagram of the 9360 shows the regular BCD (8421) sequence and in addition shows the sequence of states if a code greater than nine is preset into the counter.)

PRESET

The 9360/74192 and 9366/74193 have an asynchronous parallel load facility which permits the counter to be preset. Whenever the parallel load (PL) input is low, and master reset (MR) is low, the information present on the parallel data inputs (P_A, P_B, P_C, P_D) will be loaded into the counter and appear on the outputs independent of the conditions of the clock inputs. When the parallel load input goes high, this information is stored in the counter, and when the counter is clocked it changes to the next appropriate state in the count sequence. The parallel inputs are inhibited when the parallel load is high and have no effect on the counter.

The asynchronous master reset (MR) input, when high, overrides both clocks and parallel load and clears the counter. The asynchronous master reset overrides the parallel load and if both are active, the counter outputs will be forced to zero. Obviously, both parallel load and master reset must not be deactivated simultaneously for predictable operation.

TERMINAL COUNT LOGIC AND COUNTER CASCADING

The 9360/74192 and 9366/74193 have terminal count-up (TC_U) and terminal count-down (TC_D) outputs which allow multistage ripple binary and decade counter operations without additional logic.

The up terminal count output is low while the up clock input is low and the counter is in its highest state (fifteen for the 9366/74193, nine for the 9360/74192). Similarly, the down terminal count output is low while the down clock input is low and the counter is in state zero. The logic equations for terminal count are shown in Figure 6.

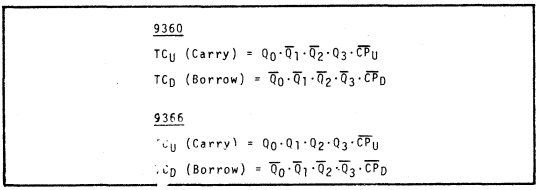


Figure 6. Terminal Count Logic Equations

The counters are cascaded (Figure 7) by feeding the up terminal-count output to the up clock input and the down terminal-count output to the down clock input of the following (more significant) counter. Therefore, when a 9366/74193 counter is in state fifteen and counting up or in state zero and counting down, a clock pulse will change the counter's state on the rising edge and simultaneously clock the following counter through the appropriate active low terminal count output. The operation of the 9360/74192 is the same except, when counting up, clocking occurs on state nine.

The delay between the clock input and the terminal count output of each counter is two gate delays (typically 16ns). Obviously these delays are accumulative when cascading counters.

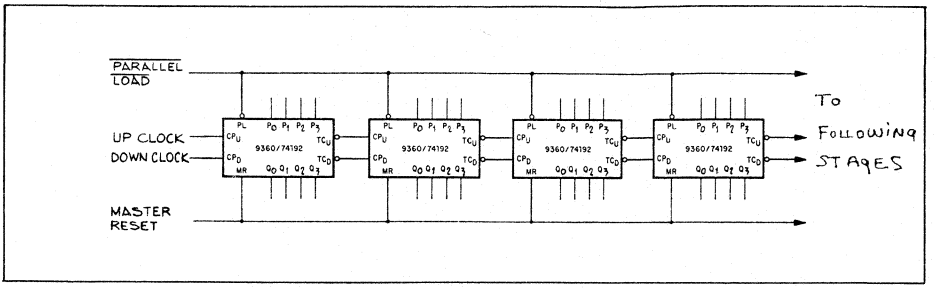


Figure 7. Connection Scheme for Multistage Up/Down Counting

When either counter is reset, the terminal-count down output will be low if the down clock is low and conversely if either counter is preset to its terminal count value, the up terminal-count output will be low while the clock is low.

APPLICATIONS

Light-Controlled Up/Down Counting

Many industrial or scientific applications require the counting of objects traveling in different directions. The circuit shown in Figure 8 is a scheme for counting moving objects as they move between a light source and phototransistors. This scheme permits the counting

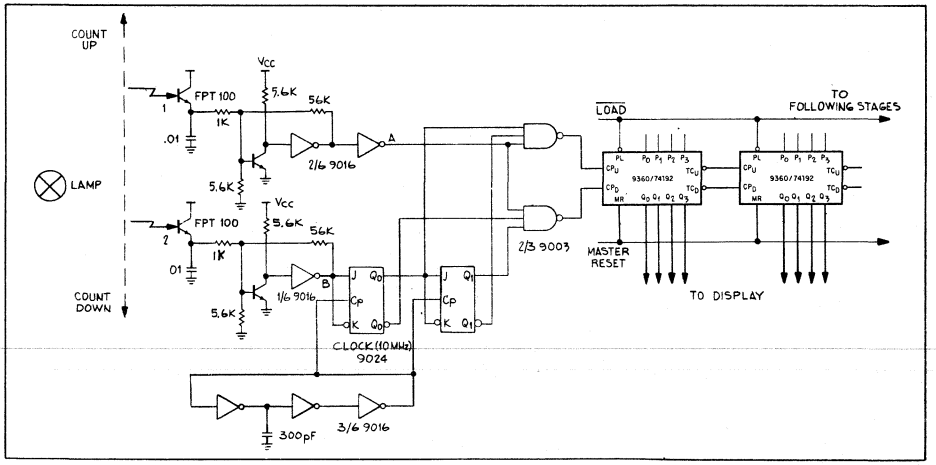


Figure 8. Light-Controlled Up/Down Counter

of objects passing in either a left or right direction and allows for reversals in movement or non-uniform movement. Each object passing from bottom to top will increment the counter, while each object passing from top to bottom will decrement the counter. Any object passing between the light source and two phototransistors will be

U

counted as long as the object is large enough to cover both transistors simultaneously.

Hex inverters serve as a clock generator and as phototransistor amplifiers. The dual flip-flop and three-input NAND gates are used to route the phototransistors signals to the up/down counters.

When an object moves from bottom to top it will cover phototransistor 2 first, bringing line B low. This will store a zero in the two-bit shift register. When the object moves further, phototransistor 1 will be covered and bring line A high. As the object moves even further it will uncover phototransistor 2, bringing line B high again. The next clock pulse will load a one into the first bit of the shift register. This one-zero combination in the shift register and high level on line A are decoded and gated with the clock to increment the counter. For an object moving from top to bottom the sequence is reversed and the counter is decremented.

Asynchronous Up/Down Pulses

A method of synchronizing asynchronous up/down input pulses and avoiding coincident pulses to the counters is shown in Figure 9. The counters will be decremented or incremented when either up or down asynchronous input makes a low to high transition. If both inputs make the transitions simultaneously, the counters are neither decremented nor incremented.

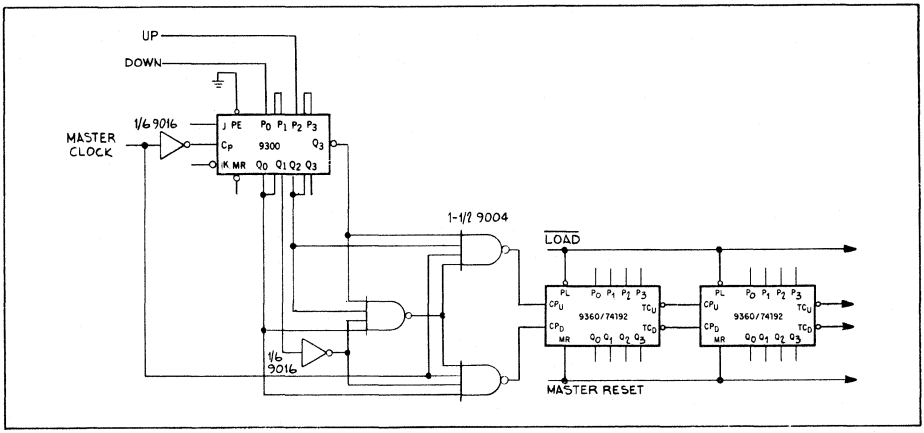


Figure 9. Synchronization and Coincident Pulse Prevention of Asynchronous Up/Down Pulses

A master clock with a frequency of at least twice the frequency of the asynchronous inputs is needed to avoid the loss of input pulses. The 9360/74192 counter outputs will be synchronized with the master clock.

The asynchronous up/down inputs are fed to a 9300 4-bit shift register, connected to form two independent two-bit shift registers. The outputs Q_0 and Q_1 reflect the information on the asynchronous down input during two clock periods and the Q_2 and Q_3 outputs reflect information on the up input during the same clock periods. This

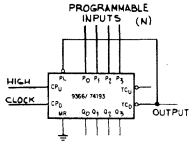
information is decoded by the three four-input NAND gates and gated with the clock to produce the 9360/74192 and 9366/74193 up or down pulses.

A low to high transition on the up input will result in Q_3 being low and Q_2 high. This is decoded and gated with the clock to increment the counter. A low to high transition on the down input will result in Q_1 being low and Q_0 high which is decoded and gated with the clock to decrement the counter. A four-input NAND gate disables both clocks to the counter when both transitions have occured simultaneously.

Programmable Dividers

The 9360/74192 and 9366/74193 can implement programmable dividers without additional logic (Figure 10). The divide ratio, N, is directly programmable in binary or BCD, by using the count down capabilities of either counter.

The divider in Figure 10 operates as follows: The counter counts down until the terminal-count value is reached, then when the clock goes low again the terminal-count output goes low and thus starts to load the initial count value into the counter. When the preset number appears on the counter outputs, the down terminal-count output will disappear and the counter will be decremented when the clock goes high.



DIVIDE RATIO	INPUT REQUIRED P_0 P_1 P_2 P_3	DECIMAL EQUIVALENT OF INPUT
1	H L L L	1
2	L H L L	2
3	H H L L	3
4	L L H L	4
5	H L H L	5
6	L H H L	6
7	H H H L	7
8	L L L H	8
9	H L L H	9
10	L H L H	10
11	H H L H	11
12	L L H H	12
13	H L H H	13
14	L H H H	14
15	H H H H	15

Figure 10. Programable Divider

The input clock width must exceed the sum of the terminal count delays (two gate delays per counter), asynchronous load delays, and clock setup time. The terminal count output is a short pulse which should be lengthened for some applications before it is applied to other logic. It may be applied to a 9601 one-shot or to a TTL flip-flop divide-by-two stage, producing a symmetrical output at half the programmed frequency.

Despite the fact that the terminal count disappears as soon as a single output changes, the internal delays are such that all flip-flops will be preset before the terminal count disappears. This is because the preset signal must propagate both through the flip-flop and the terminal count gate before the preset signal is removed. Additional delay may be desired between the terminal count output

and the parallel load input, and can be implemented with an appropriate number of inverters.

Dead End Counters

Some systems employing up/down counters require that underflow or overflow be inhibited. A change from the maximum count to zero in the count up mode or the change from zero to the maximum count value in the count down mode has to be prevented.

This limited range operation is implemented by the feedback connections illustrated in Figure 11 for the case of two 9360/74132 decade counters. The same feedback can be used with more or less than two stages and also used with the 9366/74133 binary counter. However, fifteen must be loaded into the 9366 to prevent overflow.

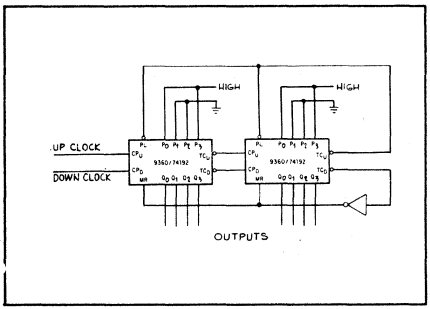


Figure 11. Dead End Up/Down Counter

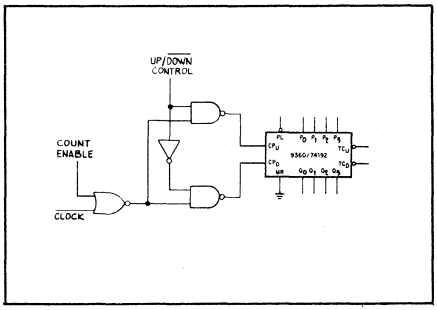


Figure 12. Single Line Up/Down Control

The lower limit for counting is established at zero by inverting the down terminal count output and applying it to the master reset input. Therefore when the counter is at state zero and a down clock is applied, terminal count down activates master reset during the entire time the clock is low keeping the counter at zero and preventing the counter from decrementing. After the down clock goes high, master reset is removed but the counter is still in state zero.

The upper limit for counting is established by connecting the up terminal count output to the parallel load input and applying the terminal count value to the preset inputs.

Single Line Up/Down Control

Figure 12 illustrates how a single line up/down control and enable can be added to the 9360/74192 or 9366/74193. All changes in the up/down enable should be done while the clock is high. This restriction is not a problem since logic transitions in most of the Fairchild TTL family follow the low to high transition of the clock pulse and thus inputs are steady before the clock goes low.

TTL/MSI 9348 12-INPUT PARITY CHECKER/GENERATOR

INTRODUCTION

The TTL/MSI 9348 is a 12-input parity checker/generator producing both odd and even parity. The 9348 is particularly suited for error detection applications including the generation and checking of parity and Hamming codes. As well as using the total capability of the 12-inputs, the device can be simply used in 8-bit, or 9-bit parity checker/generator applications. It can also be easily cascaded for longer word lengths. The 9348 is compatible with all members of the Fairchild TTL family and has features common to these units.

DESCRIPTION

The 9348 accepts 12 data inputs and provides both odd and even parity outputs. The even partiy output (PE) is high if an even number of ones are present on the inputs while the odd parity output (PO) is high if an odd number of ones are present on the inputs. Accordingly the even parity output is the complement of the odd parity output.

The Truth Table in Figure 1b (next page) summarizes the operation of the 9348.

The 9348 consists of a multi-level exclusive NOR network as shown in the logic diagram in Figure 1a.

LOGIC DIAGRAM

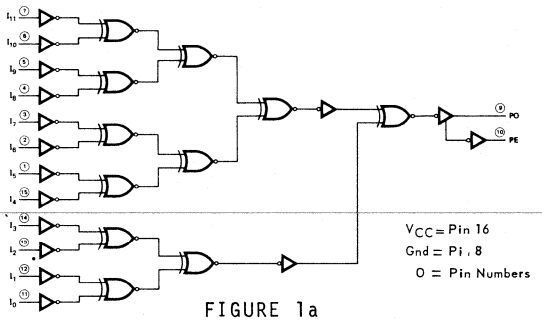


FIGURE 1a

FAIRCHILD
SEMICONDUCTOR

TRUTH TABLE

Inputs		Outputs	
I_0, I_1, I_2, I_3, I_4, I_5, I_6, I_7, I_8, I_9, I_{10}, I_{11}		P_0	P_E
All Twelve	Inputs Low	0	1
Any One	Input High	1	0
Any Two	Inputs High	0	1
Any Three	Inputs High	1	0
Any Four	Inputs High	0	1
Any Five	Inputs High	1	0
Any Six	Inputs High	0	1
Any Seven	Inputs High	1	0
Any Eight	Inputs High	0	1
Any Nine	Inputs High	1	0
Any Ten	Inputs High	0	1
Any Eleven	Inputs High	1	0
All Twelve	Inputs High	0	1

LOGIC EQUATION

$$P_0 = I_0 \oplus I_1 \oplus I_2 \oplus I_3 \oplus I_4 \oplus I_5 \oplus I_6 \oplus I_7 \oplus I_8 \oplus I_9 \oplus I_{10} \oplus I_{11}$$

$$P_E = \overline{I_0 \oplus I_1 \oplus I_2 \oplus I_3 \oplus I_4 \oplus I_5 \oplus I_6 \oplus I_7 \oplus I_8 \oplus I_9 \oplus I_{10} \oplus I_{11}}$$

FIGURE 1b

There are four exclusive NOR gate delays and three inverter delays present between eight of the inputs, I_4 through I_{11}, and the parity outputs. The remaining inputs, I_0 through I_3, have three exclusive NOR delays and three inverter delays to the parity outputs. Since inputs I_0, I_1, I_2 and I_3 have less delay, slower input signals should be applied to these inputs for maximum speed.

The parity function of the 9348 has properties associated with the exclusive NOR function that allows flexible usage. All unused inputs, for example, may be grounded or pairs of inputs connected logically high without changing the output generated by the remaining data inputs. Thus, whenever pins are unused in a single or multiple 9348 configuration they may be logically connected high or low, whichever gives faster speeds.

When all inputs are not utilized, delay through the 9348 may be minimized by proper terminations of these unused inputs. If one of the inputs of any exclusive NOR in the 9348 stays high, delay from the other input to the output is at a minimum. Therefore unused inputs should be terminated such that a high input is applied to the appropriate exclusive NOR gate input at the junction of a critical path and an unused path. Table 1 lists suggested terminations of unused inputs.

TABLE 1 - Input configurations for high speed parity checking/generations over less than twelve bits.

Number of Inputs	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8	I_9	I_{10}	I_{11}
5	D_0	L	D_1	L	D_2	L	D_3	L	D_4	L	L	L
6	D_0	L	D_1	L	D_2	L	D_3	L	D_4	L	D_5	L
7	D_0	D_1	D_2	L	D_3	L	D_4	L	D_5	L	D_6	L
8	D_0	D_1	D_2	D_3	D_4	L	D_5	L	D_6	L	D_7	L
9	D_0	D_1	D_2	D_3	D_4	D_5	D_6	L	D_7	L	D_8	L
10	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8	L	D_9	L
11	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8	D_9	D_{10}	L
12	ALL INPUTS USED											

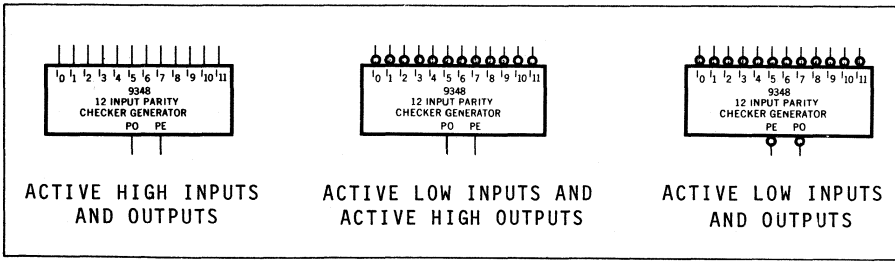
D_0 through D_N are data inputs used

L = Low Logic Level
H = High Logic Level

The function produced at each output, odd and even, can be reversed by applying a single logic high to an unused input, if one is available. For example, if parity is to be generated for eleven data bits, the one unused input can be used as a control input so that either one of the outputs produces odd or even parity functions depending on the state of the control input. Similarly provisions must be made at the checker to look at the appropriate output.

The parity functions of the 9348 can also be interpreted as shown in Figure 2, which illustrates several dual logic representations of the 9348 and indicates the use of the 9348 in systems where negative logic is used.

FIGURE 2 LOGIC REPRESENTATIONS



One 9348 parity checker/generator may be expanded by additional 9348's and/or TTL/SSI 9014 (or TTL/SSI 9N86/7486) exclusive OR gates. Depending on the application, the exclusive OR gates may be added either at the input or output of the 9348.

PARITY GENERATION AND CHECKING

The 9348, alone, will generate simultaneously both an odd and even parity bit for word lengths of up to twelve data bits. It will also perform the logically equivalent operation of checking twelve incoming bits (eleven data, one parity).

Figure 3a illustrates the generation of a parity bit for an eight-bit data word prior to the transmission of the data, and the subsequent reception and checking of the eight-bit data word and one parity bit. An even parity scheme is shown in Figure 3a. Odd parity is defined as an odd number of ones applied to the checker in a correct transmission and even parity the reverse. An odd parity scheme would utilize the opposite outputs of each 9348.

The eight data bits plus generated parity bit when applied to the 9348 checker will always have an even number of ones. This will produce a low output state on the odd parity output of the checker. If a single bit error occurs in any of the lines between generator and checker there will be an even number of ones and the checker output will go high signaling an error. A 12-bit parity generation and checking scheme is shown in Figure 3b.

8-BIT EVEN PARITY GENERATION AND CHECKING SCHEME

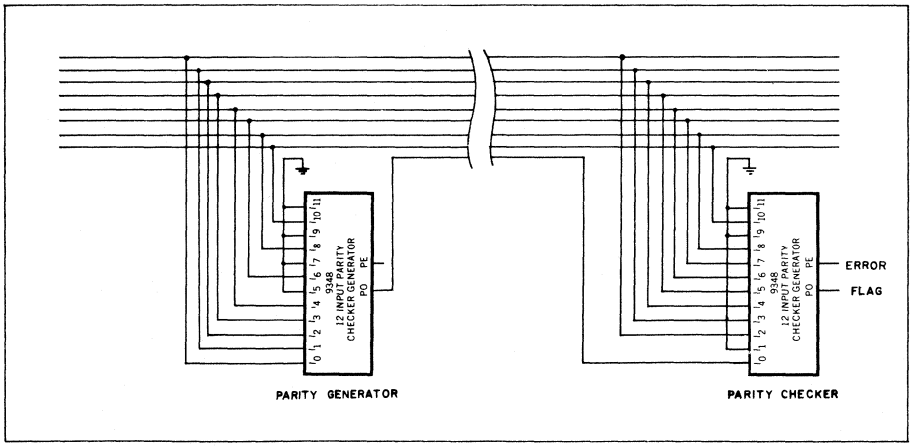


FIGURE 3a

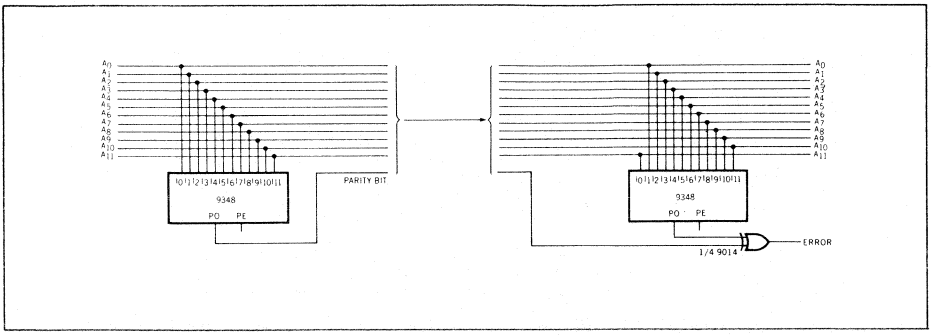


FIGURE 3b 12-BIT PARITY GENERATION AND CHECKING

Figure 4a illustrates how the 9348 can be expanded to generate odd or even parity for sixteen bits using one 9348 and check the sixteen bits plus parity bit with one 9348 and five exclusive OR gates. By applying the quad exclusive OR gates to the inputs I_0, I_1, I_2, and I_3 maximum speed is obtained. Figure 4b shows a 17-input checker that can be formed with two 9348's and without additional logic. The scheme utilizing the five exclusive OR gates has less delay than the two 9348's.

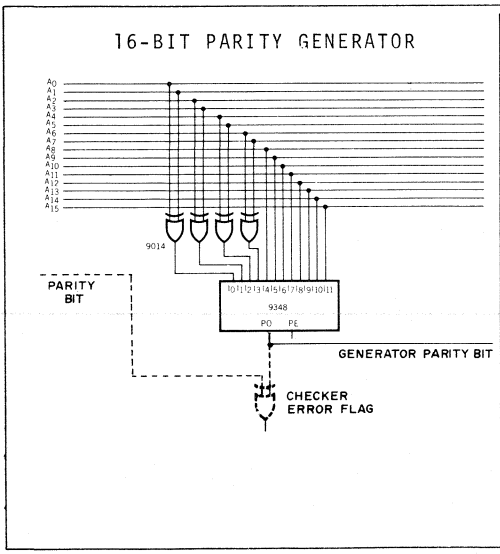


FIGURE 4a

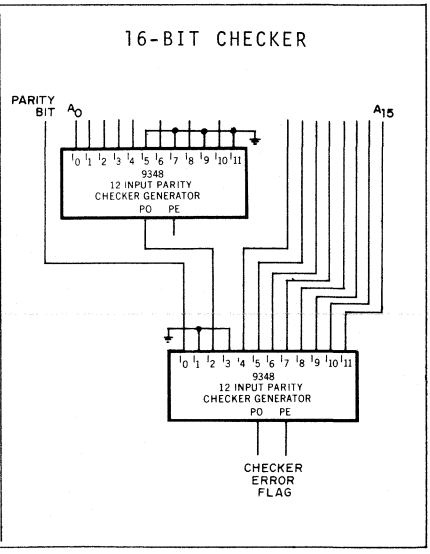


FIGURE 4b

A point is worth mentioning in regards to the overall delay of checker schemes. If a parity bit and data bits in a data register are to be checked, the number of exclusive NOR levels determines the checker delay. However, if the data bits are applied to the generator and simultaneously sent to the checker, the parity bit generated should be applied to the fastest parity input of the checker. Thus the delay of the signal in the checker and signal delay in the generator occur in parallel so that when the parity bit arrives the parity error output assumes its appropriate value sooner.

A 24-bit parity generator and checker is shown in Figure 5. The schemes have five exclusive OR delays and six delays respectively. The checker configuration can be modified slightly by putting the dashed exclusive OR on the I_0 input, for reasons just discussed.

24-BIT PARITY GENERATOR/CHECKER

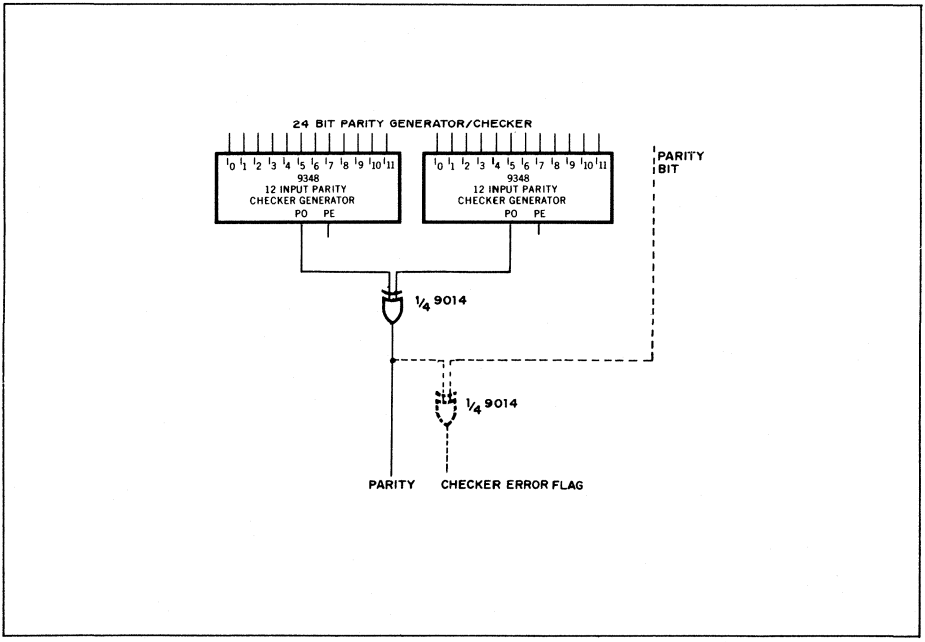


FIGURE 5

Figures 6a and 6b illustrate a 36-bit parity generator and a 48-bit generator.

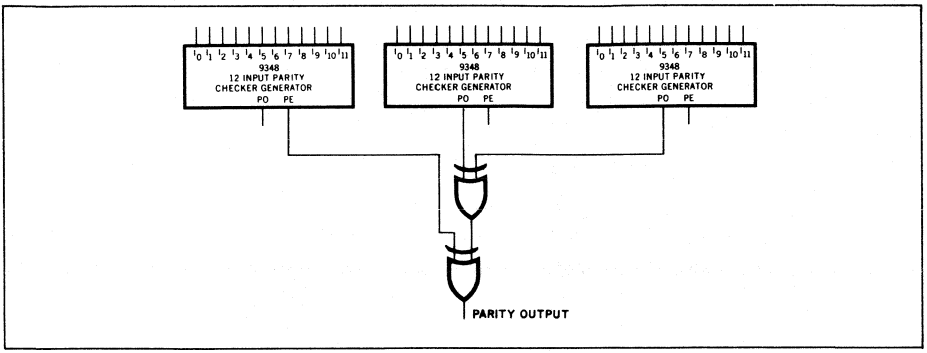


FIGURE 6a 36-BIT PARITY GENERATION

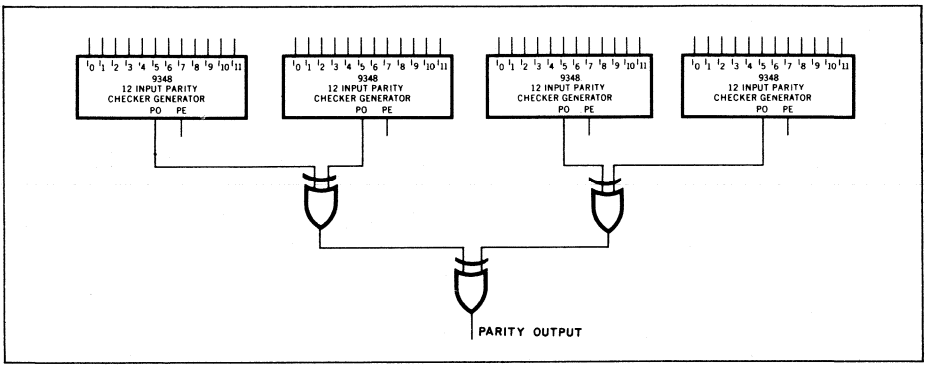


FIGURE 6b 48-BIT PARITY GENERATION

HAMMING CODE GENERATION AND CHECKING

Single error detection Hamming code schemes detect single data errors and also determine the bit in error. The Hamming parity bits are generated from the appropriate data bits and assigned specific bit locations in the transmitted word (data plus parity) so that when an error occurs the parity outputs change such that they designate the location of the error.

Figure 7 illustrates a 20-bit Hamming code generator and checker. Five 9348 parity checkers/generators examine the data bits and generate appropriate Hamming parity bits. These generated parity bits are sent with the original data bits to the destination where parity bits are again regenerated from the data bits. Then the transmitted parity bits are compared bit by bit with the parity bits regenerated at the

receiver and if a bit change has occurred its location is indicated on the output. This output can be decoded and used to recomplement the data bit in error, by the use of exclusive OR gates.

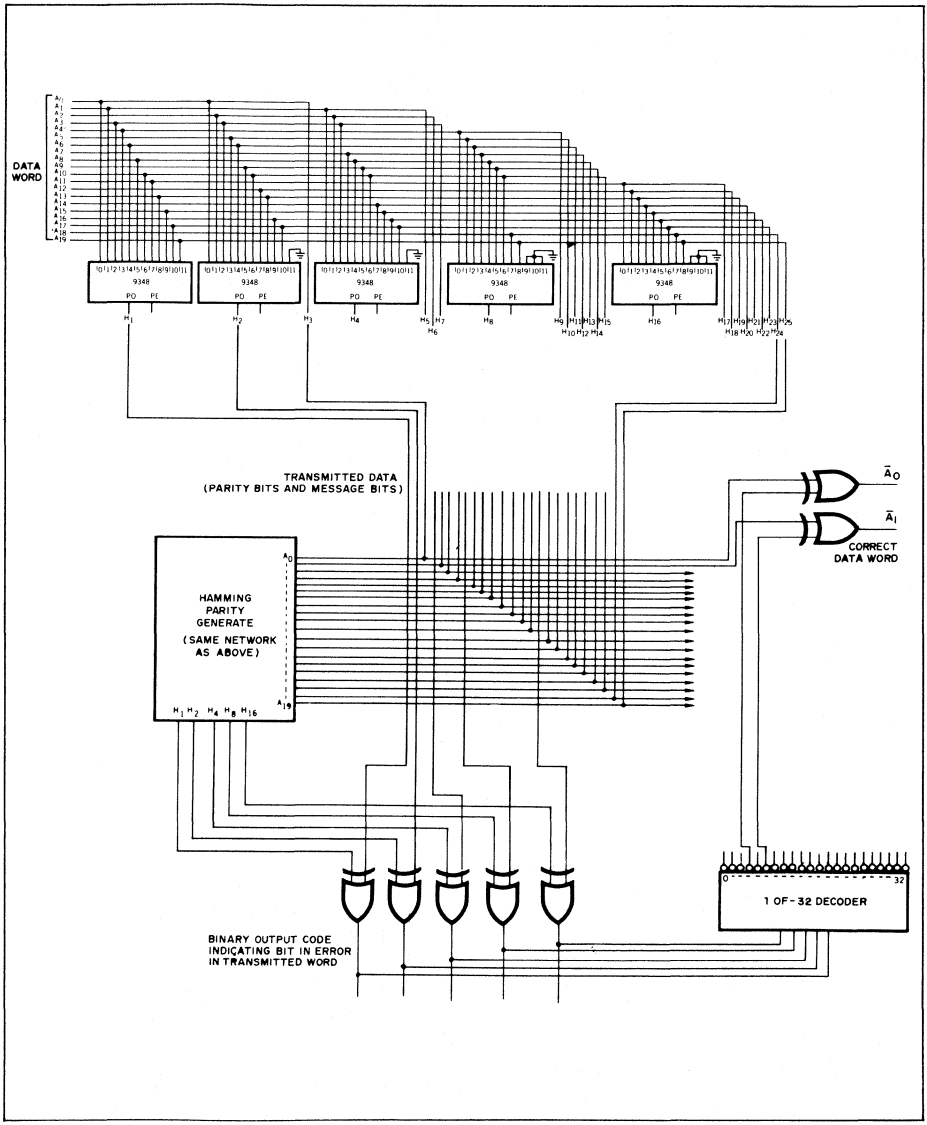


FIGURE 7 SINGLE ERROR CORRECTION HAMMING CODE GENERATION AND CHECKING FOR 20 BITS

THE 9309 AND 9312 MULTIPLEXERS

INTRODUCTION

The Fairchild MSI 9309 dual four-input multiplexer and the 9312 eight-input multiplexer are CCSL-compatible multi-functional integrated circuits. Although they are designed primarily for high-speed digital time multiplexing applications such as pulse telemetry, PCM, and computer data transfer, the 9309 and 9312 can also be used as high-speed logic function generators in random logic arrangements.

Both devices feature the following:

- Advanced TTμL technology
- High speed (25ns through delay)
- Reasonable power consumption
- Excellent noise margins
- Input clamp diodes to ground, which minimize the effects of line reflections
- Easy interfacing with Fairchild DTμL, LPDTμL, TTμL, and MSI families (CCSL).

LOGIC

The 9309 dual four-input multiplexer (Figure 1) is essentially a two-pole, four-position electronic switch whose positions are determined by logic levels at select inputs S_0 and S_1. It features (1) a common input select that permits the selection of either two bits of data or two bits of control from four sources, and (2) assertion and negation outputs that provide increased logic flexibility.

The 9312 eight-input multiplexer (Figure 2) resembles the 9309 electrically and is the electronic equivalent of a single-pole eight-position switch. Logic levels at the select inputs S_0, S_1, and S_2 determine the switch position. An active low enable input expands the multi-functional capabilities of this device. As in the 9309, greater logic flexibility is achieved by means of assertion and negation outputs.

Figures 3a and 3b show some active high/active low dual representations of the 9309 and 9312 functional block. These alternate representations often help clarify logic circuit operation.

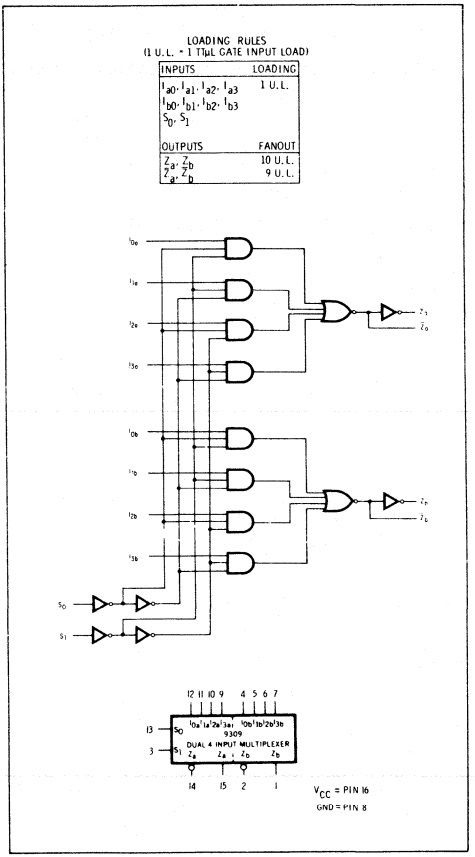


Fig. 1. 9309 Dual four-input multiplexer.

FAIRCHILD
SEMICONDUCTOR

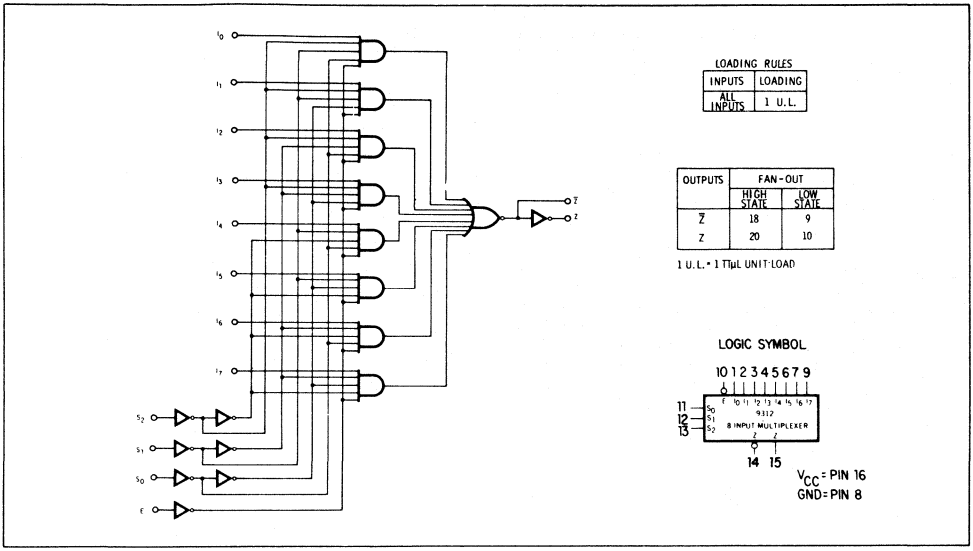


Fig. 2. 9312 Eight-input multiplexer.

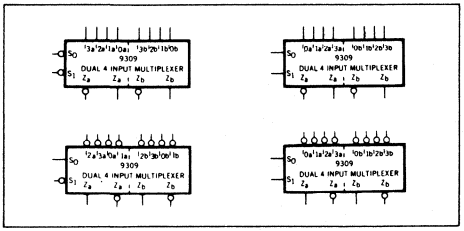


Fig. 3a. Equivalents of 9309 multiplexer.

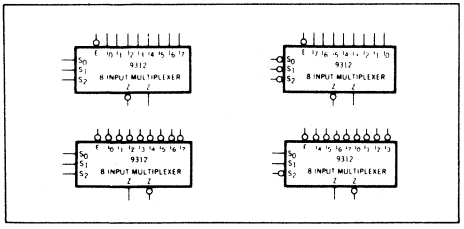


Fig. 3b. Equivalents of the 9312 multiplexer.

APPLICATIONS

Digital multiplexer applications usually fall into one of three categories: (1) data routing, (2) digital function generation, and (3) control switching. Other capabilities include adding, subtracting, sequencing, and comparing. The 9309 and the 9312 are so versatile that it is often possible to build virtually an entire logic system using just these two devices.

DATA ROUTING

Time Multiplexing

When used alone, the 9309 and the 9312 permit time multiplexing of a maximum of four and eight-data lines, respectively. By cascading these devices in two or more levels, one can increase the number of inputs. For example, in the circuit of Figure 4 two levels of multiplexers are cascaded to implement a 32-input multiplexer which has a through delay of about 50ns and which can be expanded to a 64-input multiplexer (Figure 5) with no additional delay. In the 32-input multiplexer, the 9312 enable can be used to gate the selected data out.

Data Busing of Multiple Words

Five 9309 dual four-bit multiplexers interconnected as in Figure 6 can be used to switch two bits of data from one of 16 words onto a two-bit data bus. The address supplied to the S_0, S_1, S_2, S_3 inputs selects the word to be transferred. If 12-bit words are to be transferred to a 12-bit bus, the circuit of Figure 6 would be repeated six times. Note that since the negative outputs are used at both levels, the assertion output (negation of the negation) is at a higher speed because the through delay is one gate delay less on the negation output. If the word-selecting address is held in four 9020 flip-flops (two dual packages), enough drive capability is available to select among 16 words of 16 bits each.

Decade Source Selection

The decade source selection multiplexer shown in Figure 7 switches 1-of-10 sources to an output bus which is controlled

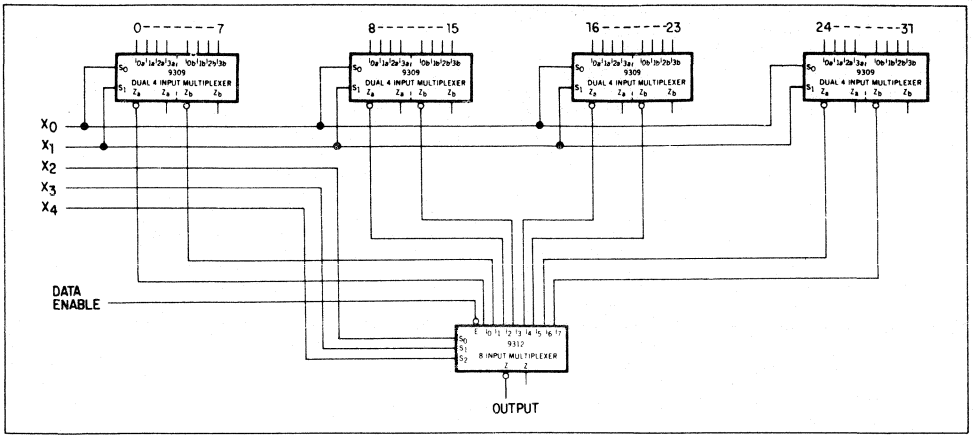


Fig. 4. Multiplexing 32 bits onto a single bus.

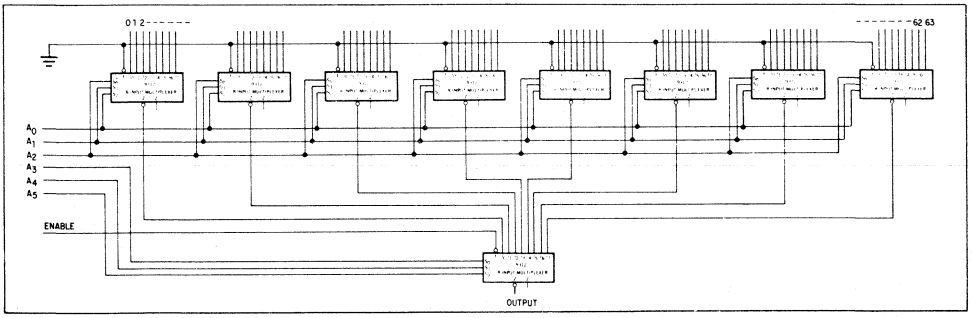


Fig. 5. 64-Input digital multiplexing scheme.

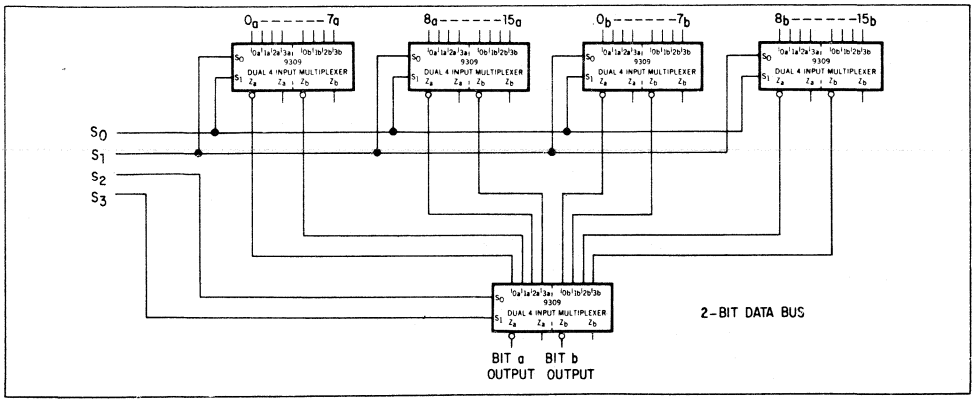


Fig. 6. Data busing of multiple words.

by a 8421 BCD code address input. One and one-half 9309's perform the decade selection. Even-numbered inputs are handled by the left half of the first-level multiplexer and odd-numbered inputs by the right half. The second-level multiplexer alternately selects between inputs I_0 and I_1 for the first eight BCD addresses and inputs I_2 and I_3 for addresses 9 and 10.

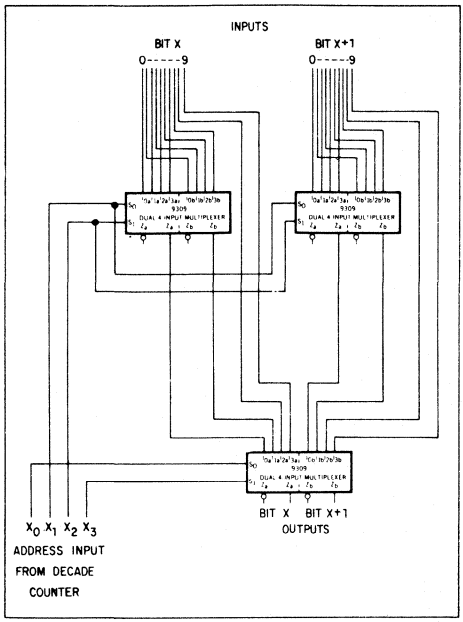


Fig. 7. Decade source selection multiplexer used to switch 1-of-10 sources to an output bus under control of an 8421 BCD code address input.

Decade Multiplexer

A decade multiplexer may be constructed as shown in Figure 8 using a 9312 and four additional gates. The terminal count (TC) output, Q_0 and Q_3, selects inputs 8 and 9, and the three-input OR gate serializes the data.

Constant-Time Shift Array

Figure 9 shows two bits, x and x + 1, of a constant-time shift array . Information on the bus is shifted in binary increments at each multiplexing stage: 2^3 (8) at stage a, 2^2 (4) at stage b, etc. A_0 is the least significant address bit, and the time taken for the shift is 60ns. Shift control is active high shift up. This scheme can be extended.

Register-to-Register Transfer

Two 9309 dual four-input digital multiplexers may be used to transfer data from one four-bit latch to any of three other four-bit latches (Figure 10). For example, the information held in the D_0 latch of any of the four-bit latches is transferred to all four D_0 latches in parallel under control of the register-to-bus select. The enable register selects which D_0 latch or latches will receive the data.

Register-to-Bus Transfer

One common use for a digital multiplexer is the register-to-bus transfer shown in Figure 11. In this circuit, one 9309 gates eight serial registers onto two bus lines, with the transfer being limited to four registers per bus. Similar schemes using the 9312 eight-input multiplexer permit the placing of additional registers onto a single bus.

Multi-Port Memory

The four-bit by eight-word multi-port memory module shown in Figure 12 uses four 9312 eight-input multiplexers for each word. This module can simultaneously read from two independently specified locations and write into a third independently selected location. Enables are provided in order that several modules may be connected to produce a larger memory. For example, a 16-bit by 64-word memory would require 32 of the modules shown in Figure 12.

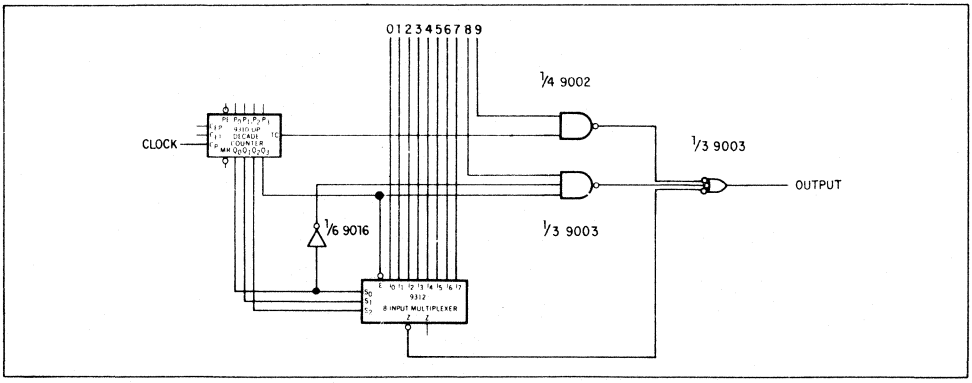


Fig. 8. Decade multiplexer.

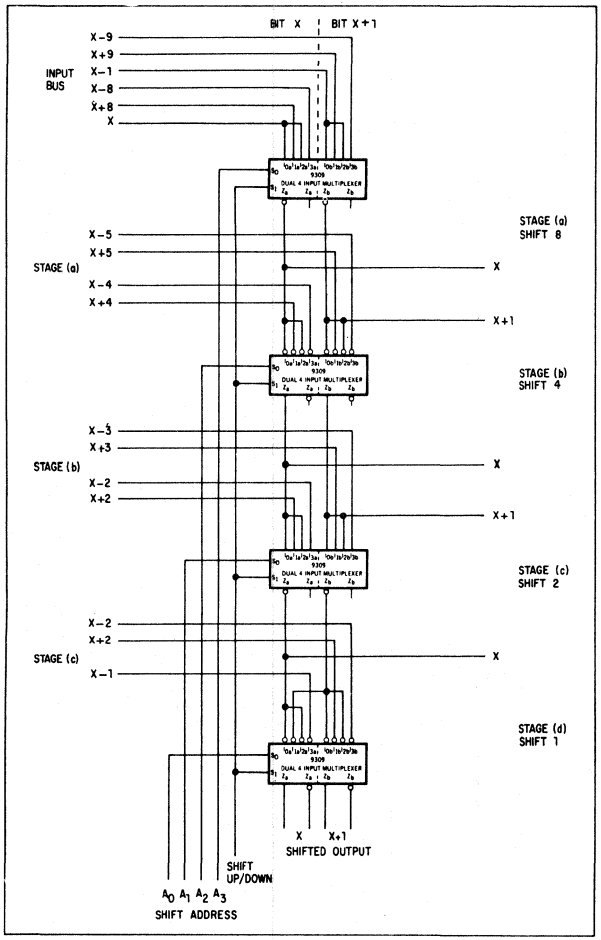


Fig. 9. Constant-time shift array.

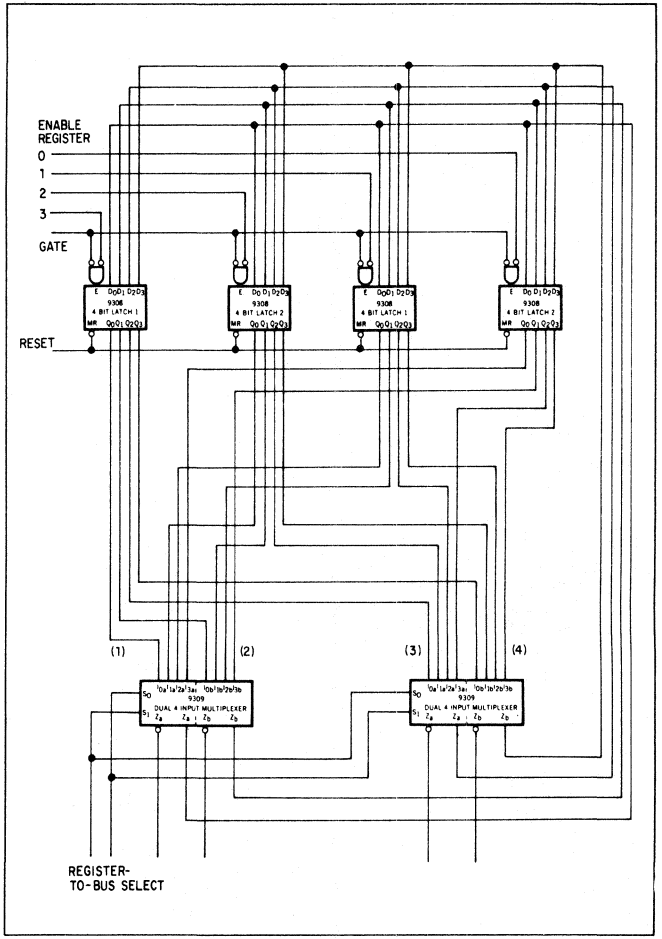


Fig. 10. Register-to-register transfer.

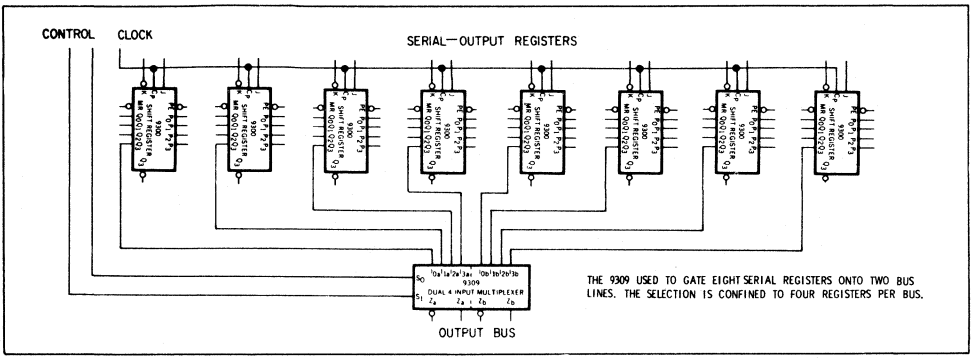


Fig. 11. Register-to-bus transfer.

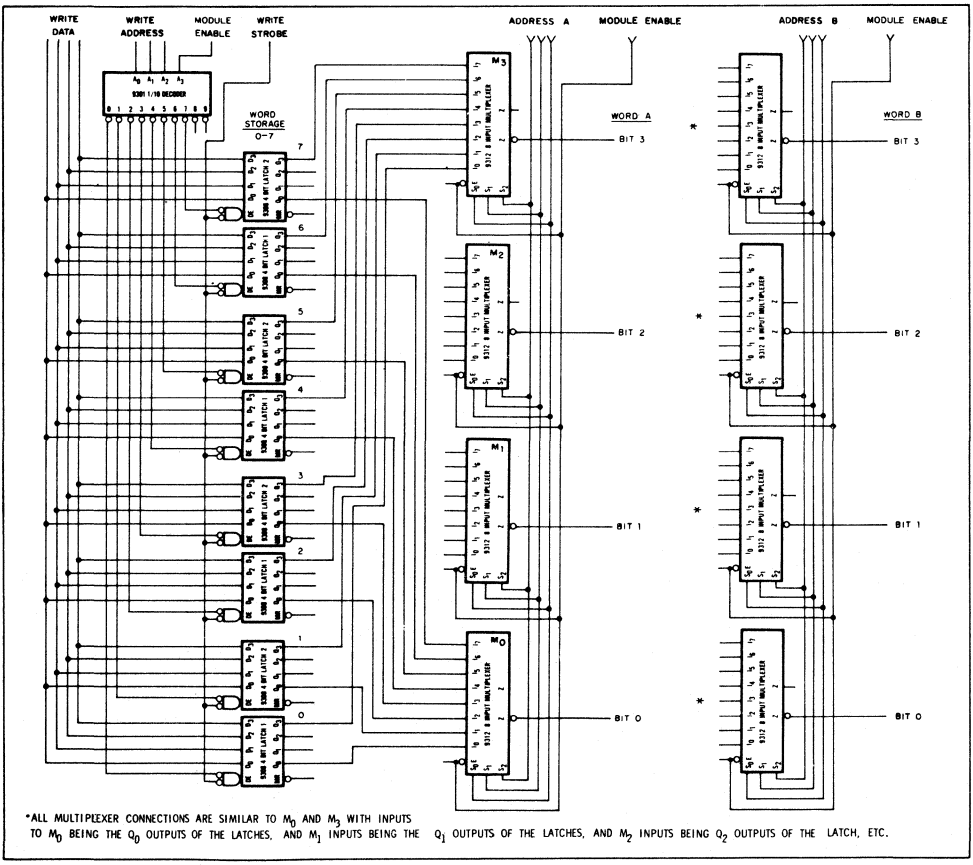


Fig. 12. A multi-port memory module.

By connecting this type of memory to a function generator unit, one could construct a processor that would execute three address instructions at a very high speed on the data contained in this type of memory. In order to utilize the speed of the memory, the instructions would also have to be contained in a fast semiconductor memory.

DIGITAL FUNCTION GENERATION

The Three-Variable Function Generator

The dual four-input multiplexer described here can produce any two functions of three variables without additional elements if there are both assertion and negation outputs of any one of the variables. To produce any two functions of three variables, the device supplies two of the variables to the input select lines and the third variable Z with values Z, $\overline{Z}$, "0", or "1" to the four input terminals I_0 - I_3. The procedure for implementing any function of three variables using this multiplexer is enumerated below:

(1) Draw truth table.
(2) Construct Karnaugh Map.
(3) Map area allotted to each input I_0 - I_3.
(4) Compare two maps to determine input signal required (Z, $\overline{Z}$, 0, or 1).

To illustrate the application of the above procedure, we will generate the Boolean function $X\overline{Y}Z + XY\overline{Z} + \overline{X}YZ + \overline{X}\overline{Y}\overline{Z}$. Figures 13a and 13b show the truth table (step (1)) and Karnaugh Map (step (2)) for this function. The map area allotted to the two input variables X, Y (supplied to select inputs) is given in Figure 13c.

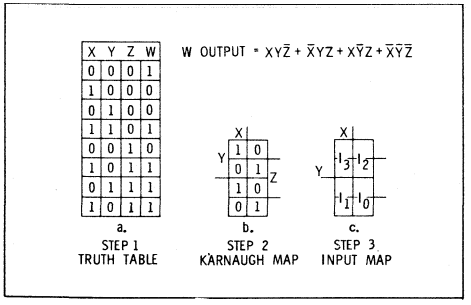


Fig. 13.

In the comparison between the two maps, the I_0 area can have the following combinations of 1's and 0's: 00, 10, 01, and 11. The placement of these combinations in each input area relative to the variable Z determines which of the four values of Z (Z, $\overline{Z}$, 0, or 1) is applied to that input. If there is a 11 combination in the input area, then a Z value of 1 (V_{CC}) must be supplied to that input; an input area with a 00 combination requires a Z value of "0" (GND); and input areas with 01 or 10 require a Z value of Z if the "1" of the 01 or 10 lies within the four sqaures assigned to Z, and $\overline{Z}$ if the "1" lies outside these four squares.

In this example, only the values Z and $\overline{Z}$ need be supplied to inputs I_0 - I_3 to implement the function. One half of the dual four-input multiplexer can be seen in Figure 14a with the values necessary to generate the desired function assigned to the inputs. To illustrate the benefits derived from this device, let us

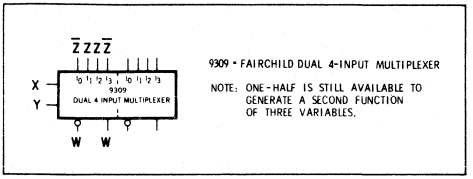


Fig. 14a. One-half of the dual four-input multiplexer.

compare the implementation of a three-variable function first using standard NAND gates and then using the digital multiplexer. The function in question, $(XY\overline{Z} + \overline{X}YZ + X\overline{Y}Z + \overline{X}\overline{Y}\overline{Z})$, has the minimum discrete gate implementation* shown in Figure 14b if the following constraints are observed:

(1) Maximum of three inputs per gate.
(2) Any gate may drive three other gates.

Inspection shows that five two-input gates and two three-input gates are needed to implement this function in NAND logic; i.e., two packages. The same function can be generated by one half of this dual four-input multiplexer, which in addition offers faster speed, lower power, fewer connections, and assertion and negation outputs.

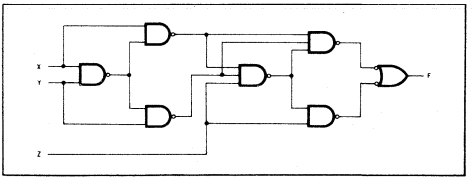


Fig. 14b. Minimum discrete gate implementation of $F = XY\overline{Z} + \overline{X}YZ + X\overline{Y}Z + \overline{X}\overline{Y}\overline{Z}$.

The Four-Variable Function Generator

The preceding description of the dual four-input multiplexer used as a digital function generator of three variables applies in general to the eight-input multiplexer used as a digital function generator of four variables. Figure 15 shows how the eight-input multiplexer can generate a function required in a digital frequency discriminator and illustrates the equivalent NAND gate implementation of the same function. The NAND gate implementation requires 2-1/2 packages and three levels of gating; the multiplexer requires only one package.

The logical power of these two MSI circuits becomes evident when one realizes that any of the 256 functions of three variables or any of the 65,536 functions of four variables may be generated using one half of the dual four-input or one eight-input multiplexer, respectively.

*Minimum discrete gate implementation can mean either minimum number of gates or minimum number of inputs.

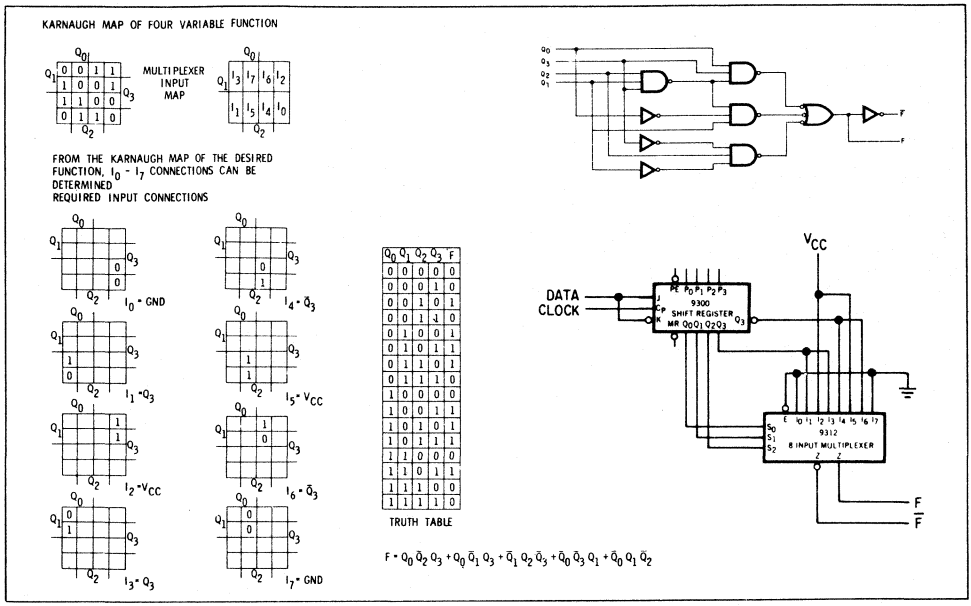

KARNAUGH MAP OF FOUR VARIABLE FUNCTION
MULTIPLEXER INPUT MAP
FROM THE KARNAUGH MAP OF THE DESIRED FUNCTION, I_0 - I_7 CONNECTIONS CAN BE DETERMINED
REQUIRED INPUT CONNECTIONS
I_0 - GND
I_1 - Q_3
I_2 - V_{CC}
I_3 - Q_3
I_4 - $\bar{Q}_3$
I_5 - V_{CC}
I_6 - $\bar{Q}_3$
I_7 - GND
TRUTH TABLE
$F = Q_0\bar{Q}_2Q_3 + Q_0\bar{Q}_1Q_3 + \bar{Q}_1Q_2\bar{Q}_3 + \bar{Q}_0\bar{Q}_3Q_1 + \bar{Q}_0Q_1\bar{Q}_2$
DATA
CLOCK
9300 SHIFT REGISTER
9312 8 INPUT MULTIPLEXER
V_{CC}
F
$\bar{F}$

Fig. 15.

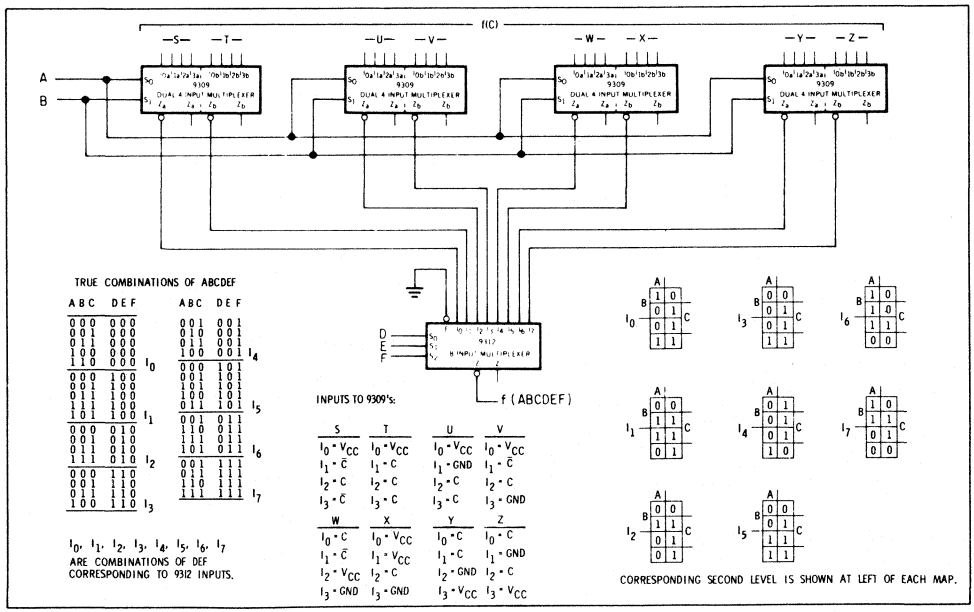

f(C)
DUAL 4 INPUT MULTIPLEXER 9309
8 INPUT MULTIPLEXER 9312
TRUE COMBINATIONS OF ABCDEF
I_0, I_1, I_2, I_3, I_4, I_5, I_6, I_7 ARE COMBINATIONS OF DEF CORRESPONDING TO 9312 INPUTS.
INPUTS TO 9309's:
f (ABCDEF)
CORRESPONDING SECOND LEVEL IS SHOWN AT LEFT OF EACH MAP.

Fig. 16.

Generation of Function of Five or More Variables

Logic circuits of five or more variables need multiple levels of multiplexing. A six-variable universal logic circuit, for instance, requires eight four-input multiplexers in the first level and one eight-input multiplexer in the second level. In practice, most function generators are called upon to generate a particular function rather than *any* function of "N" variables. When it is necessary to generate a particular function of six variables, f(ABCDEF), the procedure outlined below will provide the necessary inputs and level interconnections.

(1) Factor out each combination of D, E, and F; then obtain the function of ABC, f(ABC), that is associated with each combination factored.

(2) Collect all terms of f(ABC) corresponding to each selected input combination of D, E, and F.

(3) Implement each function of ABC thus collected as a function of three variables using the method described above for implementing any function of three variables with the dual four-input multiplexer.

(4) Connect the first-level output to corresponding eight-input multiplexer data input.

An illustration of the foregoing method of generating a function using a six-variable function f(ABCDEF), appears in Figure 16. The implementation of this function with standard NAND gates is left to the reader.

The transformed f(ABCDEF) is often more efficiently implemented by a judicious selection of variables for the first and second-level functions. In the approach shown in Figure 16, f(ABCDEF) has been transformed to f(ABC) for each combination of DEF. In Figure 17, the same function of f(ABCDEF) has been implemented by means of the transformation to f(CDB) and combinations of E, F, and A. The method of Figure 17 makes use of the fact that (1) f(CDB) is identical for second-level term I_0 and I_1, and that (2) second-level term I_7 is the negation of I_6. Figure 17 illustrates how these two conditions are used to reduce the package count. Three things to look for when selecting variables for first-level functions are:

(1) A function which reduces to fewer variables.

(2) Functions which are identical.

(3) A function which is an inversion of another.

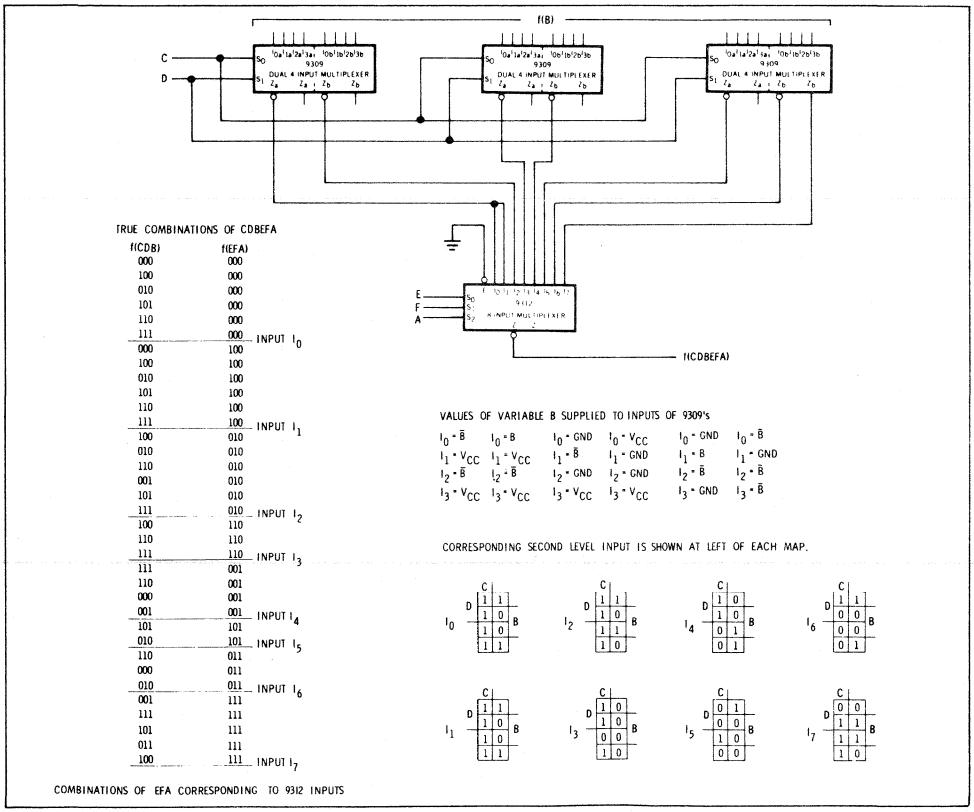


Fig. 17.

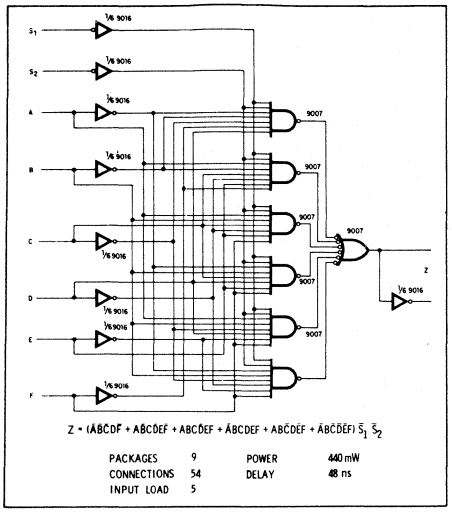


Fig. 18a. Logic function implemented with standard discrete NAND gates.

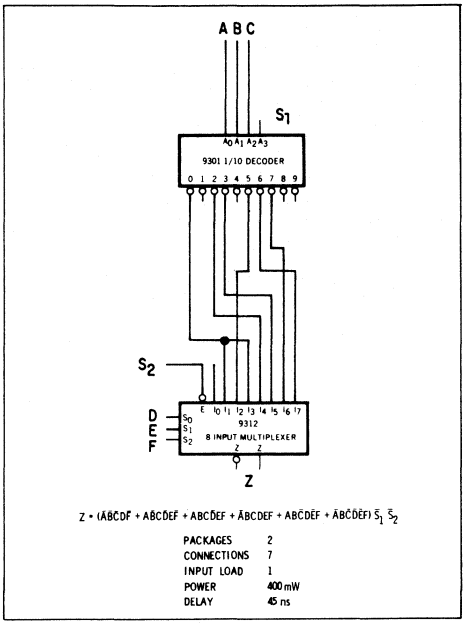


Fig. 18b. Logic function of Figure 18a implemented with MSI.

Multiplexer and Decoder Function Generators

The 9301 one-of-ten decoder and the 9312 eight-input multiplexer may be used together to generate a large number of digital functions efficiently. A six-variable function is transformed into two three-variable functions as described above, with f(ABC) supplied to the decoder and f(DEF) to the multiplexer.

Figures 18a and 18b show a logic function implemented with discrete standard NAND gates and MSI, respectively. The

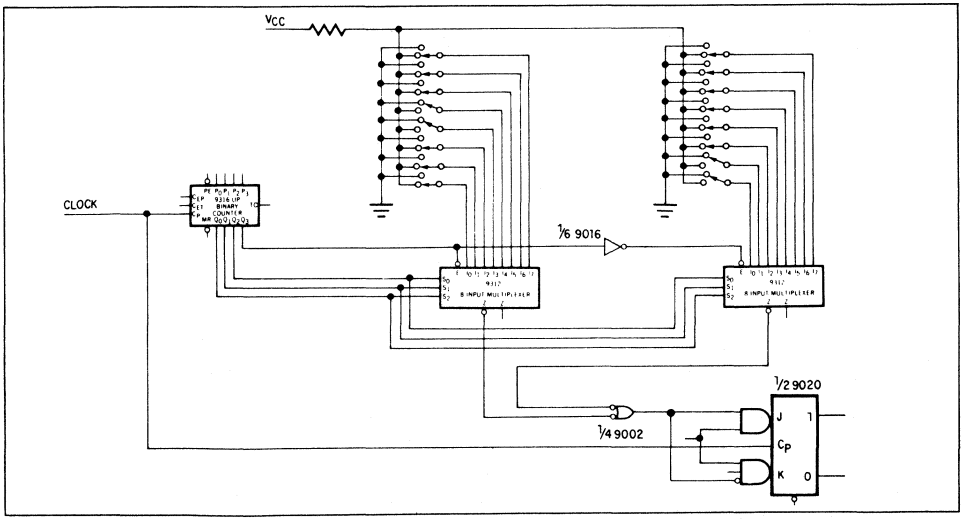


Fig. 19. 16-bit pattern generator circuit.

package count interconnection, input load, power, and speed advantages of the MSI are apparent. If a function is implemented with the 9301 and 9312 by this method, then: (1) the f(ABC) supplied to the decoder inputs should have no more than eight unique terms, and (2) no terms of DEF can be identical. (If any terms of DEF are identical, it is often possible to efficiently implement the given function with one or two discrete gates in addition to the 9301 and 9312.)

SPECIAL APPLICATIONS

16-Bit Pattern Generator Circuit

The circuit of Figure 19 illustrates how multiplexers can be used in the design of one channel of a 16-bit pattern generator. Each channel requires two 9312's, 1/2 9020, 1/4 9002, and 1/6 9016, and consists of a switch serializer/pattern generator and re-synchronizer sections with a modulo 16 binary counter to all channels.

The select inputs for the 9312 multiplexer are the three least significant bits of the binary counter. The enable inputs of the 9312 and an inverter allow the selection of either multiplexer using the most significant bit of the counter. In this manner, the 16 bits are multiplexed to the re-synchronizer — a D flip-flop that eliminates decoding spikes.

Data Commutator

Figure 20 illustrates how the 9309 dual four-input multiplexer and a 9316 up binary counter may be used for data commutation. In each selected position, I_0 - I_3, the data commutator samples data for a length of time that is determined by the clock frequencies at the four I_b multiplexer inputs. The 9316 CEP input serves as a commutation enable, while the 9316 TC output indicates the end of the commutation cycle.

General-Purpose Accumulator

A general-purpose accumulator suitable for high-speed computer applications is shown in Figure 21. The 9309 dual four-input multiplexer acts as an operation code decoder and data selector, the 9304 dual full adders perform arithmetic operations, and the 9022 dual flip-flop functions as the accumulator storage element.

Two bits of the general purpose accumulator are shown with the operation code list. The operation code presented to the multiplexer select inputs S_0, S_1 chooses data from the following sources:

1. Adjacent stage to the right for a shift-left operation
2. Adjacent stage to left for a shift-right operation
3. Adder outputs for add operation
4. Q outputs of 9022 for the complement operation

Sequencer

An unusual multiplexer application in Figure 22 shows a 9312 eight-input multiplexer used as a counter control circuit in a 16-step control sequencer. The sequencer can operate synchronously or asynchronously. The 9316 parallel inputs and parallel enable permit initializing at any point in the sequence or cycling through any portion.

Keyboard-to-Binary Converter

The keyboard-to-binary converter shown in Figure 23 produces a four-bit binary coded output corresponding to each key of the 15-key keyboard. Two 9312 eight-input multiplexers, the two-input gate G_1, and the inverter form a 16-input multiplexer which transmits a signal (low) from a depressed key to both the 9310 and 9316. The 9316 counter continuously counts modulo 16 while stepping the multiplexer through each keyboard input searching for a signal from a depressed key. Note that the grounded CEP input allows the 9310 to be used as four gated D flip-flops.

If no depressed key is found, the grounded I_7 multiplexer input simulates a strike, loading count 16 (1111) in the four D flip-flops of the 9310. (The 9310 Q_0 - Q_3 outputs are then all high, indicating no depressed key.) While count 16 is being loaded, the low activation signal to the parallel enable input of the 9310 simultaneously loads 0000 into the 9316. This loading operation immediately switches the multiplexer to the I_0 input and removes the low supplied to the parallel enable inputs, thereby allowing the 9316 to continue counting. The binary equivalent of the "struck" key remains in the 9310.

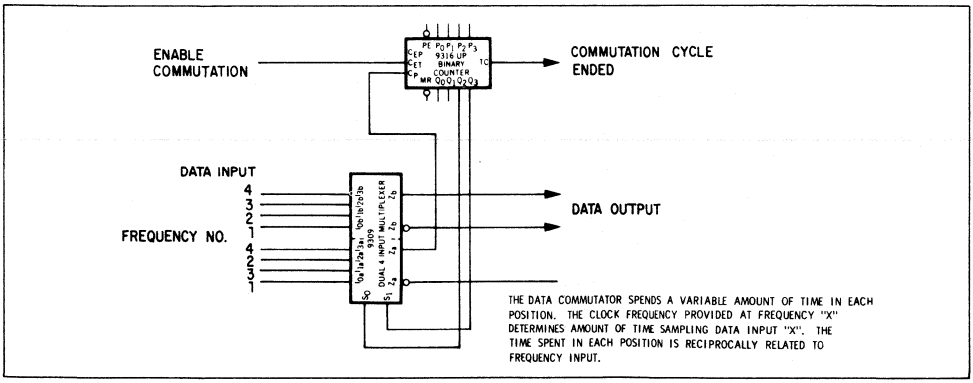


Fig. 20. Data commutator.

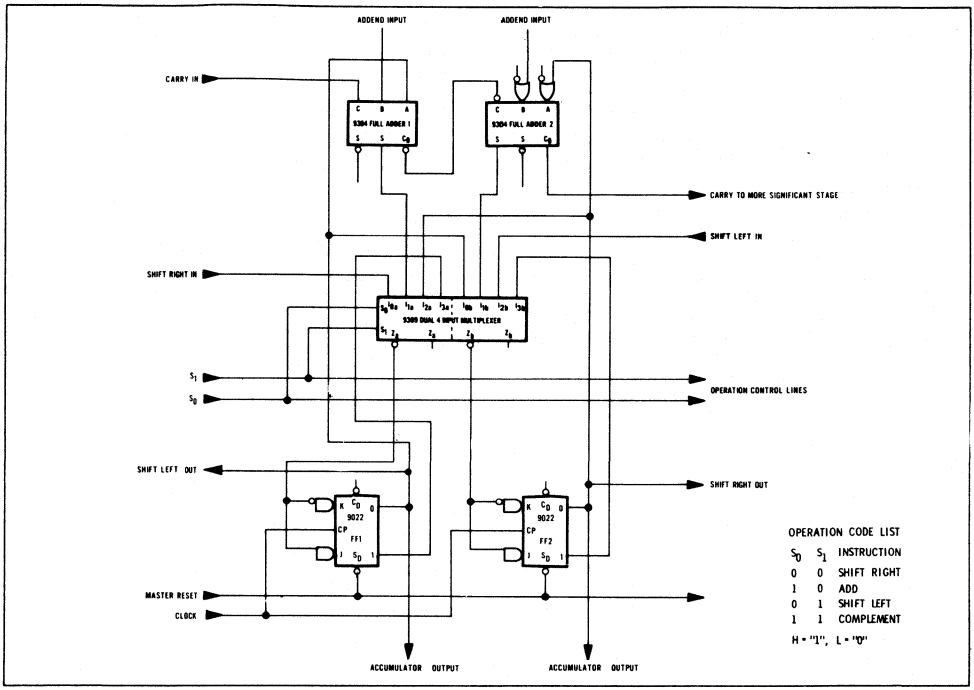


Fig. 21. General-purpose accumulator.

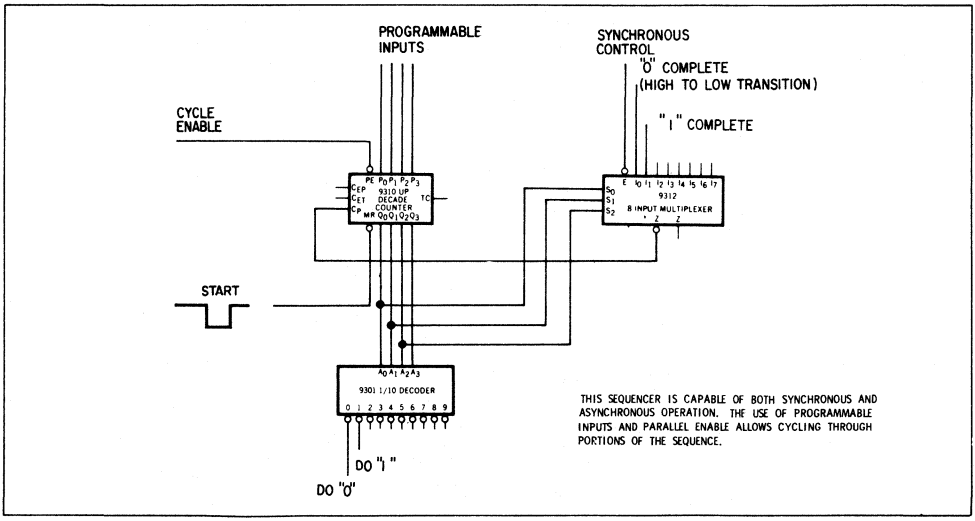


Fig. 22. Sequencer.

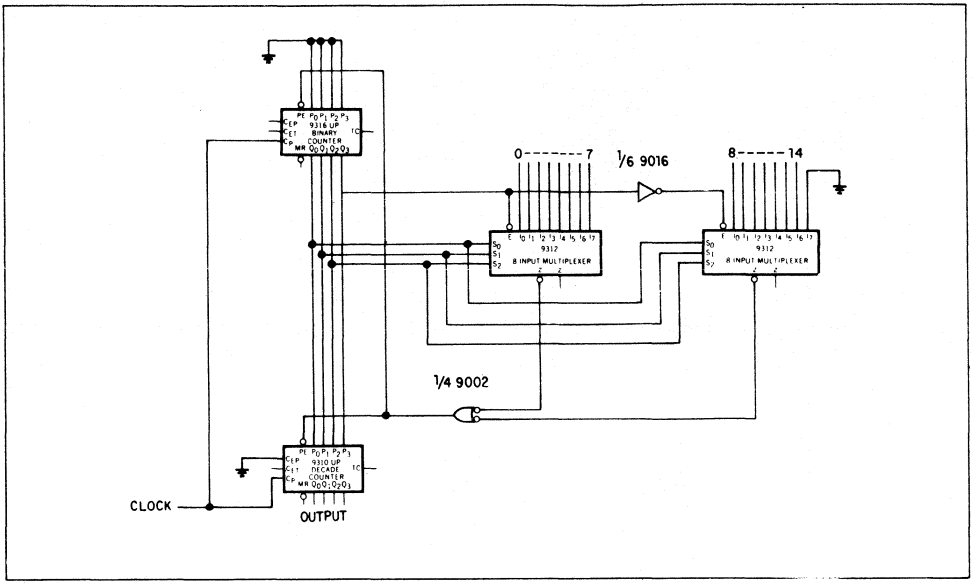


Fig. 23. Keyboard-to-binary converter.

If a depressed key is found (low signal), the multiplexer transmits this low to the 9310 which loads the binary number corresponding to that key into the 9310. Simultaneously, the 9316 is set to 0000 as before. This prevents erratic outputs from the 9310 caused by "rolling" of the keys.

This circuit may also operate as a 16-bit priority encoder. The circuit operation is identical to that of the keyboard-to-binary converter just discussed. The most significant of 16 bits is applied to the "0" input of the multiplexer with the next-to-least significant bit applied to input 14. The counter sequences the multiplexer, searching inputs 0-14 sequentially for a signal. The first bit detected will be stored in the 9310 and the search cycle restarted. Note that in this configuration, the negation of data must be supplied to the multiplexer data inputs.

MISCELLANEOUS APPLICATIONS

Thus far we have discussed three major applications of multiplexers: data routing, digital function generation, and control switching. There are many other ways in which multiplexers can be used, and in the remainder of the paper we will discuss a few of them.

Three-Bit Comparator (Figure 24a)

Three bits of data to be compared are supplied to the address and select inputs of the 9301 and 9312, respectively. If A_0, A_1, A_2 and B_0, B_1, B_2 compare, the mutually exclusive active low output of the 9301 1/10 decoder and the selected input of the 9312 multiplexer will be coincidental and COMPARE OUT will be high. The COMPARE ENABLE must be low to permit compare operation.

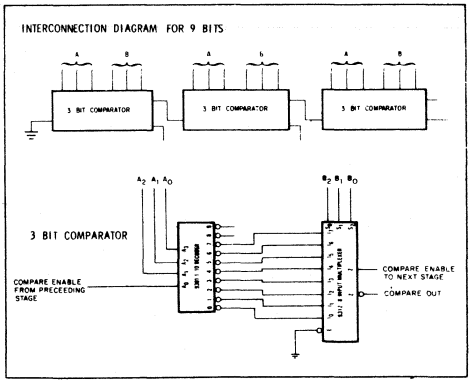


Fig. 24a. Three-bit comparator.

Ripple-Carry Addition and Subtraction (Figures 24b and 24c)

The 9309 dual four-input multiplexer, when operated as a ripple-carry parallel adder, acts as a three-variable function generator as explained in the section on logic function generator. The three-variable maps for the sum and carry are shown with the circuit in Figure 24b. Variables A and B, the bits to be added, are supplied to the S_0 and S_1 inputs, while variable C (carry) is supplied to inputs I_0 - I_4. One-half of each 9309 generates the sum, and the remaining half generates the carry. Figure 24c shows a ripple-carry parallel subtractor.

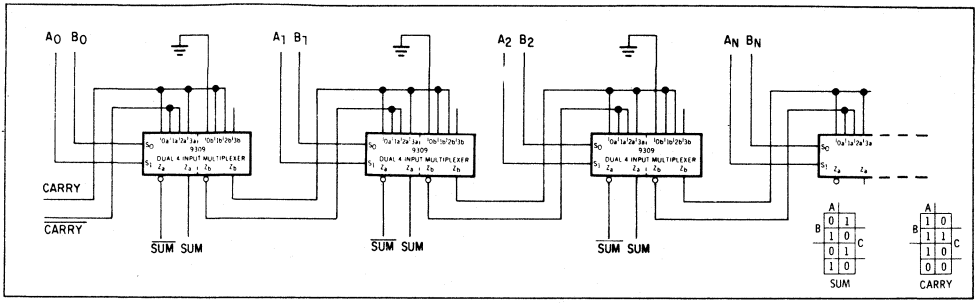


Fig. 24b. Ripple-carry parallel addition using the 9309 multiplexer.

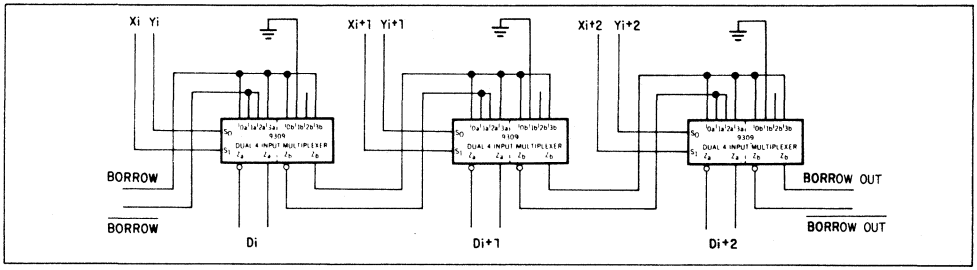


Fig. 24c. Ripple-carry parallel subtraction using 9309.

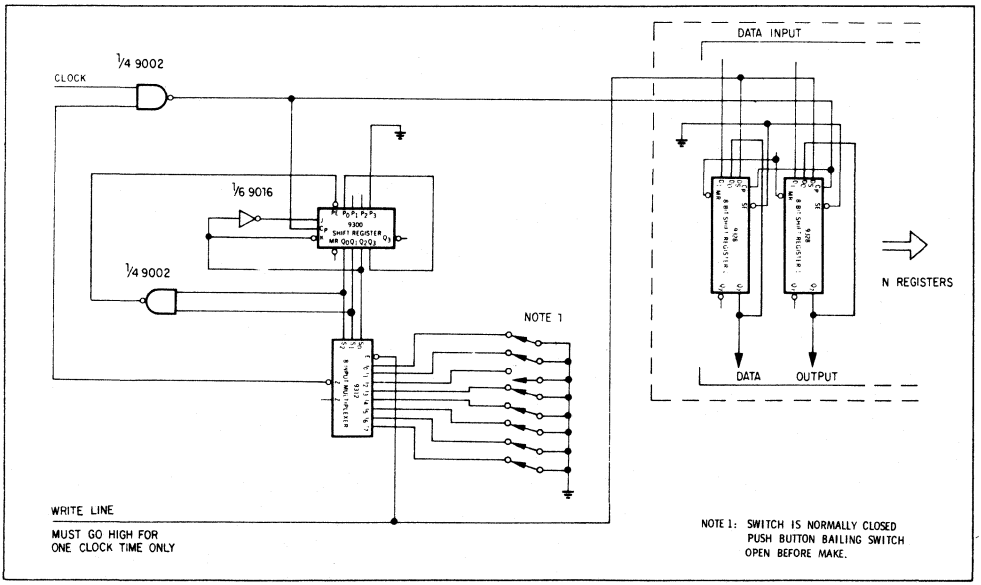


Fig. 25. N-bit-by-8 word memory using 9328 dual 8-bit shift registers.

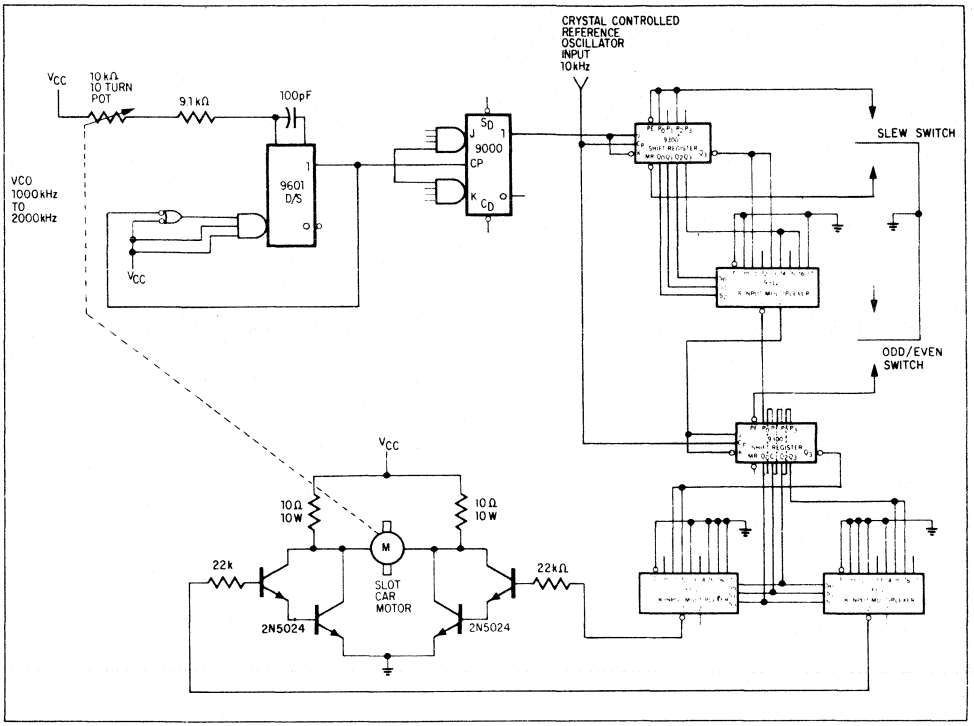


Fig. 26. Crystal-controlled detented tuner.

N-Bit-by-Eight-Word Memory (Figure 25)

By using 9328 dual eight-bit shift registers in conjunction with a 9300 universal four-bit shift register counter and a 9312 eight-input multiplexer, it is possible to construct an eight-word-by-N-bit memory that has parallel input and parallel output capabilities.

The operator uses a switch with eight push buttons to select the data word for the data output. The push button for this output, when depressed, allows enough clocks to the counter and shift registers to bring the selected word to the last position in the registers, thus providing that word as an output. In effect, the counter scans the eight-input multiplexer until it finds an open switch, and each clock that increments the counter also shifts the register.

To write into any location, one selects that location with a push button, furnishes the desired data to the parallel inputs, and raises the write line for one clock period. The high write line will both release the counter and shift registers, and at the same time select the parallel data-in (in place of the recirculation output) as an input to the shift register.

The extension of this memory to any even number of bits is limited only by the driver capability of the write input and clock.

Crystal-Controlled Detent Tuner (Figure 26)

The crystal-controlled detented tuner shown in Figure 26 can automatically and accurately tune to a specific frequency even though no signal is present at that frequency. There are three inputs to this circuit: a local oscillator output, a crystal reference frequency, and two tuning slew inputs. The outputs consist of two tuning drive signals and a dial calibrate signal. The tuning drive outputs may (1) drive a d-c tuning motor bi-directionally, or (2) charge and discharge a capacitor to generate a control voltage for voltage-controlled tuning.

With a d-c motor, channel selection is accomplished by slewing to the proper channel indication. Upon release of the slew switch, a two-stage digital frequency discriminator takes control of the tuning motor and positions the tuning control to the indicated channel. In this application, three 9312's serve as function generators replacing four packages of TTμL decoding gates.

THE MSI 9328 DUAL 8-BIT SHIFT REGISTER

INTRODUCTION

Fairchild's MSI 9328 dual 8-bit shift register is a CCSL device that features

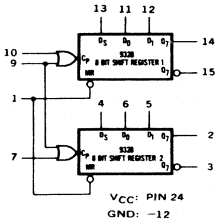
- TT_ technology
- Active pullup outputs
- High speed
- Excellent noise margins
- Grounded input diodes that minimize adverse effects due to line reflections
- Compatibility with the entire Fairchild CCSL family.

OPERATION

Figure 1 shows the symbol used to represent the 9328, the pin layout, and the loading constants. Figure 2 indicates the logic operation of the device.

Clock Circuitry

The dual shift register comprises two groups of eight clocked RS master-slave flip-flops and several gates. As can be seen in Figure 2, the two shift registers have both a common clock



NORMALIZED TTμL LOADING RULES:

INPUT LOADING	
MR, D_0, D_1	1 UNIT LOAD
SEPARATE CP (PINS 7 & 10)	1.5 UNIT LOAD
D_S	2 UNIT LOADS
COMMON CP (PIN 9)	3 UNIT LOADS
FAN OUT	
Q_7 & $\bar{Q}_7$	6 UNIT LOADS

Fig. 1. CCSL 9328 pin layout and loading constants.

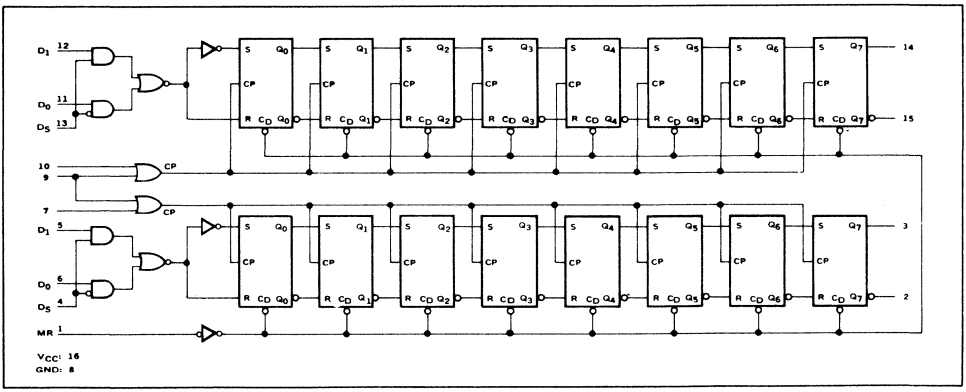


Fig. 2. 9328 Dual 8-bit shift register.

FAIRCHILD
SEMICONDUCTOR

input (pin 9) and a separate clock input (pins 7 and 10). These inputs control the clocking. The clock OR gate drives the eight clock inputs of the flip-flop in parallel. When the two clock inputs (the separate and the common) to the OR gate are low, the slave latches are quiescent, but data can enter the master latches via the R and S inputs.

If either of the clock inputs goes high while the other stays low, or if both go high simultaneously, then (1) the data inputs, R and S, are inhibited so that a subsequent change in input data will not affect the master, and (2) the information now trapped in the master is transferred to the slave. When the transfer is complete, both the master and the slave are steady as long as at least one clock input remains high.

During the high-to-low transition of the last remaining high clock input, (1) the transfer path from the master to the slave is inhibited, leaving the slave steady in the state it is in, and (2) the data inputs, R and S, are enabled so that new data can enter the master. Either of the clock inputs can act as clock enable inputs; a logic low signal will enable the other clock input.

The clocking scheme allows the three clock inputs to be used in the following ways:

- One clock common (pin 9) for 16 bits; two separate clocks (pins 10 and 7), each for eight bits.
- One clock common (pin 9) for 16 bits; two separate clock enable inputs (pins 10 and 7), one for each 8-bit shift register.
- Two separate clocks (pins 10 and 7) and one common clock enable input (pin 9).

Data Inputs

Each 8-bit shift register has a 2-input multiplexer in front of the serial data input. The two data inputs, D_0 and D_1, are controlled by the data select input D_S according to the Boolean expression:

$$\text{Serial Data In: } S_D = \bar{D}_S D_0 + D_S D_1$$

The data input circuitry gives a very flexible input scheme. If there are two input variables, A and B, there will be 16 logic functions that can be performed on A and B and 16 corresponding truth tables. Table 1 lists the minimum input logic required for implementation of any of these 16 possible functions.

TABLE I
MINIMUM INPUT PATTERN FOR OUTPUT OF ANY OF 16 POSSIBLE FUNCTIONS OF INPUTS A, B.

				A	L	H	L	H
				B	L	L	H	H
FUNCTION NAME	D_S	D_0	D_1		OUTPUT			
ALL ZEROS	X	L	L	0	L	L	L	L
NOT A AND NOT B	A	$\bar{B}$	L	1	H	L	L	L
A AND NOT B	B	A	L	2	L	H	L	L
INVERT B	B	H	L	3	H	H	L	L
NOT A AND B	A	B	L	4	L	L	H	L
INVERT A	A	H	L	5	H	L	H	L
A NOT EQUIVALENT B	A	B	$\bar{B}$	6	L	H	H	L
NOT A OR NOT B	A	H	$\bar{B}$	7	H	H	H	L
A AND B	A	L	B	8	L	L	L	H
A EQUIVALENT B	A	$\bar{B}$	B	9	H	L	L	H
DATA A	A	L	H	10	L	H	L	H
A OR NOT B	B	H	A	11	H	H	L	H
DATA B	B	L	H	12	L	L	H	H
NOT A OR B	A	H	B	13	H	L	H	H
A OR B	A	B	H	14	L	H	H	H
ALL ONES	X	H	H	15	H	H	H	H

X = DON'T CARE CONDITION

Outputs

For each 8-bit shift register, both the assertion and the negation from the last stage Q_7 are available for use.

Master Reset

The circuit has an asynchronous master reset (MR) with a low logic level that can clear all 16 stages independently of any other signal.

DEVICE CAPABILITIES

The 9328 provides economical high-speed serial storage. It can insert data from any of two data sources via the two-input multiplexers at the input of each 8-bit shift register. Figure 3 illustrates how this capability is frequently used. With the setup shown, information is kept circulating through the feedback connection, and new data are inserted at the required time by means of the data select control.

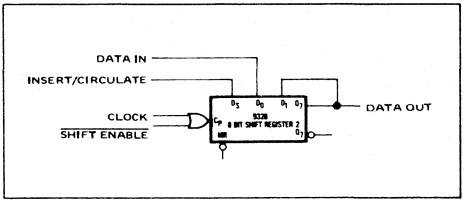


Fig. 3. 9328 Recirculating capability.

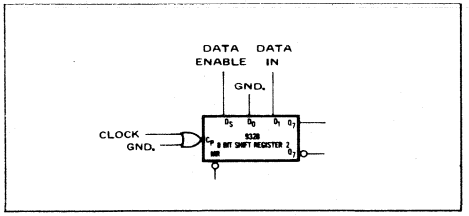


Fig. 4. 9328 Data enable capability.

In Figure 4, the 2-input multiplexer acts as a Boolean function generator of two variables. Note that the input configuration is wired to give an active high data enable control at the input of the register. This technique of using D_S, D_0, and D_1 to provide enable capability can be extended by using a 9301 active low output decoder to control data flow in a bank of eight shift registers (Figure 5). In this circuit, data enters the selected register under control of the address configuration on the 9301, and the input multiplexers are wired to give an active low data enable to conform with the output polarity of the decoder.

One of the clock inputs on the shift register can serve as an active low shift select control (Figure 6). As seen in the diagram, the 9301 determines which shift register from a bank of shift registers can accept data inputs. The input clock loading of the 9328 permits a single 9301 decoder to control 10 shift registers of up to 48 bits in length.

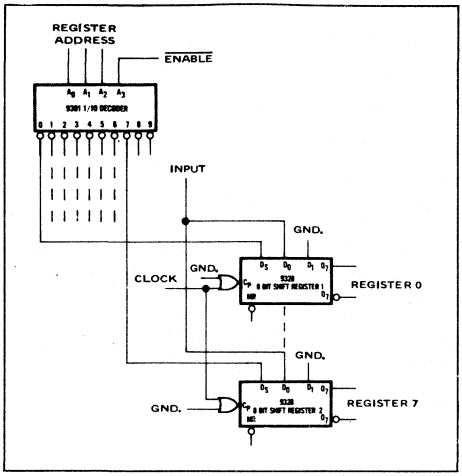


Fig. 5. 9301 Used to select data input.

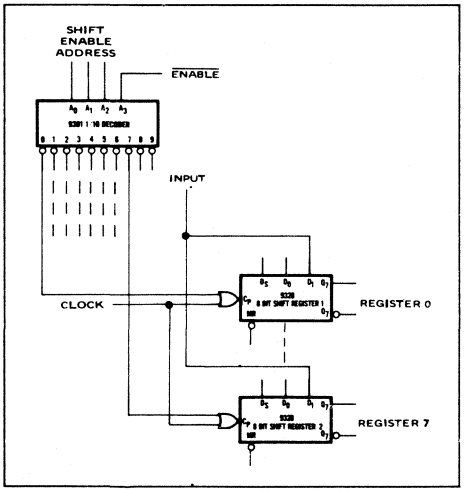


Fig. 6. 9301 Used to select shift register.

APPLICATIONS

Variable-Length Shift Registers

The 9328 can be used in conjunction with other MSI devices to implement a variable-length shift register. An example of such a circuit, consisting of three 9328's, three 9309 dual 4-input multiplexers, and two 9300 shift registers, is shown in Figure 7. This shift register can be programmed to shift data from 0 to 31 places by appropriate logic configuration on the shift address inputs. The operation is as follows:

- All incoming data enter the first half of one of the 9309 multiplexers. Data entry is governed by a circulate-enter control.
- The output of this half of the 9309 then enters the other half in one of two ways: directly, if the required length register is even; or via a single shift delay if the required length register is odd.
- At this point, the output of the second half of the 9309 multiplexer is fed to another 9309. This takes place via a 2-bit shift register if a shift of two places is required, or directly if a shift of two places is not required.
- The procedure continues with each half of a multiplexer switching the data either directly from a previous stage or via a binary-weighted shift to its output.
- The final output is fed back to the first multiplexer in order to provide circulation capability.

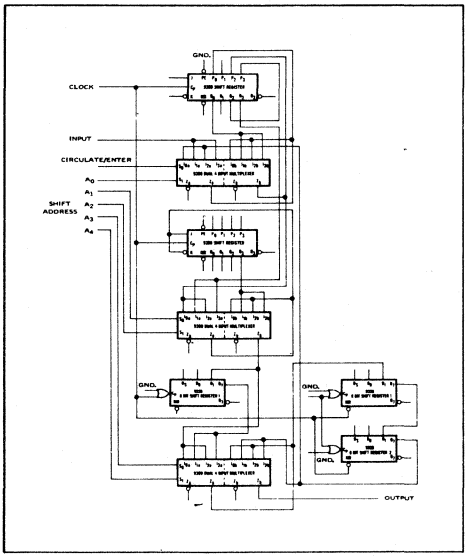


Fig. 7. Variable-length shift register.

A variable-length shift register with a slightly different wiring configuration is illustrated in Figure 8. In this circuit, the first 9300 permits two lots of data to enter: (1) the input information to the variable-length shift register, and (2) the variable-length shift register's final output (which recirculates through the circuit). To provide for these two inputs, the device is connected as a shift register in the parallel mode, and the parallel enable line is used as a circulate-enter control. The second 9300 does not have this dual entry mode of operation. Together, these two 9300's constitute an 8-bit shift register. A 9312 8-input multiplexer switches the outputs of the two 9300's to give variable-length shifting up to seven stages. The output of this 9312 is then fed to one of the eight inputs of a second 9312; the other seven inputs come from seven 9328's, and

these provide shifting in increments of eight bits. By using the address inputs of the two 9312 multiplexers, one can shift the incoming recirculating data the required number of places up to a maximum number of 63 places.

Serial Memories

Figure 9 shows a circuit diagram of an 8-word by 8-bit serial/parallel memory that uses eight 9328's. In this circuit, serial data are entered into any one of the eight 9328's. A 9301 1-in-10 decoder determines which register the data enter and whether the data are old or new. The eight outputs of the parallel shift registers are multiplexed by two 8-input 9312's to give two serial independent output data streams, A and B, which can then be applied to some additional serial processing logic.

A counting multiplex display scheme for controlling 7-segment numerical indicators is shown in Figure 10. The two 9328 shift registers hold eight decades of information, and each decade sequentially addresses a 9307 decoder which drives the segments of 7-segment indicators via buffer transistors. The 9310 decade counters count to the desired value, and when display is required, the recirculation loop is broken and the eight new decades of information are shifted into the shift registers. At any clock time, the character to be displayed is controlled by two devices: a 9316 counter connected to divide by eight, and a decoder having eight mutually exclusive control lines. These control lines are usually buffered by transistors from each character. In this time division multiplexing scheme, the buffering is needed because of the high voltages required to give normal display brightness.

In special or in general-purpose serial computers, the 9328 is an ideal high-speed serial storage element. This capability is used in the serial arithmetic logic unit shown in Figure 11. Serial information X, Y enters the unit and is controlled by signals ABC to produce various arithmetic and logic functions on the serial variables, X and Y. The flip-flop holds the carry/borrow signal needed during computation. Since the first 8-bit shift register is connected to receive active low inputs from

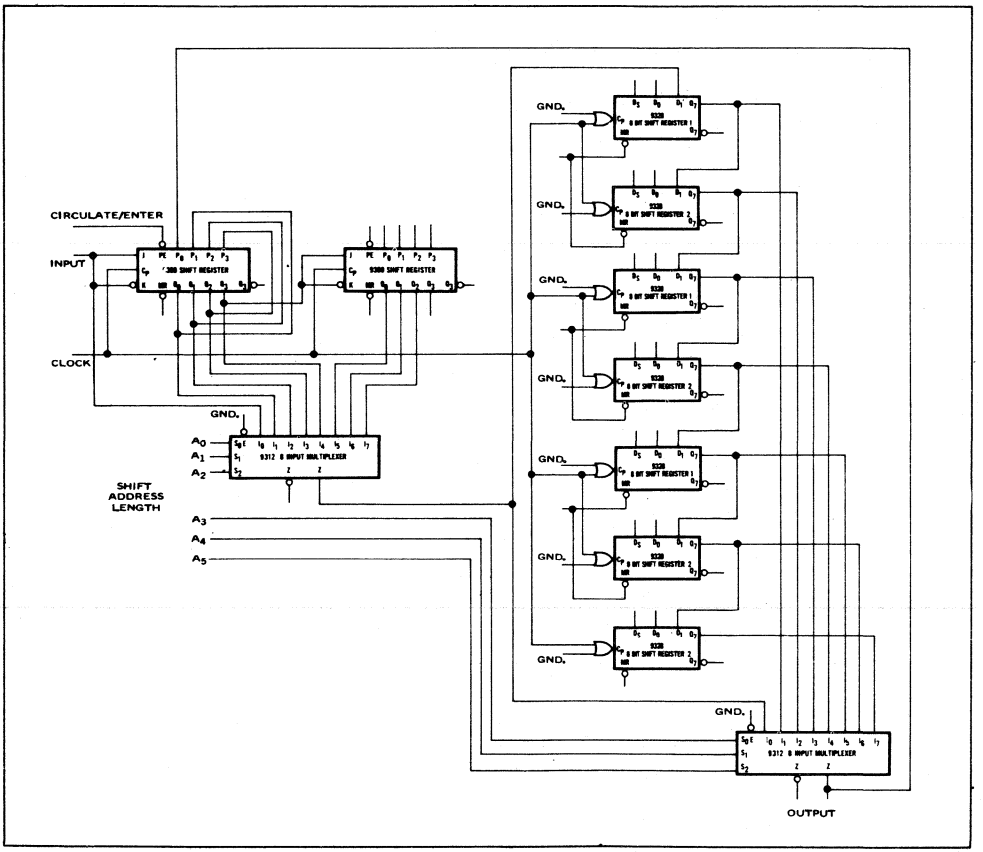


Fig. 8. Variable-length shift register.

the active low outputs (S and C_0) of the 9304 adder 1, the master reset control on the shift register when activated will set the register to the all 1's condition. The full adder 1 on the 9304 acts as an EXCLUSIVE OR generator to furnish the desired inputs to the JK 9020 flip-flop. The unit shown here provides the functions ADD, SUBTRACT, EXCLUSIVE OR, and AND on the two variables S and Y. (See Table II.) Figure 12 gives the truth tables, Karnaugh maps, and reduced functions required for implementation of the correct carry/borrow logic necessary for addition and subtraction.

TABLE II

A	B	C	FUNCTION
0	0	0	ADD X, Y
1	0	0	SUBTRACT Y FROM X
0	1	0	EX OR X, Y
1	1	0	EX OR X, Y
0	0	1	AND X, Y
1	0	1	AND X, Y
0	1	1	ALL 0's
1	1	1	ALL 0's

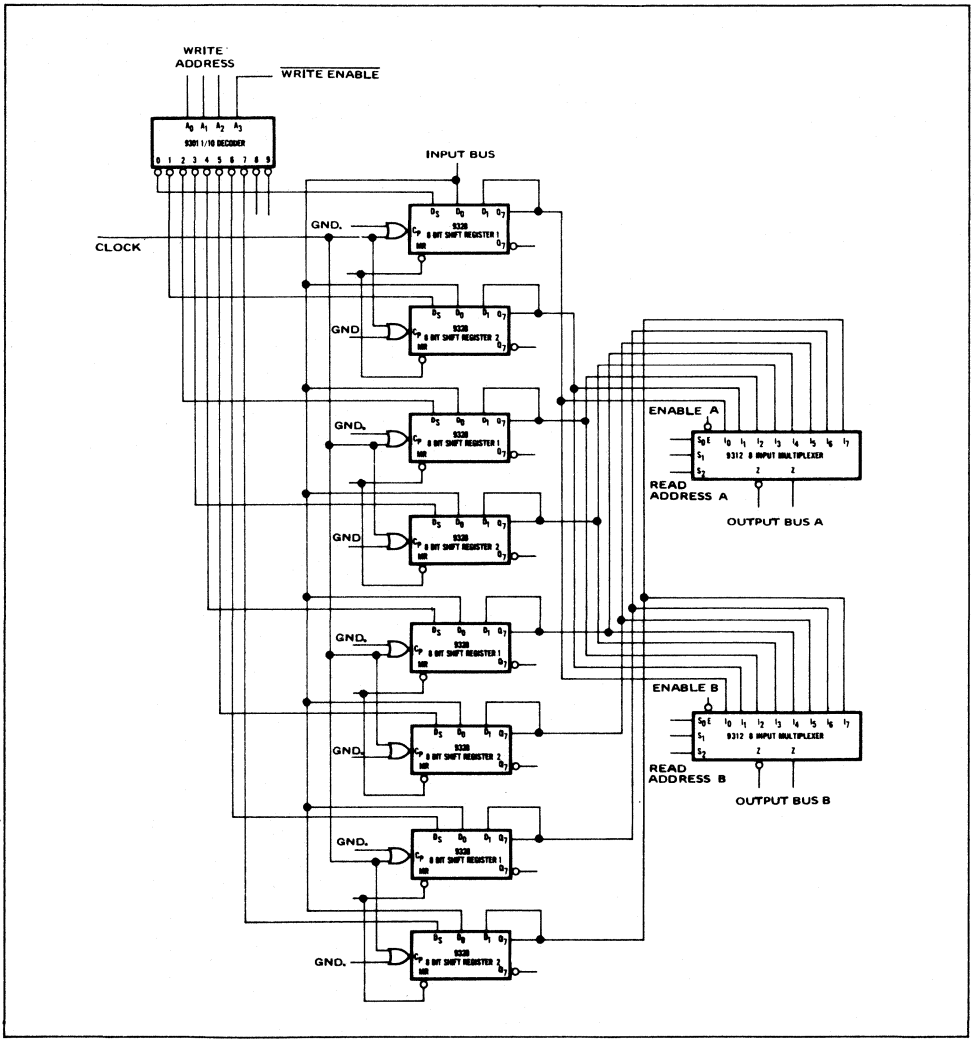


Fig. 9. Serial memory, 8 words x 8 bits.

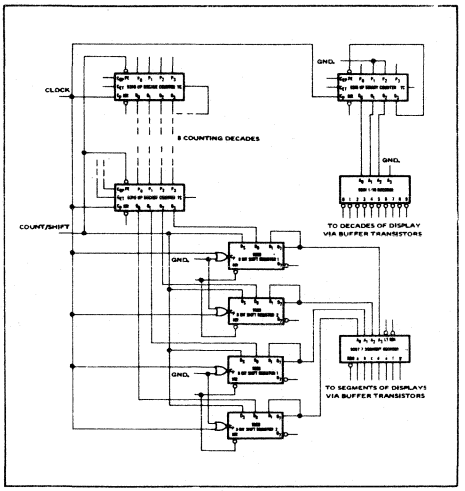


Fig. 10. Multiplex 7-segment count and display scheme.

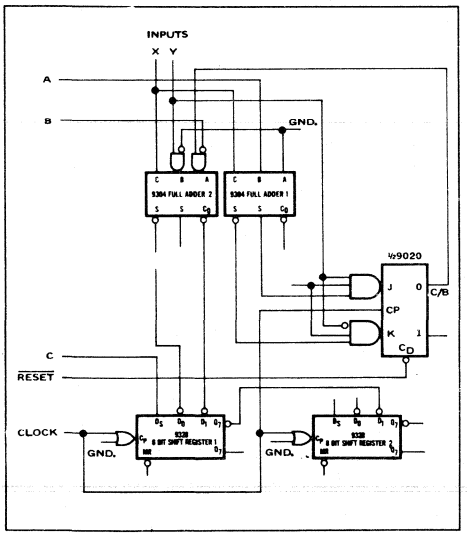


Fig. 11. Serial arithmetic logic unit.

Counters

The 9328 can act as a shift register counter in which several states are decoded and fed back to the input to force the register to pass through a loop of states. Since just the last stage of each of the device's two shift registers is available, only a small number of shift register counters can be built using one 9328.

TRUTH TABLE

X	Y	C/B_n	A	C/B_{n+1}
0	0	0	0	0
1	0	0	0	0
0	1	0	0	0
1	1	0	0	1
0	0	1	0	0
1	0	1	0	1
0	1	1	0	1
1	1	1	0	1
0	0	0	1	0
1	0	0	1	0
0	1	0	1	1
1	1	0	1	0
0	0	1	1	1
1	0	1	1	0
0	1	1	1	1
1	1	1	1	1

TRANSITION TABLE

C/B_n	C/B_{n+1}	J_n	K_n
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

KARNAUGH MAPS

J_n

C/B_n, A \ XY	00	10	11	01
00	0	0	[1]	0
10	X	X	[X]	X
11	X	X	X	[X]
01	0	0	0	[1]

$J_n = \overline{X}YC/B_n + XY\overline{C/B_n} = Y(X \oplus C/B_n)$

K_n

C/B_n, A \ XY	00	10	11	01
00	[X]	X	X	X
10	[1]	0	0	0
11	0	[1]	0	0
01	X	[X]	X	X

$K_n = \overline{X}\overline{Y}\overline{C/B_n} + X\overline{Y}\,C/B_n = \overline{Y}\,\overline{(X \oplus C/B_n)}$

Fig. 12. Serial ALU truth tables and Karnaugh maps.

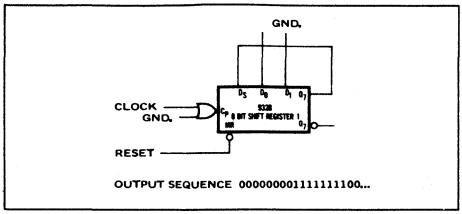


Fig. 13. Modulo 16 counter.

Figure 13 shows one half of a 9328 connected as a modulo 16 counter that produces a sequence of eight 0's and then eight 1's. The counter must be initialized since the same logic configuration could also produce other sequences, e.g. 010101, which is the sequence generated by a modulo 2 counter.

The 9328 may also be used as part of a long shift register counter to provide a pseudo-random sequence. Such a design is shown in Figure 14. This counter passes through $2^{63}-1$ states, a number so large that even at a frequency of 20 million states per second the counter would not repeat until more than 140 centuries had elapsed.

A simpler pseudo-random sequence generator is illustrated in Figure 15. The circuit uses only two IC's and recirculates every 50 milliseconds with a 20 MHz clock frequency. The required feedback connection is:

$$Q_2 \oplus Q_{19} = Q_2\bar{Q}_{19} + \bar{Q}_2 Q_{19}.$$

To implement this logic without discrete gates, Q_2 is fed into the parallel enable of the 9300 shift register, which is connected to act as a shift register even when parallel loading takes place. When Q_2 is low, the input to the shift register is Q_{19}; when Q_2 is high, the input is $\bar{Q}_{19}$ via the normal $J\bar{K}$ inputs.

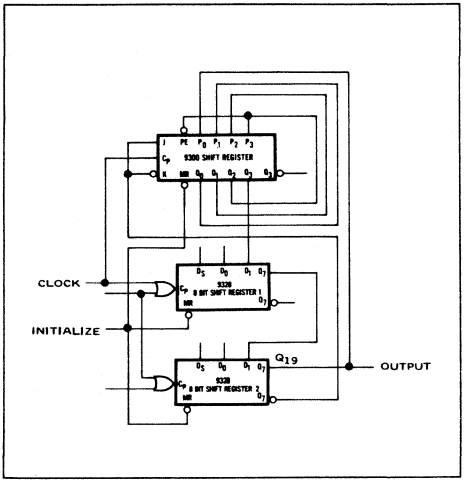


Fig. 15. Simple pseudo-random sequence generator.

CONCLUSION

The 9328 dual 8-bit shift register is an extremely powerful high-speed MSI building block that can be used in any system with a serial or parallel serial storage. Its shift enable and input multiplexing capabilities permit a great deal of flexibility and reduce the number of discrete gates and flip-flops needed to interface the shift register with other MSI devices. This results in low package count, high reliability, and efficient digital implementation.

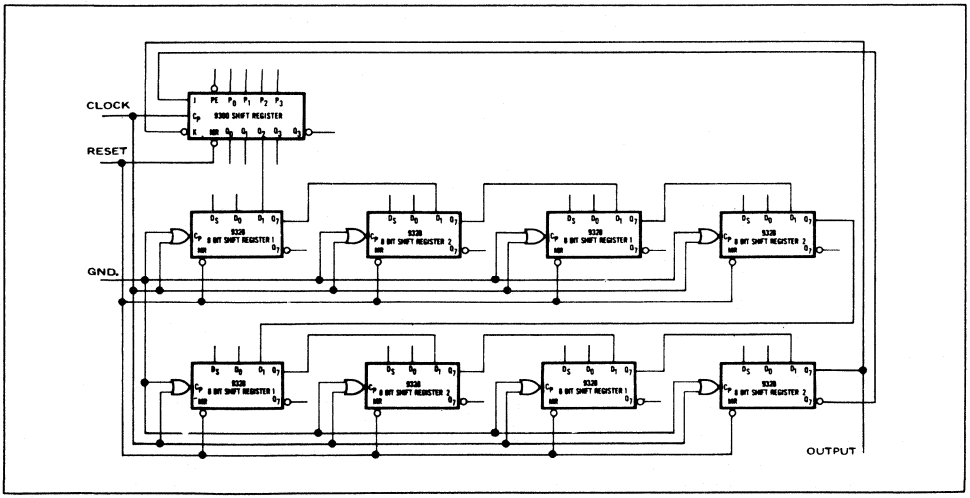


Fig. 14. Long pseudo-random sequence generator.

THE 9310–9316 COUNTERS

INTRODUCTION

The 9310 BCD decimal counter and the 9316 binary hexadecimal counter are multifunctional devices with the following features:

- Capability of being synchronously parallel loaded
- An asynchronous master reset
- An assertion output from each stage
- A terminal count activated (high) at count 9 on the 9310 and 15 on the 9316
- A count enable parallel (CEP) input and count enable trickle (CET) input that permit "enable while counting" in high-speed multiple decade counting operations
- TTμL integrated circuitry with active pullups to provide high speed with reasonable power consumption and excellent noise margins
- Input clamp diodes to ground to minimize the effects of line reflections
- Input/output characteristics that provide easy interfacing with all Fairchild TTL and DTL devices

Pin layouts, logic symbols, and loading factors are given in Figure 1.

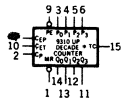
LOGIC

Logic diagrams for the 9310 and 9316 are shown in Figures 2 and 3, respectively. In each circuit, an inverting clock buffer drives the four clocked RS master/slave flip-flops in parallel to obtain synchronous operation.

When the clock input (CP) is low, the slave is steady, but data can enter the master via the R and the S inputs. During the low-to-high transition of the CP, (1) the data inputs (R and S) are inhibited, so that a later change in the input data will not affect the master, and (2) the information now trapped in the master is transferred to the slave and is reflected at the outputs. When the transfer is completed, both the master and the slave are steady as long as the clock input remains high, regardless of any other logic input, except MR.

During the high-to-low transition of the clock, (1) the transfer path from master to slave is inhibited, leaving the slave steady in its present state, and (2) the data inputs (R and S) are enabled permitting new data to enter the master. This arrangement permits synchronous operation at higher clock frequencies and requires much less external logic for most applications.

LOGIC SYMBOL



V_{CC}=PIN 16
GROUND=PIN 8
* OR 9316

PIN FUNCTIONS

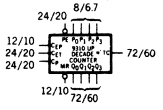
INPUTS
CP - CLOCK PULSE (POSITIVE EDGE)
C_{EP} - COUNT ENABLE PARALLEL
C_{ET} - COUNT ENABLE TRICKLE
MR - MASTER RESET (ASYNCHRONOUS)
PE - PARALLEL ENABLE (SYNCHRONOUS)
P_0, P_1, P_2, P_3 - PARALLEL (PRESET) INPUTS (SYNCHRONOUS)

OUTPUTS
TC - TERMINAL COUNT
Q_0, Q_1, Q_2, Q_3 - COUNTER OUTPUTS

LOGIC EQUATIONS
$\overline{\text{COUNT ENABLE}} = C_{EP} \cdot C_{ET} \cdot \overline{PE}$
TC (9310) = $Q_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot Q_3 \cdot C_{ET}$
TC (9316) = $Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot C_{ET}$
PRESET = PE · CP+ (RISING CLOCK EDGE)
RESET = MR
NOTE: PE AND MR ARE ACTIVE LOW INPUTS IMPLYING THE PINS ARE PE AND $\overline{MR}$. THEREFORE RESET = MR IMPLIES PIN 1 MUST BE LOW TO RESET.

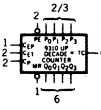
LOADING RULES

CCSL LOAD AND DRIVE FACTORS



OR 9316

TTμL LOAD AND DRIVE FACTORS



1 UNIT LOAD=1 TTμL INPUT GATE LOAD

A FULL EXPLANATION OF LOADING RULES MAY BE FOUND ON THE FAIRCHILD CCSL COMPOSITE DATA SHEET.

Fig. 1. Logic symbol, pin functions, and loading rules for the 9310 – 9316 counters.

FAIRCHILD
SEMICONDUCTOR

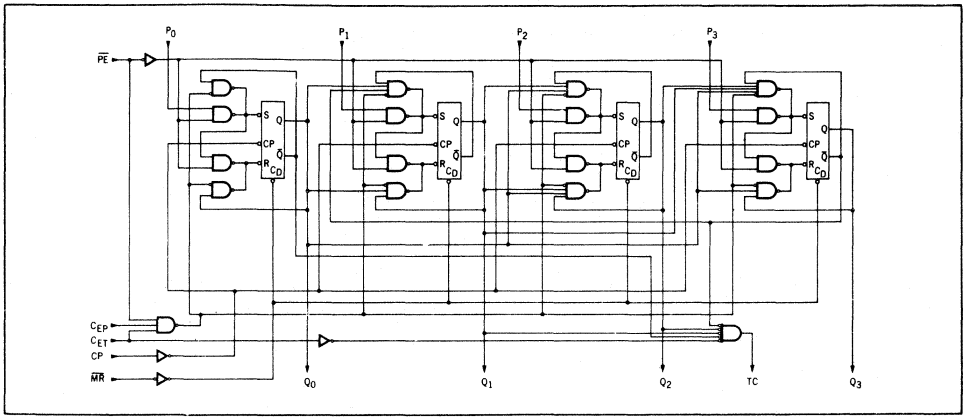


Fig. 2 9310 logic diagram

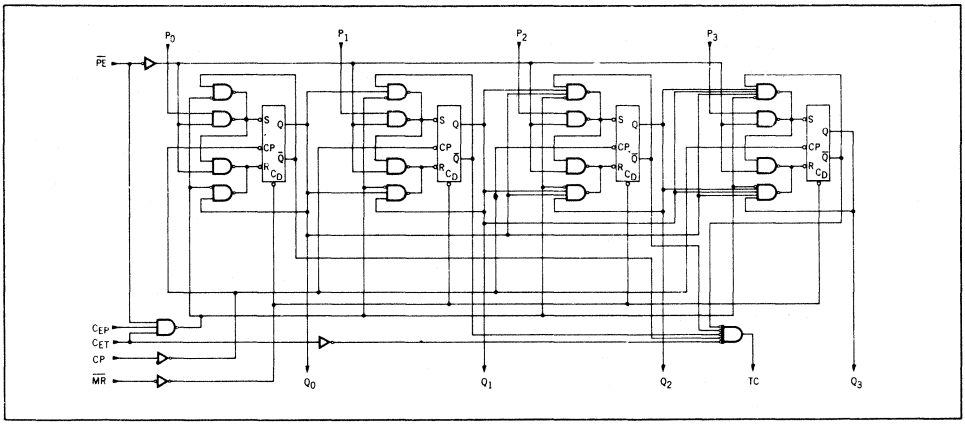


Fig. 3. 9316 logic diagram

MODE SELECTION

Three control inputs — parallel enable (PE), count enable parallel (CEP), and count enable trickle (CET) — select the mode of operation as shown in Figure 4. There are three different modes: count, preset, and no change.

$\overline{PE}$	C_{EP}	C_{ET}	MODE
L	L	L	PRESET
L	L	H	PRESET
L	H	L	PRESET
L	H	H	PRESET
H	L	L	NO CHANGE
H	L	H	NO CHANGE
H	H	L	NO CHANGE
H	H	H	COUNT

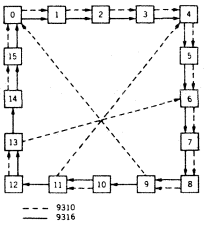
Fig. 4. 9310/9316 mode selection.

Proper logical operation requires that CP be high during the high-to-low transition of CEP or CET and the low-to-high transition of PE. In most applications, this restriction is not a hindrance since logic transitions usually follow the low-to-high transition of the clock pulse, and inputs are steady before CP goes low. The remaining transitions may be made by following the setup and release times specified under "Switching Characteristics" on the data sheet. The asychronous MR input clears the counter independent of any other input.

PRESET MODE

In each stage of the counter, the R and S inputs can be switched between two sources by the parallel enable (PE) input. When the $\overline{PE}$ input is in the low state, the R and S inputs of each of the four flip-flops are logically connected to form four independently clocked D flip-flops whose D inputs

are the parallel (or preset) inputs P_0, P_1, P_2, and P_3. The preset mode takes precedence over the two synchronous count enable controls, CEP and CET. One can preset the counters to any number between 0 and 15 by applying the binary equivalent of the number to the parallel inputs P_0, P_1, P_2, and P_3 and activating the PE input ($\overline{PE}$ low). The counter is preset on the following low-to-high transition of the clock. Counting is resumed when $\overline{PE}$, along with CEP and CET, is high and follows the sequence shown in Figure 5.



DECIMAL NUMBER	ENCODED NUMBER Q_0	Q_1	Q_2	Q_3
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
10	0	1	0	1
11	1	1	0	1
12	0	0	1	1
13	1	0	1	1
14	0	1	1	1
15	1	1	1	1

NOTE:
THE 9310 CAN BE PRESET TO ANY STATE, BUT WILL NOT COUNT BEYOND 9. IF PRESET TO STATE 10, 11, 12, 13, 14, OR 15, IT WILL RETURN TO ITS NORMAL SEQUENCE WITHIN TWO CLOCK PULSES.

Fig. 5. 9310/9316 count sequence.

MULTISTAGE COUNTING

In multistage counting, all less significant stages must be at their terminal count before the next more significant counter is enabled. The 9310 and 9316 internally decode the terminal count condition and "AND" it with the CET input to generate the terminal count (TC) output. This arrangement allows one to perform series enabling by connecting the TC output (enable signal) to the CET input of the following stage. (Figure 6a). The setup requires very few interconnections, but has the following drawback: since it takes time for the enable to ripple through the counter stages, there is a reduction in maximum counting speed. To increase the counting rate, it is necessary to decrease the propagation delay of the TC signal.

The CEP input of the 9310 and 9316 is internally "ANDED" with the CET input and connected to the R and S inputs of the individual flip-flops within the counter. This feature makes it possible to build a multistage counter (Figure 6b) that can operate as fast as a single counter stage. The advantage of the "enable while counting" method is best seen by assuming all stages except the second and last are in their terminal condition. As the second stage advances to its terminal count, an enable is allowed to trickle down to the last counter stage, but has the full cycle time of the first counter to reach it. Then as the TC of the first stage goes active (high),

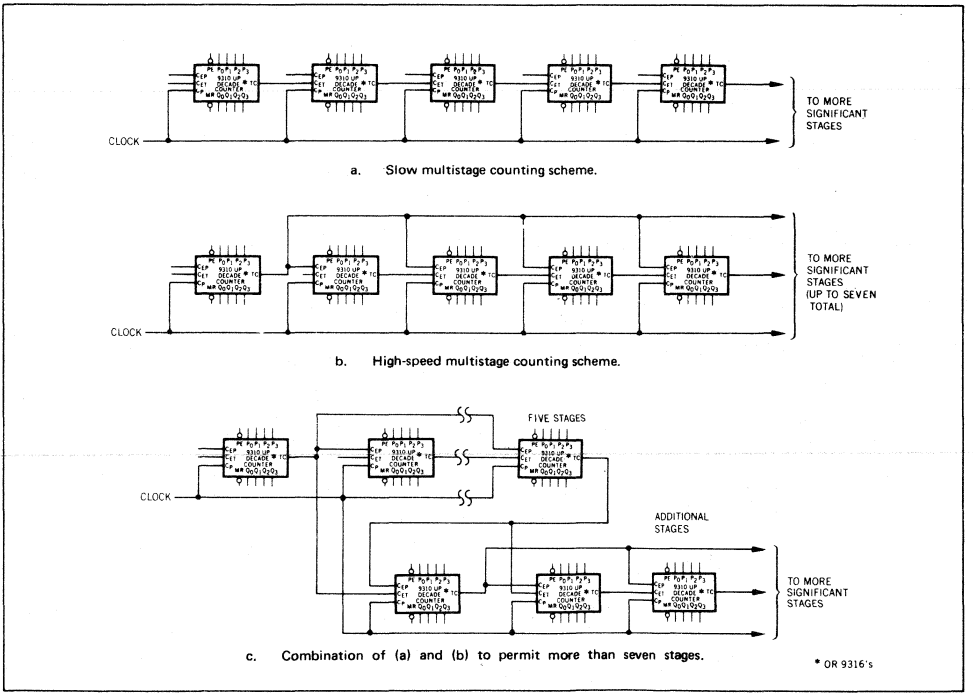


Fig. 6. Multistage counting.

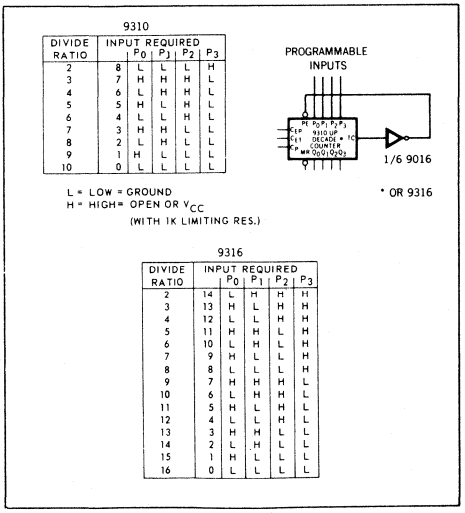
all CEP inputs are activated, allowing all stages to count on the next clock. The fan-out of TC (FO = 6) limits the configuration of Figure 6b to seven decades. More decades with no extra gates and with only a slight sacrifice in speed can be achieved by combining the two schemes of Figure 6a and 6b. This is shown in Figure 6c.

APPLICATIONS

Counters

The 9310 and 9316 can be converted into synchronous programmable counters with modulos of 2 to 10 and 2 to 16, respectively, simply by adding a single inverter (Figure 7). The counter thus formed actually simplifies certain applications. For example, most applications that seem to require that a counter counts either from zero to a predetermined number or from the number down to zero need not, in fact, be implemented in this way. Instead the operation can be performed with fewer gates by using a 9310 (or 9316) programmed with the complement of the number and allowing the device to count up until the terminal count is reached. Thus, if it is necessary to enable a line for three counts, a 9310 may be used by entering 6 (0110) (9's complement of 3) on the parallel inputs and counting up. Figure 8 shows a 9310 programmed by a 4-pole switch and used to permit 0 to 9 pulses to pass through a gate. Various types of readily available thumbwheel switches function equally well with these devices.

Note that all 9300 series devices belong to the current-sinking logic family. This means that an open input will appear to be "high" and must be grounded if a "low" is desired. For this reason, 9's complement switches providing closed contacts for "highs" only will not function directly with these devices, and a type providing shorts for "lows" must be used. The proper type is sometimes called "9's complement plus complement" or "inverted 9's complement" by thumbwheel switch manufacturers.



DIVIDE RATIO	INPUT REQUIRED	P_0	P_1	P_2	P_3
2	8	L	L	L	H
3	7	H	H	L	L
4	6	L	H	H	L
5	5	H	L	H	L
6	4	L	L	H	L
7	3	H	H	L	L
8	2	L	H	L	L
9	1	H	L	L	L
10	0	L	L	L	L

9316

DIVIDE RATIO	INPUT REQUIRED	P_0	P_1	P_2	P_3
2	14	L	H	H	H
3	13	H	L	H	H
4	12	L	L	H	H
5	11	H	H	L	H
6	10	L	H	L	H
7	9	H	L	L	H
8	8	L	L	L	H
9	7	H	H	H	L
10	6	L	H	H	L
11	5	H	L	H	L
12	4	L	L	H	L
13	3	H	H	L	L
14	2	L	H	L	L
15	1	H	L	L	L
16	0	L	L	L	L

Fig. 7. Programmable divider.

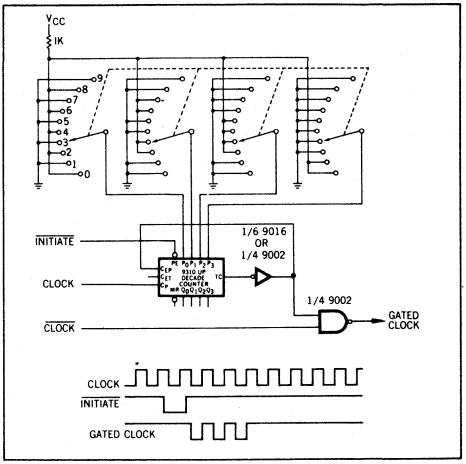


Fig. 8. Counter programmed by a rotary switch.

Figure 9 shows how the complement of a number not derived from switches may be generated. In a binary counter (9316), the negation outputs of the circuits supplying the number furnish the proper complement. If these outputs are not available, inverters will generate the complement, as shown in Figure 9a. In a decimal counter (9310), the 9's complement is easily generated by a 9309 dual 4-input multiplexer plus one inverter (Figure 9b), or by half of a 9321 dual 1-of-4 decoder plus a few gates (Figure 9c).

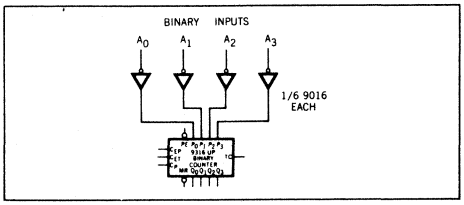


Fig. 9a. Generating the complement of a binary number.

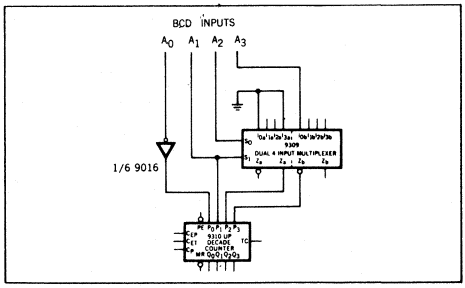


Fig. 9b. One circuit for generating the 9's complement of a BCD number.

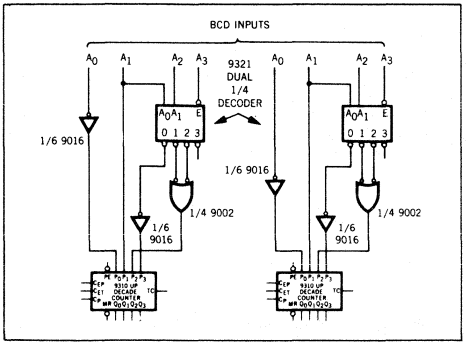


Fig. 9c. Another circuit for generating the 9 's complement of a BCD number.

Adding flip-flops enlarges the modulo of a 9316 counter to 32 or 64 states as shown by the presettable modulo-32 counter of Figure 10 and the modulo-64 counter of Figure 11.

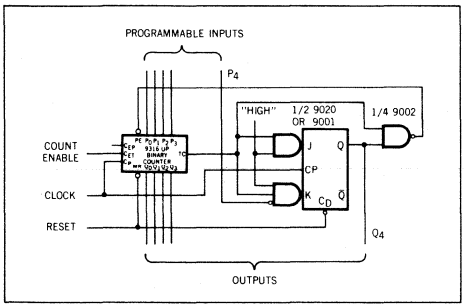


Fig. 10. Synchronously presettable modulo-32 counter.

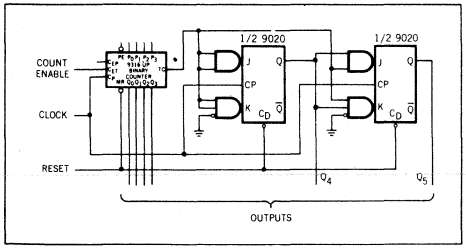


Fig. 11. Modulo-64 counter using two packages and no gates.

If a modulo-10 counter with 50% duty cycle is called for, it can be built simply by truncating a 9316 (Figure 12). An inverter between the TC output and the CEP enable input (Figure 13a), is all that is needed to stop a counter at its terminal state. The inverter, however, must not be connected to the CET enable input: since TC is a function of CET, such a connection will result in an oscillatory condition.

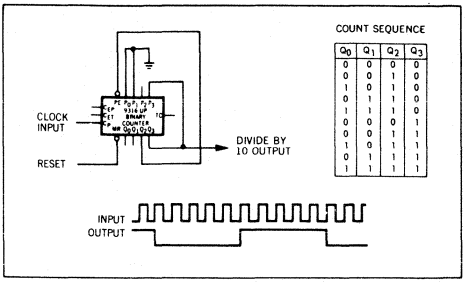


Fig. 12. Modulo-10 counter with 50% duty cycle.

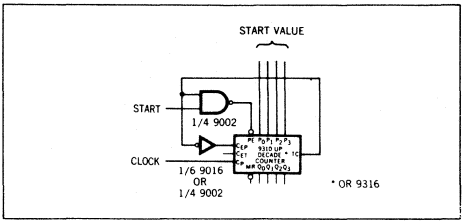


Fig. 13a. Self-stopping counter.

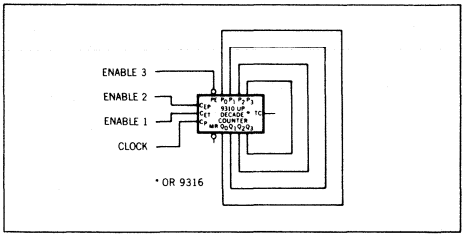


Fig. 13b. Counter with three enables.

If a particular application does not require the programmable feature, but does require three enables on a counter, then each Q output should be tied to the corresponding P input, as shown in Figure 13b, to permit the PE input to function as an enable.

Multistage Programmable Counters

In the multistage programmable decimal counter shown in Figure 14a, the terminal state is first decoded and then used as a preset signal. To get the proper count, the circuit works on a 9's complement and decodes the terminal count one count short of the all 9's condition. That is, one clock pulse before the all 9's condition, the least significant decade's Q_3 output is activated. And on the next clock pulse, each of the five decade counters is preset. This operation, which uses the 9's complement, is easier than loading the counter with the 10's complement. (The latter technique calls for an incrementer or adder.) Both techniques, however, give the same result.

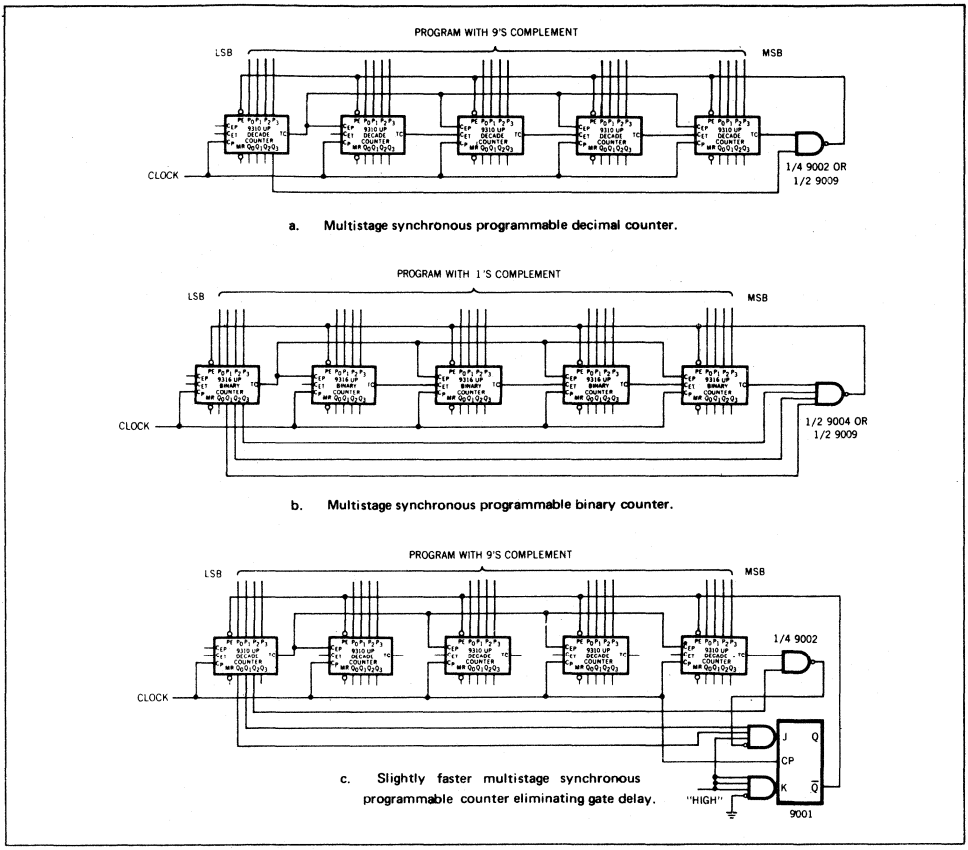


Fig. 14. Multistage programmable counters.

The multistage programmable binary counter, illustrated in Figure 14b, closely resembles the decimal counter just described, but requires a 4-input gate to decode the terminal state (14, 15, 15, ...).

Both the decimal and binary counters shown here have one drawback: the gate introduces a delay which reduces the maximum counting rate slightly. A more sophisticated decimal counter design, which eliminates this delay, can be seen in Figure 14c. In this circuit, the state prior to the terminal state is decoded and used to enable the set input of a flip-flop that controls the parallel enable (or preset) input of the counter. To enable the preset input, the counter sets the flip-flop one clock pulse prior to the actual terminal state. The next clock loads the counter, toggles the flip-flop, and removes the preset signal.

The multistage programmable counters discussed above all suffer a slight decrease in maximum allowable counting speed if they are programmed with certain numbers. For example, assume the counter shown in Figure 14a is being programmed with 999909 (or written least significant digit first as the counter is shown – 9 0 9 9 9 9). The counting sequence now goes

(MSB) 999996 (LSB)
999997
999998 – terminal count
999909 – programmed number
999910

The TC outputs are active from every stage except the first at terminal count (999998), but must not be active at the following count (999909 – the programmed number). The TC outputs therefore have to ripple low in time to prevent the most significant decade from changing on the next clock pulse. This limits the maximum counting rate to a figure slightly less than what is normally possible.

There are applications that call for counters that start at zero and reset upon reaching a predetermined number. (This

number may be derived from a switch position, it may be derived from internal logic signals, or it may be a permanently fixed number.) Two such counters are shown in Figures 15a and 15b. In the circuit of Figure 15a, a NAND gate decodes the terminal count, and on the next clock pulse the decoded output resets the counter through the PE inputs. The PE inputs make it possible to reset the counters synchronously by grounding all the P inputs. If the asynchronous MR input were used to reset the counter, a race condition would result. In the circuit of Figure 15b, 9324 comparators compare the count value against a value generated by logic circuits. The A<B output of the comparator serves as a preset signal to the counters.

The 9310 and 9316 can control a higher speed counter that is one of the stages of a programmable divider, and in so doing, extend the operating frequency by a factor of 10. This is illustrated by the circuit of Figure 16 in which a selectable divide-by-10 or divide-by-11 high-speed counter acts as the clock source for the subsequent counter stages and for a control counter. The control counter and 10/11 counter form the units counter of the programmable divider. Following the loading of the four 9310's, the control counter enables the divide-by-11 mode of the high-speed counter for the duration of the units cycle. When the units cycle is over, the control counter enables the divide-by-10 mode, causing the high-speed counter to become a divide-by-10 counter that functions as a normal decade units counter stage.

Up/Down Counters

The 9310 and 9316, when combined with gating circuitry, can be used as up/down counters. Figures 17a, b, c, d show four such counters.

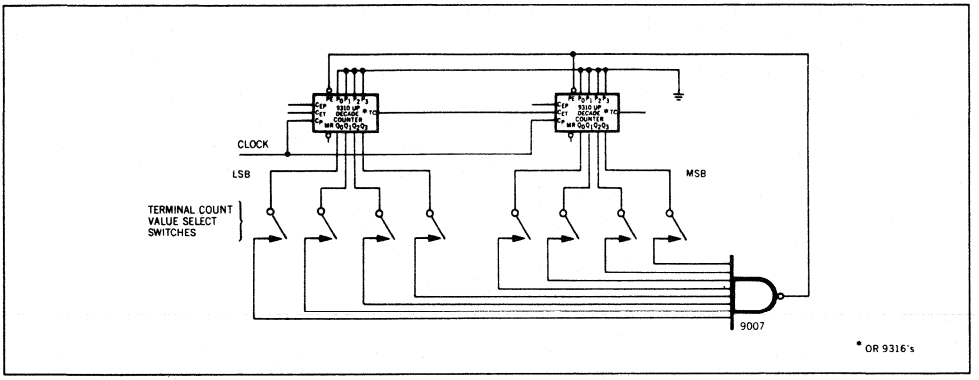


Fig. 15a. Switch programmable counter starting at zero.

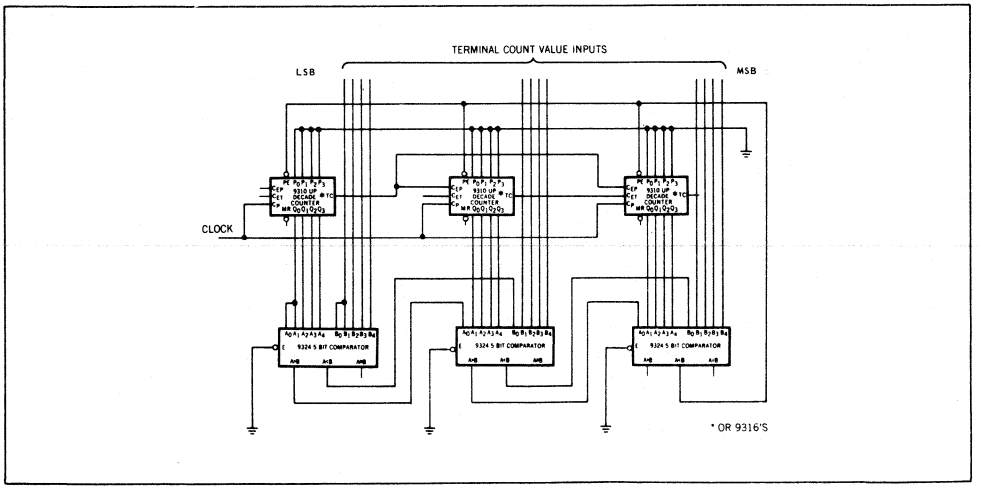


Fig. 15b. Programmable counters starting at zero.

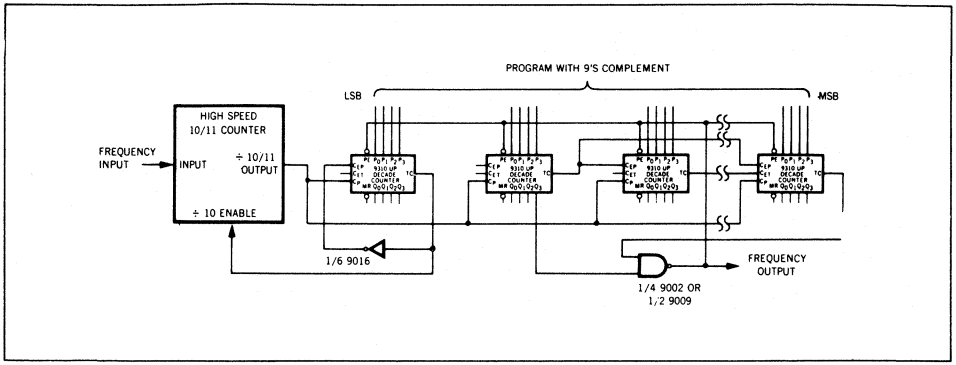


Fig. 16. Very-high-speed programmable divider.

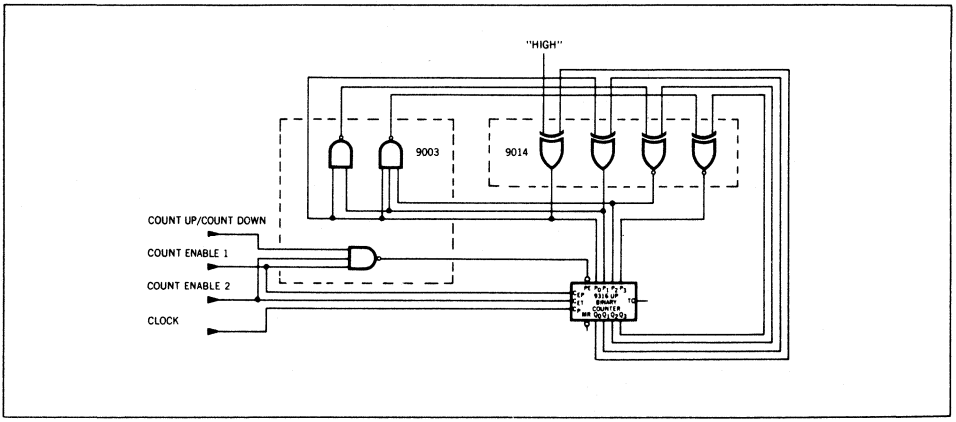


Fig. 17a. Binary up/down counter.

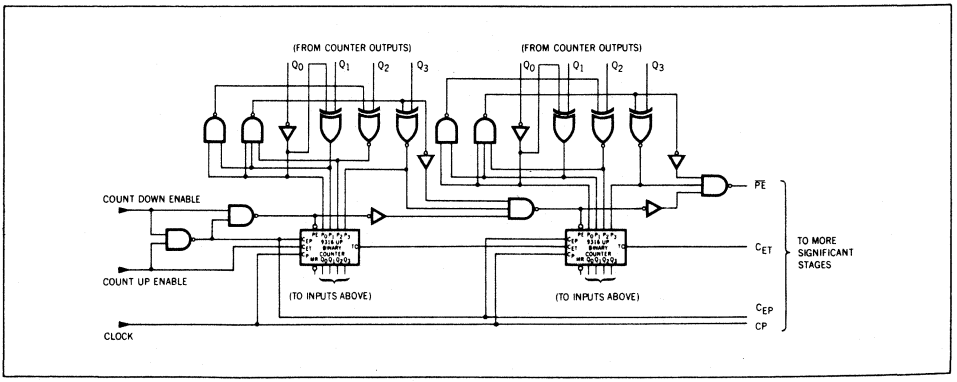


Fig. 17b. Binary up/down counter extended to more stages.

In Figure 17a, the binary up/down counter consists of three packages, one of which is a 9316. To count down, the PE is enabled, and the present number minus one, generated by the gates, is entered into the 9316 on the next clock pulse.

The technique may be extended to any number of stages by adding gating between stages as shown in Figure 17b, where two enables are provided, one for counting up and one for counting down. If both enables are high, the counter does not count.

In Figure 17c, 9310's are part of a decimal up/down counter which also includes a 9301 and two gating packages per decade.

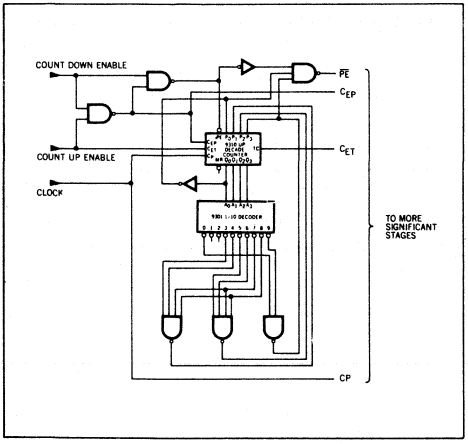


Fig. 17c. Decimal up/down counter.

Some up/down counter applications need only the count down capability for returning to a count after a test indicates the counter has advanced one count too far. Instead of including an up/down counter, the design may use a latch to store the previous count, as shown in Figure 17d.

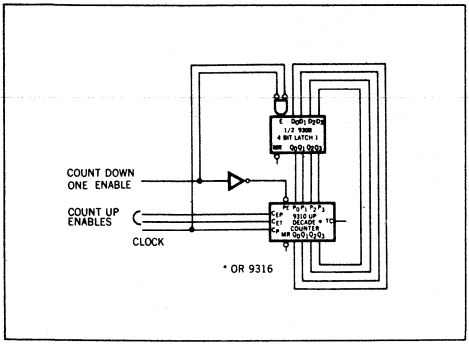


Fig. 17d. Counter with "return to previous count" feature.

Other Applications

The synchronous parallel load facility of the 9310 (or 9316) enables these counters to be used in applications not customarily associated with counters. For example, if the PE input of the 9310 (or 9316) is permanently grounded, the device behaves like four dual-rank D-input flip-flops, thereby decreasing the number of different parts needed for a system.

A resynchronizer using a 9310 (or 9316) as four D-input flip-flops is shown in Figure 18. In this circuit the $\overline{PE}$ input is grounded, and the resynchronizing input is applied to the CP input.

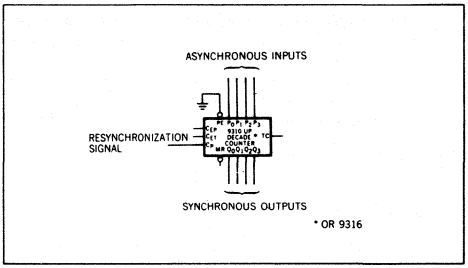


Fig. 18. Resynchronizer.

The contents of a 9310 or 9316 may be shifted out serially. In the circuit of Figure 19a, each 9310 (or 9316) has its Q outputs connected to the next more significant P input for shifting the most significant bit first. When the $\overline{\text{shift enable}}$ is high, the 9310's (or 9316's) perform the normal counting operation; when the $\overline{\text{shift enable}}$ is activated (low), the contents of the two-decade counter are shifted out serially at the Q_3 output of the second decade counter. If each 9310 (or 9316) output is connected to the next less significant parallel input, the least significant bit is shifted out first. Q_0 of the least significant stage provides the serial output.

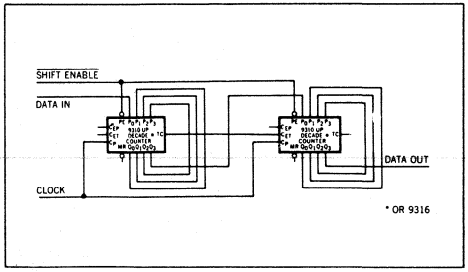


Fig. 19a. Combination counter/serial shift register.

The decade counter illustrated in Figure 19b shifts data out of each counter, in parallel, by decade, with the most significant decade shifted first. To shift the least significant decade first, it would be necessary to connect each output to the next less significant decade parallel inputs.

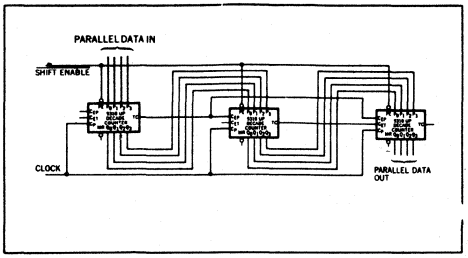


Fig. 19b. Combination counter/decade shift register.

A general scheme for programming a 9310 (or 9316) counter is shown in Figure 20. A diode matrix used as a read only memory or a decoding matrix (depending on how it is viewed) generates the desired code to be entered in the 9310 (or 9316); a 9301 or 9311 decoder selects the proper word; and 9935 inverters present this word to the parallel inputs. These inverters (standard DTμL inverters without input diodes) are needed to maintain noise immunity on the inputs.

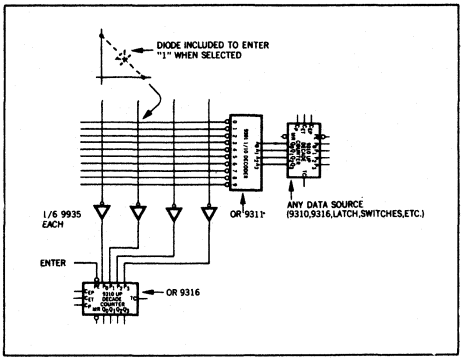


Fig. 20. Reading diode matrix into counter.

Cyclic D/A Conversion

Figure 21 is a schematic of a dual D/A PDM converter implemented with 9310's (or 9316's). This circuit uses one programmable counter per channel plus one reference counter. The number to be converted is supplied to the parallel inputs of the programmable counter and entered when the reference counter is at terminal count (TC active). The programmable counter count value is greater than the count value of the reference counter by a number of counts equal to the digital input. To produce a PDM output directly proportional to the phase difference of the two counters, the terminal counts of the programmable and reference counters alternately set and reset the 9020 flip-flop. Additional D/A conversion channels are easily obtained by adding a programmable counter and flip-flop for each channel desired.

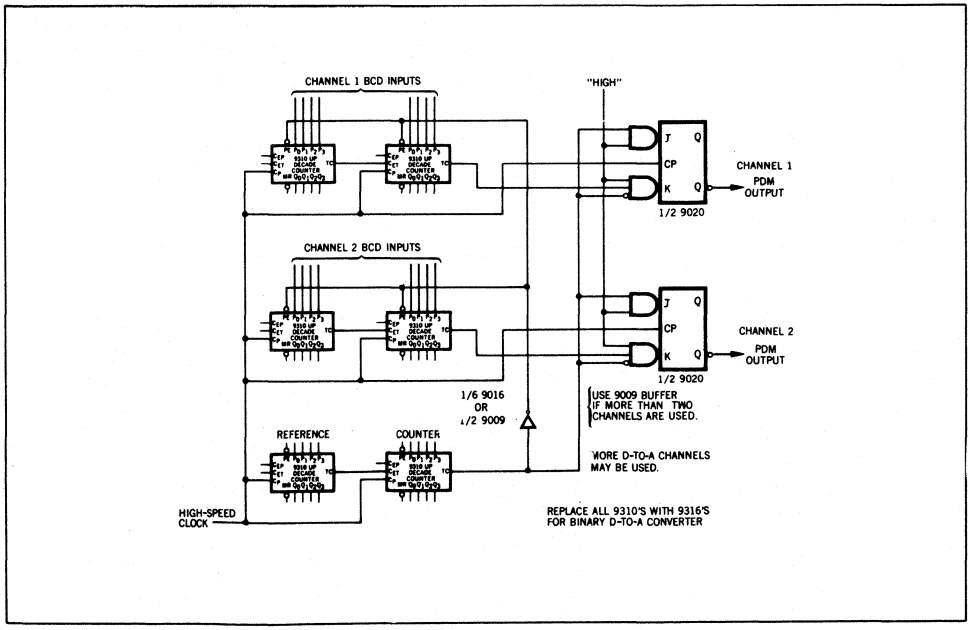


Fig. 21. Digital to analog converter with PDM output.

USING THE 93402 ASSOCIATIVE MEMORY

INTRODUCTION

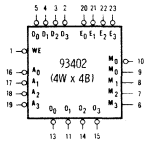
Fairchild's 93402 is a high-speed four-word-by-four-bit associative memory, useful in table look-up, decoding, scratch-pad memory, and other temporary storage applications. The principal feature of the device is its ability to search for specific information stored in it, and to indicate in which words that information is written.

The 93402 is fully compatible with Fairchild DTL and TTL and can be a versatile component in an MSI system. Its function can be expanded into a memory array by wire-ORing the outputs of several units.

GENERAL DESCRIPTION

Figure 1 shows the logic symbol and loading rules for the 93402. Data on the inputs ($\overline{D}_0$ to $\overline{D}_3$) can be written into any location in the memory by placing a LOW on the corresponding word Address line ($\overline{A}_0$ to $\overline{A}_3$), and on the Write Enable ($\overline{WE}$) line. The data in any word addressed will appear on the outputs ($\overline{O}_0$ to $\overline{O}_3$). Data stored in the memory can be compared with data on the inputs. If the word on the inputs matches a stored word, the Match output (M_0 to M_3) for that stored word will go HIGH. In both Write and Compare operations, only the Data inputs for which the corresponding Bit Enable ($\overline{E}$) input is LOW are active. Inputs for which the Bit Enable is HIGH are ignored or "masked". All outputs are uncommitted collectors for wired-OR use.

LOGIC SYMBOL



PIN 12: GROUND
PIN 24: V_{CC}

LOADING RULES

	HIGH LEVEL (TTL Unit Loads)	LOW LEVEL (TTL Unit Loads)
Address	1.0	1.0
Bit Enable	1.5	1.5
Write Enable	1.5	1.5
Data Input	1.0	1.0
Data Output	Open Collector	6.2
Match Output	Open Collector	6.2

1 Low-Level TTL Unit Load = −1.6 mA
1 High-Level TTL Unit Load = 60 μA

Fig. 1. Logic symbol and loading rules for the 93402 associative memory.

Reading

Any word in the memory may be selected by applying a LOW to an Address input. If desired, more than one word may be addressed simultaneously. The contents of the addressed word appear on the data outputs. If more than one word is addressed, the data outputs will contain the OR combination (active LOW) of the words addressed. If no words are addressed, all data outputs will be HIGH.

Writing

New data may be written into the memory by addressing the appropriate word or words and placing a LOW on the $\overline{WE}$ input. The information present at the Data inputs will be written into the selected words in each bit for which the corresponding Bit Enable input is LOW. To write a complete new word, there must be a LOW on the Address input, the Write Enable input, and all four Bit-Enable inputs.

Matching

The principal feature of the 93402 is its comparing function. The device can indicate a correspondence between data present on the inputs and data already stored in the memory. Each input bit that is enabled will be compared with the corresponding bit in each of the four stored words. The Enable inputs act as a mask; input bits that are not enabled are ignored. If any stored word matches the data on the input in each enabled bit, a match will be indicated by a HIGH level on the corresponding Match output.

To compare stored words with data on the inputs in all bits, all Bit Enable inputs must be LOW. There will be a HIGH on the Match output of each word that is identical with the data on the inputs. In the Match operation, the input data is called the "descriptor".

FAIRCHILD
SEMICONDUCTOR

Expansion

All the output leads are open-collector terminals. This type of connection makes it possible for the user to decide his own output capabilities by specifying the value of the collector resistor. A large resistor will increase the number of wired-OR connections possible, but will reduce fanout and switching speed. A small resistor will increase fanout, but decrease the number of wired-OR's possible. The upper and lower limits of the resistor value are given by the inequality below:

$$\frac{5.1}{10 - 1.6\,F} \leq R \leq \frac{2.1}{L + 0.06\,F}$$

where R = value of collector resistor in kΩ
F = fanout (number of TTL loads driven)
L = sum of the leakage currents of all interconnected outputs

The logic symbol of the device shows active LOW outputs. This is to emphasize the wired-OR function. If the logical *1's* are written into the memory as LOW logic levels, the outputs can simply be tied together to obtain an OR function for logical *1's* over all bits. If any output is LOW, the common line will also be LOW. Conversely, the Match outputs when tied together become wired-AND's, because their active level is HIGH. The process at the $\overline{O}$ and M outputs is the same, only the interpretation is different.

However, there is no inversion through the memory cell. A HIGH level written in at an input will be read as a HIGH level on an output. Sometimes it is more convenient to use the device with active HIGH inputs and outputs, particularly if the wired-OR capability is not desired.

The $\overline{M}_0$-output is an inverter directly on the M_0-line, and is affected by the wired-OR on M_0. This inverter is useful for expansion techniques.

APPLICATIONS

Expansion to More Words

Since the outputs of the 93402 can be wire-OR'ed, word expansion is very simple. The corresponding bit outputs of each 93402 are tied together, as illustrated in *Figure 2*. When a word is addressed, any logical *1's* in the word will produce a LOW at the output. Since all corresponding bit outputs are tied together, the common O line for that bit goes LOW. The system can be expanded in this manner to a maximum of 120 words (if fanout is unity).

Expansion to Larger Words

Figure 3 illustrates expansion of four 93402 associative memory units into a system that can handle 16-bit words. The bit expansion is accomplished by placing parts of each word in different memories. Four memories are required to accommodate the 16 bits. The Match outputs from all four memories for parts of the same word are tied together. In the Match mode, the stored word must match the input data in all 16 bits to produce a HIGH on the wire-OR'ed Match outputs.

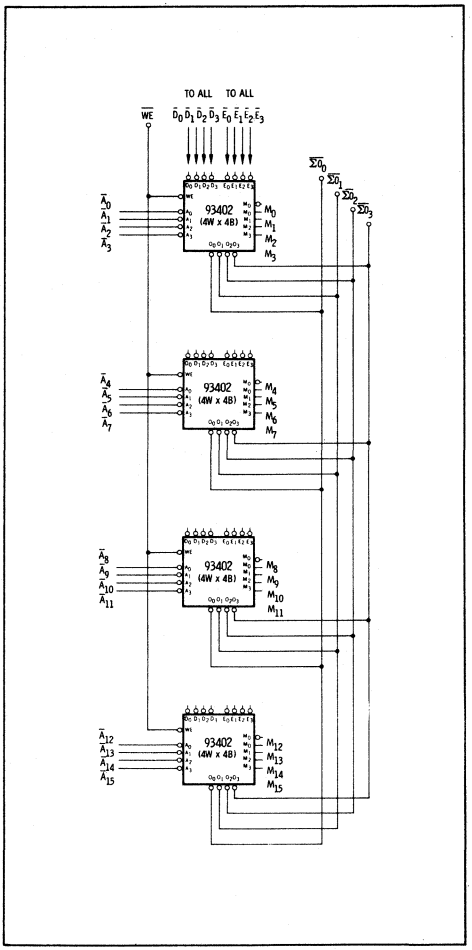


Fig. 2. Expansion of the 93402 associative memory to process 16 words. Pull up resistors to V_{CC} are required on all output lines.

Figure 3 shows how the inverted M_0 - output ($\overline{M}_0$) can be used to indicate "no match". The word segments have been placed in staggered locations in the four memories so that part of each word can appear in an A_0-location. If there is a match in any word, then at least one M_0 - output must be HIGH and corresponding $\overline{M}_0$ LOW. The four $\overline{M}_0$ - outputs are wire-OR'ed so that if there is a match in any word, the "no-match" line will be LOW. If there is no match, all the M_0's will be LOW, all the $\overline{M}_0$'s will be HIGH, and the "no match" line will be HIGH.

Table Look-Up

The 93402 can be used for one-way or two-way table look-up operations. A table look-up is essentially a read-only memory

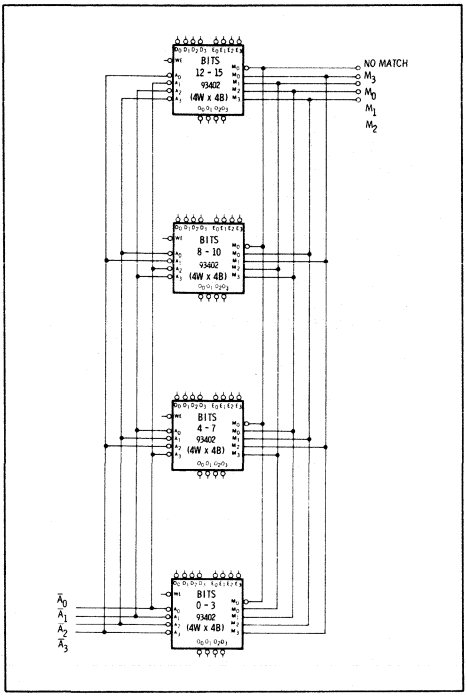


Fig. 3. Expansion of the 93402 associative memory to process 16-bit words.

or decoder. *Figure 4* shows six associative memories connected as a 1-of-12 decoder. An 8-bit word presented at the inputs is compared with the 12 8-bit words stored in the memories. A match is indicated by a HIGH level on one of the 12 Match outputs. The Match outputs could be used to address some word in a 93435, 64-bit random-access memory. The advantage of a system such as this is that the encoding pattern can be altered at any time, simply by loading the 93402 with new information. This system could be used to decode information from a magnetic ink reader, where there is a unique 8-bit code for each of the digits 0 through 9.

Multifield Association

Information can be stored in a multifield associative memory in such a manner that data in one field can be used to obtain related data from the other fields by using a match in one field to address the entire word. This is illustrated in *Figure 5* which shows a 16-bit-by-16-word associative field memory formed from word and bit expansions of 16 93402's.

The field concept can be applied to this array to make a two-way table. The eight bits of memory on the left could be loaded with one set of data, and the eight bits on the right with a corresponding set of data. For instance, the left side of each word might contain a binary number x, and the right side of the same word a binary number for log x. The data inputs for the corresponding bits are tied together and the Enable inputs for each half connected as shown in *Figure 6a.*

If the Select input is HIGH, all left-field bits will be enabled and all right-field bits masked. A binary number presented on the Data inputs will be compared with data on the left side of the memory. If the Select input is LOW, data will be compared

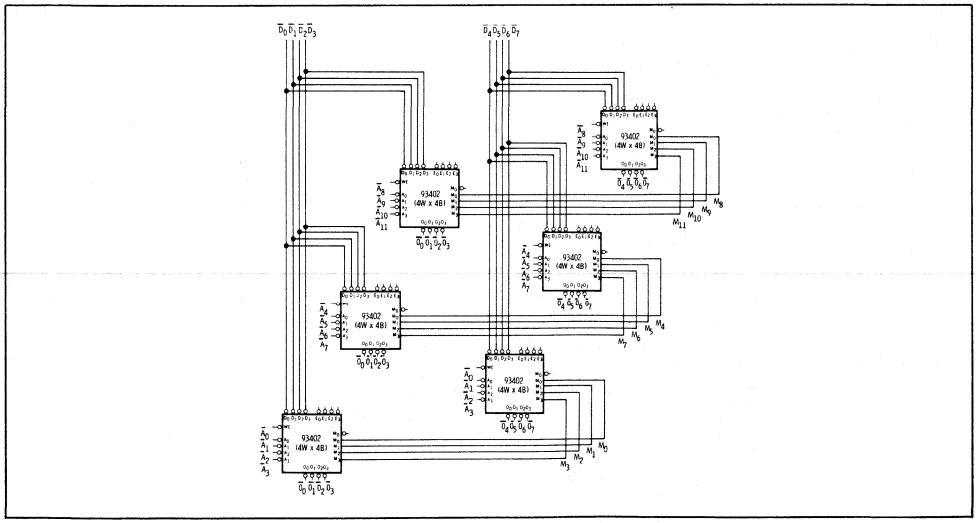


Fig. 4. Expansion of six 93402's into an 8-bit-by-12-word system used as a table look-up.

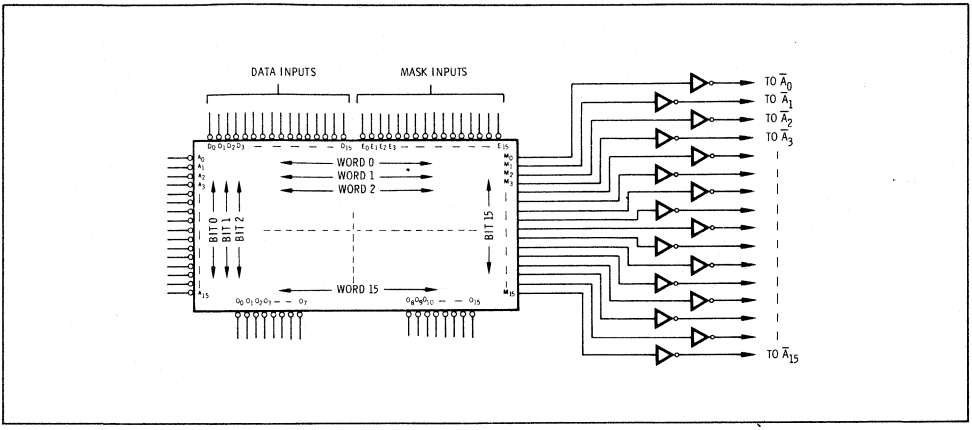


Fig. 5. A 16-bit-by-16-word associative field memory formed from 93402's. Match outputs are inverted and used to address words which produced the match.

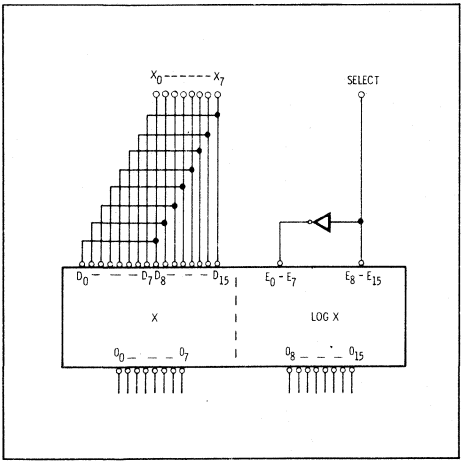


Fig. 6a. A two-field associative memory useful as a two-way table. Numbers are stored in left field and logs in right field. Either field can be used to obtain the corresponding number from the other field.

with the right side of the memory and the left side will be masked. Match signals are fed back to address the entire word producing the match. If a number x is placed on the Data inputs and the Select input is HIGH, the outputs will contain x on the left and log x on the right. If the Select is LOW, the outputs will contain x on the right and antilog x on the left. A match in the preselected field causes corresponding information from both fields to appear at the output.

This scheme can be broadened to include more than two fields. For example, five fields might be used in an air traffic control system: (1) plane identification, (2) range, (3) altitude, (4) speed, and (5) status code.

Figure 6b illustrates such an arrangement. The operator selects the information he is interested in and the memory reads out all related information. If Field 1 were enabled, information about a particular plane could be obtained. If Field 2 were enabled, data about all planes within a certain range could be read out. If information about all planes in holding patterns were desired, then Field 5 would be enabled. If information were requested that would produce more than one set of data, the multiple-match system discussed below would be used. The readout can also be converted to a CRT display.

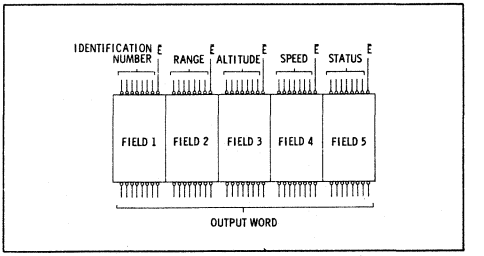
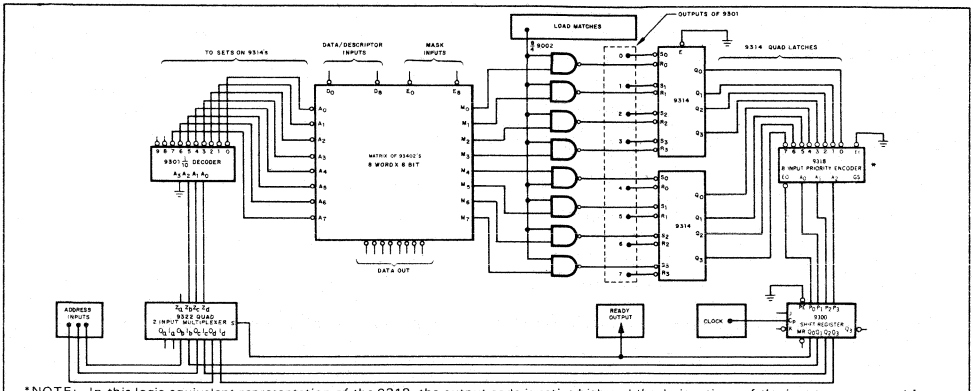


Fig. 6b. Five-field memory. Matches may be searched in any field by enabling only bits in that field. When a match is located, all related data will be read out.

Handling Multiple Matches

If several words in the associative memory produce matches simultaneously, it may be necessary to segregate those match signals in order to read out the words one at a time. This case will arise frequently when (1) the descriptor is heavily masked (reduced to a few "tag bits", for example), and (2) the words matching the descriptor are to be read out rather than all operated on at once.

When this circumstance arises, the 9318 priority encoder is



*NOTE: In this logic equivalent representation of the 9318, the output code is active high and the designations of the inputs are reversed from the normal order. The input labeled "0" is highest priority. This is the "7" input on the ordinary representation of the 9318.

Fig. 7. System for processing multiple matches.

a convenient tool for processing the match signals. The 9318 has eight inputs and produces a three-bit code designating the particular input which is active. Moreover, if several inputs are active simultaneously, only that input of highest priority is reflected in the output. Although the specific assignment of priority possible with the 9318 is most likely not a valuable feature in this case, nevertheless it does provide a convenient method of separating the several match signals into a serial representation of individual match signals. Such a scheme is illustrated in *Figure 7.*

The input labeled "load matches" is made HIGH when the descriptor and mask are applied. This allows the match signals to be latched into the 9314 quad R-S latches. A match signal causes the corresponding latch to be RESET. The "load" signal, descriptor and mask may then be removed. The matches are now stored and applied to the input of the priority encoder, which produces an output code for the match of highest priority. The EO output goes high, indicating that there is at least one active input on the 9318. When the 9300 register is clocked, the three code bits and the EO bit are stored and fed to the multiplexer. The EO bit causes the multiplexer to channel the register code to the decoder, which in turn addresses the corresponding word in the associative memory and SETS the latch containing the match signal.

The next match signal is then the highest priority and is encoded by the 9318. The process continues, with each clock causing another matching word to be read out of the memory, until there are no more matches remaining in the latches. When this occurs, the EO output will go low, and on the next clock, the multiplexer will shift back to the external address inputs and the "Ready" line will go LOW.

Buffer Memory Applications

The 93402, in association with the 93435 Read/Write Memory, can be of great value in speeding up memory access in a computer. The basic scheme is illustrated in *Figure 8.* Match signals from the associative memory are used to address locations in the 93435 memory. The associative section will ordinarily contain some kind of descriptive information about

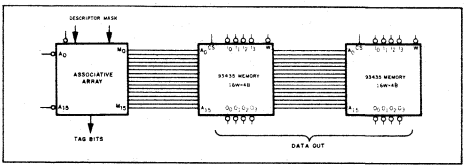


Fig. 8. Memory system formed by interconnection of associative and ordinary read/write memories.

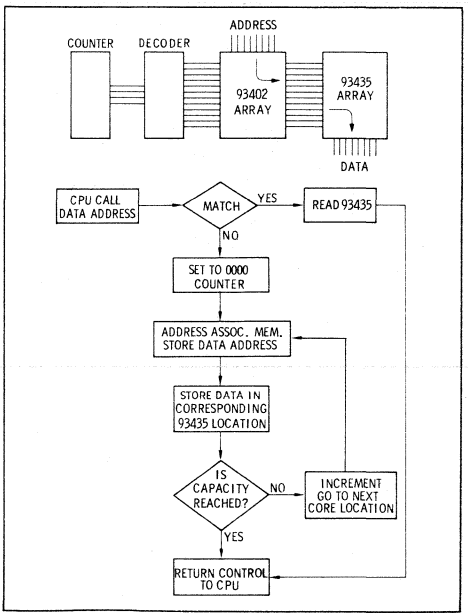


Fig. 9. Information flow diagram of high-speed memory section.

corresponding data in the 93435's. Data is written into both types of memory simultaneously. (Writing into a word in the 93402 always causes the match line for that word to go HIGH.)

One application of such a scheme is a kind of indirect addressing. The associative memory contains a virtual address for data. Whenever that address is called, a match signal is generated, causing the 93435 to produce the true address for the data. This system makes it a simple matter to assign and alter memory location addresses, with a minimal time required to locate information.

Another way to use this kind of arrangement is to store data addresses (or "page" addresses) in associative memory and data in semiconductor read/write memory.

The system illustrated in *Figure 9* is one way in which this might be done. Whenever an address is called by the control system (CPU), the associative memory is checked for that address. If the address is present, then the requested data is read from high speed semiconductor memory. If the address is not present in the associative memory, then the data are retrieved from core instead. In addition, the new data are stored in semiconductor memory and the address in associative memory. The system in *Figure 9* then proceeds to remove an entire block of data from core and store it in semiconductor memory. This is done because most likely the next addresses called will be from those locations immediately following the last address. By anticipating the calling of consecutive addresses, it is possible to maintain the data currently being accessed in high speed semiconductor storage. The diagram in *Figure 9* uses a counter to sequentially retrieve words from core. In the IBM 360/85 "cache" memory, the associative memory stores "page" numbers, and blocks of data are moved in parallel from core to semiconductor storage.

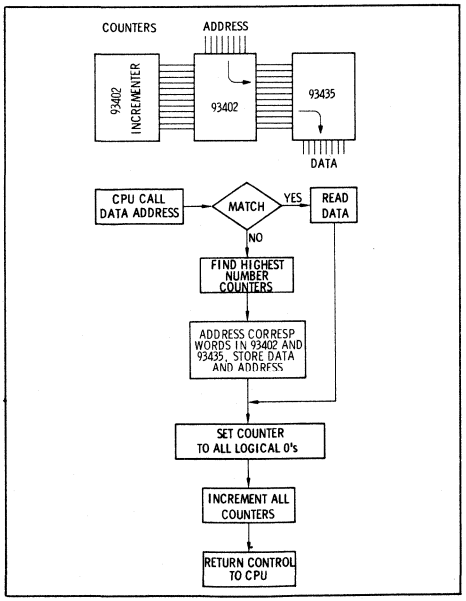


Fig. 10. Information flow diagram of a high-speed push-down memory.

The other system, illustrated in *Figure 10*, is a form of push-down memory and is a little more sophisticated than the previous one. For this unit, data is transferred from the core to a set of 93402's and 93435's, as in the earlier system. This time, however, data is brought in only as it is needed. One set of 93402's is used to keep track of how often each word has been called, and the least used data in the system is replaced by the new data.

Whenever the memory system is called, the count for each word is incremented by one. The count for the word actually used is reset to zero. If a new word is to be written in, the location selected is the one with the highest count, that is, the location which has been used the least. Such a system automatically maintains the most frequently used information in the rapid-access semiconductor memory. The highest count in the counter memory is found by counting down on the memory inputs from the maximum possible count until a match is achieved. The words in the memory can be incremented simultaneously by a scheme described in the following section.

Multiword Processing

An important application of associative memories is "associative processing". Associative processing may be defined as simultaneous operation on all data having specific characteristics. In practice, this implies a system in which all words in the memory are searched for some characteristic, and all those words having that characteristic are simultaneously altered in some fashion.

The system illustrated in *Figure 11*, although not particularly practical, serves to demonstrate this type of operation. Functionally, it is a "multiword incrementer". On command, it simultaneously increments every stored word.

The 9322 multiplexers around the memory are used to select whether the memory is being used in the "increment" mode or in the normal mode. Selection is controlled by the TC (Terminal Count) output of the 9316 counter.

Incrementing is initiated by strobing the master reset (MR) on the 9316, setting it to 0000. The 9316 and the 9001 then count up. The most significant three bits of the counter are used to enable the associative memory bits one at a time. These most significant bits change every four clock pulses. The two less significant bits go through four states for each state of the three more significant bits. These four states are used to implement the addition algorithm shown in *Table 1*. For each word in the memory there is one spare location in the memory (bit 7) used to keep track of a Carry bit. When the words are written in, the Carry locations are all loaded with logical 7's. Each N-bit is added to the Carry bit, and a new N-bit and Carry bit are written into the memory. Incrementing is based on the algorithm shown in *Table 1*.

TABLE I

PRESENT STATE		NEW STATE		OPERATION
N-Bit	Carry Bit	N-Bit	Carry Bit	
0	0	0	0	Do nothing
0	1	1	0	Write logical 1 in N-bit, write 0 in Carry bit
1	0	1	0	Do nothing
1	1	0	1	Write logical 0 in N-bit

The two states requiring action are detected and the appropriate changes are made for each bit of the word, beginning with the least significant, bit *0*.

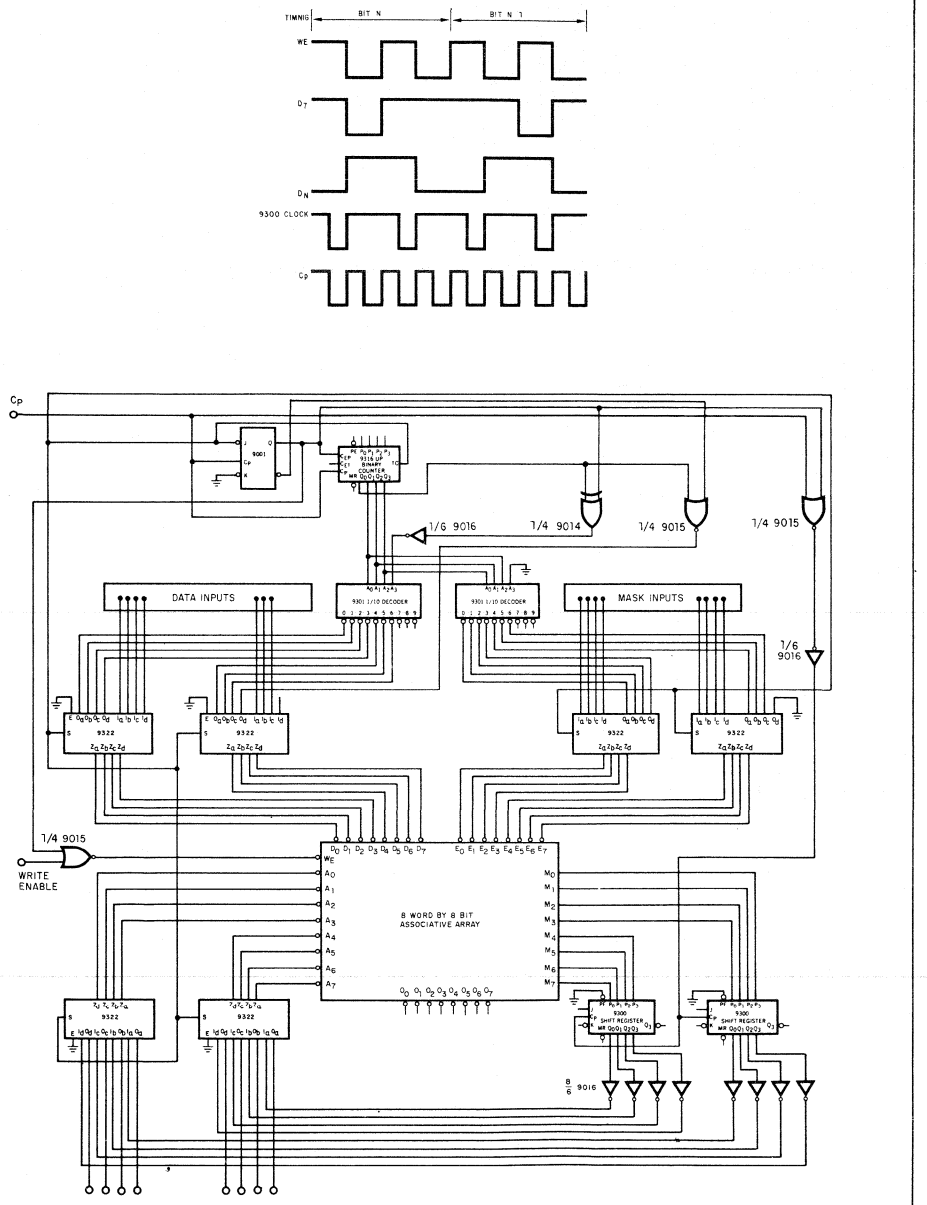


Fig. 11. An associative processing system: Multiword incrementer.

State 00 applies a 1 (negative logic) to the D_7 and a 1 to bit N. The next clock pulse loads the match signals into the 9300s. State 10 enables the write input and writes a 1 into D_7 and a 0 into D_N. State 01 searches for a 1 in D_7 and and a 0 in D_N; matches are loaded and state 11 writes a 0 in D_7 and a 1 in D_N. The next clock causes the most significant three bits to increment, so that bit N+1 will be operated upon for the next four bits. When the counter reaches 01111, it stops and the multiplexers switch back to ordinary operation. Lowering MR will cause another increment cycle.

The incrementer described above can be expanded to add pairs of words. One field of the associative memory is used as an accumulator (A), another as a register (R), and a third field contains a Carry bit (C). The R holds one of the addends, the A-field holds the other addend and it will contain the sum on completion of the process.

TABLE II

PRESENT STATE			NEW STATE		OPERATION
A_n	R_n	C	A_n	C	
0	0	0	0	0	Do nothing
0	0	1	1	0	$A_n \rightarrow 1$, $C \rightarrow 0$
0	1	0	1	0	$A_n \rightarrow 1$
0	1	1	0	1	Do nothing
1	0	0	1	0	Do nothing
1	0	1	0	1	$A_n \rightarrow 0$
1	1	0	0	1	$A_n \rightarrow 0$, $C \rightarrow 1$
1	1	1	1	1	Do nothing

The scheme shown in *Table II* is identical to that used in the incrementer, but operates over three bits instead of two.

A system similar to the incrementer is set up to sample for each of the four conditions requiring changes and write the correct results in each bit. Four Time Slots will now be required for each bit in the words to be added.

The associative process can greatly enhance speed when a large number of word pairs must be added. However, for additions of only a few words, the process described above is expensive and cumbersome. For those cases, addition could be more efficiently accomplished using other methods.

CONTROL APPLICATION

The associative memory can also be used to detect check points in numerically controlled processes. In such applications, it is used essentially as a series of comparators, comparing the output of the control unit with some preset numbers.

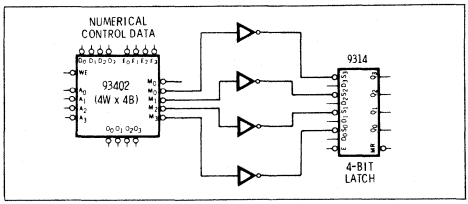


Fig. 12. Use of the associative memory as a limit detector.

One application is the use of the memory as a limit detector with hysteresis. The limits are written into the memory and the memory will signal when the limit is reached. The limit signal might be held in a 9314 latch, as shown in *Figure 12*. If this kind of system is used, it is necessary that the control word exactly match the word stored in the memory. Thus the numerical control system should be of a type that proceeds sequentially rather than jumping from one number to another.

CONCLUSION

The 93402 is a versatile associative memory which can be easily expanded into a large memory system. It can be used either as an extremely high speed scratch pad in general-purpose computers or as a storage device in special-purpose instruments that must call up particular information on request.

The 93402 can replace a large number of logical devices with a single-package unit, and can provide substantial savings in cost and equipment size wherever the associative function is required.

DIGITAL DISPLAY SYSTEMS

CONTENTS

INTRODUCTION

Automation continues to demand better display readout devices for desk calculators, digital VTOMs, frequency meters, counters, etc. The result is a wide variety of shapes, sizes, input drive requirements and principles of operation of display units. Most electronic readout devices use neon, fluorescent, incandescent, electroluminescent or gallium arsenide methods to form or illuminate the readout display. A discussion and comparison of several decoder/drivers and methods of multiplexing most of the more common displays is the basis for this paper.

A display decoder/driver takes 4-bit (usually BCD) input data and decodes it into the correct format for the particular display being activated. Outputs must be of sufficient current and voltage and correct polarity to drive the display. Such decoder/drivers are now available for many display types in a single integrated circuit. Decoder/drivers for the more popular commercially available neon, fluorescent and incandescent displays are covered in this paper. Descriptions of driving the displays in multiplexed and nonmultiplexed modes are included. The multiplexing techniques (sometimes referred to as time-share) are applicable to other display systems including cathode ray tubes and mechanical devices with the correct input/output interface.

DISPLAYS

One of the oldest electronic numeric readouts is the one-of-ten display such as the NIXIE* tube. An inherent disadvantage is that each of the numbers within the tube is not on the same plane. This is very evident when a number of displays are used side by side. Additionally, the red illumination of the displays makes it difficult to change the readout color. Also, they are difficult to multiplex because of relatively high voltage requirements.

Seven segment numeric displays are becoming more popular due to their lower prices and aesthetically pleasant numeral format. Fluorescent seven segment displays are perhaps the easiest to drive and the most economical to purchase. Their relatively low current and voltage requirements make them easy to multiplex. The spectrum of light output is a wide band in the green region and can be filtered to certain other colors without undue light loss.

Seven segment neon displays are very easy to read and are relatively small. They do have a disadvantage in that a relatively high anode potential is required making them difficult to multiplex.

Seven segment incandescent displays have the advantage that they can be made relatively large, colored and bright, depending upon the lamps used for the display. Their main disadvantage is that incandescent lamps have relatively low reliability; segment failure is common. Also, multiplexing incandescent readouts does not offer much advantage in parts count as each of the display segments requires a diode to stop sneak electrical paths.

A number of solid state display devices using gallium arsenide light emitting diodes are available. These displays are normally very small, with character heights of from less than 1/8" to slightly over 1/4". Light emitting diode displays are bright red and offer the advantage of reliable operation under severe mechanical conditions.

A cross reference of most of the decoder/driver circuits and display types is on page 4 in the form of a table. This includes information about the manufacturers of the various types of displays.

*NIXIE is a registered trademark of Burroughs Corporation.

FAIRCHILD
SEMICONDUCTOR

TABLE I DECODER/DRIVER LOGIC TABLE

9307 • 9317 • 9327 • 9337 • 9357A (5446–7446) 9357B (5447–7447)
9358 (5448 7448) • 9359 (5449 7449) DECODER DRIVERS

The seven segment decoder/driver accepts a 4 Bit BCD 8421 code input and produces the appropriate outputs for selection of segments in a seven segment matrix display used for representing the decimal numbers 0–9. The seven outputs (a, b, c, d, e, f, g) of the decoder select the corresponding segments in the matrix shown below. The numeric designations chosen to represent the decimal numbers are shown in the truth tables.

The device has provision for automatic blanking of the leading and/or trailing edge zeroes in a multidigit decimal number, resulting in an easily readable decimal display, conforming to normal writing practice. In an eight digit mixed integer fraction decimal representation, using the automatic blanking capability, (0060.0300) would be displayed as (60.03). Leading edge zero suppression is obtained by connecting the Ripple Blanking Output ($\overline{RBO}$) of a decoder to the Ripple Blanking Input ($\overline{RBI}$) of the next lower stage device. The most significant decoder stage should have the $\overline{RBI}$ input grounded. Since the suppression of the least significant integer zero in a number is not usually desired, the $\overline{RBI}$ input of this decoder stage should be left open. A similar procedure for the fractional part of a display will provide automatic suppression of trailing edge zeroes.

The decoder has an active low input Display Test which overrides all other input combinations and enables a check to be made on possible display malfunctions. The $\overline{RBO}$ terminal of the decoder can be OR-tied with a modulating signal via isolating buffer for either pulse duration intensity modulation or display blanking.

9307 DECODER

SEGMENT DESIGNATION

SEGMENTS ALL ACTIVE HIGH OUTPUTS

TRUTH TABLE

LT	RBI	A	B	C	D	a	b	c	d	e	f	g	RBO	DECIMAL OR FUNCTION
L	X	X	X	X	X	H	H	H	H	H	H	H	H	
H	L	L	L	L	L	L	L	L	L	L	L	L	L	0
H	H	L	L	L	L	H	H	H	H	H	H	L	H	0
	X	H	L	L	L	L	H	H	L	L	L	L	H	1
		L	H	L	L	H	H	L	H	H	L	H	H	2
		H	H	L	L	H	H	H	H	L	L	H	H	3
		L	L	H	L	L	H	H	L	L	H	H	H	4
		H	L	H	L	H	L	H	H	L	H	H	H	5
		L	H	H	L	H	L	H	H	H	H	H	H	6
		H	H	H	L	H	H	H	L	L	L	L	H	7
		L	L	L	H	H	H	H	H	H	H	H	H	8
		H	L	L	H	H	H	H	H	L	H	H	H	9
		L	H	L	H	L	L	L	H	H	L	H	H	10
		H	H	L	H	L	L	L	H	L	L	H	H	11
		L	L	H	H	L	H	H	L	L	H	H	H	12
		H	L	H	H	H	L	H	H	L	H	H	H	13
		L	H	H	H	L	L	L	H	H	H	H	H	14
H	X	H	H	H	H	L	L	L	L	L	L	L	H	15

9317 9337

SEGMENT DESIGNATION

SEGMENTS ALL ACTIVE LOW OUTPUTS

TRUTH TABLE

$\overline{LT}$	$\overline{RBI}$	A_0	A_1	A_2	A_3	$\overline{a}$	$\overline{b}$	$\overline{c}$	$\overline{d}$	$\overline{e}$	$\overline{f}$	$\overline{g}$	$\overline{RBO}$	DECIMAL OR FUNCTION
L	X	X	X	X	X	L	L	L	L	L	L	L	H	
H	L	L	L	L	L	H	H	H	H	H	H	H	L	0
H	H	L	L	L	L	L	L	L	L	L	L	H	H	0
	X	H	L	L	L	H	H	H	H	L	L	H	H	1
		L	H	L	L	L	L	H	L	L	H	H	H	2
		H	H	L	L	L	L	L	L	H	H	L	H	3
		L	L	H	L	H	L	L	H	H	L	L	H	4
		H	L	H	L	L	H	L	L	H	L	L	H	5
		L	H	H	L	H	H	L	L	L	L	L	H	6
		H	H	H	L	L	L	L	H	H	H	H	H	7
		L	L	L	H	L	L	L	H	H	L	L	H	8
		H	L	L	H	L	L	L	H	H	L	H	H	9
		L	H	L	H	H	H	H	H	H	H	H	L	10
		H	H	L	H	H	H	H	H	H	H	H	L	11
		L	L	H	H	H	H	H	H	H	H	H	L	12
		H	L	H	H	H	H	H	H	H	H	H	L	13
		L	H	H	H	H	H	H	H	H	H	H	L	14
H	X	H	H	H	H	H	H	H	H	H	H	H	L	15

9327

SEGMENT DESIGNATION

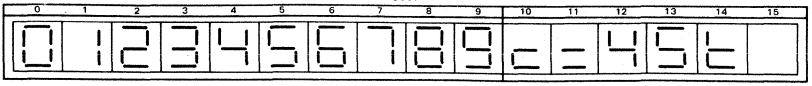
SEGMENTS ARE ACTIVE HIGH OUTPUTS

H = HIGH VOLTAGE LEVEL
L = LOW VOLTAGE LEVEL
X = DON'T CARE CONDITION

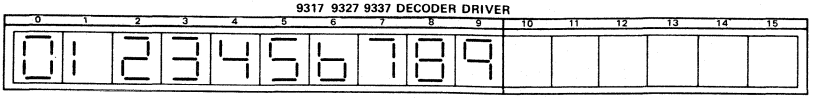
TRUTH TABLE

$\overline{LT}$	$\overline{RBI}$	A	B	C	D	a	b	c	d	e	f	g	$\overline{RBO}$	DECIMAL OR FUNCTION
L	X	X	X	X	X	H	H	H	H	H	H	H	H	
H	L	L	L	L	L	L	L	L	L	L	L	L	L	0
H	H	L	L	L	L	H	H	H	H	H	H	L	H	0
	X	H	L	L	L	L	L	L	L	H	H	L	H	1
		L	H	L	L	H	H	L	H	H	L	H	H	2
		H	H	L	L	H	H	H	H	L	L	H	H	3
		L	L	H	L	L	H	H	L	L	H	H	H	4
		H	L	H	L	H	L	H	H	L	H	H	H	5
		L	H	H	L	L	L	H	H	H	H	H	H	6
		H	H	H	L	H	H	H	L	L	L	L	H	7
		L	L	L	H	H	H	H	H	H	H	H	H	8
		H	L	L	H	H	H	H	L	L	H	H	H	9
		L	H	L	H	L	L	L	H	H	L	L	L	10
		H	H	L	H	L	L	L	H	L	L	L	L	11
		L	L	H	H	L	L	L	L	H	H	L	L	12
		H	L	H	H	L	L	L	L	L	L	L	L	13
		L	H	H	H	L	L	L	L	L	L	L	L	14
H	X	H	H	H	H	L	L	L	L	L	L	L	L	15

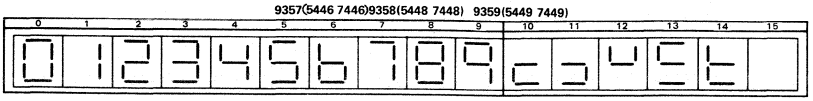
9307



9317 9327 9337 DECODER DRIVER

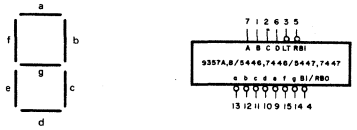


9357(5446 7446)9358(5448 7448) 9359(5449 7449)



9357A(5446 7446)
9357B(5447 7447)

SEGMENT DESIGNATION

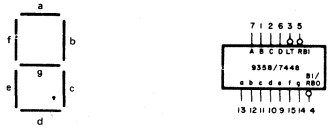


TRUTH TABLE

$\overline{LT}$	$\overline{RBI}$	A_0	A_1	A_2	A_3	$\overline{a}$	$\overline{b}$	$\overline{c}$	$\overline{d}$	$\overline{e}$	$\overline{f}$	$\overline{g}$	BI OR $\overline{RBO}$	DECIMAL OR FUNCTION
L	X	X	X	X	X	L	L	L	L	L	L	L	H	TEST
H	L	L	L	L	L	H	H	H	H	H	H	H	L	BLANK
H	H	L	L	L	L	L	L	L	L	L	L	H	H	0
	X	H	L	L	L	H	L	L	H	H	H	H	H	1
		L	H	L	L	L	L	H	L	L	H	L	H	2
		H	H	L	L	L	L	L	L	H	L	L	H	3
		L	L	H	L	H	L	L	H	H	L	L	H	4
		H	L	H	L	L	H	L	L	H	L	L	H	5
		L	H	H	L	H	H	L	L	L	L	L	H	6
		H	H	H	L	L	L	L	H	H	H	H	H	7
		L	L	L	H	L	L	L	L	L	L	L	H	8
		H	L	L	H	L	L	L	H	H	L	L	H	9
		L	H	L	H	H	H	H	L	L	H	L	H	10
		H	H	L	H	H	H	L	H	H	L	L	H	11
		L	L	H	H	H	L	H	H	H	L	L	H	12
		H	L	H	H	L	H	H	L	H	L	L	H	13
		L	H	H	H	H	H	H	L	L	L	L	H	14
H	X	H	H	H	H	H	H	H	H	H	H	H	H	15

9358(5448 7448)

SEGMENT DESIGNATION



TRUTH TABLE

$\overline{LT}$	$\overline{RBI}$	A	B	C	D	a	b	c	d	e	f	g	BI OR $\overline{RBO}$	DECIMAL OR FUNCTION
L	X	X	X	X	X	H	H	H	H	H	H	H	H	TEST
H	L	L	L	L	L	L	L	L	L	L	L	L	L	BLANK
H	H	L	L	L	L	H	H	H	H	H	H	L	H	0
	X	H	L	L	L	L	H	H	L	L	L	L	H	1
		L	H	L	L	H	H	L	H	H	L	H	H	2
		H	H	L	L	H	H	H	H	L	L	H	H	3
		L	L	H	L	L	H	H	L	L	H	H	H	4
		H	L	H	L	H	L	H	H	L	H	H	H	5
		L	H	H	L	L	L	H	H	H	H	H	H	6
		H	H	H	L	H	H	H	L	L	L	L	H	7
		L	L	L	H	H	H	H	H	H	H	H	H	8
		H	L	L	H	H	H	H	L	L	H	H	H	9
		L	H	L	H	L	L	L	H	H	L	H	H	10
		H	H	L	H	L	L	H	H	L	L	H	H	11
		L	L	H	H	L	H	H	H	L	L	H	H	12
		H	L	H	H	H	L	H	H	L	H	H	H	13
		L	H	H	H	H	H	L	L	H	H	H	H	14
H	X	H	H	H	H	L	L	L	L	L	L	L	L	15

9359(5449 7449)

SEGMENT DESIGNATION

THE 9359/7449 IS AN OPEN COLLECTOR VERSION OF THE 9358/7448 AND IS AVAILABLE IN FLAT PACK ONLY

H = HIGH VOLTAGE LEVEL
L = LOW VOLTAGE LEVEL
X = DON'T CARE CONDITION

TRUTH TABLE

$\overline{BI}$	A	B	C	D	a	b	c	d	e	f	g	DECIMAL OR FUNCTION
L	X	X	X	X	L	L	L	L	L	L	L	BLANK
H	L	L	L	L	H	H	H	H	H	H	L	0
	H	L	L	L	L	H	H	L	L	L	L	1
	L	H	L	L	H	H	L	H	H	L	H	2
	H	H	L	L	H	H	H	H	L	L	H	3
	L	L	H	L	L	H	H	L	L	H	H	4
	H	L	H	L	H	L	H	H	L	H	H	5
	L	H	H	L	L	L	H	H	H	H	H	6
	H	H	H	L	H	H	H	L	L	L	L	7
	L	L	L	H	H	H	H	H	H	H	H	8
	H	L	L	H	H	H	H	L	L	H	H	9
	L	H	L	H	L	L	L	H	H	L	H	10
	H	H	L	H	L	L	H	H	L	L	H	11
	L	L	H	H	L	H	L	L	L	H	H	12
	H	L	H	H	H	L	L	H	H	H	H	13
	L	H	H	H	L	L	L	L	L	L	H	14
H	H	H	H	H	L	L	L	L	L	L	L	15

FAIRCHILD CIRCUIT	TYPE OF DECODER	OUTPUTS			REMARKS	DISPLAYS	MANUFACTURER**
		ACTIVE	VOLTS	mA			
9301	1-of-10	Low	Logic Levels 10 Unit Loads		Drives further logic and discrete transistors for operating lamps, incandescent, neon or CRT displays and relays, etc. Useful for scan decoder in multiplexed systems. Blanks on BCD 10 through 15.	Multiplexed Systems	As Applicable
9307	7-Segment	High	Logic Levels 10 Unit Loads		Drives discrete transistors for all types of 7-segment displays, LEDs or CRT displays. RBI for suppression of leading edge zeros. Blanks on BCD 15 or RBO tied low.	All Seven Segment Displays (with external drivers)	As Applicable
9315 (7441)	1-of-10	Low	0–65	7	Drives gas filled (neon) cold cathode displays; NIXIES†, all types except alpha/numeric. Scan decoder for multiplexed fluorescent displays. Blanks on BCD 12 and 13 only.	ZM 1000 NL 5750, NL 940	Amperex – Slaytorsville, Rhode Island Burroughs – Plainsfield, New Jersey National Electronics – Japan
9317A B C D	7-Segment	Low	30 20 30 20	40 40 20 20	Drives incandescent displays and light emitting diode displays	MS 400B, 4100, 250A and MSM series 106N, 110	Alco – Lawrence, Massachusetts Dialight Corp. – Brooklyn, New York EDP – Orlando, Florida James Electronics – Chicago, Illinois Luminetics – Pompano Beach, Florida Mesa – Bristol, Pennsylvania Pinlight – Fairfield, New Jersey
9325 (54141/ 74141)	1-of-10	Low	55	7	Drives gas filled (neon) cold cathode displays, NIXIES† – all types except alpha/numeric. Scan decoder for multiplexed fluorescent displays. Full decoding is provided for all possible input states. For Binary inputs 10 through 15, all outputs are inactive.	ZM 1000 NL 5750, NL 940, etc. (All cold cathode)	Amperex – Slaytorsville, Rhode Island Burroughs – Plainsfield, New Jersey National Electronics – Japan Raytheon – Quincy, Massachusetts
9327A 9327B	7-Segment	High	55 25	7 5	Drives fluorescent displays	Legitron DG10, 12H, 19C NEC DG12E/LD915, DG10E/LD938 Digivac Fluorotron	General Electric – Owensboro, Kentucky Legi Electronics – Los Angeles, California (Iseden – Japan) Nippon Electric Co. – Japan (Los Angeles, California) Tung-Sol Div. of Wagner – Livingston, New York Sylvania – Seneca Falls, New York
9331A (7445) 9331B (74145)	1-of-10	Low	30 15	80 80	High Current lamp or relay driver. It can be used with pullup resistor and outputs "OR" tied to provide a function generator.	High Current 1-of 10 incandescent projection displays	As Applicable
9337	7-Segment	Low	60	10	Drives 7-Segment neon displays. It can drive seven individual neon lamps such as NE 2 in 7 for display.	Elfin SP 730	Alco – Lawrence, Massachusetts Mesa – Bristol, Pennsylvania Sperry Information Systems Div. – Scottsdale, Arizona
9352 (5442/ 7442)	1-of-10	Low	Logic Levels 10 Unit Loads		Drives further logic and discrete transistors for operating lamps, incandescent, neon or CRT displays and relays, etc. Useful for scan decoder in multiplexed systems. Blanks BCD 10 through 15.	Multiplexed Systems	As Applicable
9357A (5446/ 7446) 9357B (5447/ 7447)	7-Segment	Low	30 15	20 20	Drives incandescent and common anode light emitting diode displays,* any 7-segment display within current rating.	MS 250A 710 106N M645, P645	Alco – Lawrence, Massachusetts Dialco – Brooklyn, New York EDP – Orlando, Florida Luminetics – Pompano Beach, Florida Pinlite – Fairfield, New Jersey
9358 (5448/ 7448)	7-Segment	High	Logic Levels 10 Unit Loads		Drives discrete drive transistors for all types of 7-segment displays. Blanks on BCD 15 only.	All Seven Segment Displays (with external drivers)	As Applicable
9359	7-Segment	High	5.5	10	Open collector. No RBI or RBO. Has blanking input for total display blanking. Flat pack only.	All Seven Segment Displays	As Applicable

*Light emitting diode display selection guide is on page 16.

**This is not intended to be a complete listing of all manufacturers of display tubes.

†NIXIE is a registered trademark of Burroughs Corporation.

TABLE II DECODER AND DISPLAY TABLE

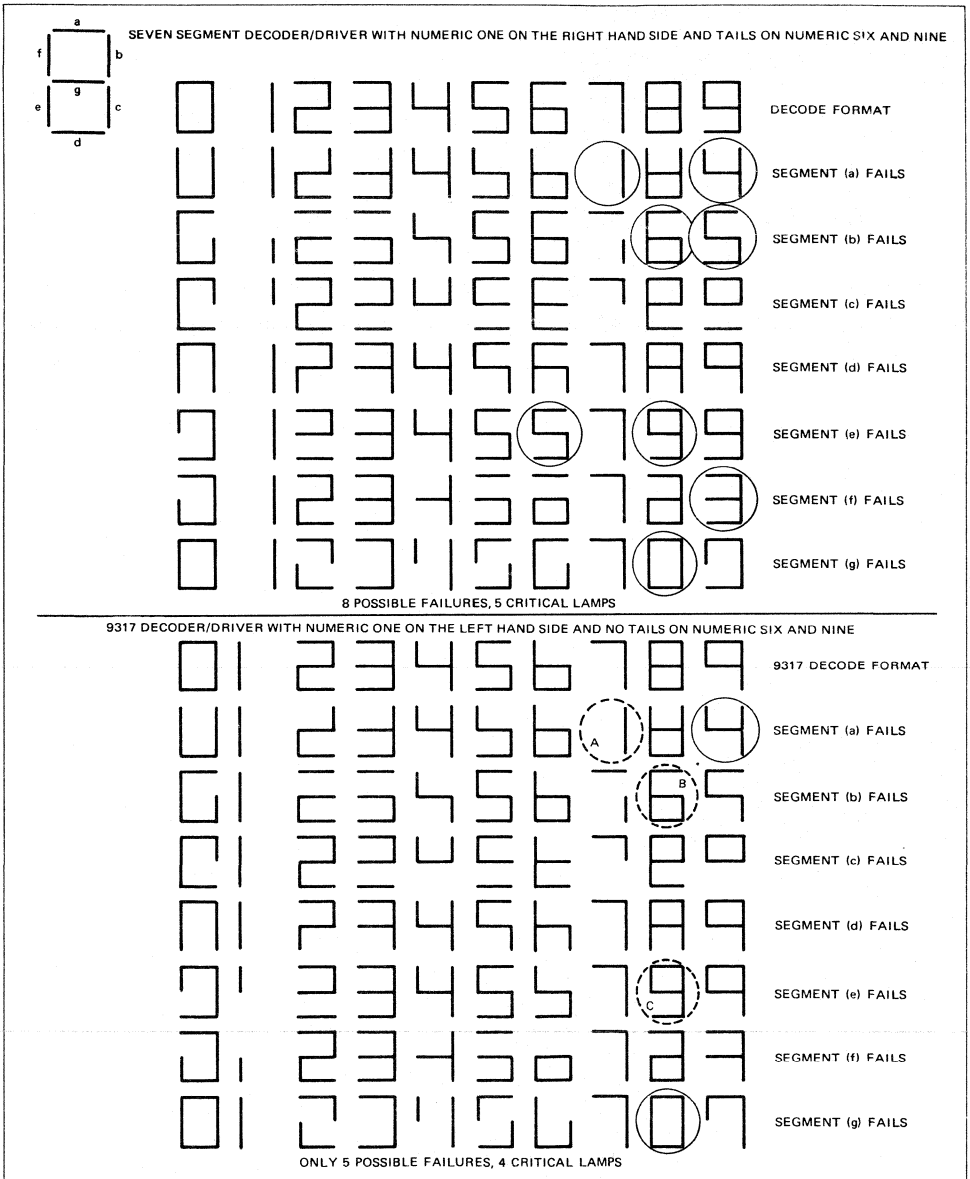


Fig. 1. Critical lamp considerations for seven segment lamp displays.

SEVEN SEGMENT DECODER/DRIVER FORMAT

Seven segment decoder/driver logic is derived from three logic decode formats. Output drive capability and polarity are adjusted to suit the display device. The decoder/drivers below are listed by group; each group uses its own logic decode format. Refer to Table I.

Group 1. 9307
Group 2. 9317, 9327, 9337
Group 3. 9357 (7445 & 7446), 9358 (7448), 9359 (7449)

The decode format of the 9317 conforms to military specifications for seven segment displays. This specification is primarily concerned with erroneous readout due to lamp segment failure. The elimination of the tails on the six and nine provides the greatest single contribution to reliability (Figure 1). Placing the decimal one on the left hand segments also increases reliability. This is because the distribution of segment use for all ten numerals is more equal. Note figures below.

LAMP SEGMENT USED	SEGMENT USE DISTRIBUTION WITH NUMERIC ONE POSITION ON . . .	
	L.H. SIDE	R.H. SIDE
B	7	8
C	8	9
E	5	4
F	7	6

Figure 1 shows possible failures and critical lamp considerations for both formats (decimal one on right segments with tails on six and nine and decimal one on left segments without tails on six and nine). Note that on the bottom half of the figure, for the 9317 decoder driver, dotted surrounds show actual numerics even with segment failures but the numeric formats are wrong. Thus, there are actually only two possible failures and two critical lamps if the viewer realizes that numbers 1, 6 and 9 are in the wrong format. Considering all *readable* numerics, there are five failures and four critical lamps.

RB_I/RB_O CAPABILITIES

The RB_O has two functions. It can be used as an active low output to detect a BCD zero when RB_I is low. With the 9317, 9327 and 9337, RB_O is low for any codes above BCD 9, regardless of the state of RB_I. For certain applications, this feature can be utilized for detecting or blanking illegal input codes.

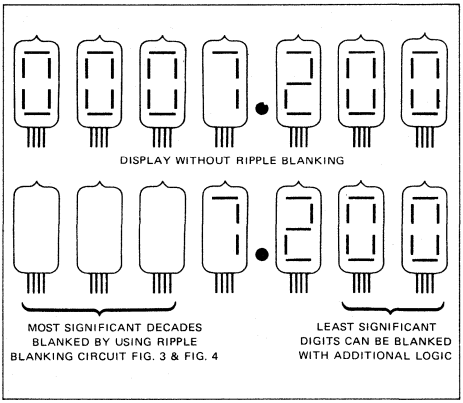


Fig. 2. Ripple blanking.

The RB_O can also be used as an OR tied input for complete display blanking or for controlling the brightness of the display by applying pulse duration intensity modulation. The unit used for the OR tie should be an open collector TTL device or a DTL unit (Figure 3), or a discrete transistor (Figure 4).

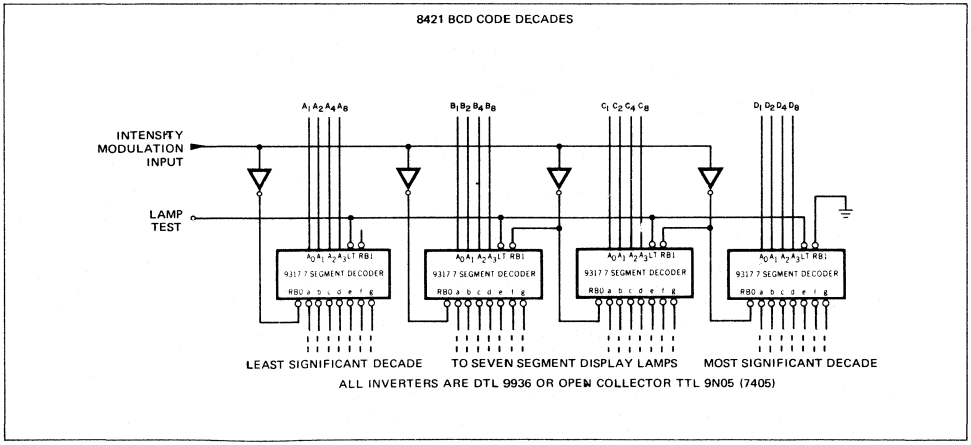


Fig. 3. Four decade seven segment integer display scheme incorporating automatic blanking of leading edge zeros and intensity modulation.

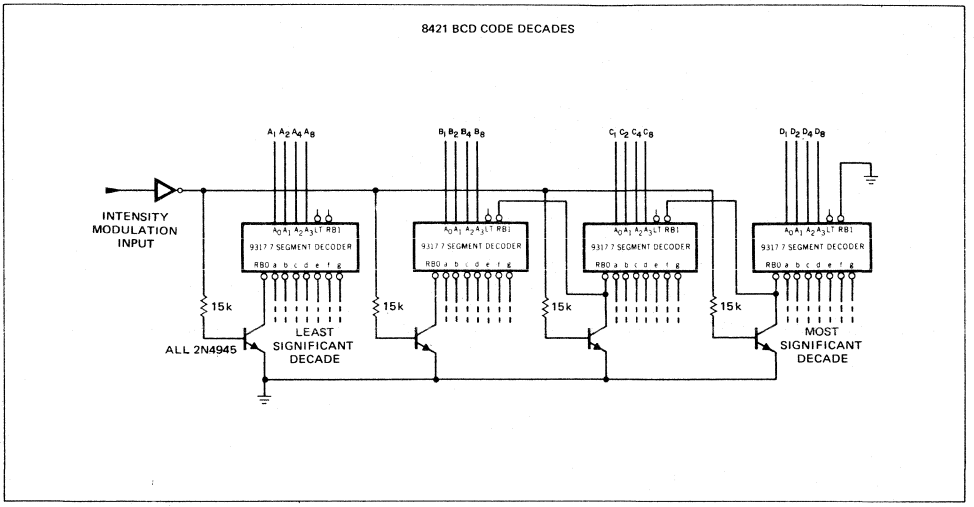


Fig. 4. Display scheme as in Figure 3 but with a TTL device and discrete transistor for the OR tie.

SEVEN SEGMENT INCANDESCENT DISPLAYS

Seven segment incandescent displays are possibly the oldest of all digital displays and have been used extensively for many military applications. They are available with character heights from 1/4 inch to several feet in a variety of colors.

Since these displays employ incandescent lamps, high brightnesses can be achieved and they are available in a wide range of voltages and currents. The simplest seven segment display is lamps placed behind seven slots in some opaque material. Some of the more advanced types use fiber optics or light-carrying beams to illuminate the seven segments.

The major disadvantage of incandescent displays is filament failure causing ambiguous readings. This can be minimized by careful selection of character decode format explained on page 6. Also, there are displays available with two lamps per segment, increasing reliability.

Another type of incandescent display is now available utilizing seven filaments in a tube-type glass envelope aligned to form a seven segment display.

MULTIPLEXING SEVEN SEGMENT INCANDESCENT DISPLAYS

Multiplexed incandescent displays receive power in pulses for only a fraction of the complete scan period. For adequate brightness voltage must be increased. The wattage for an incandescent lamp at a stated brightness will remain constant regardless of duty cycle or waveform shape, providing the multiplexing rate is faster than the time-constant of the filament. Power dissipation for a constant load is proportional to the square of the input voltage. Therefore, calculation of the required supply voltage for multiplexed operation is possible.

Multiplexed voltage = $\sqrt{\text{Number of displays}}$ X DC voltage of lamps, i.e., eight digits of multiplexed display readouts – 6.3 volt lamps – $\sqrt{8}$ X 6.3 = 17.5 volts.

This table gives the factors for common numbers of multiplexed units.

UNITS	FACTOR
4 Displays	2 X DC Voltage
6 Displays	2.45 X DC Voltage
8 Displays	2.8 X DC Voltage
10 Displays	3.1 X DC Voltage
12 Displays	3.45 X DC Voltage

Voltage drops across the integrated circuits and switching transistors must be added to the above figures.

The number of discrete devices required in the driving circuits for incandescent displays is an important economic consideration. The circuit shown in Figure 5, using emitter followers for the scan decoder/drivers, offers an economical method since all transistors are of the same low-cost type. Another advantage of this method is that it is easily adapted to drive lamps of other voltages by adjusting R_L of the level conversion transistor. A slight disadvantage is the power loss (75 mW/digit) caused by the two base-emitter drops of driving emitter followers.

A failsafe circuit is important in multiplexed incandescent displays. Even momentary failure causes lamp burnout since the clock applies more than twice the rated voltage. A failsafe circuit is described on page 19.

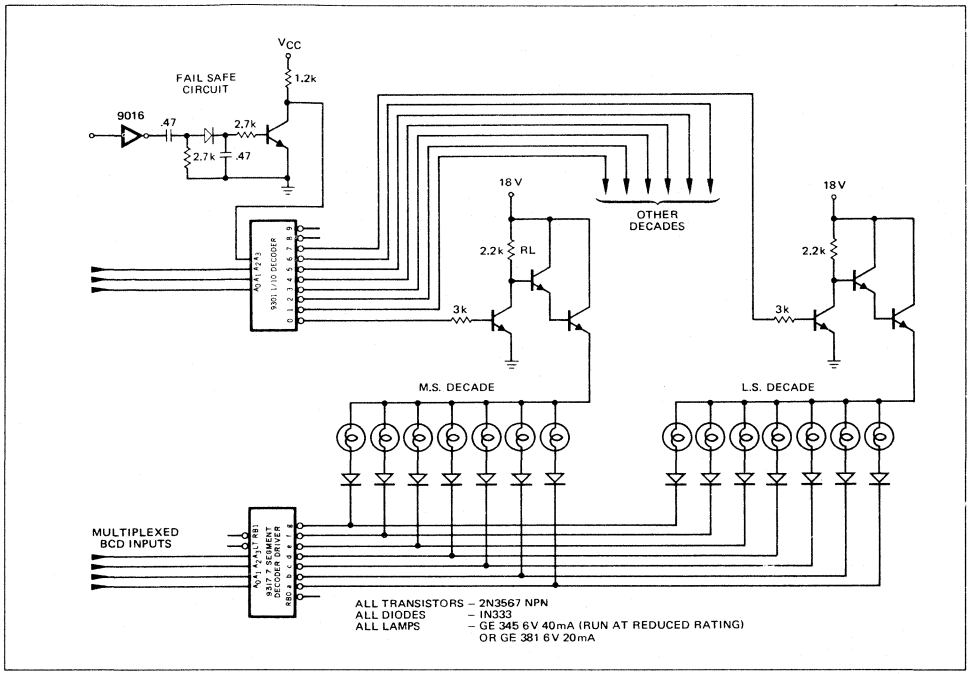


Fig. 5. Multiplexing system for seven segment incandescent displays.

SEVEN SEGMENT FLUORESCENT DISPLAYS

Fluorescent displays are basically vacuum tube diodes or triodes in which the anodes form a visible seven (or eight) segment character. Each anode is coated with phosphor. A positive potential between anode and cathode (filament) accelerates electrons to the anode phosphor causing the anode to glow. The light emitted by the phosphors is a wide spectrum in the blue/green region which can be filtered to certain other colors with little light loss. The cathode (filament) is suspended in front of the display segments and is hardly visible since it is only heated sufficiently for electron emission.

Of the two types of fluorescent displays, triodes are somewhat easier to operate in a multiplexed mode because they have an extra, almost invisible control grid electrode between the filament and the anode. Multiple digit displays of up to ten digits in a single glass and metal enclosure are available using fluorescent triodes.

The main advantages of fluorescent displays are their economy, low power requirements, wide viewing angle, single plane readout and minimum likelihood of erroneous readout with display failures. Two disadvantages are the need for a filament supply and their fragile structure.

DECODER/DRIVERS FOR SEVEN SEGMENT FLUORESCENT DISPLAYS

The selection of a decoder/driver for fluorescent displays should take into account the fact that some displays have altered segment shapes (Figure 6). Some decode formats provided by the decoders generate aesthetically unpleasant characters. Following are some points to note when selecting a fluorescent display decoder/driver. Refer to Figure 7.

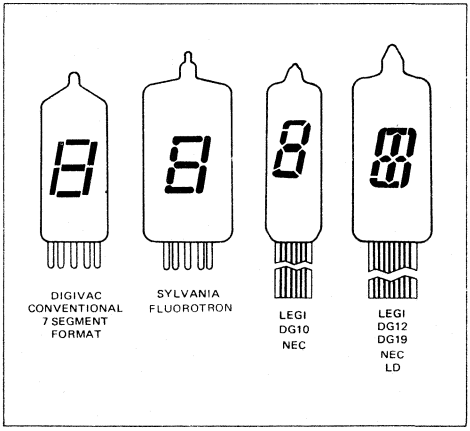


Fig. 6. Several fluorescent display character formats. Note various segment shapes.

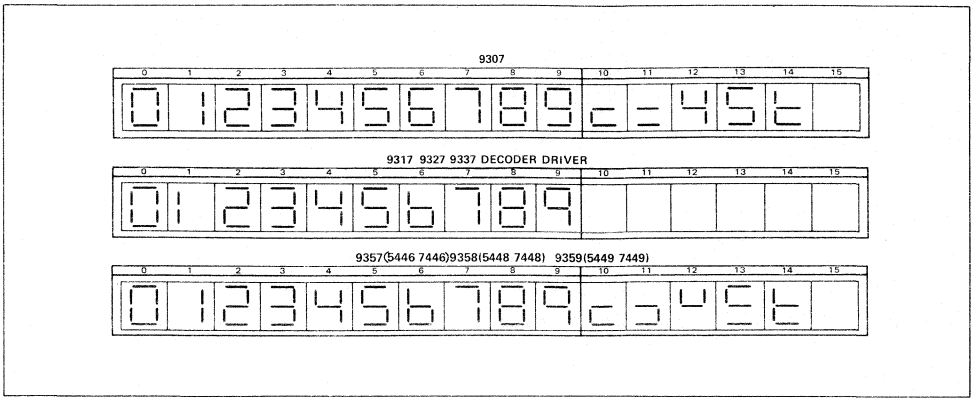


Fig. 7. Three conventional character formats.

9307 The decoder format is acceptable for all types of seven segment displays. The decimal one appears on the right hand segments.

9327 This unit has active outputs and requires seven pull-up resistors. The decimal one uses the left hand segments and there are no tails on the decimal six or nine. It provides a good format for the Digivac display. On other displays, the decimal one is displayed short and the decimal six is deformed.

9358/9359 With these decoders, the decimal six looks poor on all except the Digivac display. The decimal one is shown on the right hand side.

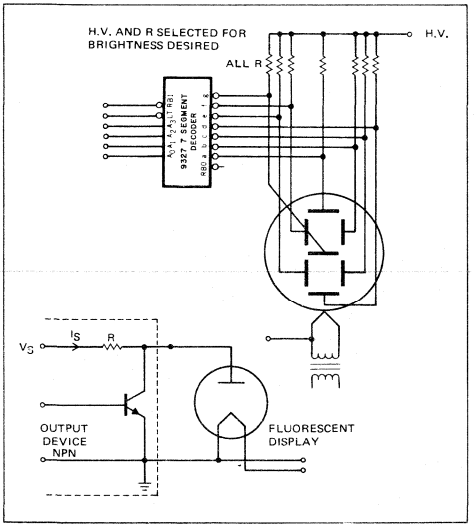


Fig. 8. Load resistor circuit, 9327 decoder/driver.

The 9327 decoder/driver is the only unit which can drive fluorescent displays directly with the aid of pull up resistors. Also, it is the only device suitable for driving individual tubes in a non-multiplexed mode. The active high outputs are high voltage NPN types and require a pull up resistor connected to the high voltage (20V to 60V) positive supply. When these output transistors are on, the appropriate segments are blanked.

The value of the load resistor selected for use with the 9327 is the result of a compromise between power dissipation in the resistor in the on and off states. See Figure 8. When off, the full supply voltage is across the resistor and maximum power is dissipated. While on, the only voltage drop is due to the segment current. There are two versions of the 9327 available with the following differences:

	9327A	9327B
Minimum output high voltage	64V	30V
Output current	7 mA	5 mA
Maximum sinking current low state	7 mA	5 mA

The voltage parameters indicate that the device will not latch up (loss of control) below the rated voltage with a current of 7 mA or 5 mA forced (constant current surge) into the device.

Typical operating conditions for a non-multiplexed fluorescent display are 25 volts and .5 mA to 1 mA per segment. The following example uses a 9327B with a 30V supply.

With a maximum allowable supply of 30V, allowing for a 5V drop, .5 mA current per segment, R = 10 KΩ. For displaying a decimal eight (all segments illuminated) total current = 7 segments X .5 mA = 3.5 mA. This means 105 mW supply power is required. In a blanked display, the current is 3 mA per segment (7) or 21 mA requiring 630 mW supply power. The off to on power ratio is 630:105 or 6:1, worst case.

This would indicate that voltage regulation is required to maintain even brightness for all numerals displayed. A substantially better on to off ratio is obtainable with a 9327A and a higher supply voltage.

With a supply voltage of 60V, allowing for a 35V drop across R, 5 mA per segment = 70 KΩ. When displaying a decimal eight (3.5 mA), W = 60 X 3.5 or 210 mW. With the display blanked, current per segment is .85 mA or 6 mA. W = 60 X 6 or 360 mW. The off to on power ratio is 360:210 or 1.6:1.

The minimum value of R is dictated by the maximum current rating of 9327.

MULTIPLEXING SEVEN SEGMENT FLUORESCENT DISPLAYS

Fluorescent displays are perhaps the easiest of all display devices to multiplex. Fluorescent triodes can offer an advantage with as little as four digits multiplexed. With diodes, six digits can be multiplexed with economic advantages. Fluorescent triode displays have a control grid which is used to turn the display on or off and makes multiplexing easier.

ments keeps them hot during the off period. Each of the display heaters has a transistor (Q) and a diode (D). The display is active when the transistor is conducting. When the transistor is off, active resistor R pulls up the cathode to a +V potential, reverse biasing the diode leaving no potential across the display tube.

The circuit shown in Figure 10 is for eight multiplexed displays. It is easily changed to six digit system by changing the scan counter to a Modulo 6. The filament voltage required when operating in a pulsed mode is expressed as:

$V_P = (\sqrt{N} \times V_F)$ + diode and switching losses

when; V_P = Required voltage

N = Number of parts in scan cycle

V_F = Filament voltages of display

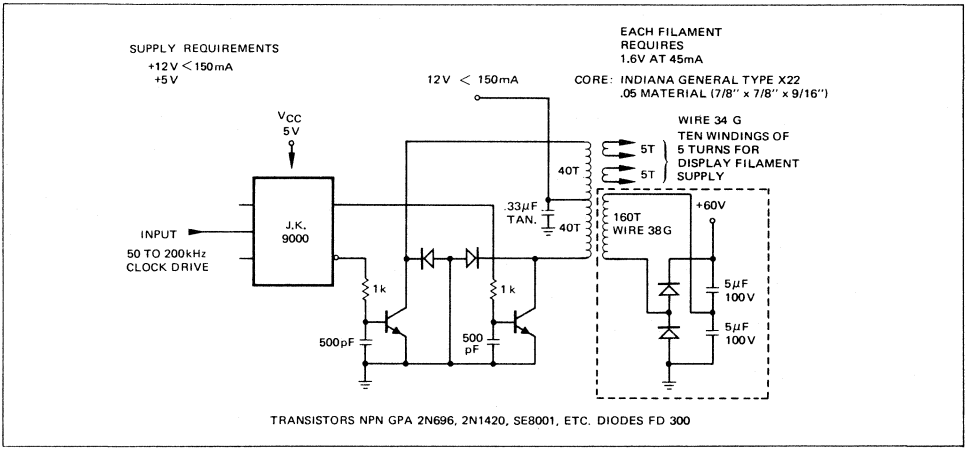


Fig. 9. Invertor supply for fluorescent displays.

MULTIPLEXING SEVEN SEGMENT FLUORESCENT DIODE DISPLAYS

When multiplexing fluorescent diodes, the basic consideration is the isolation of the display filaments while supplying filament power. Three methods can be used.

1. Use a multi secondary filament power transformer with one winding for each digit of the multiplexed display.
2. Use a low power inverter circuit with a multi secondary transformer, one winding for each digit, (Figure 9). This is advantageous in battery operated equipment because it is small and efficient. It can be mounted on the same printed circuit board as the displays.
3. Use transistor switches in series with each filament and with power supplied in pulse form.

The multiplexing system shown in Figure 10 supplies the display heaters from convenient +5V logic levels using a 1/8 (eight digit display) duty cycle. Heater power to the displays is supplied in pulse form and the thermal inertia of the fila-

In the eight digit example shown in the circuit,

V_F = 1.4 volts, diode/switch losses are .9V (.7V diodes, .2V transistors),

$V_P = (\sqrt{8} \times 1.4) + .9$ or 4.9 volts.

A failsafe circuit is added to the most significant digit of the scan decoder to prevent full filament supply voltage from being applied to any one heater should the clock fail. With the counter operating pulses are supplied to diode D_F and the CR resistor network, biasing transistor Q_F on. Failure removes the bias on Q_F and the input code to the scan decoder addresses unused outputs 8 and 9. This circuit operates with clock frequencies up to 20 kHz.

MULTIPLEXING SEVEN SEGMENT FLUORESCENT TRIODE DISPLAYS

The only decoder/driver which provides the correct decode format for fluorescent triode displays is the 9307 and it requires the use of extra drive components. See Figure 11. The

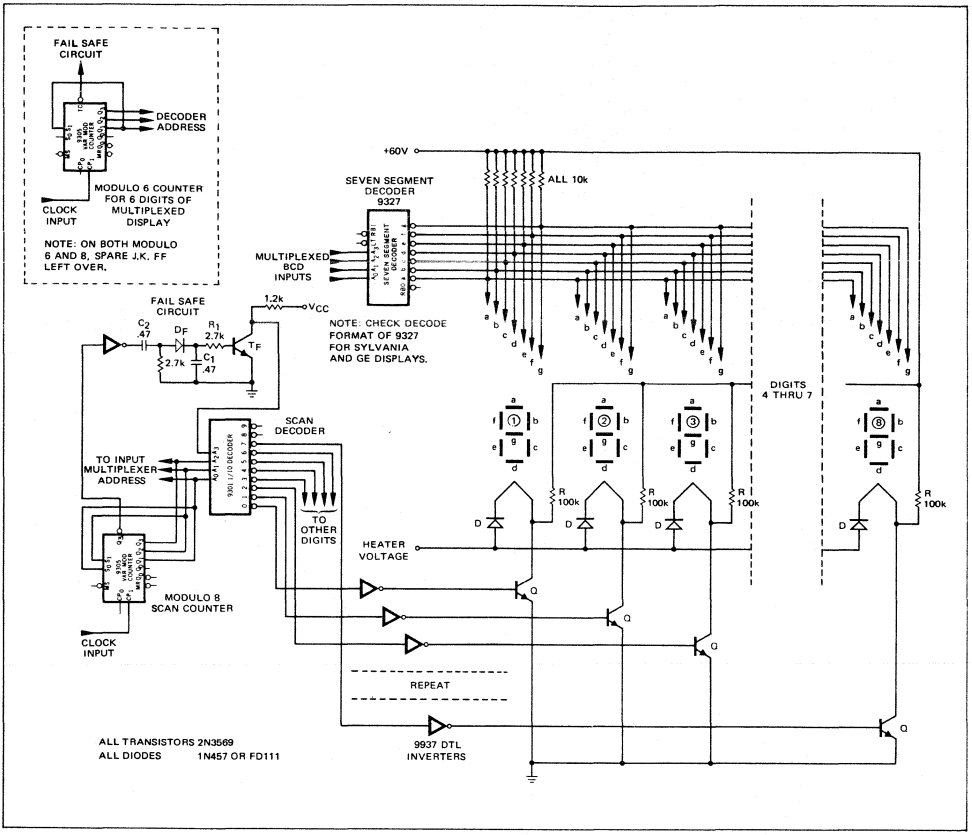


Fig. 10. Multiplexing seven segment fluorescent diode displays.

most economical method uses PNP drive transistors with negative supply voltage. The active high output of the 9307 biases the transistor emitter more negative than the base, turning the transistor on. Diodes D_1 and D_2 insure that the transistor is back biased in the off position. Collector resistors are used so that capacitance charges of the anodes can be leaked off quickly. See Figure 12.

Control grids of fluorescent displays are activated to the same potential as the anodes to obtain full brightness. They are activated by a PNP switch transistor. This is driven directly by the output of the scan decoder 9301 which has active low outputs. The base-emitter current on the PNP transistor is limited by a single resistor in common with all the PNP emitters.

Multiplexed fluorescent displays may be driven from a positive supply using the 9327 decoder/driver and pull up resistors. If the decoding format of the 9327 is unacceptable, a 9307 and two transistors should be used.

A LOW POWER MULTIPLEXING CIRCUIT USING THE 9327

Power is important with battery operation of a readout display. A substantial power saving results when the circuits in Figure 13 are used. When using the 9327 in standard configuration, the worst case power dissipation of the circuit occurs when some or all of the outputs are in low condition (BLANK OR ONE). The power is dissipated in load resistor R_L. When the display is illuminated, a relatively small amount of power is required. Significant power can be saved (at the expense of more parts) by using an emitter follower and increasing the pull up resistors R_L.

EIGHT SEGMENT FLUORESCENT DISPLAYS

A number of fluorescent displays are available in an eight segment format, offering a plus or a minus sign and the decimal one in the center. These displays provide the same numerical readout as seven segment units, except for the numbers one and four, which use the additional center segment (h). In

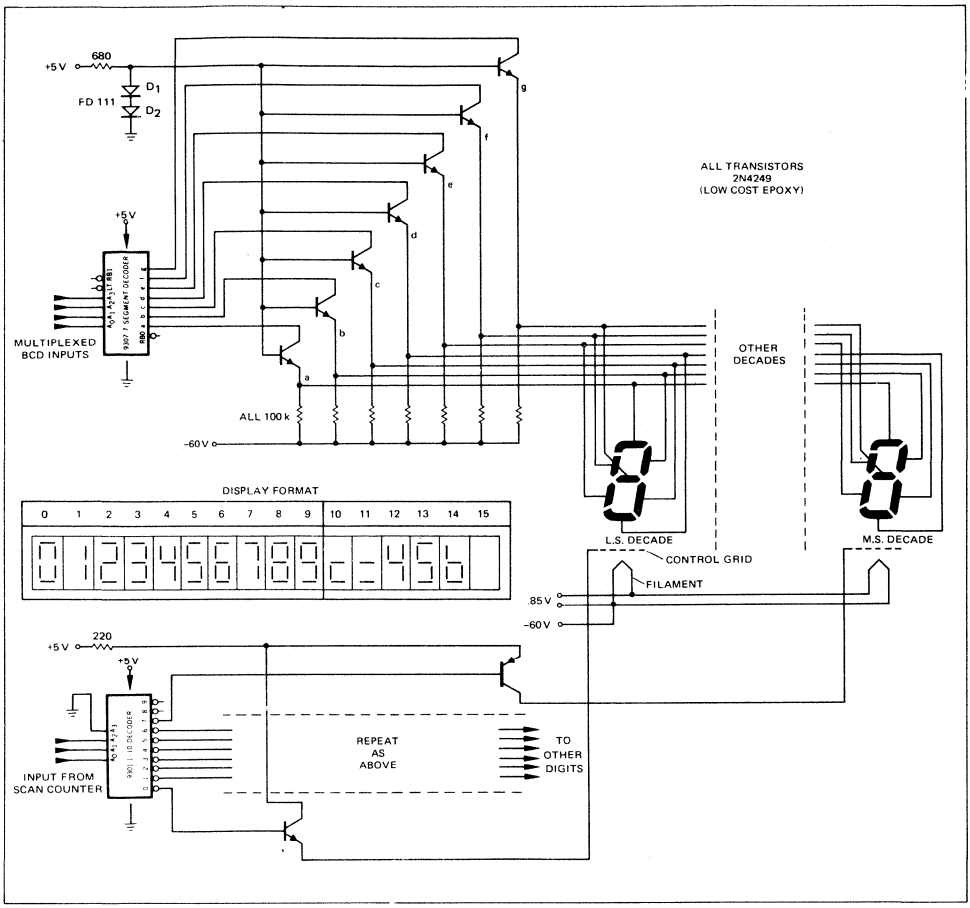


Fig. 11. Multiplexing seven segment fluorescent triode displa, s.

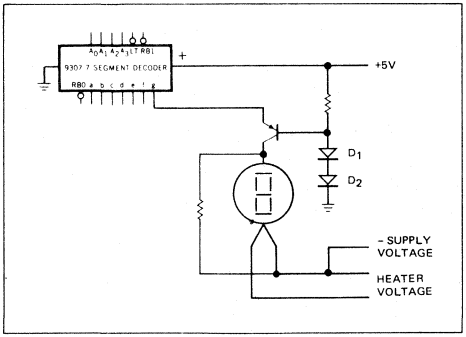


Fig. 12. Basic multiplexing circuit.

operation, Gate G_1 detects the decoder output states $\bar{a}bc$ which are unique for numerals one and four. Refer to Figure 14. G_1 blocks the output to segments a and b through G_2 and G_3. The output of G_1 controls segment h. The plus and minus signs can only be activated with a BCD zero input and RB_I low. RB_O only goes low for BCD zero and RB_I low. This facility is normally used for suppressing most significant decade zeros. In this instance it is used to insure that segments g and h are not activated while displaying decimal numerics.

SEVEN SEGMENT COLD CATHODE OR NEON DISPLAYS

There are two types of cold cathode or neon displays. One type uses seven small neon lamps mounted behind seven slots in an opaque material. The other type (See Figure 15) is a small vacuum tube type envelope enclosing a specially constructed seven segment unit with a character height of 7/16".

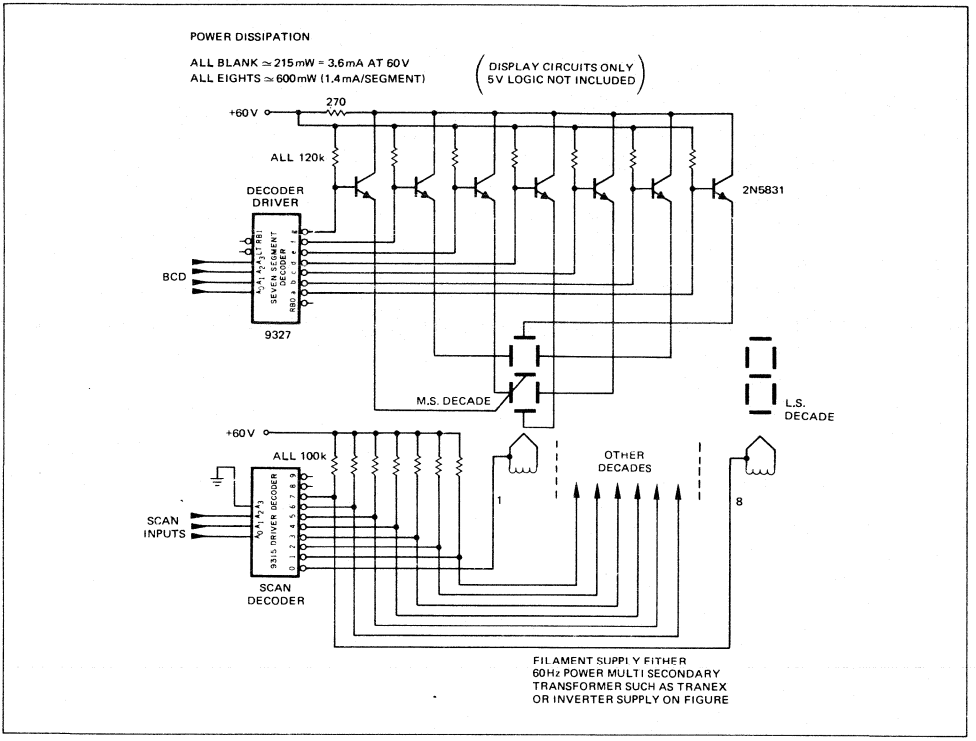


Fig. 13. Low power multiplexing circuit using the 9327 decoder/driver.

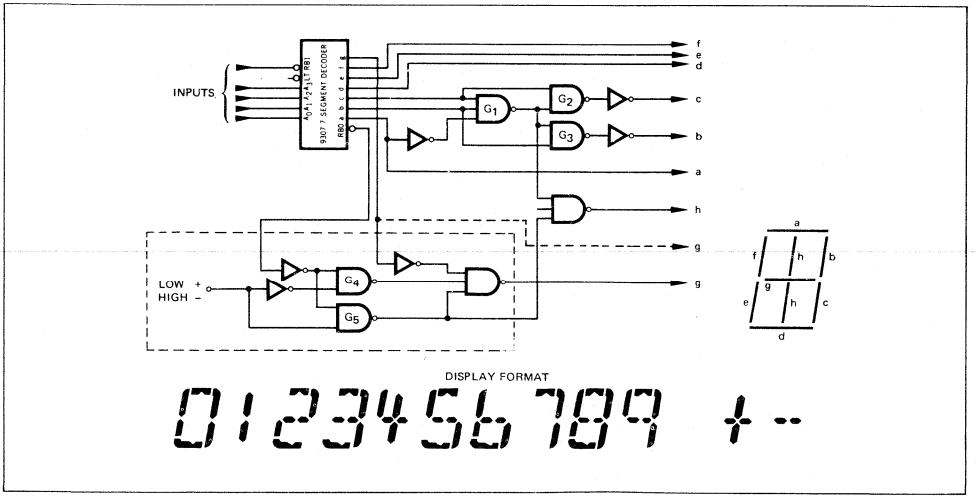


Fig. 14. Eight segment fluorescent display circuit and format.

X

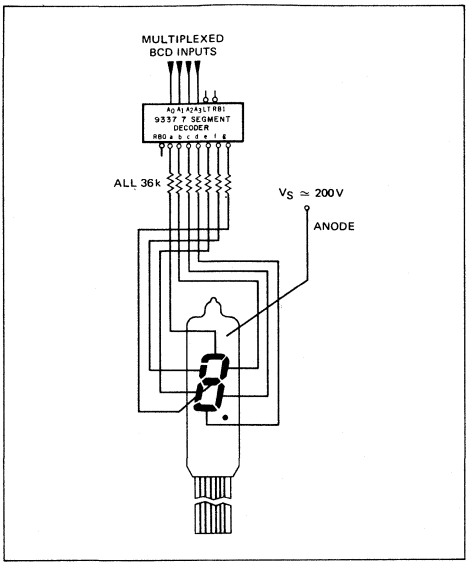


Fig. 15. Seven segment neon display.

This type is the "ELFIN", manufactured by Alco Electronics. Figure 16 shows a multiplex drive circuit for this type of display.

The 9337 decoder/driver is suitable for driving a seven segment neon display or seven individual neon lamps such as the NE 2, forming a seven segment display. The decoding format is the same as that of the 9317.

Seven segment neon displays require a resistor in series with each of the cathodes. A separate resistor is required because the voltage required to start ionization is higher than that required to maintain ionization. Once ionization takes place, the resistor lowers the voltage applied between segment cathode and anode to maintain correct segment current. Seven segment neon displays can be multiplexed with the same technique used for 1-of-10 cold cathode displays described on page 15.

1-OF-10 COLD CATHODE OR NEON DISPLAYS

The Nixie* type cold cathode displays are perhaps the most popular digital readout devices in use in standard equipment such as DVMs, counters, etc. These displays are available in a wide variety of shapes and sizes from miniature sizes with character heights of just over 1/4 inch to jumbo sizes with

*NIXIE is a registered trademark of Burroughs Corporation.

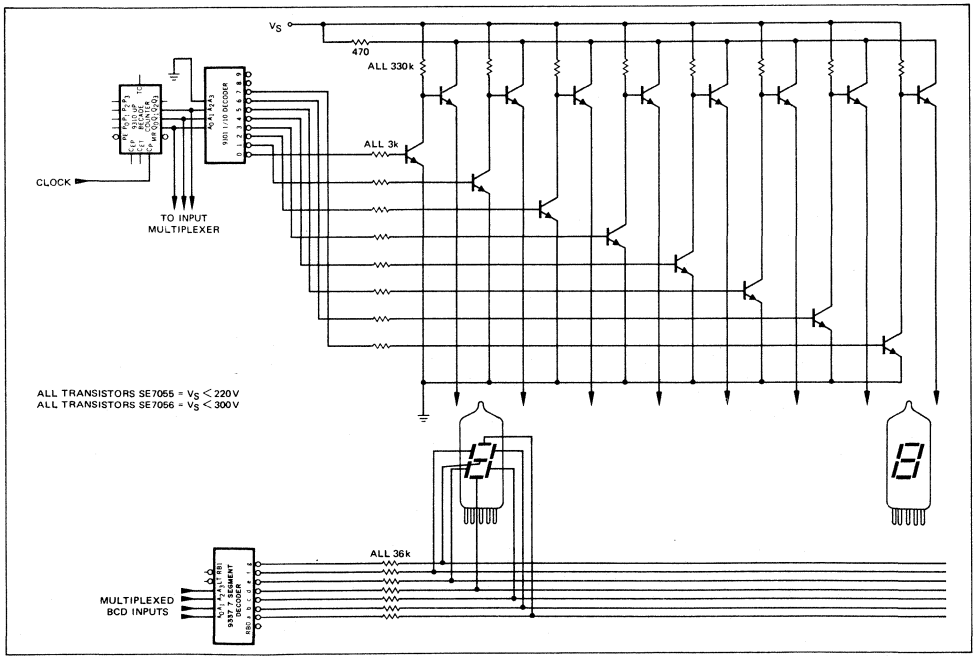


Fig. 16. Multiplex drive circuit for Alco seven segment neon displays.

2 inch characters. Displays are enclosed in a glass tube-type envelope and are available in both side and end viewing types. Special characters are available also.

This type of tube has ten stacked cathodes in the shape of the characters mounted behind an almost invisible anode in a glass envelope filled with neon gas. A high potential between anode and cathode causes ionization and the character glows a dull red. The advantages of this type of display are their availability, reliability, wide range of size and style and their low power consumption.

However, there are some disadvantages. They require high voltage, they are difficult to multiplex, the color is difficult to change and the display readout is not a single plane.

Cold cathode displays require a 1-of-10 decoder/driver with high voltage breakdown NPN transistors on the outputs. The transistors must have low leakage characteristic in the off mode as leakage will cause a background glow. Voltage across the displays after ionization takes place is controlled by a series resistor R. See Figure 17. This resistance value is stated by the display manufacturers.

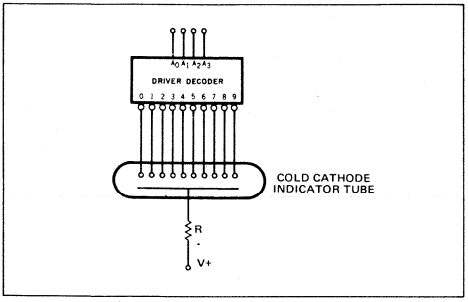


Fig. 17. Basic single cold cathode display.

MULTIPLEXING 1-OF-10 COLD CATHODE OR NEON DISPLAYS

It is necessary to sequentially switch the high voltage anode supply when multiplexing this type of display so that only one digit is addressed at a time. There are two basic approaches for accomplishing this, the series method and the shunt method. Refer to Figures 18, 19A and 19B.

Part count and economy are not considerations; they are similar in both systems. The series method offers an advantage with lower power dissipation but places higher voltage and leakage requirements on the transistors. Leakage is not as important in the shunt method.

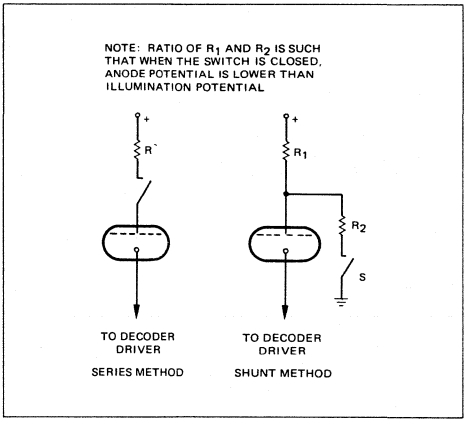


Fig. 18. Basic multiplexing methods for cold cathode displays.

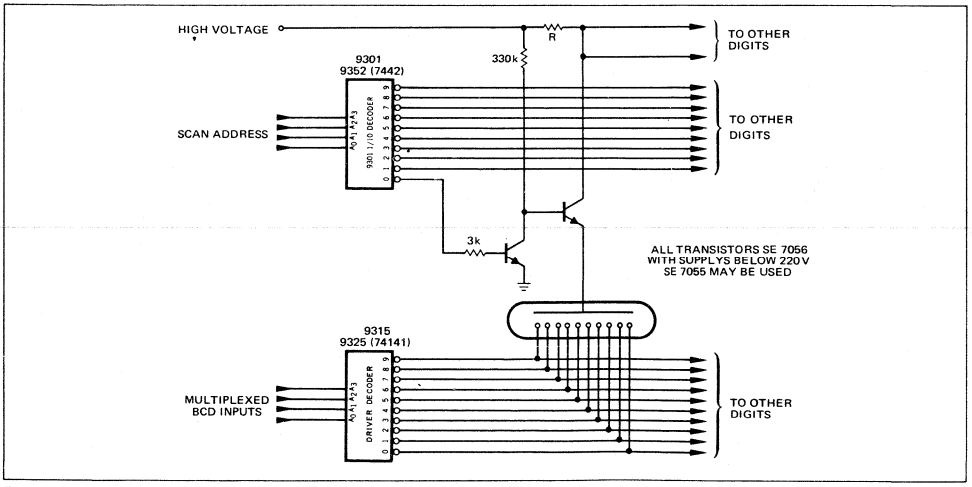


Fig. 19A. Series method, 1-of-10 cold cathode display multiplexing.

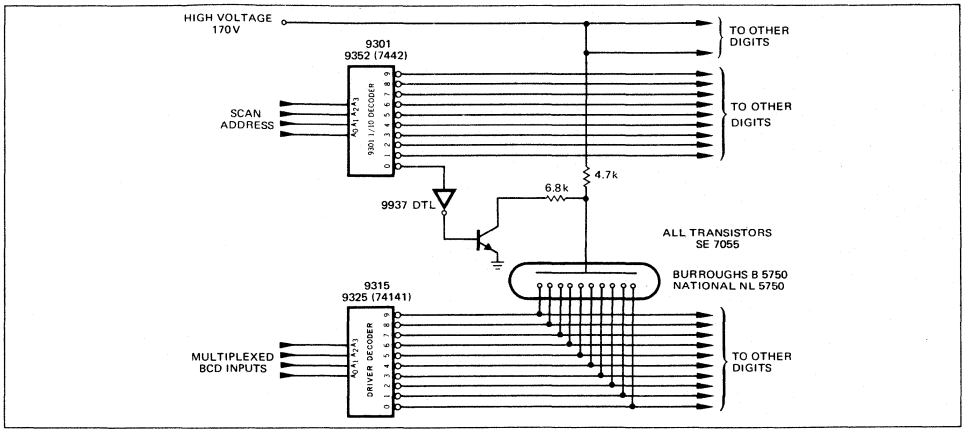


Fig. 19B. Shunt method 1 of 10 cold cathode display multiplexing.

LIGHT EMITTING DIODE DISPLAYS

New light emitting diode (LED) displays are gaining acceptance in many areas. Their small size, single plane readout, TTL compatibility and low power requirements make them attractive for portable display instruments. They are appearing in digital voltmeters, electronic stop watches, thermometers, light meters, radiation meters and similar equipment. Manufacturers of low cost desk calculators favor LED readout for the same reasons. In addition, they are easy to use with MOS calculator integrated circuits.

Low cost LED displays generally have a small character height (approximately 1/8") but appear larger. The largest character

MANUFACTURER	MODEL	SIZE	TYPE	DIGITS	CURRENT (mA)	VOLTAGE	REMARKS	DECODER/DRIVER SINGLE DIGIT	FOR MULTIPLEXING CIRCUIT, SEE
Bowmar Canada Ltd.	R7M Elite	.19	Common Cathode	Single	15	1.4	——	9307 + Resistors	Figure 21
Fairchild Microwave & Optoelectronics	FND10	.122	Common Cathode	Single	5	1.65	——	9307 + Resistors	Figure 21
Hewlett-Packard	HP5082 HP7210 HP7211 HP7212 HP7215 HP7216 HP7217	.1	Common Cathode	 Three Four Five Three Four Five	 5 5 5 5 5 5	 1.65 1.65 1.65 1.65 1.65 1.65	 —— 	 Must be multiplexed	 Figure 21
Litronics	Data Lite 8 10 6	 .24 .27 .6	 Common Anode	 Single	 20 20 20	 1.65 3.4 3.4	 MAN 1 Duplicate	 9317 + Resistors	 Figure 22
Master Speciality	908	.85		Single	50	1.6	——		
Monsanto	MAN 1 MAN 3	.27 .115	Common Anode Common Cathode	Single Single	20 5	3.4 1.7	 —— 	9317 + Resistors	Figure 22 Figure 21
Motorola	MOR 33	.125	Common Cathode	Single	10	1.6	——		Figure 21
Opoca	SLA 1	.33	Common Anode	Single	15	2.2	——	9317 + Resistors	Figure 22
Texas Instruments	TIXL 301 TIXL 302	.1 .25	Common Anode Common Anode	Single 	15 20	1.7 3.4	 MAN 1 Duplicate	9317 + Resistors 9317 + Resistors	Figure 22 Figure 22

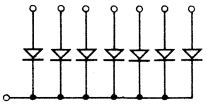
TABLE III LIGHT EMITTING DIODE DISPLAY SELECTION GUIDE

height presently available is about 0.6". The displays are bright red with sharply defined characters. Green and orange displays may be possible in the future. A polarized filter improves viewing under normal light circumstances. See Table III for a list of currently available LED displays.

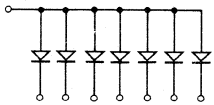
LED displays use either gallium phosphide (GaP) or gallium arsenide phosphide (GaAsP). Both types seem to have equal advantages and disadvantages. They are available in two character formats, a 5 X 7 dot matrix which can display alphanumerics and the lower cost seven segment displays.

Seven segment LED displays use either common anode or common cathode techniques. See Figure 20. Monolithic LED technology (.1" character height) calls for the common cathode. Hybrid construction can be either, but the common cathode seems more popular. With the common cathode method, the decoder/driver must be able to source current into the display. The common anode variety requires the decoder/driver to sink current, which is presently somewhat easier to do.

Electrically, the LED is the same as the familiar solid state diode with its inherent characteristics. Below the knee of the I/V curve they pass little current. Above the knee, current increases linearly with voltage. Thus, uniform brightness of each segment and digit requires a constant current source rather than constant voltage. Light output increases linearly with current for low values until light saturation is reached and further current does not increase light output. Current should be limited to avoid device failure.



COMMON CATHODE

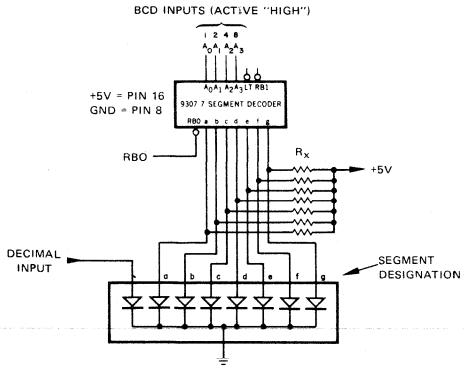


COMMON ANODE

	GaP	GaAsP
1 DIODE	≃ 2.1V	≃ 1.65V
2 DIODES	≃ 4.2V	≃ 3.4V

TYPICAL APPLICATION

(UTILIZING FAIRCHILD TYPE 9307 BCD-TO-SEVEN SEGMENT DECODER/DRIVER.)



TO CALCULATE EXTERNAL PULL-UP RESISTOR VALUES
(INTERNAL PULL-UP RESISTOR OF 9307 = 2KΩ NOMINAL)

$R_x = \frac{3.3}{I_{SEG} - 1.6}$

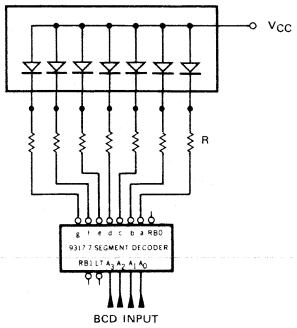
R_x: EXTERNAL PULL-UP RESISTOR (NOMINAL VALUE, IN KΩ)

($R_x \geq 560\Omega$)

I_{SEG}: CURRENT/SEGMENT, IN mA

EXAMPLE: FOR I_{SEG} = 5 mA, R_x = 985 Ω

COMMON CATHODE



COMMON ANODE

Fig. 20. LED displays, common anode or common cathode.

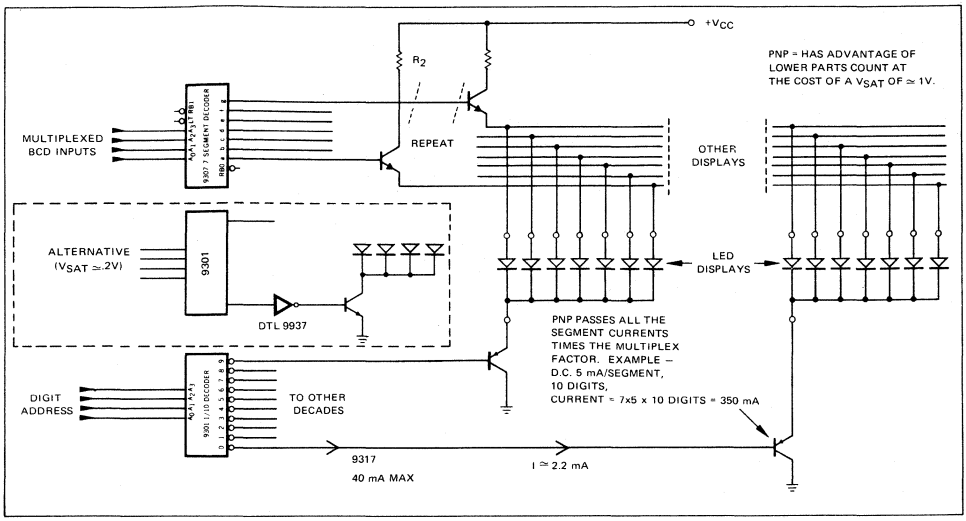


Fig. 21. Multiplexing common cathode LED displays.

MULTIPLEXING LIGHT EMITTING DIODE DISPLAYS

LED displays have electrical and light output rise times in the nanosecond region. This means they can be operated at a low duty cycle with high scanning rates when multiplexed. Scanning rates above 1 kHz are recommended. As many as 24 displays can be multiplexed. See Figures 21 and 22. Because the human eye tends to peak-detect, a low duty cycle with high peak current pulses into LED displays provides apparent brightness.

Forward voltage drop across the LEDs is almost independent of the current passing through the diodes (above the knee on the I/V curve). In order to achieve a brightness (equivalent to static operation) in a multiplexed system, the pulsed current must be increased in proportion to the number of displays used. Ten digits multiplexed would require ten times the current of a single digit alone to achieve similar brightness.

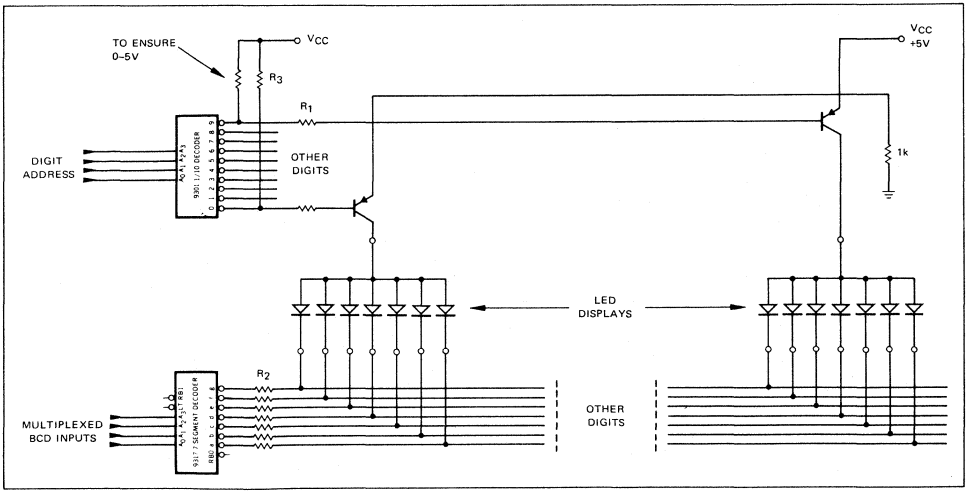


Fig. 22. Multiplexing common anode LED displays.

The drive requirements for the seven segment decoder/driver are not as stringent as those for character or digit address where the total pulsed current of all seven segments must pass through. Ideally, the decoder/driver would be either a constant current source or a constant current sink, depending upon the device type. The digit address would be a low resistance switch.

BASIC MULTIPLEXING SYSTEM

Five units are used in the basic multiplexing circuit. See Figure 23.

1. A *decoder/driver* usually decoding BCD input data to the code requirements of the display device, normally seven segment or one-of-ten decode.
2. An *input address selector* (multiplexer or shift register) taking the BCD input data to be displayed to the decoder/driver.
3. A *scan decoder* selecting the display to be energized.
4. A *scan counter* addressing the scan decoder and input address selector.
5. A *clock input* determining the multiplexing rate.

All multiplexing systems described in this section are applicable to any display device.

Multiplexing a small number of displays is not economical unless the data input is in serial form. Multiplexing can offer advantages after about four digits for some display types. The maximum number of digits is about 12, (except LED displays – 24 possible). Beyond this number, it becomes difficult to power each display unit for its diminishing share of time. For a given brightness the display will require a given power whether or not it is multiplexed. When multiplexed, this power is supplied to the display in pulses for a fraction of the complete scan cycle. Hence, voltage and/or current must be increased over that for the DC conditions.

Multiplexing incandescent displays is less attractive because each filament of the display requires a diode to stop sneak electrical paths. Refer to Figure 5 on page 8.

ADVANTAGES

1. Generally fewer parts – lower system cost.
2. Generally easier printed circuit layout.
3. Reduced interconnection wiring when readout is remote from display logic.
4. System hook-up generally requires fewer parts.

DISADVANTAGES

1. Higher operating voltages required for equivalent brightness.
2. Scan rate must be above 1 kHz to reduce flicker.
3. Careful decoupling of power supplies to stop switching transients is required.
4. Clock failure results in full power to display devices damaging an unprotected system.

FAILSAFE CIRCUIT

The failsafe circuit detects clock failure and disables the address to avoid excessive voltage to any one display. Incoming clock pulses are applied to a diode and capacitor. Capacitor C2 is charged to the peak voltage of the incoming pulse, which, via base resistor of the transistor, supplies sufficient drive to maintain the transistor on. AC coupling is used in case the clock fails in the high condition. The transistor output is applied to the most significant bit of the scan decoder (Figure 24) and in normal operation stays low. If

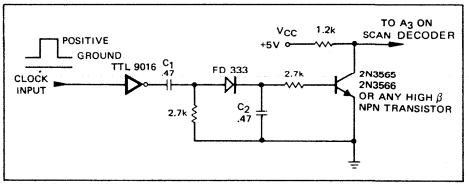


Fig. 24. Failsafe circuit.

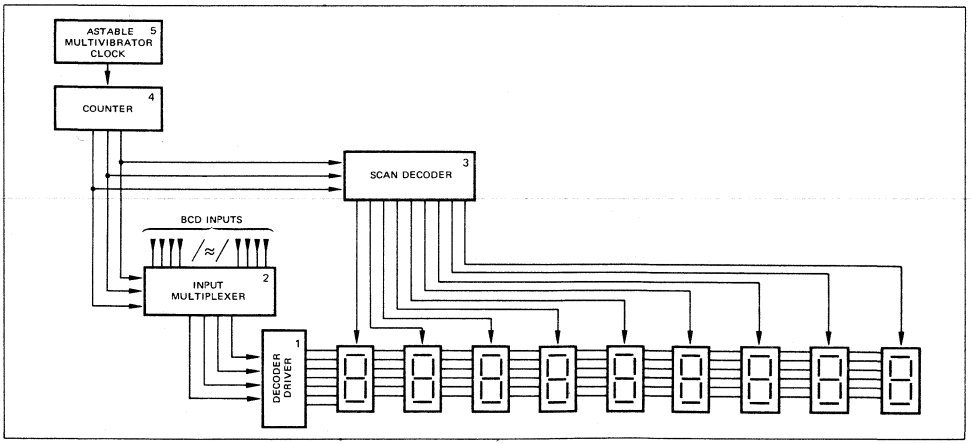


Fig. 23. Basic multiplexing system.

the clock pulse fails the transistor output goes high and the scan decoder addresses the two unused outputs. As shown it will operate satisfactorily from 1 kHz up with duty cycle pulse widths down to 10%.

MULTIPLEXING SYSTEM NO. 1, A SIMPLE EIGHT DIGIT SYSTEM FOR SEVEN SEGMENT FLUORESCENT DISPLAYS

The circuit in Figure 25 illustrates one of the simplest and most straightforward methods of multiplexing systems. Four 9312 8-input multiplexers select the BCD input data for the 9327 decoder drive. Address for the multiplexers and the scan decoder from the 9316 binary counter uses only the first three bits. Each 3-bit address selects the BCD input data to be displayed and the scan decoder energizes the correct display readout device. The counter progresses through all eight counts and repeats, activating each display unit for 1/8th of the scanning cycle. Higher operating voltage must be applied for the displays to have the same brightness as displays in a static mode (DC). A description of the most significant decade blanking circuit is included later in this section, on page 22

MULTIPLEXING SYSTEM NO. 2, AN EIGHT DIGIT SYSTEM FOR SEVEN SEGMENT INCANDESCENT DISPLAYS WITH STORAGE

Figure 26 shows a multiplexing system with storage capability. Operation of this system is as follows. Each bit of 4-bit BCD code inputs is supplied to one of four 9312 multiplexers. The multiplexer input addresses are selected by a 3-bit binary output from 9316 counter. The multiplexer outputs are fed into four 8-bit shift registers when data select (D_S) is low. The multiplexer steps from one input address to the next on each clock pulse. Simultaneously, information is propagated through the shift registers to the decoder/driver. With D_S high, shift register output information is returned to the input to form a recirculating memory. Information continues to circulate as long as D_S is high and power is maintained. Information must be present at the inputs for at least one complete scan period to insure that the multiplexers sample all inputs.

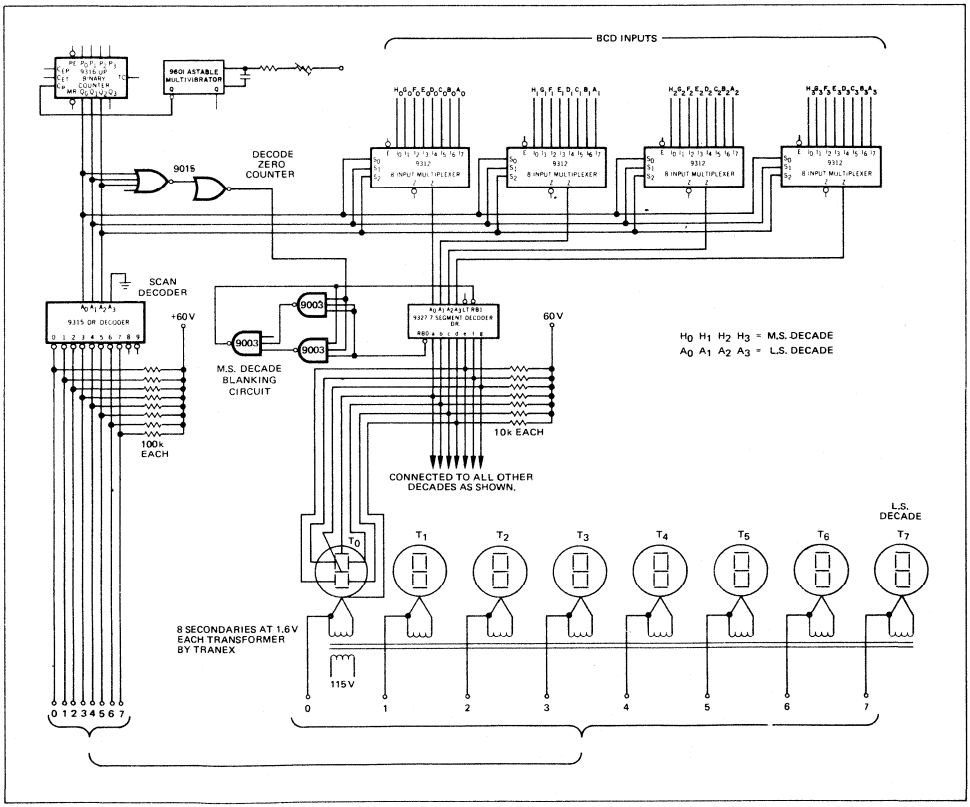


Fig. 25. Simple eight digit multiplex readout system for seven segment fluorescent displays.

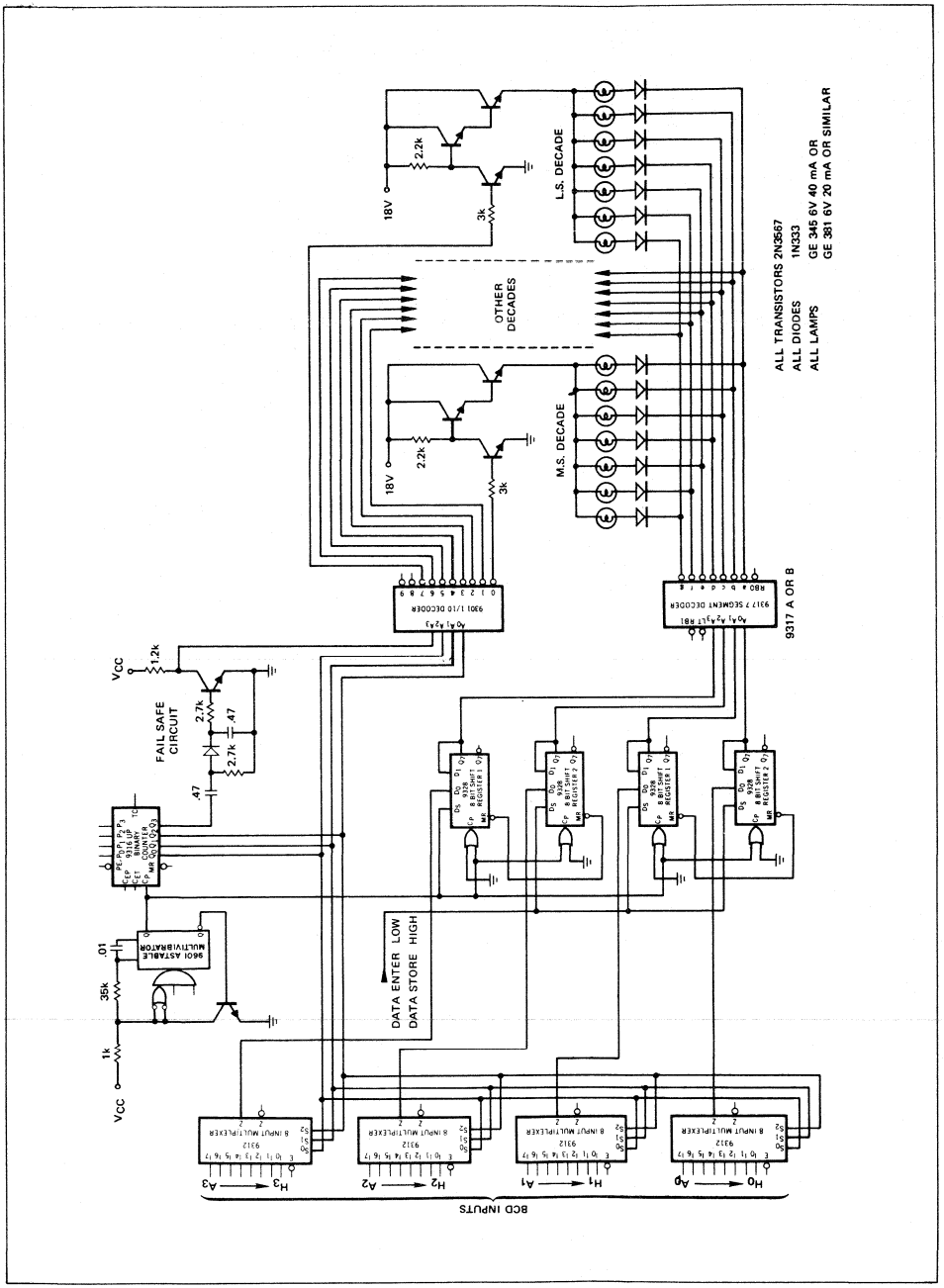


Fig. 26. Multiplexing system for seven segment incandescent displays with storage.

MOST SIGNIFICANT DECADE BLANKING FOR SYSTEMS NO. 1 AND NO. 2

The objective of the circuit shown in Figure 27 is to hold RB_I low during a scan period until a decimal number other than zero appears and then shift RB_I high for the rest of that scan period. The most significant decade is at the start of the scan period; the least significant is at the end.

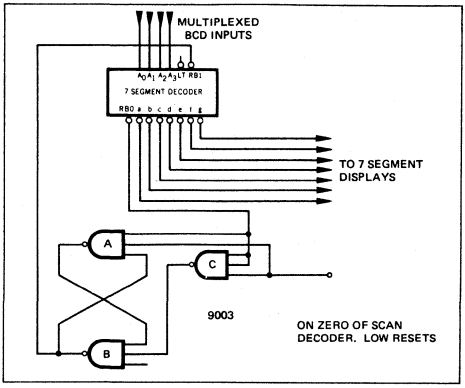


Fig. 27. Most significant decade blanking for Systems no. 1 and no. 2.

When RB_I is low, any decimal zeros to the decoder will be blanked on the display, however any decimal number is displayed. Control of this input achieves most significant digit blanking.

The circuit sets the flip flop (gates A and B) so gate B is low at the start of the scan period (zero count on scan decoder, active low). With RB_I low and BCD zeros into the decoder, RB_O is low. With the first decimal number of the scan period, RB_O goes high. As the reset line is also high, gate C output goes low setting FF, (gate B output high, therefore RB_I is high). This sequence repeats each scan period.

MULTIPLEXING SYSTEM NO. 3, AN EIGHT DIGIT SYSTEM FOR SEVEN SEGMENT FLUORESCENT DISPLAYS WITH STORAGE

In this system (Figure 28), four rows of 8-bit parallel loadable shift registers with outputs fed back to inputs form a recirculating memory. Each row stores one bit of BCD code. Decade information (eight decades) is stored in serial form. Information enters the shift registers through parallel inputs when parallel enable (P_E) goes low. This only occurs for one pulse of the scanned eight by decoding the 3-bit scan counter with a 4-input gate (G_1). The remaining gate input is used as a load command control. When low, it inhibits loading; when high, new information is loaded at the parallel enable pulse (least significant decade).

Four lines of serial information are fed into the 9327 which drives the display tube. All tube anodes are in parallel. Multiplexing is achieved by sequentially switching the cathodes (filament) to ground with the scan decoder. A disadvantage of this system is that input information must be present for at least one complete scan period (eight scan pulses). A modified method (Figure 29) of activating shift register P_E shortens loading time to one clock pulse.

MULTIPLEXING SYSTEM NO. 4, STORAGE/COUNTER

This system serves a dual purpose as a counter display and a parallel load storage system similar to a latch decoder combination (Figure 30). When S_1 is in the upper position, parallel enable P_E is connected to V_{CC} and is inactive, allowing the 9310 decade counter to operate normally. Switch S_1 in the lower position activates P_E. Information is loaded in parallel to the 9310 counters on the first clock pulse after P_E goes low. An astable multivibrator (9601) used as shown to operate the clock pulse (C_P) also provides a storage mode. This multivibrator operates with S_2 in the lower position. With S_2 in the upper position, it is inhibited. S_2 acts as a control for LOAD and STORE of parallel input information. Master reset (M_R) in both modes of operation overrides all other information either stored or being loaded.

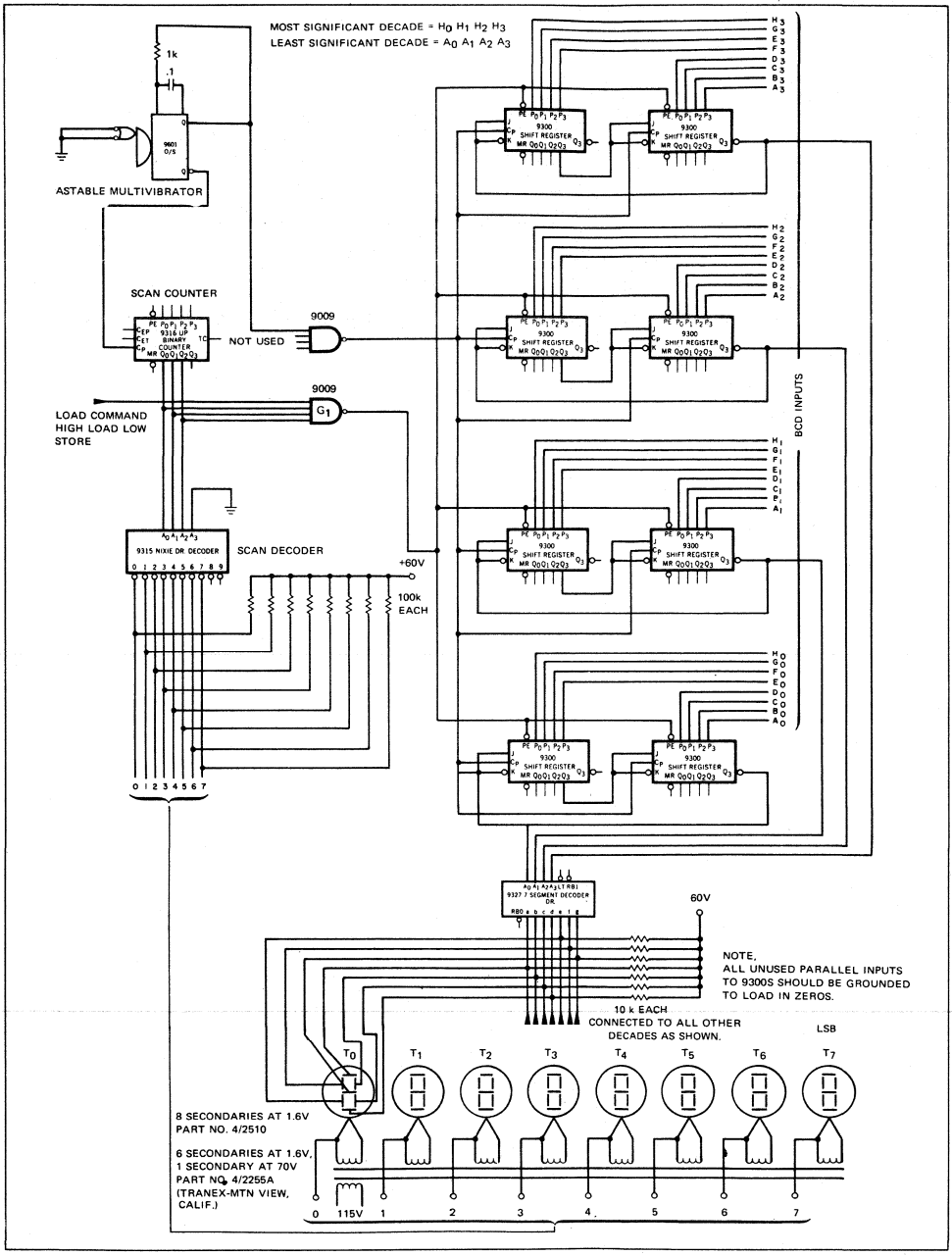


Fig. 28. Multiplexing system for seven segment fluorescent displays with storage.

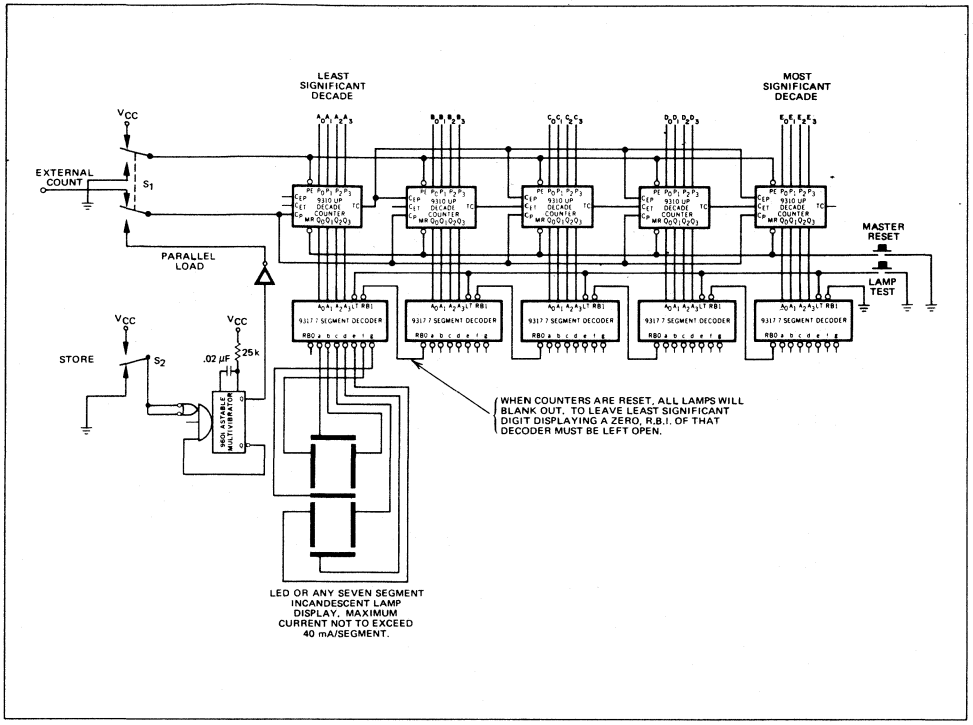
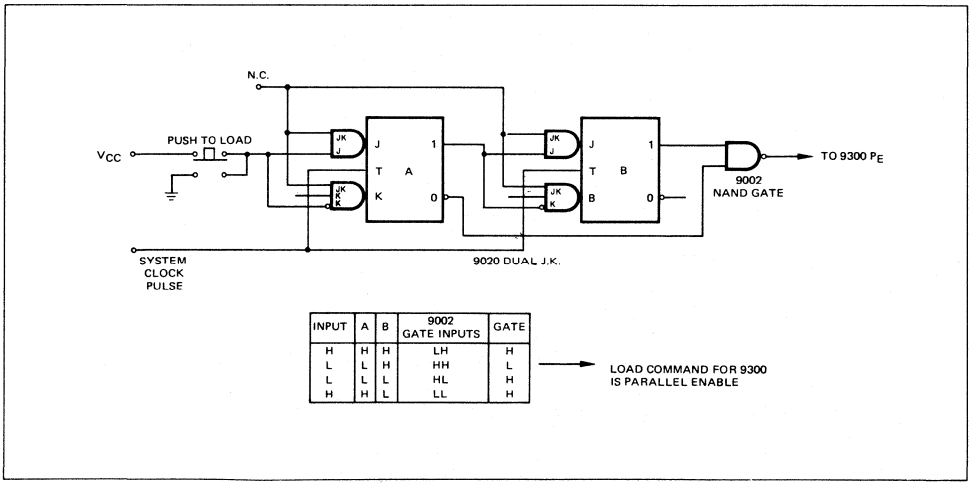


Fig. 29. Instant load circuit for System no. 3.



INPUT	A	B	9002 GATE INPUTS	GATE
H	H	H	LH	H
L	L	H	HH	L
L	L	L	HL	H
H	H	L	LL	H

LOAD COMMAND FOR 9300 IS PARALLEL ENABLE

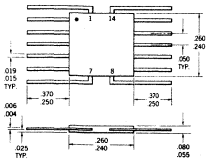
Fig. 30. System no. 4, Storage/Counter.

FAIRCHILD SEMICONDUCTOR

Meet SSI & MSI

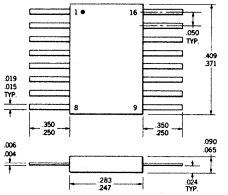
TTL PACKAGE DRAWINGS

in accordance with JEDEC (TO-86) outline 14 Lead Cerpak — 3I*



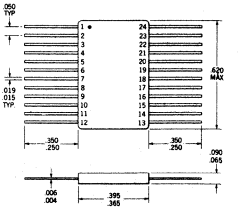
NOTES:
All dimensions in inches.
Leads are gold-plated kovar.
Package weight is 0.26 gram.
3B is used for larger die, the outline dimensions are the same as 3I.

16 Lead BeO Cerpak — 4L



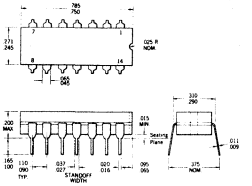
NOTES:
All dimensions in inches.
Leads are gold-plated kovar.
Package weight is 0.4 gram.

24 Lead BeO Cerpak — 4M



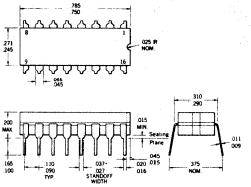
NOTES:
All dimensions in inches.
Leads are gold-plated kovar.
Package weight is 0.8 gram.

in accordance with JEDEC (TO-116) outline 14 Lead Dual In-line — 6A



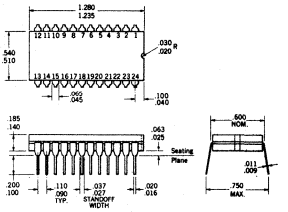
NOTES:
All dimensions in inches.
Leads are intended for insertion in hole rows on .300" centers.
They are purposely shipped with "positive" misalignment to facilitate insertion.
Board-drilling dimensions should equal your practice for .020 inch diameter lead.
Hermetically sealed alumina ceramic package.
Leads are tin-plated kovar.
Package weight is 2.0 grams.

16 Lead SSI Dual In-line — 6B



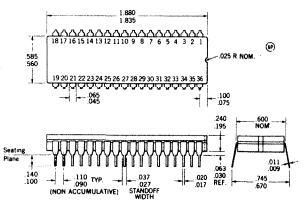
NOTES:
All dimensions in inches.
Leads are intended for insertion in hole rows on .300" centers.
They are purposely shipped with "positive" misalignment to facilitate insertion.
Board-drilling dimensions should equal your practice for .020 inch diameter lead.
Leads are tin-plated kovar.
Package weight is 2.0 grams.
Hermetically sealed alumina ceramic package.
* The .027 dimension does not apply to the corner leads.

24 Lead Dual In-line — 6N



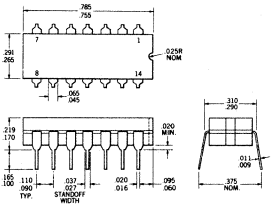
NOTES:
All dimensions in inches.
Leads are intended for insertion in hole rows on .600" centers.
They are purposely shipped with "positive" misalignment to facilitate insertion.
Leads are tin-plated kovar.
Package weight is 6.5 grams.

36 Lead MSI Dual In-line — 6P



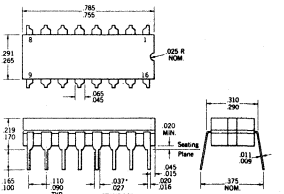
NOTES:
All dimensions in inches.
Leads are intended for insertion in hole rows on .600" centers.
They are purposely shipped with "positive" misalignment to facilitate insertion.
Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead.
Hermetically sealed alumina ceramic package.
Leads are tin-plated kovar.
Package weight is 14.3 grams.

Similar* to JEDEC (TO-116) outline 14 Lead MSI Dual In-line — 7A

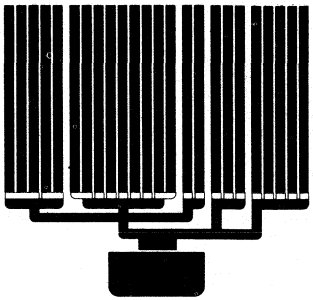


NOTES:
All dimensions in inches.
Leads are intended for insertion in hole rows on .300" centers.
They are purposely shipped with "positive" misalignment to facilitate insertion.
Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead.
Hermetically sealed alumina ceramic package.
Leads are tin-plated kovar.
Package weight is 2.2 grams.
* Similar to JEDEC TO-116 except for package width.

16 Lead MSI Dual In-line — 7B



NOTES:
All dimensions in inches.
Leads are intended for insertion in hole rows on .300" centers.
They are purposely shipped with "positive" misalignment to facilitate insertion.
Board-drilling dimensions should equal your practice for .020 inch diameter lead.
Hermetically sealed alumina ceramic package.
Leads are tin-plated kovar.
Package weight is 2.2 grams.
* The .027 dimension does not apply to the corner leads.



LOADING CHARTS

INTRODUCTION The optimum design of a data processing system should take into account the difference in speed requirements for various parts of the system. It may be advantageous to mix high-speed, standard, and low-power TTL devices in the same system in order to minimize cost and power consumption and increase performance. For this reason, all devices in the Fairchild TTL family are completely compatible in supply voltage, logic input and output voltages and noise margins.

Still, there are some variations in input and output loading characteristics of high-speed, standard and low-power TTL circuits. These differences must be considered when mixing circuits in a system. The following tables list the input and output loading factors for each device in the Fairchild TTL family.

These loading tables are normalized around the standard TTL family. The input and output loads of the standard TTL circuits are given a numerical value of 1, and all other devices are defined in relation to the standard circuits.

The devices within any particular family are generally designed to drive up to 10 similar circuits. For example, a 9N or 9300-series device can drive up to 10 similar devices; however, a 9N-series device will drive only eight 9H-series circuits. A 9L or 93L-series circuit will drive up to 10 9L or 93L circuits, but will drive only two 9N or 9H-series devices.

The table below shows the actual and normalized relationship between the three TTL families.

	SERIES 9000 9N/54, 74 9300/54, 74	SERIES 9H/54H, 74H 93H	SERIES 9L 93L
Max Input "O" Current	1.6 mA	2.0 mA	0.40 mA
Normalized Fan In	1	1.25	0.25
Max Output "O" Current	16 mA	20 mA	4.0 mA
Normalized Fan Out	10	12.5	2.5

TTL/SSI 9000 SERIES

DEVICE TYPE	TERMINAL	NORMALIZED INPUT FACTOR	NORMALIZED OUTPUT FACTOR
9000	J, K, C_P Inputs JK Input $\overline{S_D}$, $\overline{C_D}$ Outputs	1.0 2.0 2.7	 10.0
9001	J, K, C_P Inputs JK Input $\overline{S_D}$, $\overline{C_D}$ Outputs	1.0 2.0 2.7	 10.0
9002	Any Input Any Output	1.0	 10.0
9003	Any Input Any Output	1.0	 10.0
9004	Any Input Any Output	1.0	 10.0
9005	Any Input Any Output	1.5	 10.0
9006	Any Input Any Output	1.5	 N/A
9007	Any Input Any Output	1.0	 10.0
9008	Any Input Any Output	1.5	 10.0
9009	Any Input Any Output	2.0	 30.0
9012	Any Input Any Output	1.0	 O.C.
9014	Any Input Any Output	1.5	 10.0

LOADING CHARTS

TTL/SSI 9000 SERIES

DEVICE TYPE	TERMINAL	NORMALIZED INPUT FACTOR	NORMALIZED OUTPUT FACTOR
9015	Any Input Any Output	1.0	 10.0
9016	Any Input Any Output	1.0	 10.0
9017	Any Input Any Output	1.0	 O.C.
9020	J, K Inputs C_P Input $\overline{C}_D$ Inputs JK Input Outputs	1.0 2.0 2.7 4.0	 10.0
9022	J, $\overline{K}$ Inputs C_P Input $\overline{S}_D$, $\overline{C}_D$ Inputs JK Input Outputs	1.0 2.0 2.7 4.0	 10.0
9024	J, $\overline{K}$ Inputs C_P, $\overline{S}_D$ Inputs $\overline{C}_D$ Input Outputs	1.0 2.0 3.0	 10.0

TTL/SSI 9N/54, 74 SERIES

DEVICE TYPE	TERMINAL	NORMALIZED INPUT FACTOR	NORMALIZED OUTPUT FACTOR
9N00/ 7400, 5400	Any Input Any Output	1.0	 10.0
9N01/ 7401, 5401	Any Input Any Output	1.0	 O.C.
9N02/ 7402, 5402	Any Input Any Output	1.0	 10.0
9N03/ 7403, 5403	Any Input Any Output	1.0	 O.C.
9N04/ 7404, 5404	Any Input Any Output	1.0	 10.0
9N05/ 7405, 5405	Any Input Any Output	1.0	 O.C.
9N08/ 7408, 5408	Any Input Any Output	1.0	 10.0

TTL/SSI 9N/54, 74 SERIES

DEVICE TYPE	TERMINAL	NORMALIZED INPUT FACTOR	NORMALIZED OUTPUT FACTOR
9N10/ 7410, 5410	Any Input Any Output	1.0	 10.0
9N11/ 7411, 5411	Any Input Any Output	1.0	 10.0
9N20/ 7420, 5420	Any Input Any Output	1.0	 10.0
9N30/ 7430, 5430	Any Input Any Output	1.0	 10.0
9N40/ 7440, 5440	Any Input Any Output	1.0	 30.0
9N50/ 7450, 5450	A, B, C, or D Input X and $\overline{X}$ Input Any Output	1.0 N/A	 10.0
9N51/ 7451, 5451	Any Input Any Output	1.0	 10.0
9N53/ 7453, 5453	A, B, C, D, E, F, G and H Input X or $\overline{X}$ Input Output	1.0 N/A	 10.0
9N54/ 7454, 5454	Any Input Any Output	1.0	 10.0
9N60/ 7460, 5460	Any Input X or $\overline{X}$ Output	1.0	 N/A
9N70/ 7470, 5470	J_1, J_2, J*, K_1, K_2, K* Inputs Clock Input Preset or Clear Input Q or $\overline{Q}$ Output	1.0 1.0 2.0	 10.0
9N72/ 7472, 5472	J_1, J_2, J_3, K_1, K_2, K_3 Inputs Clock Input Preset or Clear Inputs Q or $\overline{Q}$ Output	1.0 2.0 2.0	 10.0
9N73/ 7473, 5473	J or K Input Clock Input Clear Input Q or $\overline{Q}$ Output	1.0 2.0 2.0	 10.0

LOADING CHARTS

TTL/SSI 9N/54, 74 SERIES

DEVICE TYPE	TERMINAL	NORMALIZED INPUT FACTOR	NORMALIZED OUTPUT FACTOR
9N74/ 7474, 5474	D Input	1.0	
	Clock Input	2.0	
	Preset Input	2.0	
	Clear Input	3.0	
	Q or $\overline{Q}$ Output		10.0
9N76/ 7476, 5476	J or K Input	1.0	
	Clock Input	2.0	
	Clear Input	2.0	
	Preset Input	2.0	
	Q or $\overline{Q}$ Output		10.0
9N86/ 7486, 5486	Any Input	1.0	
	Any Output		10.0

TTL/SSI 9L SERIES

DEVICE TYPE	TERMINAL	NORMALIZED INPUT FACTOR	NORMALIZED OUTPUT FACTOR
9L00	Any Input	0.25	
	Any Output		2.5
9L04	Any Input	0.25	
	Any Output		2.5
9L24	J, $\overline{K}$ Inputs	0.25	
	C_P, $\overline{S}_D$ Inputs	0.50	
	$\overline{C}_D$ Input	0.75	
	Outputs		2.5
9L54	Any Input	0.25	
	Any Output		2.5

TTL/SSI 9H SERIES

DEVICE TYPE	TERMINAL	NORMALIZED INPUT FACTOR	NORMALIZED OUTPUT FACTOR
9H00/ 74H00, 54H00	Any Input	1.25	
	Any Output		12.5
9H01/ 74H01, 54H01	Any Input	1.25	
	Any Output		O.C.
9H04/ 74H04, 54H04	Any Input	1.25	
	Any Output		12.5
9H05/ 74H05, 54H05	Any Input	1.25	
	Any Output		O.C.
9H10/ 74H10, 54H10	Any Input	1.25	
	Any Output		12.5
9H20/ 74H20, 54H20	Any Input	1.25	
	Any Output		12.5
9H30/ 74H30, 54H30	Any Input	1.25	
	Any Output		12.5
9H40/ 74H40, 54H40	Any Input	1.25	
	Any Output		37.5
9H72/ 74H72, 54H72	J_1, J_2, J_3, K_1, K_2, K_3 Inputs	1.25	
	Preset or Clear Inputs	2.50	
	Clock Input	1.25	
	Q or $\overline{Q}$ Output		12.5
9H73/ 74H73, 54H73	J, K, or Clock Input	1.25	
	Clear Input	2.50	
	Q or $\overline{Q}$ Output		12.5
9H76/ 74H76, 54H76	J, K, or Clock Input	1.25	
	Clear or Preset Input	2.50	
	Q or $\overline{Q}$ Output		12.5

TTL/MSI 93/54, 74 SERIES

DEVICE TYPE	TERMINAL	NORMALIZED INPUT FACTOR	NORMALIZED OUTPUT FACTOR
9300	$\overline{PE}$ Input	2.3	
	P_0 to P_3, J, $\overline{K}$, $\overline{MR}$ Inputs	1.0	
	C_P Input	2.0	
	All Outputs		6.0
9301	All Inputs	1.0	
	All Outputs		10.0
9304	A, B, C, $\overline{A}_2$, $\overline{B}_2$, $\overline{C}_2$ Inputs	4.0	
	C_0 Output		7.0
	S Output		10.0
	$\overline{S}$ Output		9.0
9305	S_0, S_1 Inputs	2.0	
	All Other Inputs	1.0	
	All Outputs		8.0

DEVICE TYPE	TERMINAL	NORMALIZED INPUT FACTOR	NORMALIZED OUTPUT FACTOR
9306	P_0 to P_3 Inputs	0.67	
	$\overline{PE}$, CP Inputs	2.0	
	CE_0 to CE_5, $\overline{C}_D$ Inputs	1.0	
	All Outputs		6.0
9307	A_0 to A_3 Inputs	1.0	
	$\overline{LT}$ Input	4.0	
	$\overline{RBI}$ Input	0.5	
	$\overline{RBO}$ Output		1.5
	All Other Outputs		7.0
9308	D_0 to D_7 Inputs	1.5	
	$\overline{E}_0$, $\overline{E}_1$, $\overline{MR}$ Inputs	1.0	
	Q_0 to Q_3 Outputs		9.0
9309	All Inputs	1.0	
	Z_a, Z_b Outputs		10.0
	$\overline{Z}_a$, $\overline{Z}_b$ Outputs		9.0

LOADING CHARTS

TTL/MSI 93/54,74 SERIES

DEVICE TYPE	TERMINAL	NORMALIZED INPUT FACTOR	NORMALIZED OUTPUT FACTOR
9310	$\overline{PE}$, $\overline{CET}$, C_P Inputs	2.0	
	CEP, $\overline{MR}$ Inputs	1.0	
	P_0 to P_3	0.67	
	All Outputs		6.0
9311	All Inputs	1.0	
	All Outputs		10.0
9312	All Inputs	1.0	
	$\overline{Z}$ Output		10.0
	$\overline{Z}$ Output		9.0
9314	$\overline{E}$, $\overline{S}_0$ to $\overline{S}_3$, $\overline{MR}$ Inputs	1.0	
	D_0 to D_3 Inputs	1.5	
	All Outputs		9.0
9315/ 7441	All Inputs	1.0	
	All Outputs		N/A
9316	$\overline{PE}$, $\overline{CET}$, C_P Inputs	2.0	
	CEP, $\overline{MR}$ Inputs	1.0	
	P_0 to P_3 Inputs	0.67	
	All Outputs		6.0
9317	A_0, A_1, A_2, A_3 Inputs	1.0	
	$\overline{LT}$ Input	4.0	
	$\overline{RBI}$ Input	0.5	
	$\overline{RBO}$ Output		1.5
	All Other Outputs		N/A
9318	$\overline{0}$ Input	1.0	
	$\overline{1}$ to $\overline{7}$, $\overline{EI}$ Inputs	2.0	
	$\overline{EO}$ Output		5.0
	$\overline{GS}$ Output		6.0
	$\overline{A}_0$, $\overline{A}_1$, $\overline{A}_2$ Outputs		10.0
9321	All Inputs	1.0	
	All Outputs		10.0
9322	All Inputs	1.0	
	All Outputs		10.0
9324	All Inputs	2.0	
	A<B, A>B Outputs		9.0
	A = B Output		10.0
9325/ 54141, 74141	All Inputs	1.0	
	All Outputs		N/A
9327	A_0, A_1, A_2, A_3 Inputs	1.0	
	$\overline{LT}$ Input	4.0	
	$\overline{RBI}$ Input	0.5	
	$\overline{RBO}$ Output		1.5
	All Other Outputs		N/A

DEVICE TYPE	TERMINAL	NORMALIZED INPUT FACTOR	NORMALIZED OUTPUT FACTOR
9328	D_S Input	2.0	
	D_0, D_1, $\overline{MR}$ Inputs	1.0	
	C_P (Common)	3.0	
	C_P (Separate)	1.5	
	All Outputs		6.0
9334	A_0, A_1, A_2, D, $\overline{C}$ Inputs	1.0	
	$\overline{E}$ Input	1.5	
	All Outputs		6.0
9337	A_0, A_1, A_2, A_3 Inputs	1.0	
	$\overline{LT}$ Input	4.0	
	$\overline{RBI}$ Input	0.5	
	$\overline{RBO}$ Output		1.5
	All Other Outputs		N/A
9338	A_0, A_1, A_2 Inputs	0.67	
	B_0, B_1, B_2 Inputs	0.67	
	C_0, C_1, C_2 Inputs	0.67	
	D_A, C_P, $\overline{SLE}$	0.67	
	All Outputs		10.0
9340	$\overline{A}_0$ to $\overline{A}_3$, $\overline{B}_0$ to $\overline{B}_3$, $\overline{CG}_1$ Inputs	3.0	
	S_0, S_1, $\overline{CP}_1$, $\overline{CP}_2$, $\overline{CG}_3$ Inputs	1.0	
	$\overline{CG}_2$ Input	2.0	
	COE Input	1.5	
	All Outputs		10.0
9341/ 54181, 74181	$\overline{A}_0$ to $\overline{A}_3$, $\overline{B}_0$ to $\overline{B}_3$, Inputs	3.0	
	S_0 to S_3 Inputs	4.0	
	C_{IN} Input	5.0	
	$\overline{CE}$ Input	1.0	
	$C_{0'}$ $\overline{CG}$, A = B Outputs		8.0
	$\overline{CP}$ Output		7.0
	$\overline{F}_0$ to $\overline{F}_3$ Outputs		10.0
9342/ 54182, 74182	C_{IN} Input	2.0	
	$\overline{CP}_0$ to $\overline{CP}_3$ Inputs	4.0	
	$\overline{CG}_0$, $\overline{CG}_2$ Inputs	9.0	
	$\overline{CG}_1$ Input	10.0	
	$\overline{CG}_3$ Input	5.0	
	All Outputs		10.0
9348	All Inputs	2.0	
	All Outputs		10.0
9350	$\overline{MR}$, MS Inputs	1.0	
	$\overline{CP}_0$ Input	2.0	
	$\overline{CP}_1$ Input	4.0	
	All Outputs		10.0
9352/ 5442, 7442	All Inputs	1.0	
	All Outputs		10.0
9353/ 5443, 7443	All Inputs	1.0	
	All Outputs		10.0
9354/ 5444, 7444	All Inputs	1.0	
	All Outputs		10.0

LOADING CHARTS

TTL/MSI 93/54,74 SERIES

DEVICE TYPE	TERMINAL	NORMALIZED INPUT FACTOR	NORMALIZED OUTPUT FACTOR
9356	MR Input	1.0	
	$\overline{CP}_0$, $\overline{CP}_1$ Inputs	2.0	
	All Outputs		10.0
9357A/ 5446, 7446	A, B, C, D, $\overline{RBI}$, $\overline{LT}$ Inputs	1.0	
	$\overline{BI/RBO}$ Input	2.6	
	$\overline{a}$ to $\overline{g}$ Outputs		12.5
	BI/RBO Output		5.0
9357B/ 5447, 7447	A, B, C, D, $\overline{RBI}$, $\overline{LT}$ Inputs	1.0	
	$\overline{BI/RBO}$ Input	2.6	
	$\overline{a}$ to $\overline{g}$ Outputs		12.5
	$\overline{BI/RBO}$ Output		5.0
9358/ 5448, 7448	A, B, C, D, $\overline{RBI}$, $\overline{LT}$ Inputs	1.0	
	$\overline{BI/RBO}$ Input	2.6	
	a to g Outputs		6.0
	$\overline{BI/RBO}$ Output		5.0
9359/ 5449, 7449	All Inputs	1.0	
	All Outputs		6.0
9360/ 54192, 74192	All Inputs	1.0	
	All Outputs		10.0
9366/ 54193, 74193	All Inputs	1.0	
	All Outputs		10.0
9375/ 5475, 7475	D_1, D_2, D_3, D_4 Input	2.0	
	CP_{1-2}, CP_{2-3} Input	4.0	
9377/ 5477, 7477	All Outputs		10.0
9380/ 5480, 7480	A_1, A_2, B_1, B_2, A_C, B_C Input	1.0	
	A* or B* Input	1.65	
	C Input	5.0	
	Σ or $\overline{\Sigma}$ Output		10.0
	$\overline{C}_{n+1}$ Output		5.0
	A* or B* Output		3.0
9382/ 5482, 7482	A_1 or B_1 Input	4.0	
	A_2 or B_2 Input	1.0	
	C_{IN} Input	4.0	
	C_2 Output		5.0
	Σ_1 or Σ_2 Output		10.0

DEVICE TYPE	TERMINAL	NORMALIZED INPUT FACTOR	NORMALIZED OUTPUT FACTOR
9383/ 5483, 7483	A_1, B_1, A_3, B_3 Inputs	4.0	
	A_2, B_2, A_4, B_4 Inputs	1.0	
	C_{IN} Input	4.0	
	C_4 Output		5.0
	Σ_1, Σ_2, Σ_3, Σ_4, Outputs		10.0
9390/ 5490, 7490	R_{01}, R_{02}, R_{91}, R_{92} Input	1.0	
	$\overline{CP}_{B\text{-}D}$ Input	4.0	
	$\overline{CP}_A$ Input	2.0	
	All Outputs		10.0
9391/ 5491, 7491	A or B Input	1.0	
	CP Input	1.0	
	Q or $\overline{Q}$ Output		10.0
9392/ 5492, 7492	R_{01} or R_{02} Input	1.0	
	$\overline{CP}_{B\text{-}C}$ Input	4.0	
	$\overline{CP}_A$ Input	2.0	
	All Outputs		10.0
9393/ 5493, 7493	R_{01} or R_{02} Input	1.0	
	$\overline{CP}_B$ Input	2.0	
	$\overline{CP}_A$ Input	2.0	
	All Outputs		10.0
9394/ 5494, 7494	P_{1A} to P_{1D}, P_{2A} to P_{2D} Inputs	1.0	
	D_S, CP, C_L Inputs	1.0	
	PE_1, PE_2 Inputs	4.0	
	All Outputs		10.0
9395/ 5495, 7495	M Input	2.0	
	P_A to P_D, $\overline{CP}_1$, $\overline{CP}_2$, D_S Inputs	1.0	
	All Outputs		10.0
9396/ 5496, 7496	PE Input	5.0	
	P_A to P_E, D_S, CP, $\overline{C}_L$ Inputs	1.0	
	All Outputs		10.0

LOADING CHARTS

TTL/MSI 93L SERIES

DEVICE TYPE	TERMINAL	NORMALIZED INPUT FACTOR	NORMALIZED OUTPUT FACTOR
93L00	$\overline{PE}$ Input P_0 to P_3, J, $\overline{K}$, $\overline{MR}$ Inputs C_P Input All Outputs	0.575 0.25 0.50	 2.0
93L01	All Inputs All Outputs	0.25	 2.5
93L08	D_0 to D_3 Inputs $\overline{E}_0$, $\overline{E}_1$, $\overline{MR}$ Inputs Q_0 to Q_3 Outputs	0.375 0.25	 2.25
93L09	All Inputs Z_a, Z_b Outputs $\overline{Z}_a$, $\overline{Z}_b$ Outputs	0.25	 2.50 2.25
93L10	$\overline{PE}$, CET, C_P Inputs CEP, $\overline{MR}$ Inputs P_0 to P_3 Inputs All Outputs	0.5 0.25 0.17	 1.5
93L11	All Inputs All Outputs	0.25	 2.5
93L12	All Inputs Z Output $\overline{Z}$ Output	0.25	 2.5 2.25
93L14	$\overline{E}$, $\overline{S}_0$ to $\overline{S}_3$, $\overline{MR}$ Inputs D_0 toD_3 Inputs All Outputs	0.25 0.375	 2.25

DEVICE TYPE	TERMINAL	NORMALIZED INPUT FACTOR	NORMALIZED OUTPUT FACTOR
93L16	$\overline{PE}$, CET, C_P Inputs CEP, $\overline{MR}$ Inputs P_0 toP_3 Inputs All Outputs	0.5 0.25 0.17	 1.5
93L18	$\overline{0}$ Input $\overline{1}$ to $\overline{7}$, EI Inputs $\overline{EO}$ Output $\overline{GS}$ Output $\overline{A}_0$, $\overline{A}_1$, $\overline{A}_2$ Outputs	0.25 0.5	 1.25 1.5 2.5
93L21	All Inputs All Outputs	0.25	 2.5
93L22	All Inputs All Outputs	0.25	 2.5
93L24	All Inputs A < B A > B Output A = B Output	0.5	 2.25 2.5
93L28	D_S Input D_0, D_1, $\overline{MR}$ Inputs C_P (Common) C_P Separate All Outputs	0.5 0.25 0.75 0.375	 2.0
93L40	$\overline{A}_0$ to $\overline{A}_3$, $\overline{B}_0$ to $\overline{B}_3$, $\overline{CG}_{-1}$ Inputs S_0, S_1, $\overline{CP}_{-1}$, $\overline{CP}_{-2}$, $\overline{CG}_{-3}$ Inputs $\overline{CG}_{-2}$ Input COE Input All Outputs	0.75 0.25 0.5 0.375	 2.5

TTL/MEMORY

DEVICE TYPE	TERMINAL	NORMALIZED INPUT FACTOR	NORMALIZED OUTPUT FACTOR
93400	X_0 to X_5 Inputs Y_0 to Y_5 Inputs R/W Input Output	1.0 0.18 0.12	 6.0
93401	E_1 to E_4 Inputs A_0 to A_3 Inputs X_0 to X_5 Outputs	0.25 0.25	 8.0
93402	$\overline{A}_0$ to $\overline{A}_3$ Inputs $\overline{D}_0$ to $\overline{D}_3$ Inputs $\overline{E}_0$ to $\overline{E}_3$ Inputs $\overline{WE}$ Input M_0 to M_3, $\overline{M}_0$ Outputs $\overline{O}_0$ to $\overline{O}_3$ Outputs	1.0 1.0 1.5 1.5	 6.0 6.0
93403	A_0 to A_3 Inputs D_0 to D_3 Inputs $\overline{WE}$, $\overline{CS}$ Inputs $\overline{O}_0$ to $\overline{O}_3$ Outputs	1.0 1.0 1.0	 6.0

DEVICE TYPE	TERMINAL	NORMALIZED INPUT FACTOR	NORMALIZED OUTPUT FACTOR
93406	A_0 to A_7 Inputs CS_0 to CS_1 Inputs O_0 to O_3 Outputs	0.5 0.5	 10.0
93433	X_0 to X_3 Inputs Y_0 to Y_3 Inputs $\overline{W}_0$, W_1 Inputs $\overline{S}_0$, $\overline{S}_1$ Outputs	11 mA at 2.1 V 11 mA at 2.1 V 1.0	 12.5/25
93434	A_0 to A_4 Inputs $\overline{E}$ Input $\overline{O}_0$ to $\overline{O}_7$ Outputs	1.0 1.0	 6.0
93435	A_0 to A_{15} Inputs I_0 to I_3 Inputs CS, $\overline{WE}$ Inputs $\overline{O}_0$ to $\overline{O}_3$ Outputs	1.0 2.0 1.0	 6.0

LOADING CHARTS

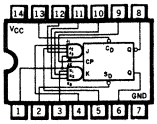
TTL/INTERFACE 9600 SERIES

DEVICE TYPE	TERMINAL	NORMALIZED INPUT FACTOR	NORMALIZED OUTPUT FACTOR
9600	Any Input Any Output	1.0	6.0
9601	Any Input Any Output	1.0	6.0
9602	Any Input Any Output	1.0	6.0
9614	Input Output	1.0	15 mA
9615	Input Output	N/A	10.0
9616	Input Output	1.0	15 mA
9617	Input Output	N/A	10.0
9620	Line Input Output	N/A	10.0
9621	Line Input Output	1.5	20 mA
9622	Line Input Strobe Input Output	N/A 1.0	8.0
9624	Input Output	1.0	N/A
9625	Input Output	N/A	1.0
9644	Input Output	0.5	500 mA, 30 V
9664/ 7524, 9665/ 7525	Sense Input Strobe Input Output	N/A 1.0	10.0

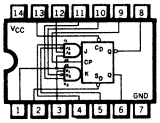
TTL/SSI

TOP VIEW

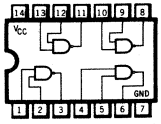
9000



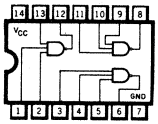
9001



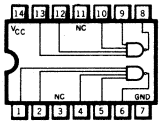
9002



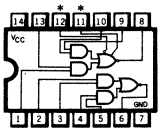
9003



9004

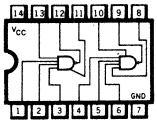


9005

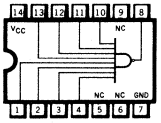


*FOUR EXTENDERS (9006) MAY BE TIED TO THESE PINS.

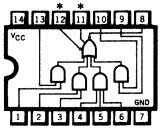
9006



9007

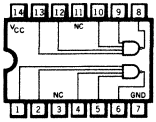


9008

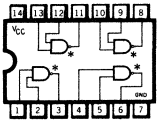


*FOUR EXTENDERS (9006) MAY BE TIED TO THESE PINS.

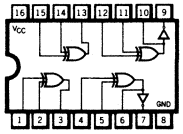
9009



9012

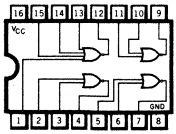


9014

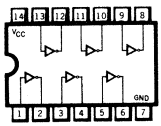


*OPEN COLLECTOR

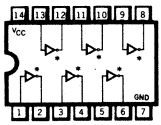
9015



9016



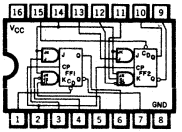
9017



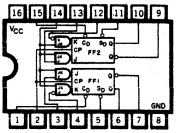
*OPEN COLLECTOR

TTL/SSI

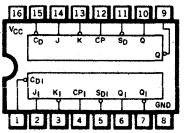
9020



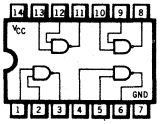
9022



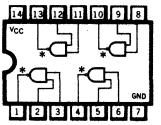
9024



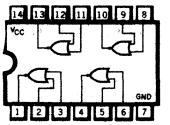
9N00/5400, 7400



9N01/5401, 7401

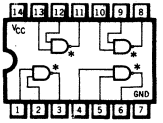


9N02/5402, 7402



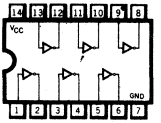
*OPEN COLLECTOR

9N03/5403, 7403

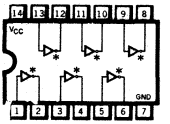


*OPEN COLLECTOR

9N04/5404, 7404

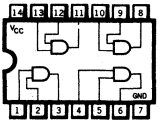


9N05/5405, 7405

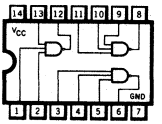


*OPEN COLLECTOR

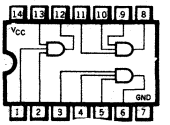
9N08/5408, 7408



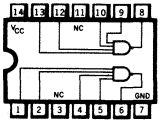
9N10/5410, 7410



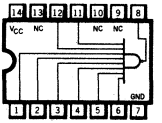
9N11/5411, 7411



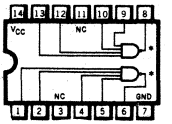
9N20/5420, 7420



9N30/5430, 7430



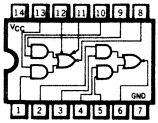
9N40/5440, 7440



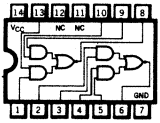
* BUFFER

TTL/SSI

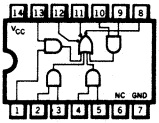
9N50/5450, 7450



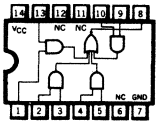
9N51/5451, 7451



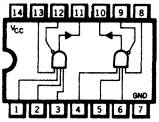
9N53/5453, 7453



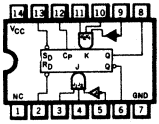
9N54/5454, 7454



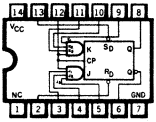
9N60/5460, 7460



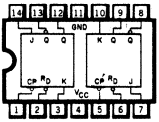
9N70/5470, 7470



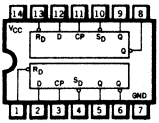
9N72/5472, 7472



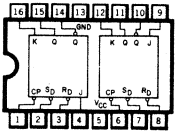
9N73/5473, 7473



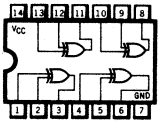
9N74/5474, 7474



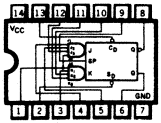
9N76/5476, 7476



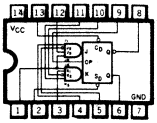
9N86/5486, 7486



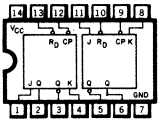
9N104/54104, 74104



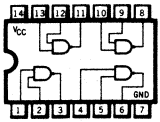
9N105/54105, 74105



9N107/54107, 74107

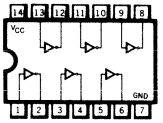


9L00

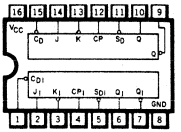


TTL/SSI

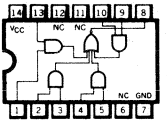
9L04



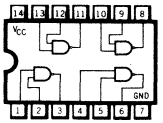
9L24



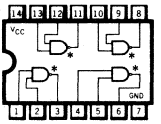
9L54



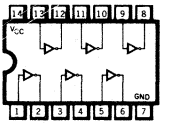
9H00/54H00, 74H00



9H01/54H01, 74H01

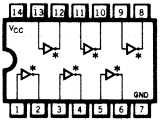


9H04/54H04, 74H04

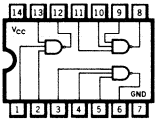


*OPEN COLLECTOR

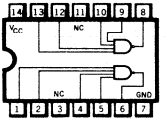
9H05/54H05, 74H05



9H10/54H10, 74H10

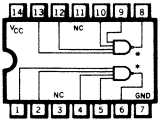


9H20/54H20, 74H20

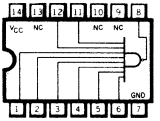


*OPEN COLLECTOR

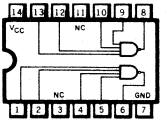
9H22/54H22, 74H22



9H30/54H30, 74H30

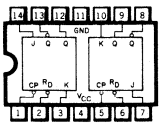


9H40/54H40, 74H40

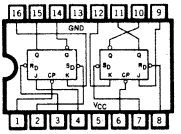


*OPEN COLLECTOR

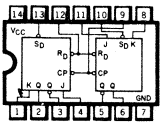
9H73/54H73, 74H73



9H76/54H76, 74H76

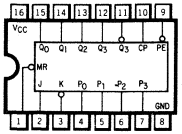


9H78/54H78, 74H78

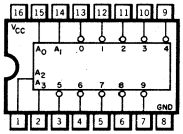


TTL/MSI

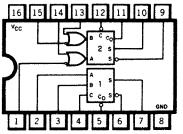
9300



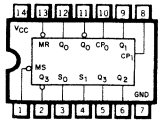
9301



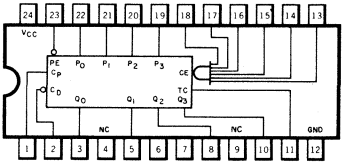
9304



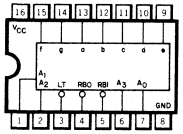
9305



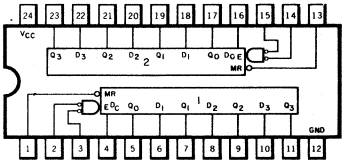
9306



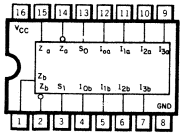
9307



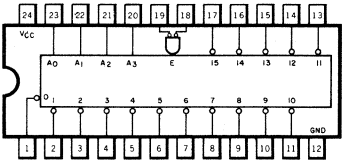
9308



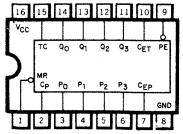
9309



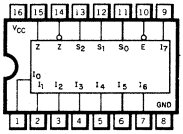
9311



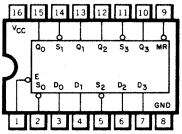
9310



9312

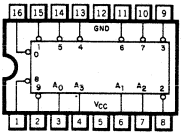


9314

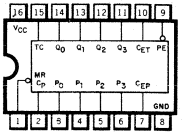


TTL/MSI

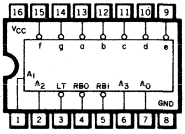
9315/7441



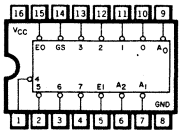
9316



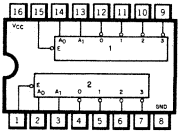
9317



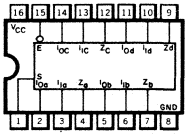
9318



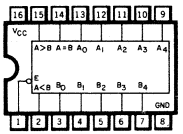
9321



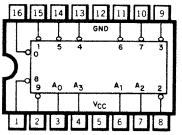
9322



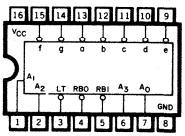
9324



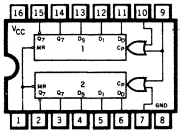
9325/54141, 74141



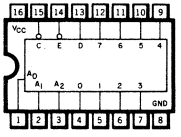
9327



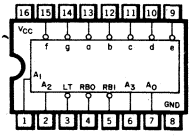
9328



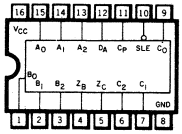
9334



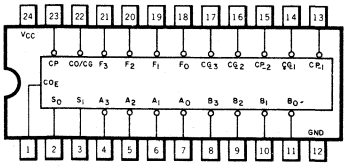
9337



9338

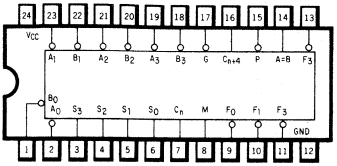


9340

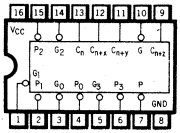


TTL/MSI

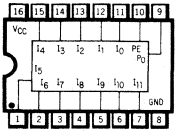
9341/54181, 74181



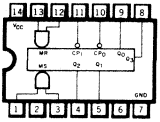
9342/54182, 74182



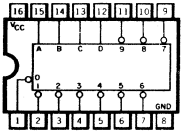
9348



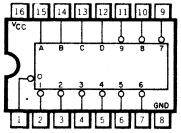
9350



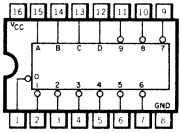
9352/5442, 7442



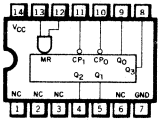
9353/5443, 7443



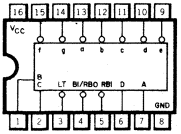
9354/5444, 7444



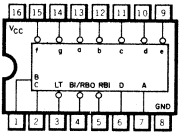
9356



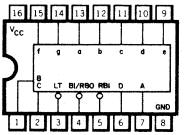
9357A/5446, 7446



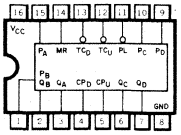
9357B/5447, 7447



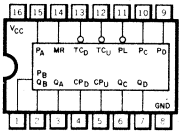
9358/5448, 7448



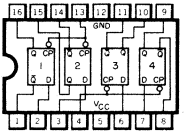
9360/54192, 74192



9366/54193, 74193

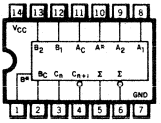


9375/5475, 7475

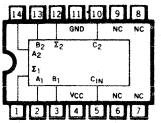


TTL/MSI

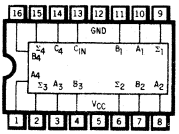
9380/5480, 7480



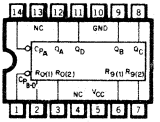
9382/5482, 7482



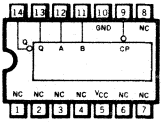
9383/5483, 7483



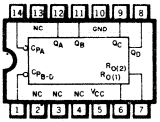
9390/5490, 7490



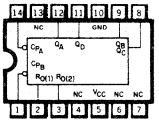
9391/5491, 7491



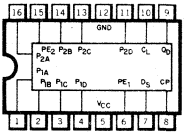
9392/5492, 7492



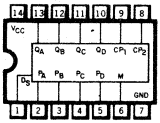
9393/5493, 7493



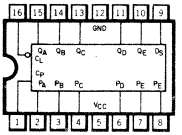
9394/5494, 7494



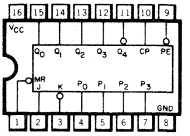
9395/5495, 7495



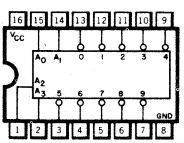
9396/5496, 7496



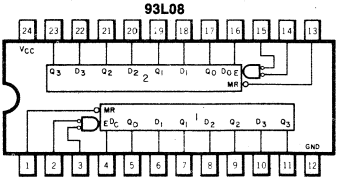
93L00



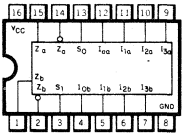
93L01



93L08

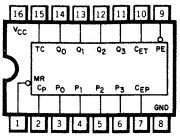


93L09

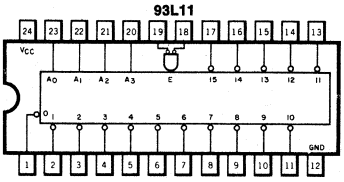


TTL/MSI

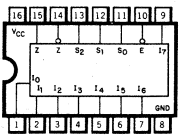
93L10



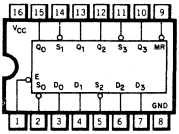
93L11



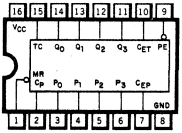
93L12



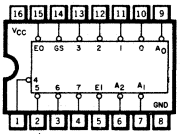
93L14



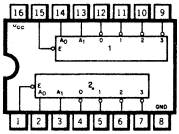
93L16



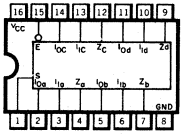
93L18



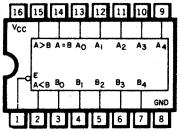
93L21



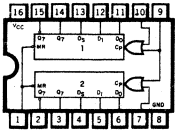
93L22



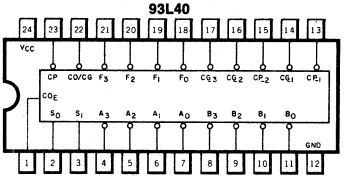
93L24



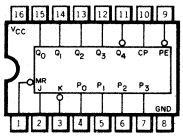
93L28



93L40



93H00



93H70/74196

TO BE ANNOUNCED

93H72

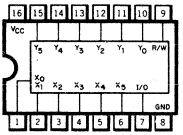
TO BE ANNOUNCED

93H76/74197

TO BE ANNOUNCED

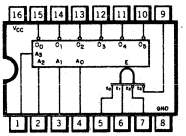
TTL/MEMORY

93400



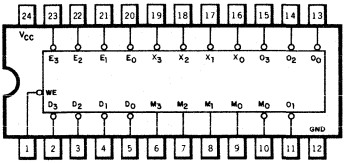
FORMERLY 4100

93401



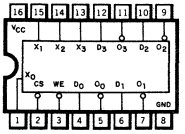
FORMERLY 4101

93402



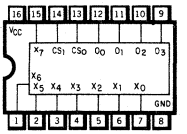
FORMERLY 4102

93403



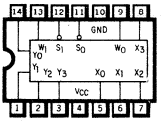
FORMERLY 4103

93406



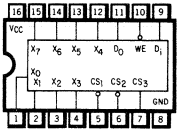
FORMERLY 4106

93407



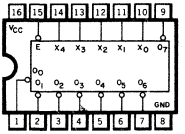
FORMERLY 5033

93410



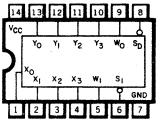
FORMERLY 4110

93412, 93434



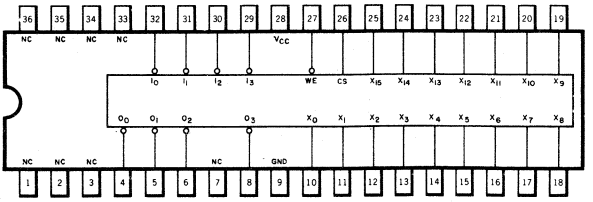
FORMERLY 4112, 9034

93433



FORMERLY 9033

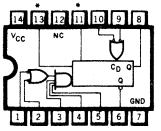
93435



FORMERLY 9035

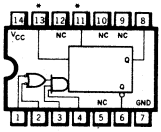
TTL/INTERFACE

9600



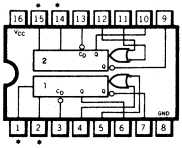
*PINS FOR EXTERNAL TIMING.

9601



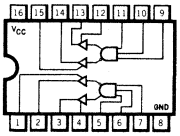
*PINS FOR EXTERNAL TIMING.

9602

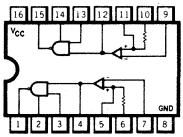


*PINS FOR EXTERNAL TIMING.

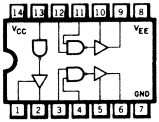
9614



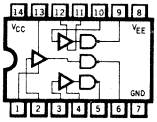
9615



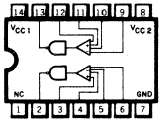
9616



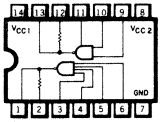
9617



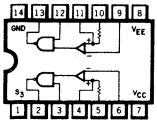
9620



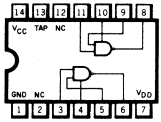
9621



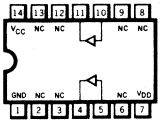
9622



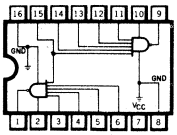
9624



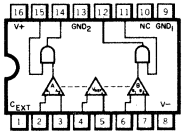
9625



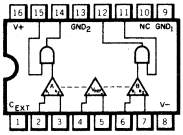
9644



9664/7524



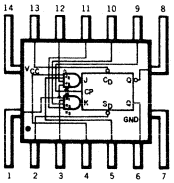
9665/7525



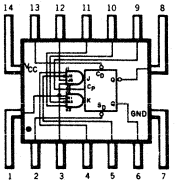
TTL/SSI

TOP VIEW

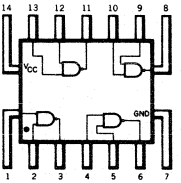
9000



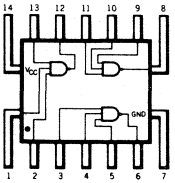
9001



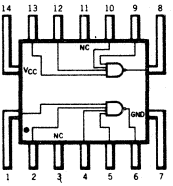
9002



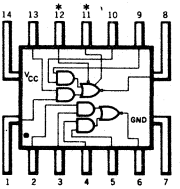
9003



9004

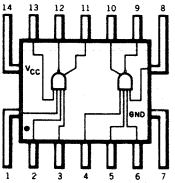


9005

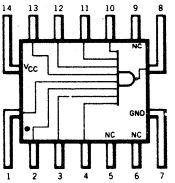


*FOUR EXTENDERS (9006) MAY BE TIED TO THESE PINS.

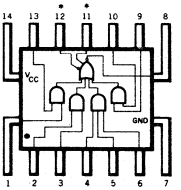
9006



9007

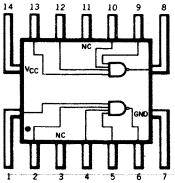


9008

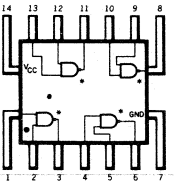


*FOUR EXTENDERS (9006) MAY BE TIED TO THESE PINS

9009

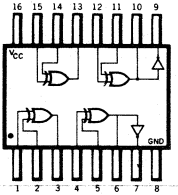


9012

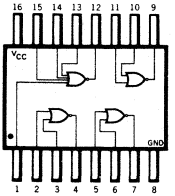


*OPEN COLLECTOR

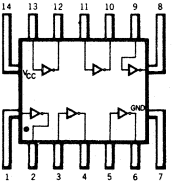
9014



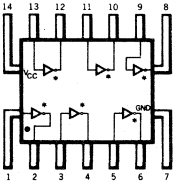
9015



9016



9017

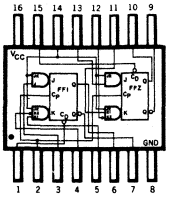


*OPEN COLLECTOR

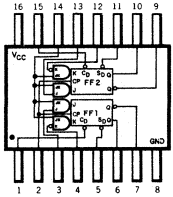
Y

TTL/SSI

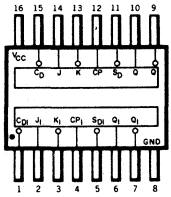
9020



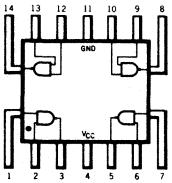
9022



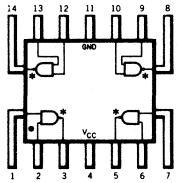
9024



9N00/5400, 7400

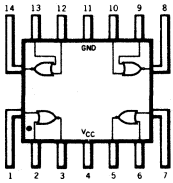


9N01/5401, 7401

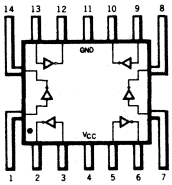


*OPEN COLLECTOR

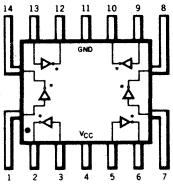
9N02/5402, 7402



9N04/5404, 7404

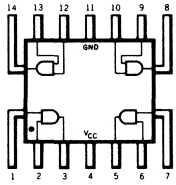


9N05/5405, 7405

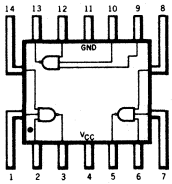


*OPEN COLLECTOR

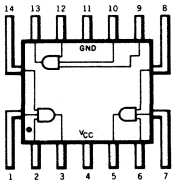
9N08/5408, 7408



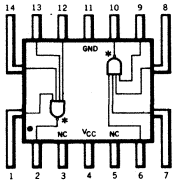
9N10/5410, 7410



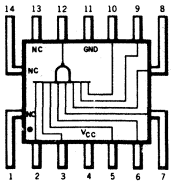
9N11/5411, 7411



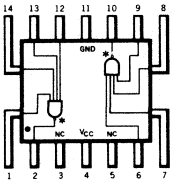
9N20/5420, 7420



9N30/5430, 7430

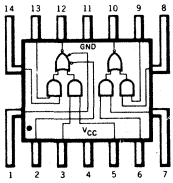


9N40/5440, 7440



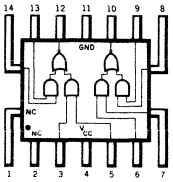
*BUFFER

9N50/5450, 7450

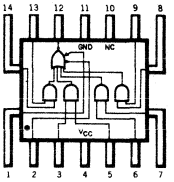


TTL/SSI

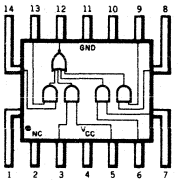
9N51/5451, 7451



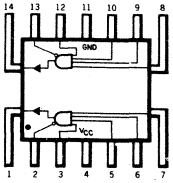
9N53/5453, 7453



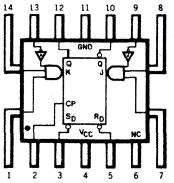
9N54/5454, 7454



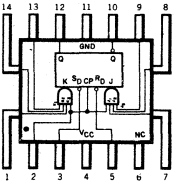
9N60/5460, 7460



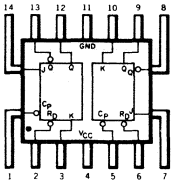
9N70/5470, 7470



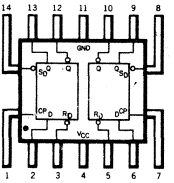
9N72/5472, 7472



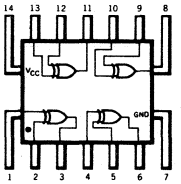
9N73/5473, 7473



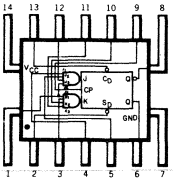
9N74/5474, 7474



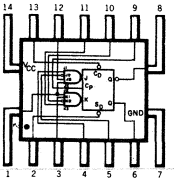
9N86/5486, 7486



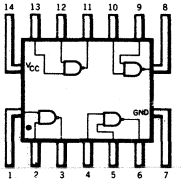
9N104/54104, 74104



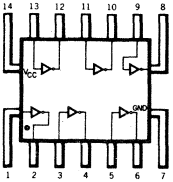
9N105/54105, 74105



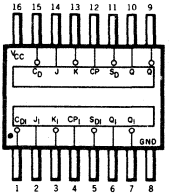
9L00



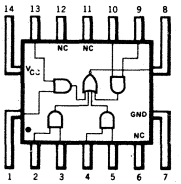
9L04



9L24

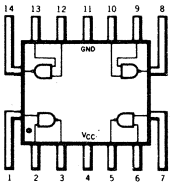


9L54

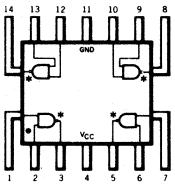


TTL/SSI

9H00/54H00, 74H00

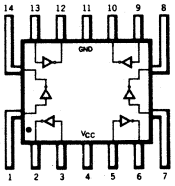


9H01/54H01, 74H01

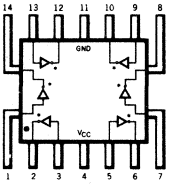


*OPEN COLLECTOR

9H04/54H04, 74H04

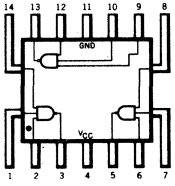


9H05/54H05, 74H05

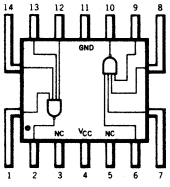


*OPEN COLLECTOR

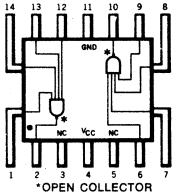
9H10/54H10, 74H10



9H20/54H20, 74H20

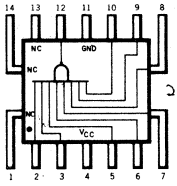


9H22/54H22, 74H22

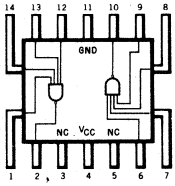


*OPEN COLLECTOR

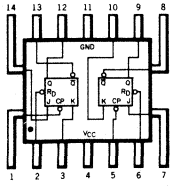
9H30/54H30, 74H30



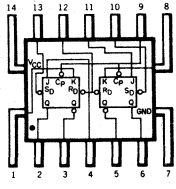
9H40/54H40, 74H40



9H73/54H73, 74H73

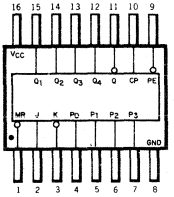


9H78/54H78, 74H78

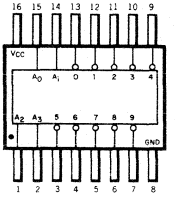


TTL/MSI

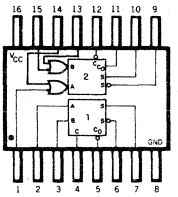
9300



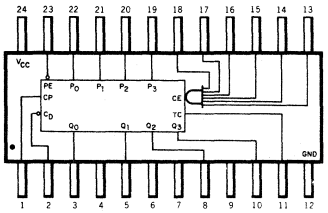
9301



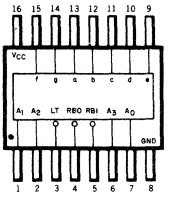
9304



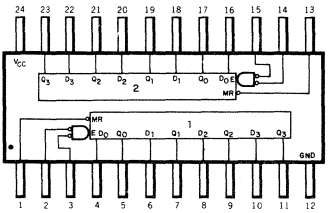
9306



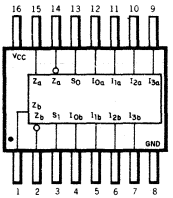
9307



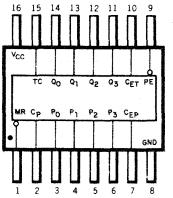
9308



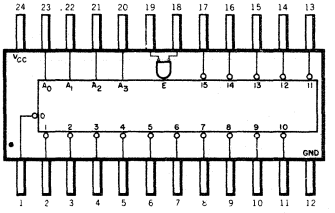
9309



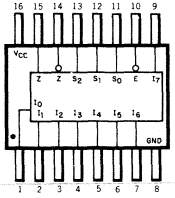
9310



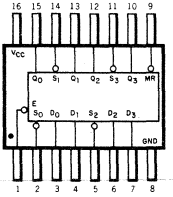
9311



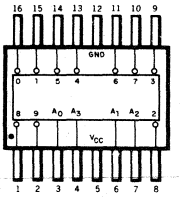
9312



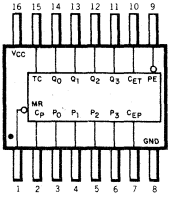
9314



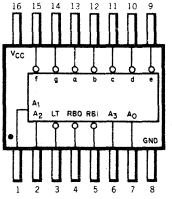
9315/7441



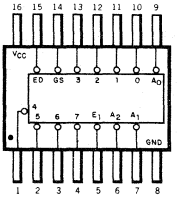
9316



9317

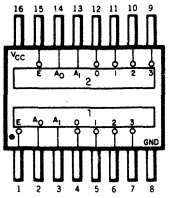


9318

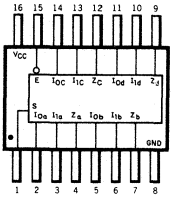


TTL/MSI

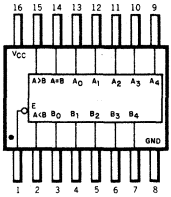
9321



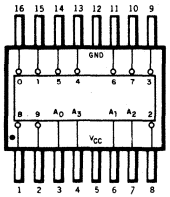
9322



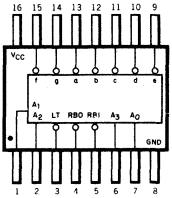
9324



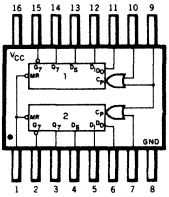
9325/54141, 74141



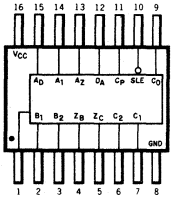
9327



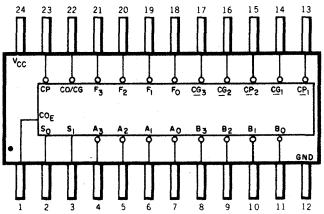
9328



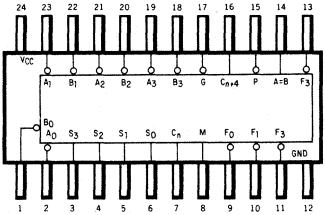
9338



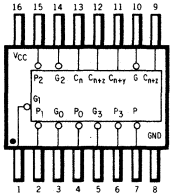
9340



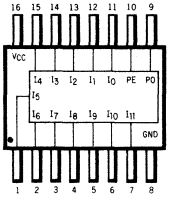
9341/54181, 74181



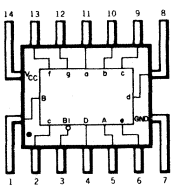
9342/54182, 74182



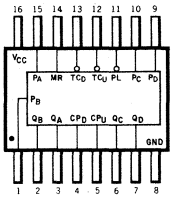
9348



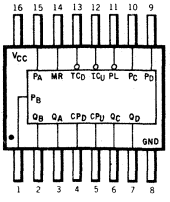
9359/5449, 7449



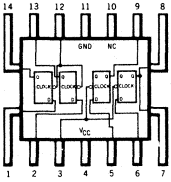
9360/54192, 74192



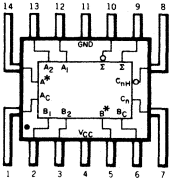
9366/54193, 74193



9377/5477/7477

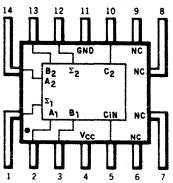


9380/5480, 7480

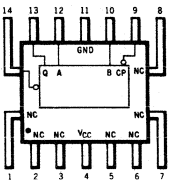


TTL/MSI

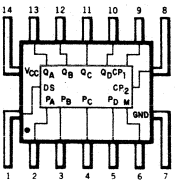
9382/5482, 7482



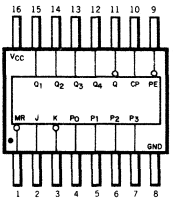
9391/5491, 7491



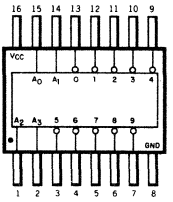
9395/5495, 7495



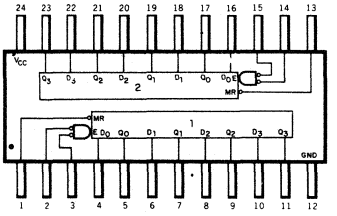
93L00



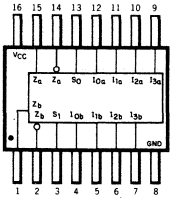
93L01



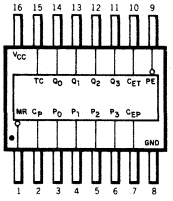
93L08



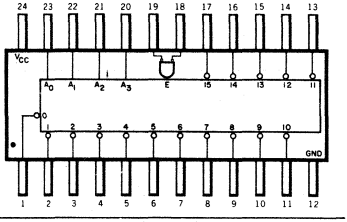
93L09



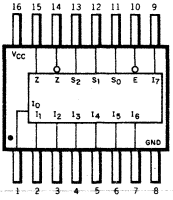
93L10



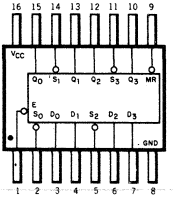
93L11



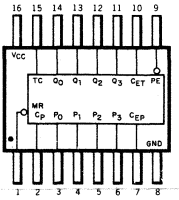
93L12



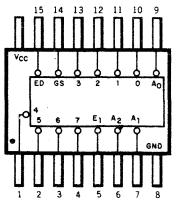
93L14



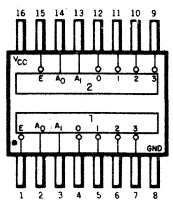
93L16



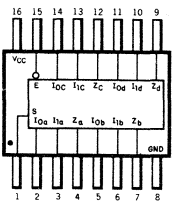
93L18



93L21

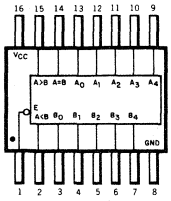


93L22

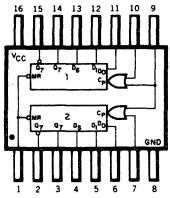


TTL/MSI

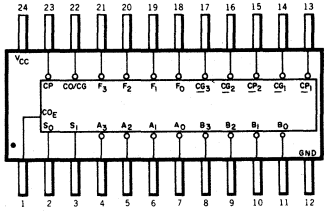
93L24



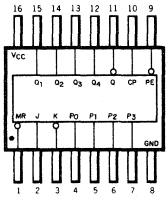
93L28



93L40



93H00



93H70/74196

TO BE ANNOUNCED

93H72

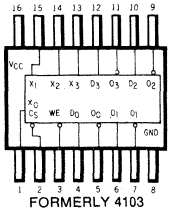
TO BE ANNOUNCED

93H76/74197

TO BE ANNOUNCED

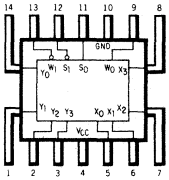
TTL/MEMORY

93403



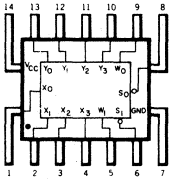
FORMERLY 4103

93407



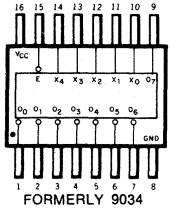
FORMERLY 5033

93433



FORMERLY 9033

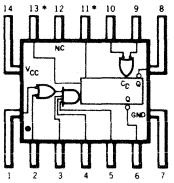
93434



FORMERLY 9034

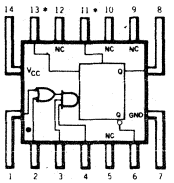
TTL/INTERFACE

9600



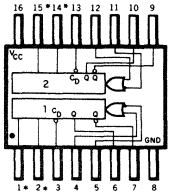
*PINS FOR EXTERNAL TIMING.

9601



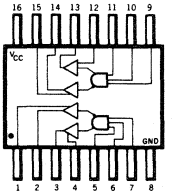
*PINS FOR EXTERNAL TIMING.

9602

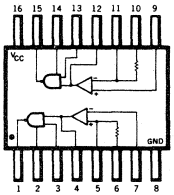


*PINS FOR EXTERNAL TIMING.

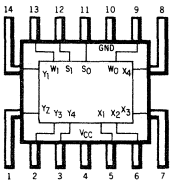
9614



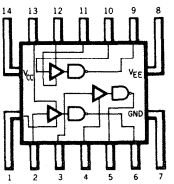
9615



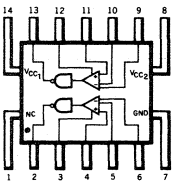
9616



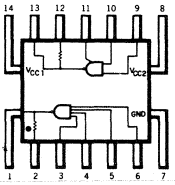
9617



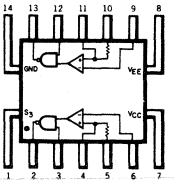
9620



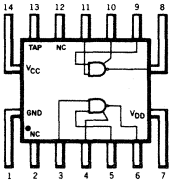
9621



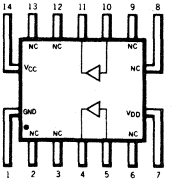
9622



9624



9625



MOS PRODUCT PROFILE

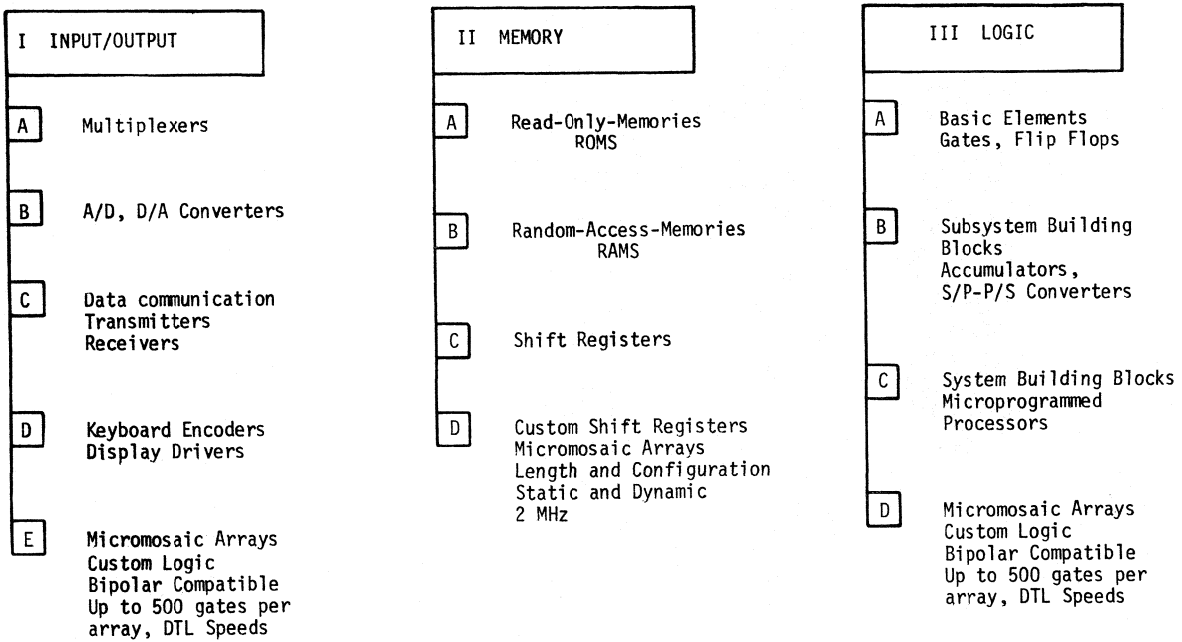
Index by Device Type and Function

FAIRCHILD SEMICONDUCTOR

MOS Product Profile

CONTENTS

FAIRCHILD'S MOS/LSI PRODUCT SUMMARY



PRODUCT SUMMARY BY INPUT/OUTPUT TYPE

MULTIPLEXERS - IA

Product	Description	Application
3700	4 Channel, H.V.	A/D Converters Analog or Digital Signal Routing: Instrumentation Systems.
3701	6 Channel, H.V.	
3705	8 Channel, Decoded 1.0 μs.	
3708	8 Channel, Decoded 400 ns.**	

A/D, D/A CONVERTERS - IB

Product	Description	Application
3750	10 bit D to A Converter	Telemetry, Process Control, Servo Systems
3751	12 bit A to D Converter	Telemetry, Industrial Control, DVM's

**Silicon Gate Product

PRODUCT SUMMARY BY INPUT/OUTPUT TYPE

TRANSMITTERS/RECEIVERS - IC

Product	Description	Applications
3730*	Parallel to Serial Data Converter; Formatter/ Transmitter; Synchronous/ Asynchronous Operation.**	Computer Terminals; Timeshare Data Bussing
3731*	Serial to Parallel Data Converter; Deformatter/ Receiver; Synchronous/ Asynchronous Operation.**	Computer Terminals; Timeshare Data Bussing

*To be announced - First quarter 72

**Silicon Gate Products

PRODUCT SUMMARY BY INPUT/OUTPUT TYPE

KEYBOARD ENCODER - ID

Product	Description	Application
3720*	ASCII Keyboard Encoder up to 128 keys, single pole; key bounce protection.**	CRT Terminals; Scientific Calculators; Stock exchange terminals; Airline reservation terminals. 5, 6, 7 or 8 bit codes.
	By adding a 128 bit shift register, N key rollover is obtained.	
	By adding a ROM, other codes (e.g. EBCDIC) can be obtained.	

DISPLAY DRIVERS (Character Generators) - ID

Product	Description	Application
3250	X, Y, and Z axis signal generator for CRT displays, 7 segment characters.	Test Equipment; Cockpit Displays Process Control Monitors

*To be announced - First quarter 72

**Silicon Gate Products

PRODUCT SUMMARY BY INPUT/OUTPUT TYPE

DISPLAY DRIVERS (Character Generators) - (Contd.) - ID

Product	Description	Application
3255	16 Characters; 5 X 7 font, 7 line output. Static; 2MHz; On chip strobing; one space between characters.**	CRT Displays Plasma Displays
3256	16 Characters; 5 X 7 font, 7 line output. Static; 2 MHz; On chip strobing; Two spaces between characters.**	CRT Displays Plasma Displays
3257	64 Characters; 5 X 7 font, 7 line output. Static; 2 MHz; On chip strobing.**	CRT Displays Plasma Displays
3258	64 Characters; 5 X 7 font, 5 line output. Static; 2 MHz; On chip strobing.**	CRT Displays

**Silicon Gate Products

PRODUCT SUMMARY BY MEMORY TYPE

ROM - IIA

Product	Description	Application
3501	1024 bit Static; high voltage; 128 X 8, 4.0 μs	ROM applications are as follows: Micro-programming, Code Conversion, Table Look-up, Control Logic, and General Combinatorial Logic
3507	2048 bit Static; high voltage; 256 X 8, 2.0 μs	
3580/84	2048 bit Static; high voltage; 512 X 4, 2.0 μs	
3512	2048 bit Static; low voltage; 256 X 8, 600ns**	
351219A	Selectric Line code to ASCII and ASCII to Selectric Line code	Terminal and I/O communications
3513	2560 bit Static; low voltage; 256 X 10, 600ns**	
351319A	Selectric Bail code to ASCII and ASCII to Selectric Bail code	Terminal and I/O communications
3514*	4096 bit Static; low voltage; 512 X 8, 600ns**	
351419A	EBCDIC to ASCII and ASCII to EBCDIC	Terminal and I/O communications

*To be announced - First quarter 72

**Silicon Gate Products.

MICROMOSAIC ARRAYS - IE and IIID

Product	Description	Application
3401	Micromosaic™; over 100 standard metal gate cells in CAD library; Gates, Flip-Flops, Latches, Buffers; high voltage (100 ns/logic level) or low voltage (150 ns/logic level); up to 300 gate complexity; operation to +125°C.	1.5 MHz logic family (1.200 MHz if +125°C); Industrial, Commercial, Military, Consumer. About 1/2 DTL system speeds.
3402	Micromosaic™; over 90 silicon gate cells in CAD library; Gates, Flip-Flops, complete 1 out of 10 Decoders, complete Counters; low voltage (50 ns/logic level); DTL, TTL compatible; up to 500 gate complexity; operation to +125°C.	3 MHz logic family (2.4 MHz if +125°C); directly replaces DTL; same system speeds.

PRODUCT SUMMARY BY MEMORY TYPE - (cont'd.)

RAM - IIB

Product	Description	Application
3532	512 bit, two phase, Static; fully decoded DTL, TTL compatible; Expandable, 500 ns**	General purpose storage element

SHIFT REGISTERS - IIC

3341*	Quad Static FIFO**	Buffer Element
3342*	Quad 64 Static, Single Phase**	Storage Element
3343	Dual 128 Static, Single Phase**	Storage Element
3344	Dual 132 Static, Single Phase**	Storage Element
3345	Dual 136 Static, Single Phase**	Storage Element
3346	Dual 144 Static, Single Phase**	Storage Element
3347	Quad 80 Static, Single Phase**	Storage Element

*To be announced - First quarter 72

**Silicon Gate Products

SHIFT REGISTERS - IIC - (Contd.)

Applications: Serial Memories; CRT Refresh; Radar/Sonar Data Processing; Calculator Registers; Printer Storage Registers.

	Description						
Product	a	b	c	d	e	f	g
3300	25	S	1	H	T	.25	Single 25
3303	50	D	2	H	T	.5	Dual 25
3304	32	S	2	H	T	1.0	Dual 16
3305	64	S	1	H	D	1.0	Quad 16
3306	64	S	1	H	T	1.0	Dual 16 Single 32
3307	200	S	2	H	T	1.0	Dual 100
3325	**256	D	2	L	T	1.0	Quad 64, MPXD I/O
3326	198	D	2	H	T	.5	Triple 66
3329	**512	D	2	L	T	2.0	Single 512
3330	**480	D	2	L	T	2.0	Single 480
3331	**500	D	2	L	T	2.0	Single 500
3383	**256	D	2	L	T	2.0	Single 256 with Recirculate Gating
Custom - IID	N	D	2	L	-	2.0	Max N=512 Bits 8 week delivery 1,000 bits 3rd qtr

**Silicon Gate Products

a - Number of Bits
b - Static(S) or Dynamic(D)
c - Number of clocks
d - High(H) or Low(L) voltage
e - Package; T for 10 lead TO-5,
D for 16 lead DIP
f - Maximum frequency in MHz
g - Configuration

PRODUCT SUMMARY BY LOGIC TYPE

GATES, FLIP-FLOPS - IIIA

Product	Description	Application
3100	5 Input Gate	Basic Logic Element
3101	Dual J-K Flip-Flop	Basic Logic Element
3102	3 Input Gate	Basic Logic Element

STANDARD SUBSYSTEMS BUILDING BLOCKS - IIIB

Product	Description	Application
3800	8 Bit Parallel Accumulator	General Purpose Arithmetic Unit
3801	10 Bit S/P-P/S Converter	General Purpose S/P-P/S Data Converter
3814*	5 Stage Counter/ MPXR**	4 1/2 Digit DVMs
3815*	5 Stage Counter/ MPXR**	5 Digit DMM Building Block
3816*	Modulo N Divider**	General Purpose Programmable Counter

*To be announced - First quarter 72

**Silicon Gate Product

STANDARD SYSTEM BUILDING BLOCKS (Microprogrammed Processors) - IIIC

Product	Description	Application
3805**	BCD Arithmetic Unit One 25 digit register	These building blocks are used to design micro-programmed serial processors. A custom, Micromosaic, output chip is sometimes required depending on the application. Simple 4 rule calculators, for example, need only one ROM, do not require 3809 and do require an output chip to drive the display or printer. Scientific calculators may require several ROM's and/or memory arrays. For additional information, ask for Calculator Building Block Series, Preliminary Application Notes 213 and 214
3806**	Function and Timing Unit	
3807**	Keyboard Encoder Unit, 31 keys, 20 mode switches Legato***	
3808**	Storage Register Unit three 25 digit (100 bit) registers	
3809**	Same as 3808, used for multi-register expansion of set***	
3810**	256 X 12 Microprogrammed ROM***	

**Silicon Gate Products

***Expandable with no extra components

Mighty MOS Data Sheets

3100
FIVE-INPUT GATE
MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 3100 dual five-input gate is a MOS monolithic integrated circuit. This device can be utilized as a logic block in an all MOS system, or as a breadboarding gate in designing customer integrated circuits. Input protection is provided on all inputs.

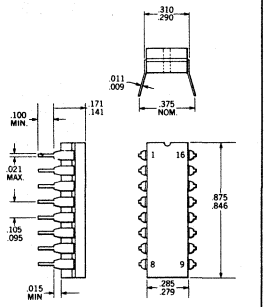
FEATURES

- **GATE PROTECTION**
- **INVERTED AND NON-INVERTED OUTPUT BUFFERS**
- **AND/OR, NAND/NOR CAPABILITY**

ABSOLUTE MAXIMUM RATINGS (Notes 2 & 3)

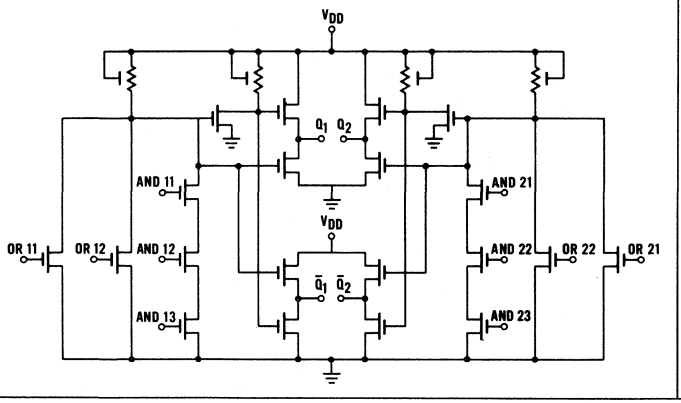
Storage Temperature	−65°C to +150°C
Operating Temperature	−55°C to +85°C
Power Dissipation at +25°C	200 mW
Positive Voltage on any pin	+0.3 V
Negative Voltage on any pin	−30 V

PHYSICAL DIMENSIONS
16 Lead Dual In-Line

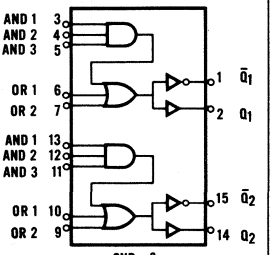


ORDER PART NO. A6J310014X

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM



GND = 8
V_{DD} = 16

NOTE: Polarity indicators (o) external to the solid box conform to MIL-STD-806B where 0 indicates the less positive state is active. Internal to the box and in the remainder of this data sheet conventional MOS polarities are used, where HI = "1" ≃ −10V and LO = "0" ≃ Gnd.

NOTES:
(1) These ratings are limiting values above which serviceability may be impaired.
(2) Voltage levels are with respect to GND Pin.

Electrical Characteristics on Page 2

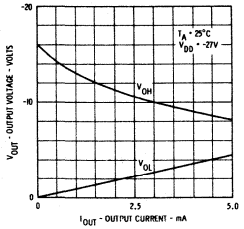
*Planar is a patented Fairchild process.

FAIRCHILD
SEMICONDUCTOR

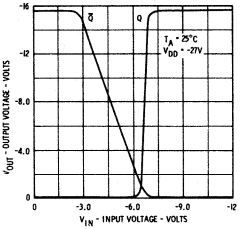
ELECTRICAL CHARACTERISTICS ($V_{DD} = -27 \pm 2$ Volts, Load = 10 MΩ, 10 pF, $T_A = +25°C$ unless otherwise specified)

CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Output Impedance to Ground		1.0	1.5	kΩ	$I_{OUT} = 100\ \mu A$
Input Leakage Current			1.0	μA	$V_{IN} = -20$ V
Input Capacitance		5.0		pF	$V_{IN} = 0$ V
Input Logic Levels					
"0" Level	0		−2.0	Volts	
"1" Level	−9.0			Volts	
Input Data Pulse Width	0.5			μs	
Output Logic Levels					
"0" Level			−1.0	Volts	
"1" Level	−10			Volts	
t_{pd+} (Q)		0.4		μs	
t_{pd-} (Q)		0.4		μs	
t_{pd+} ($\bar{Q}$)		0.4		μs	
t_{pd-} ($\bar{Q}$)		0.6		μs	
Power Consumption		60		mW	

TYPICAL OUTPUT CHARACTERISTIC



TYPICAL TRANSFER CHARACTERISTICS



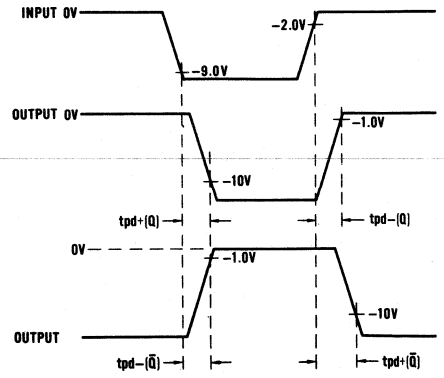
TRUTH TABLE

A OR_1	B OR_2	C AND_1	D AND_2	E AND_3	Q	$\bar{Q}$
0	0	0	0	0	0	1
0	0	0	0	1	0	1
0	0	0	1	0	0	1
0	0	0	1	1	0	1
0	0	1	0	0	0	1
0	0	1	0	1	0	1
0	0	1	1	0	0	1
0	0	1	1	1	1	0
0	1	X	X	X	1	0
1	0	X	X	X	1	0
1	1	X	X	X	1	0

Logical '1' is more negative than −9.0 V
Logical '0' is more positive than −2.0 V and ≤ 0 V
X is either '1' or '0'

BOOLEAN FUNCTION: $Q = A + B + C \cdot D \cdot E$
$\bar{Q} = A + B + C \cdot D \cdot E$

TYPICAL PROPAGATION DELAY



3101
DUAL JK FLIP-FLOP
MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 3101 dual JK flip-flop is a MOS monolithic integrated circuit utilizing P-Channel enhancement technology. This device can be utilized as a logic block in an all MOS system, or as a breadboarding flip-flop in designing custom integrated circuits. Input protection is provided on all inputs.

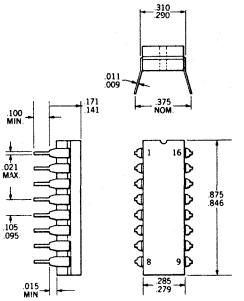
FEATURES

- **INPUT PROTECTION**
- **BUFFERED OUTPUTS**
- **ASYNCHRONOUS SET AND CLEAR**
- **SEPARATE CLOCK LINES**

ABSOLUTE MAXIMUM RATINGS (Notes 1 & 2)

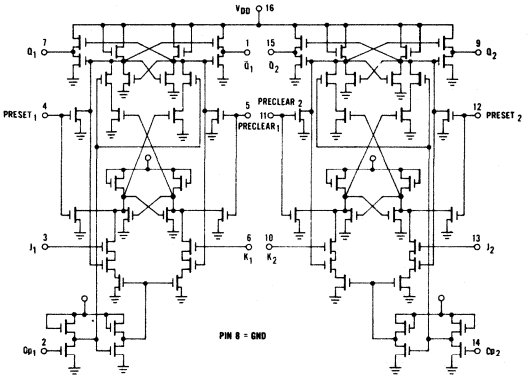
Storage Temperature	−65°C to +150°C
Operating Temperature	−55°C to +85°C
Power Dissipation at +25°C	200 mW
Positive Voltage on any pin	+0.3 V
Negative Voltage on any input pin	−30 V

PHYSICAL DIMENSIONS
16 Lead Dual In-Line

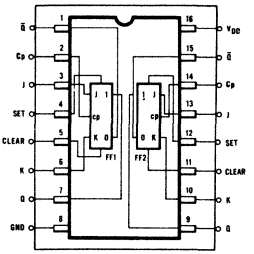


ORDER PART NO. A6J310114X

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM
(TOP VIEW)



NOTE: Polarity indicators (o) external to the solid box conform to MIL-STD-806B where 0 indicates the less positive state is active. Internal to the box and in the remainder of this data sheet conventional MOS polarities are used, where HI = "1" ≃ −10V and LO = "0" ≃ Gnd.

NOTES:
(1) These ratings are limiting values above which serviceability may be impaired.
(2) Voltage levels are with respect to the GND Pin.

FAIRCHILD
SEMICONDUCTOR

ELECTRICAL CHARACTERISTICS ($V_{DD} = -27 \pm 2$ Volts, $T_A = 25°C$ unless otherwise specified)

CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Clock Frequency	DC		250	kHz	$V_{DD} = -26$ V
Clock Amplitude	−9.0			Volts	
Clock Pulse Width	1.0			μs	
Input Leakage Current			1.0	μA	$V_{IN} = -20$ V
Input Capacitance		5.0		pF	$V_{IN} = 0$ V
Input Logic Levels					
"0" Level	0		−2.0	Volts	
"1" Level	−9.0			Volts	
Input Data Pulse Width	1.0			μs	
Output Impedance to Ground			1.0	kΩ	
Output Logic Levels					
"0" Level			−1.0	Volts	
"1" Level	−10			Volts	
t_{setup}		0.5		μs	
$t_{release}$		0.5		μs	
t_{pd+}		1.0		μs	
t_{pd-}		0.5		μs	
Power Consumption		75		mW	

TRUTH TABLE

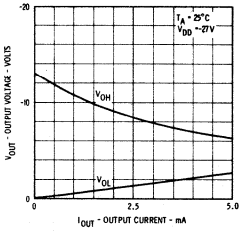
J $t = n$	K $t = n$	Q $t = n + 1$
0	0	X^n
0	1	0
1	0	1
1	1	$\overline{X}^n$

Logical '1' is more negative than −9.0 V

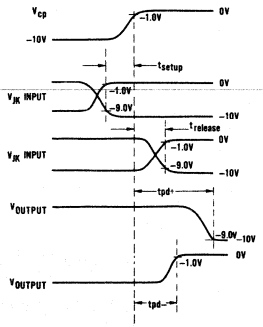
Logical '0' is more positive than −2.0 V and ≤ 0

X^n is the output state at time n

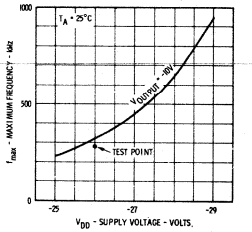
TYPICAL OUTPUT CHARACTERISTICS



TYPICAL SWITCHING WAVEFORMS



MAXIMUM FREQUENCY VERSUS SUPPLY VOLTAGE



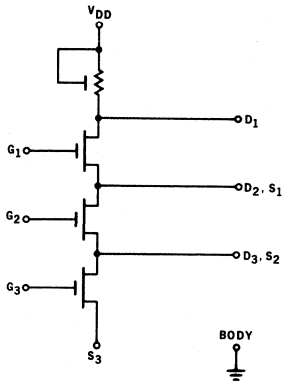
3102
3 INPUT GATE
MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 3102 is a MOS Monolithic 3-Input Gate Integrated Circuit. This device can be utilized as a vehicle in gaining familiarity with MOS integrated circuit logic versatility, as a building block in an all MOS system, or as a breadboarding gate in designing complex custom integrated circuits. Input protection is provided on all gate inputs.

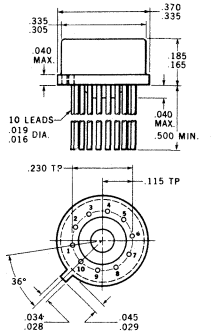
ABSOLUTE MAXIMUM RATINGS (Note 1)

Storage Temperature	−65°C to +150°C
Operating Temperature	−55°C to +85°C
Positive Voltage on any Pin ($V_{Body} = 0$)	+0.3 Volt
Negative Voltage on any Pin ($V_{Body} = 0$)	−35 Volts
Power Dissipation at $T_A = 25°C$	≤200 mW

SCHEMATIC DIAGRAM



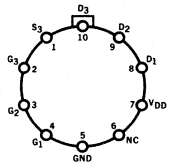
PHYSICAL DIMENSIONS
(In accordance with JEDEC TO-100)



NOTES: All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.02 grams

ORDER PART NO. A5F3102XXX

CONNECTION DIAGRAM



TOP VIEW

NOTES:
(1) These ratings are limiting values above which serviceability of the device may be impaired.

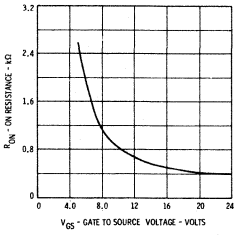
FAIRCHILD
SEMICONDUCTOR

FAIRCHILD MOS INTEGRATED CIRCUIT 3102

ELECTRICAL CHARACTERISTICS ($V_{Body} = 0$; $T_A = 25°C$)

CHARACTERISTICS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
R_{Load}	$V_{DD} = -27\ V \pm 2.0\ V$ $V_{D1} = Gnd$		140		kΩ
R_{ON}(See Figure 1)	$V_{IN} = -20\ V$		500		Ω
Input Leakage Current	$V_{IN} = -25\ V$			1.0	μA
Threshold Voltage (V_{TH})	$V_D = V_G$, $I_D = -10\ \mu A$	−2.0		−5.5	V
Input Capacitance			4.0		pF
Power Consumption	$V_{DD} = -30\ V$, $V_{IN} = -10\ V$		6.0		mW

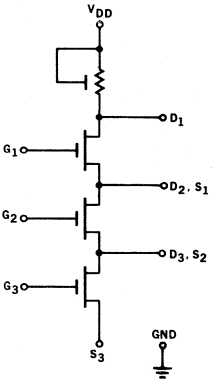
FIG. 1
TYPICAL "ON" RESISTANCE



RESISTANCE CHARACTERISTIC

Parameters	Conditions	TYP.
R_{Load}	$V_{DD} = -25\ V$ $V_{D1} = 0\ V$	140 kΩ
R_{ON}	$V_{GS} = -20\ V$ $V_{DS} \leq -1.0\ V$ $V_{D2} = 0\ V$	500 Ω
R_{ON}	$V_{GS} = -9.0\ V$ $V_{DS} \leq -1.0\ V$ $V_{D2} = 0\ V$	800 Ω

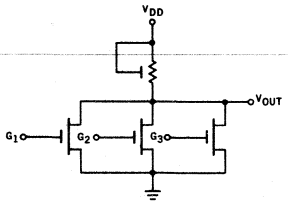
SCHEMATIC DIAGRAM



NOR GATE CONFIGURATION

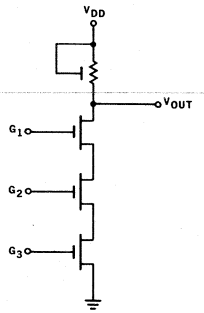
Pin 8 = Pin 10 = V_{OUT}
Pin 1 = Pin 9 = GND
$V_{DD} = -27\ V \pm 2.0\ V$

	LOGIC LEVEL	VOLTAGE LEVEL MIN.	VOLTAGE LEVEL MAX.
V_{IH}	1	−9.0 V	
V_{IL}	0		−2.0 V
V_{OH}	1	−10 V	
V_{OL}	0		−1.0 V



NAND GATE CONFIGURATION

Pin 5 = GND
Pin 8 = OUTPUT
$V_{DD} = -27\ V \pm 2.0\ V$



FAIRCHILD MOS INTEGRATED CIRCUIT 3102

FIG. 2
TYPICAL DRAIN TO SOURCE CHARACTERISTICS

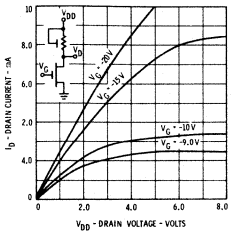
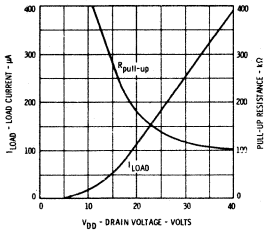
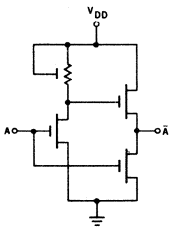


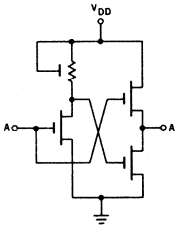
FIG. 3
TYPICAL PULL-UP RESISTANCE



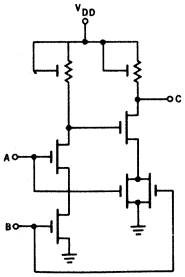
APPLICATIONS — MOS logic will provide the versatility to build many different functions. The following circuits show how to build the functions using one or two 3102 packages.



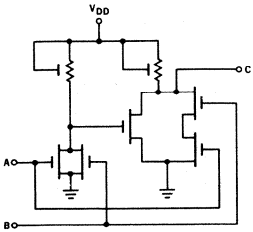
INVERTING BUFFER



NON-INVERTING BUFFER

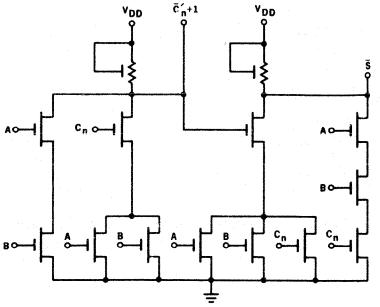


C = A B + $\bar{A}\bar{B}$
EXCLUSIVE NOR

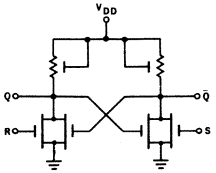


C = $\bar{A}$ B + $\bar{B}$ A
EXCLUSIVE OR

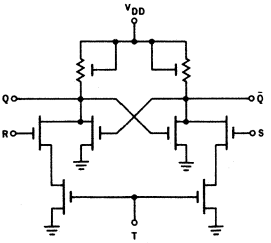
FAIRCHILD MOS INTEGRATED CIRCUIT 3102



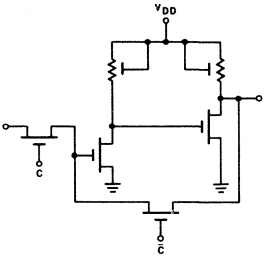
$C'_{n+1} = AB + C_n(A + B)$
$S = (A+B+C_n)\,C'_{n+1} + ABC_n$
FULL ADDER



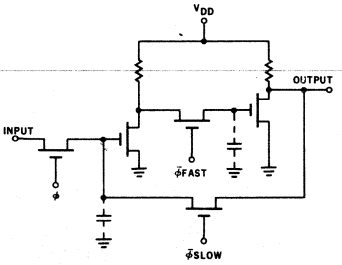
RS FLIP-FLOP



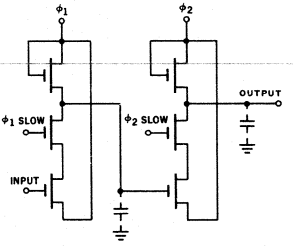
RST FLIP-FLOP



TYPE D FLIP-FLOP



STATIC (DC) SHIFT REGISTER BIT



DYNAMIC 4-PHASE (4ϕ)
SHIFT REGISTER BIT

3255 . 3256

DOT MATRIX CHARACTER GENERATORS
16 CHARACTER 5 x 7 BITS
FAIRCHILD SILICON GATE MOS INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The 3255 and 3256 are dot matrix character generators organized to display 16 characters in a 5 column by 7 output matrix. They are MOS monolithic, P–channel enhancement integrated circuits utilizing Silicon Gate Technology. The 3255 provides single space blanking between characters while the 3256 provides double space blanking.

FEATURES

- **350 ns TYPICAL ACCESS TIME**
- **DIRECT INTERFACING WITH TTL/DTL***
- **ON CHIP COLUMN SELECT COUNTER**
- **ONLY +5 V and –12 V REQUIRED**
- **STATIC OPERATION**
- **16 LEAD PACKAGE**

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Voltage on any pin (Note 1)	–25 V to +0.3 V
Storage Temperature	–55°C to +150°C
Operating Temperature	0°C to +70°C

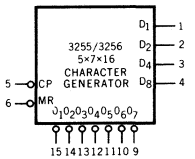
Note 1: All voltages with respect to V_{SS}

APPLICATIONS

Horizontal Raster Scan (TV) Displays
Vertical Raster Scan Displays
Dot Matrix Displays such as Billboards
Solid State 5 x 7 Dot Matrix Displays

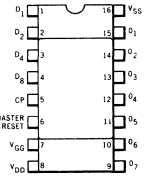
*See Figure 9.

LOGIC SYMBOL

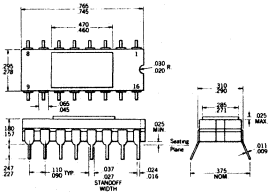


V_{SS} = PIN 16
V_{DD} = PIN 8
V_{GG} = PIN 7

PIN CONFIGURATION

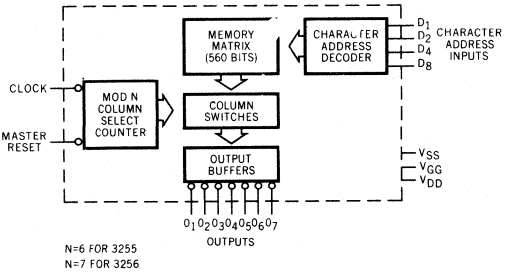


PHYSICAL DIMENSIONS



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are gold-plated kovar
Package weight is 1.3 grams

BLOCK DIAGRAM



FAIRCHILD SEMICONDUCTOR

OPERATIONAL DESCRIPTION – In operation a 4-bit Binary word presented to the character address inputs is decoded to select 1 of 16 characters in the memory matrix. The 5 columns in each character are selected by the first 5 states of the Modulo N counter (N = 6 for 3255, N = 7 for 3256). The last states of the counter provide blanking between characters (1 space for 3255, 2 spaces for 3256). A logic LOW at the Master Reset input resets the counter to the Nth state independent of the character address input or clock level.

D C CHARACTERISTICS

Standard Operating Conditions (unless otherwise specified) V_{SS} = +5 V ±5%, V_{GG} = −12 V ±5%, V_{DD} = 0 V (GND), 0°C ≤ T_A ≤ 70°C

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
	Input Logic Levels					Note 1
V_{IL}	Logic "LOW"	V_{GG}	0	+0.85	Volts	
V_{IH}	Logic "HIGH"	V_{SS} −1		V_{SS}	Volts	
I_L	Input Leakage Current		0.010	1.0	μA	Note 1, V_{IN} = −18 V, V_{SS} = 0 V
I_{SS}	Supply Current Drain		18	22	mA	Outputs Open V_{SS} = +5.25 V, V_{GG} = −12.6 V
P_D	Power Consumption		320	400	mW	Outputs Open V_{SS} = +5.25 V, V_{GG} = −12.6 V
	Output Logic Levels					
V_{OL}	Logic "LOW"		+0.30	+0.40	Volts	I_{OUT} = 2.4 mA Current Into Output
V_{OH}	Logic "HIGH"	V_{SS} −0.5	V_{SS} −0.04		Volts	I_{OUT} = 10 μA Current Out of Output
V_{OH}	Logic "HIGH"	3.6	4.0		Volts	I_{OUT} = 0.60 mA

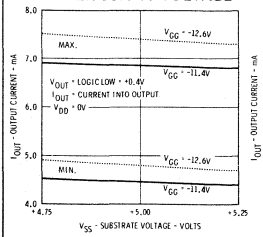
A C CHARACTERISTICS

Standard Operating Conditions (unless otherwise specified) V_{SS} = +5 V ±5%, V_{GG} = −12 V ±5%, V_{DD} = 0 V (GND), 0°C ≤ T_A ≤ 70°C

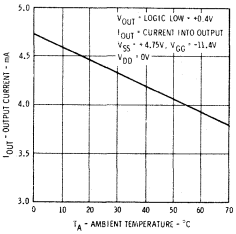
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
f	Clock Frequency	DC		2.0	MHz	
$t_{\phi W}$	Clock Pulse Width	300*	170		ns	*Worst Case
$t_{\phi R}$, $t_{\phi F}$	Clock Rise or Fall Time			2.0	μs	10% to 90% Points
t_{RST}	Reset Pulse Width	300			ns	
t_{CRD}	Clock-to-Reset Time Delay	200			ns	Note 3, Fig. 5
	Access time:					
t_{AO}	Address Input to Output		250	400	ns	Note 4, Fig. 2
t_{CO}	Clock to Output		350	600	ns	Note 4, Fig. 3
t_{RO}	Reset to Output		250	400	ns	Note 4, Fig. 4
C_I	Input Capacitance		5.0	10.0	pF	Notes 1 and 2

NOTES:
1. Includes character address, clock and reset inputs.
2. Guaranteed by design.
3. Reset must return to a logic HIGH, as specified, before a positive to negative clock transition to guarantee output levels during that clock time.
4. Access time logic LOW level is defined as +0.4 V at 2.4 mA, into output, and logic HIGH level is defined as +2.4 V at 0.6 mA, out of output.

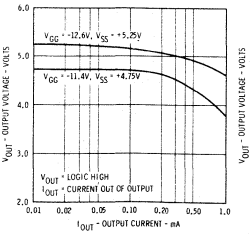
OUTPUT CURRENT VERSUS POWER SUPPLY VOLTAGE



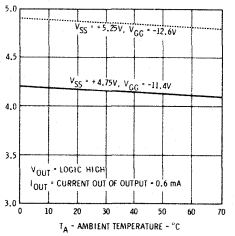
OUTPUT CURRENT VERSUS AMBIENT TEMPERATURE



OUTPUT VOLTAGE VERSUS OUTPUT CURRENT

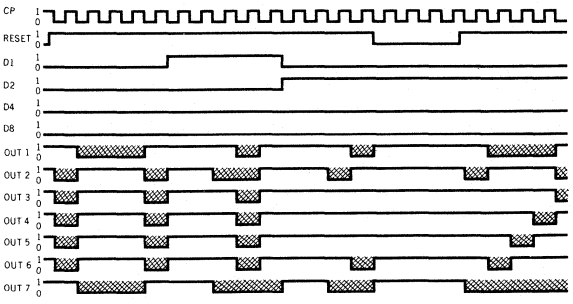


OUTPUT VOLTAGE VERSUS AMBIENT TEMPERATURE



TYPICAL FUNCTIONAL TIMING DIAGRAM (for 3255, i.e. 1 space blanking)

Fig. 1



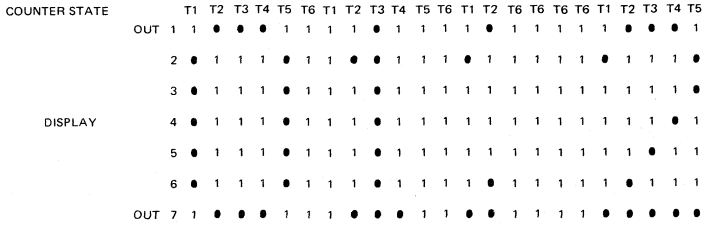


Fig. 2

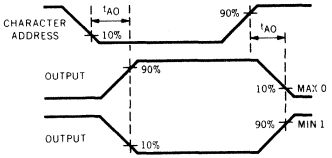


Fig. 3

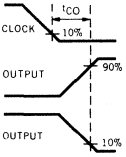


Fig. 4

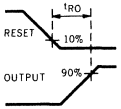
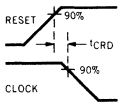
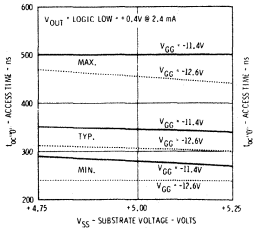


Fig. 5

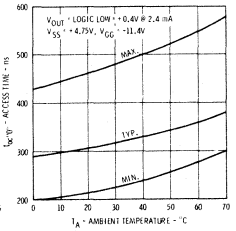


ACCESS TIME CHARACTERISTICS

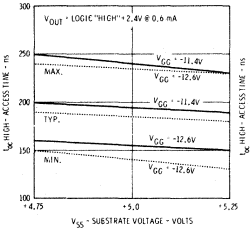
ACCESS TIME (t_{CO} LOW) VERSUS POWER SUPPLY VOLTAGE



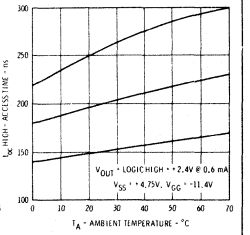
ACCESS TIME (t_{CO} LOW) VERSUS AMBIENT TEMPERATURE



ACCESS TIME (t_{CO} HIGH) VERSUS POWER SUPPLY VOLTAGE



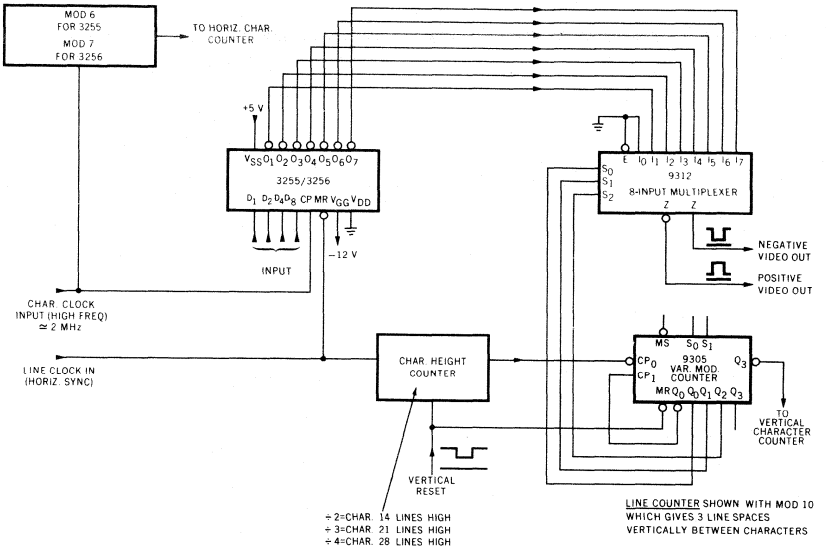
ACCESS TIME (t_{CO} HIGH) VERSUS AMBIENT TEMPERATURE



HORIZONTAL RASTER SCAN APPLICATIONS

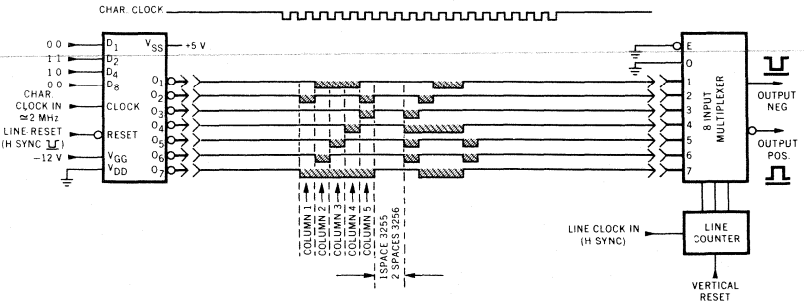
In the horizontal mode of operation the clock input is a high frequency clock (approximately 2 MHz) synchronized with the horizontal sync of the display. Each of the seven outputs gives 5 bits of serial information (plus one or two blanks), which forms one horizontal line of a character. These seven outputs are fed into a line selector comprised of a multiplexer and a counter, while the output of the multiplexer is fed to the video display. By selecting either the assertion or negation output of the multiplexer, black or white characters can be obtained.

Using characters 14 horizontal lines high, 256 characters can be placed upon a standard TV screen and are easily readable at normal viewing distances. A clock frequency of approximately 2.0 MHz is required. As the devices have no terminal count output on the internal column counter, a separate counter of the same modulus has to be run in parallel in order to count horizontal character position.



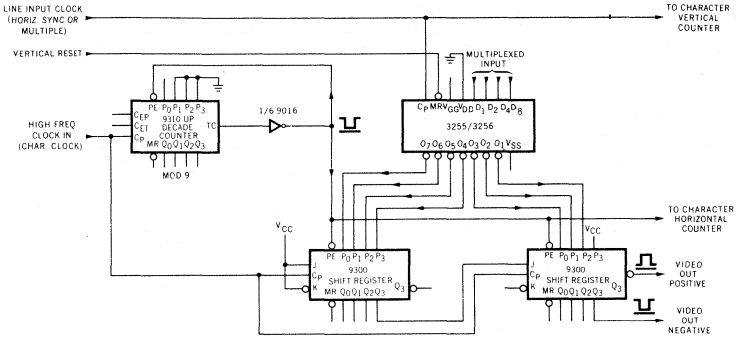
NOTE: LINE CLOCK DETERMINES VERTICAL HEIGHT, WHILE CHAR. CLOCK DETERMINES WIDTH OF CHARACTERS.

GRAPHICAL REPRESENTATION



VERTICAL RASTER SCAN APPLICATIONS

The seven outputs of the 3255 or 3256 are fed into a seven bit parallel to serial shift register. When the parallel enable to the shift register is activated, the seven bits of information, one column at a time are loaded into the shift register and then are shifted out to the video display. This operation is repeated for each of the five columns controlled by the internal line counter of the character generator. It should be noted that the vertical spacing between characters is obtained by adding non-addressed bits to the shift register.



GRAPHICAL REPRESENTATION

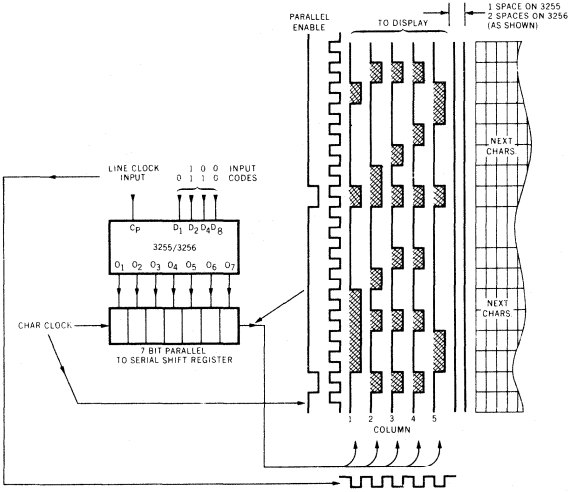
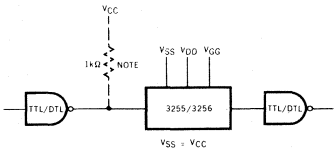


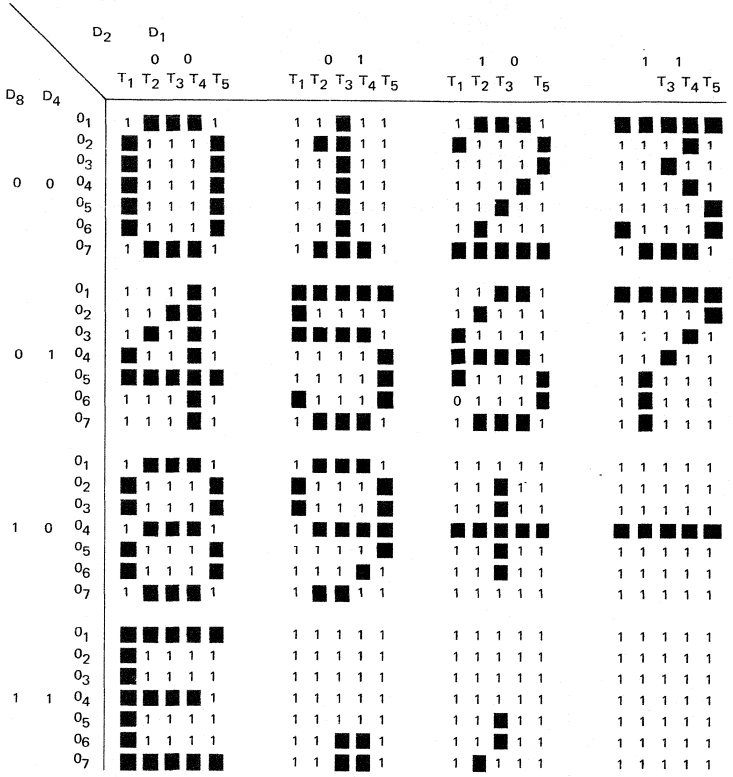
Fig. 9 INTERFACING



NOTE: Directly compatible at outputs with TTL/DTL. Inputs directly compatible with DTL. When being driven by TTL, no pullup resistor needed if TTL output swings to (V_{SS} −1) volts (e.g., if TTL is driving only one MOS device and no TTL devices).

CHARACTER FONT

DOT = LOW ≅ GND
BLANK = HIGH ≅ V_{SS}



ORDER PART NOS. A7K325519X and A7K325619X for character font shown. Any 16 character font may be made available upon request.

3257

DOT MATRIX CHARACTER GENERATOR 64 CHARACTERS 5 x 7 BITS

FAIRCHILD SILICON GATE MOS INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The 3257 is a Character Generator designed to display 64 characters in a 5 x 7 font. An on-chip column-select counter sequences through the 5 columns of each character. The 7 output buffers will each drive one TTμL/DTμL load directly at a 1 MHz input address rate making the 3257 an ideal device for vertical scan CRT displays. The chip enable allows Wired-OR capability if more than 64 characters are required.

FEATURES:

- **500 ns TYPICAL ACCESS TIME**
- **ASCII ENCODED**
- **DIRECT INTERFACING WITH TTμL/DTμL (FIGURE 11)**
- **WIRED–OR CAPABILITY**

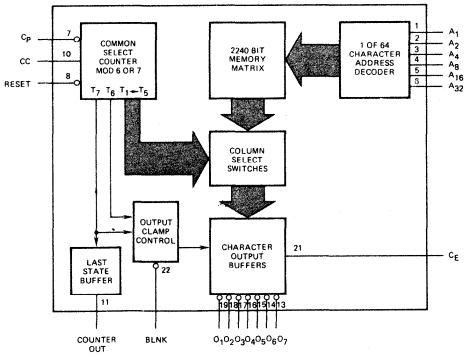
ABSOLUTE MAXIMUM RATINGS – (Above which useful life may be impaired)

Storage Temperature T_S	−65°C to +150°C
Operating Temperature T_A	0°C to +70°C
Voltage on any Pin Relative to V_{SS}	−20 V to +0.3 V

APPLICATIONS:

CRT Displays
Billboard Displays
LED Matrix Displays

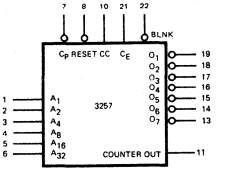
BLOCK DIAGRAM



V_{SS} = Pin 24
V_{GG} = Pin 23
V_{DD} = Pin 12

Fig. 4

LOGIC SYMBOL



V_{SS} = Pin 24
V_{GG} = Pin 23
V_{DD} = Pin 12

Fig. 1

PIN CONFIGURATION

TOP VIEW

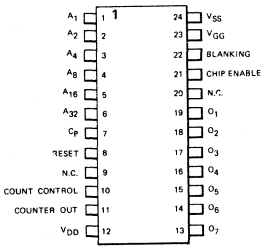
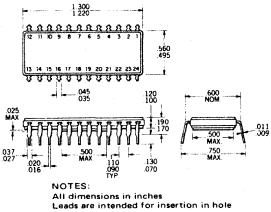


Fig. 2

PHYSICAL DIMENSIONS



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .600" centers. They are purposely shipped with "positive" misalignment to facilitate insertion
Base, cap and leads are gold-plated kovar
Package weight is 5.2 grams

Fig. 3

FAIRCHILD SEMICONDUCTOR

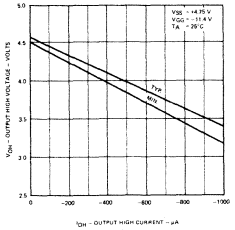
OPERATIONAL DESCRIPTION – A RESET pulse (~GND) is required to set the counter to the last state. A 6-bit binary word presented to the character address inputs is decoded to select 1 of 64 characters in the memory. Information, representing the first column of the character, is available the next clock time after RESET returns HIGH ($\sim V_{SS}$). The remaining 4 columns are sequentially selected by the next 4 states of the counter. The last state(s) of the counter clamps the outputs HIGH ($\sim V_{SS}$) to provide 1 or 2 space blanking between characters (COUNT MODE CONTROL $\sim V_{SS} \Rightarrow$ MOD 7, COUNT MODE CONTROL ~ GND $\Rightarrow$ MOD 6). When the last state (6th or 7th) of the counter is reached the COUNTER OUTPUT goes HIGH ($\sim V_{SS}$). When the CHIP ENABLE pin goes HIGH ($\sim V_{SS}$) the chip is activated while a LOW (~ GND) at this pin floats the outputs to allow common output bussing. A LOW (~GND) on the BLANKING input pulls the outputs HIGH ($\sim V_{SS}$), providing blanking, independent of the counter state or the character address.

D.C. CHARACTERISTICS – Standard Operating Conditions (unless otherwise specified)
$T_A = 0°C$ to $+70°C$, $V_{SS} = +5\ V \pm 5\%$, $V_{GG} = -12\ V \pm 5\%$, $V_{DD} = 0\ V$

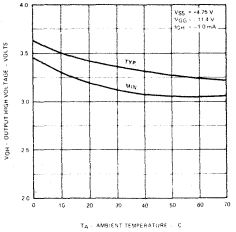
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
V_{IH}	Input High Voltage	$V_{SS}-1$		V_{SS}	Volts	Note 1
V_{IL}	Input Low Voltage	V_{GG}	0	0.85	Volts	Note 1
V_{OH}	Output High Voltage	$V_{SS}-0.5$		V_{SS}	Volts	$I_{OH} = -10\ \mu A$
		2.4	3.0	V_{SS}	Volts	$I_{OH} = -0.5$ mA
V_{OL}	Output Low Voltage	0	0.3	0.4	Volts	$I_{OL} = 1.6$ mA
I_{IL}	Input Leakage Current			−1.0	μA	$V_{SS} = 0\ V$, $V_{IN} = -18\ V$, Note 1
I_{OL}	Output Leakage Current			1.0	μA	$V_{SS} = 0\ V$, $V_{OUT} = -6\ V$, Note 2
C_{IN}	Input Capacitance		5.0	1.0	pF	f = 1.0 MHz, 0V Bias, Note 1
I_{SS}	Supply Current Drain		20	40	mA	$V_{SS} = 5.25\ V$, $V_{GG} = -12.6\ V$ Outputs Open
P_C	Power Consumtpion		360	715	mW	

NOTES:
1. Inputs include CHARACTER ADDRESS, COUNT CONTROL, CLOCK and RESET.
2. CHIP ENABLE = LOW
3. $I_{SS} = -I_{GG}$ (V_{GG} Supply Current)

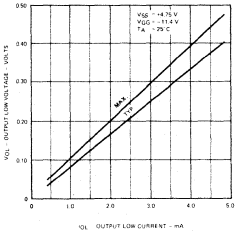
OUTPUT HIGH VOLTAGE VERSUS OUTPUT CURRENT



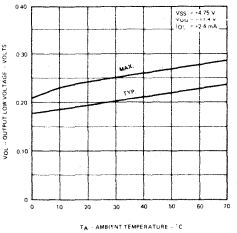
OUTPUT HIGH VOLTAGE VERSUS AMBIENT TEMPERATURE



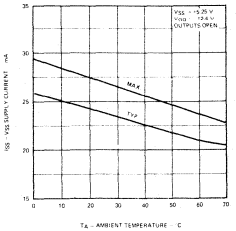
OUTPUT LOW VOLTAGE VERSUS OUTPUT CURRENT



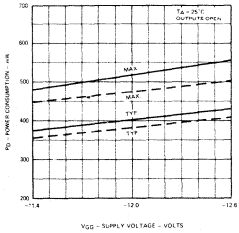
OUTPUT LOW VOLTAGE VERSUS AMBIENT TEMPERATURE



WORST CASE V_{SS} SUPPLY CURRENT VERSUS AMBIENT TEMPERATURE



POWER DISSIPATION VERSUS SUPPLY VOLTAGE

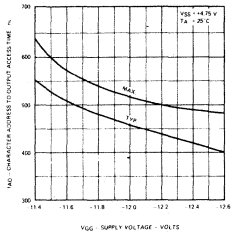


A.C. ELECTRICAL CHARACTERISTICS – Standard Test Conditions (unless otherwise specified)
V_{SS} = +5 V ±0.25 V, V_{GG} = −12 V ±0.6 V, V_{DD} = 0 V, T_A = 0°C to +70°C, C_L = 10 pF

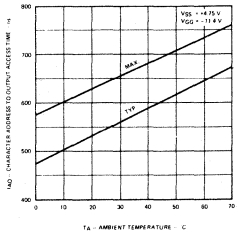
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
f	Clock Frequency	DC		1.0	MHz	
C_{pw}	Clock Pulse Width	500			ns	
t_r, t_f	Clock Rise & Fall Time (10%-90%)			2.0	μs	
R_{pw}	Reset Pulse Width	500			ns	
t_{CRD}	Clock to Reset Time Delay	100	300		ns	Fig. 9
t_{AO}	Character Address to Output Access Time		500	1000	ns	Notes 4 & 5, Fig. 5
t_{CO}	Clock to Output Access Time		500	1000	ns	Notes 4 & 5, Fig. 6
t_{RO}	Reset to Output Time Delay		300	600	ns	Notes 4 & 5, Fig. 7
t_{BO}	Blanking to Output Time Delay		300	1000	ns	Notes 4 & 5, Fig. 10
t_{CCO}	Clock to Counter Output Time Delay		300	500	ns	Notes 4 & 5, Fig. 6
t_{CRO}	Reset to Counter Output Time Delay		300	500	ns	Notes 4 & 5, Fig. 7
t_{OE}	Output Enable Delay Time		300	600	ns	Notes 4 & 5, Fig. 8
t_{OD}	Output Disable Delay Time		300	600	ns	Notes 4 & 5, Fig. 8

NOTES:
4. A.C. Output LOW level is defined as 0.4 volts @ 1.6 mA, current sinking (i.e., 1 TTμL load).
5. A.C. Output HIGH level is defined as 2.4 volts @ −0.6 mA, current sourcing (i.e., 1 TTμL load).

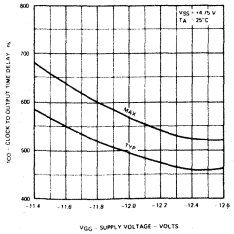
CHARACTER ADDRESS TO OUTPUT ACCESS TIME VERSUS SUPPLY VOLTAGE



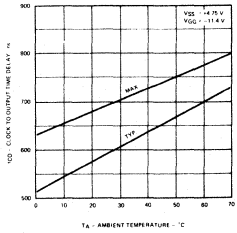
CHARACTER ADDRESS TO OUTPUT ACCESS TIME VERSUS AMBIENT TEMPERATURE



CLOCK TO OUTPUT TIME DELAY VERSUS SUPPLY VOLTAGE



CLOCK TO OUTPUT TIME DELAY VERSUS AMBIENT TEMPERATURE



TIMING DIAGRAM

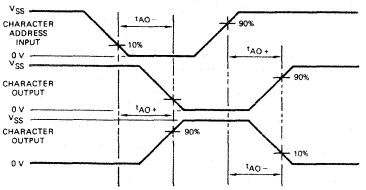


Fig. 5

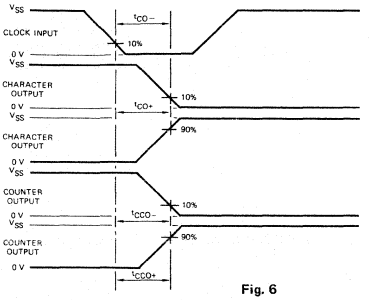


Fig. 6

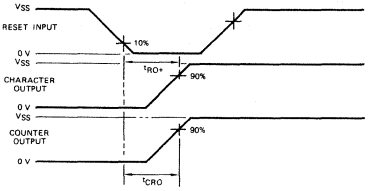


Fig. 7

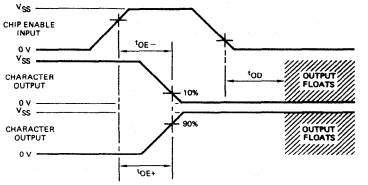


Fig. 8

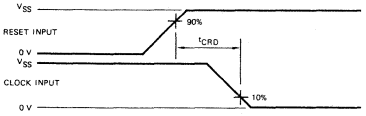


Fig. 9

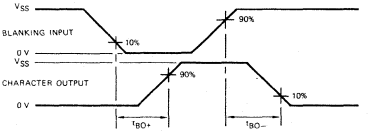
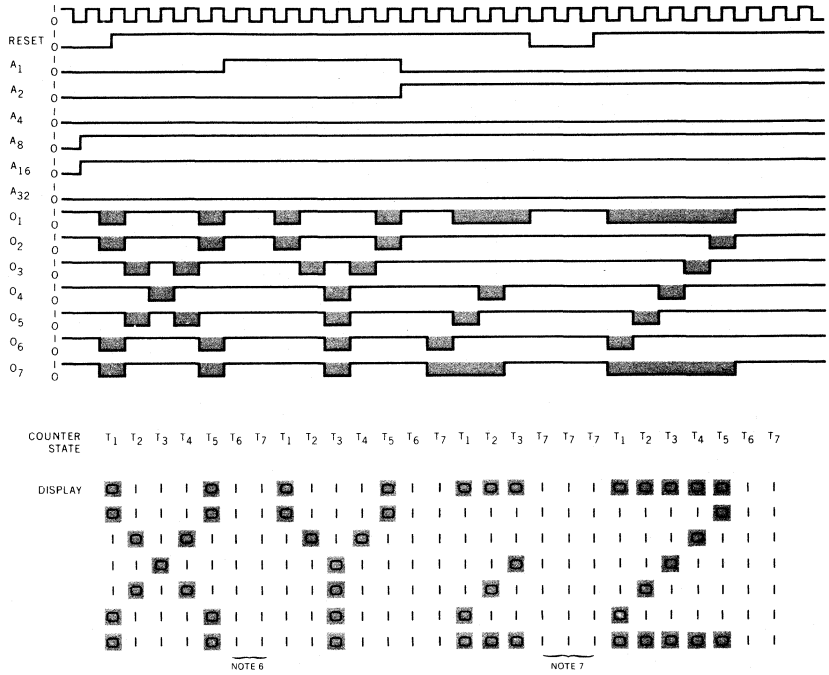


Fig. 10

GLOSSARY OF TERMS

1. V_{SS} The most positive voltage applied to the device.
2. V_{GG} The most negative voltage applied to the device.
3. V_{DD} The next most negative voltage applied to the device.
4. t_{CRD} Clock to reset time delay – reset must return to a logical HIGH within the period t_{CRD}, before a positive to negative clock transition to insure character output levels during that clock time.
5. t_{AO} The time for a character output to change logic levels after a character input changes logic levels.
6. t_{CO} Time for a character output to change logic levels after the clock input reaches a logic LOW level.
7. t_{RO} Time for a character output to reach a logic HIGH after reset reaches a logic LOW.
8. t_{BO} Time for a character output to change logic levels after the blanking input changes logic levels.
9. t_{CCO} Time for the counter output to change logic levels after the clock input reaches a logic LOW level.
10. t_{CRO} Time for the counter output to reach a logic HIGH level after the reset input reaches a logic LOW level.
11. t_{OE} Time before information is available at the character outputs after the chip enable input reaches a logic HIGH level.
12. t_{OD} Time before the character outputs are disabled after the chip enable input reaches a logic LOW level.

TYPICAL FUNCTIONAL TIMING DIAGRAM



NOTES:
6. Last two counter states (count mode control = HIGH ⇒ MOD 7) provide blanking.
7. Counter is Reset to the last state.

INTERFACING

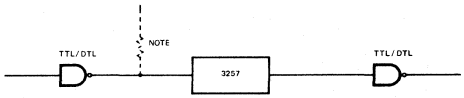
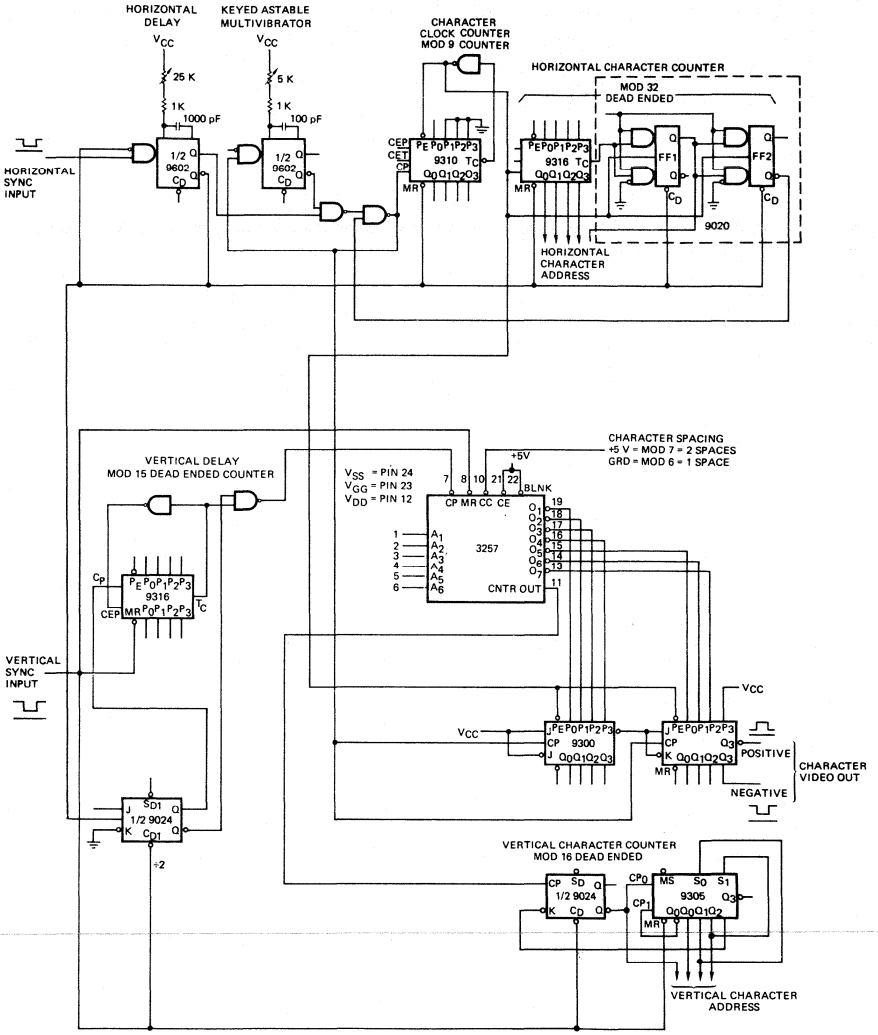


Fig. 11

Note: Directly compatible at outputs with TTμL/DTμL. Inputs directly compatible with DTμL. When being driven by TTμL, no pullup resistor needed if TTμL output swings to (V_{SS} −1) volts.



NOTE:
Horizontal and vertical are referred to as in a standard T.V. type raster.
16 Characters per line, 32 character lines in system.
Each character 10 raster lines wide.

Fig. 12 TYPICAL VERTICAL RASTER SCAN APPLICATION

ORDERING INFORMATION

Order A7C325719X for character font shown

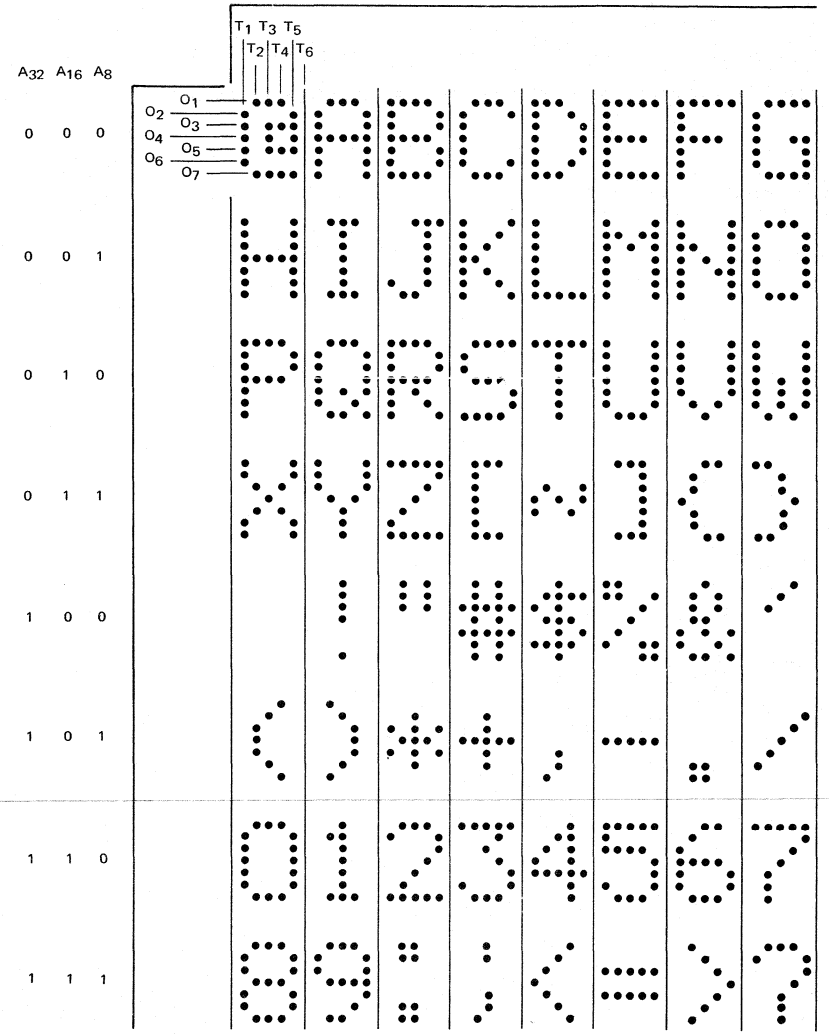
Additional patterns may be made available upon request. The 3257 is programmed on IBM cards or IBM forms in the coding format shown below:

A logical "1" = A more positive voltage nominally +5 V
A logical "0" = A more negative voltage nominally 0 V
The character "dots" are defined as logic "0"

6, 7, 8, 9, 10, 11	Character address input code. The most significant bit (A32) is in column 11.
22, 23, 24, 25, 26, 27, 28	The first column of the character addressed. The most significant bit (07) is in Column 28.
30, 31, 32, 33, 34, 35, 36	The next column of the character addressed. The most significant bit (07) is in Column 36.
38, 39, 40, 41, 42, 43, 44	The next column of the character addressed. The most significant bit (07) is in Column 44.
46, 47, 48, 49, 50, 51, 52	The next column of the character addressed. The most significant bit (07) is in Column 52.
54, 55, 56, 57, 58, 59, 60	The last column of the character addressed. The most significant bit (07) is in Column 60.
73, 74, 75, 76, 77, 78, 79, 80	Coding these columns is not essential and may be used for card identification purpose.

3257 CHARACTER FONT FOR (COUNT MODE CONTROL ≅ GND ⇒ MOD 6)

A_1	0	1	0	1	0	1	0	1
A_2	0	0	1	1	0	0	1	1
A_4	0	0	0	0	1	1	1	1



3258
DOT MATRIX CHARACTER GENERATOR
64 CHARACTERS 5 x 7 BITS
FAIRCHILD SILICON GATE MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The 3258 is a character generator designed to display 64 characters in a 5 x 7 dot matrix. An on-chip row-select counter sequences through the seven rows of each character. The five output buffers will each drive one TTL/DTL load directly at a 1.6 MHz input address rate making the 3258 an ideal device for CRT displays. Special input amplifiers on the CLOCK, MASTER RESET, and ADDRESS lines have eliminated the need for pull-up resistors and allow direct operation at TTL/DTL logic levels.

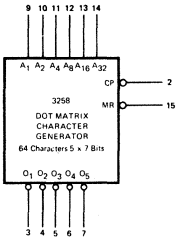
- **500 ns TYPICAL ACCESS TIME**
- **16 PIN DUAL IN-LINE PACKAGE**
- **DIRECT TTL/DTL INTERFACE AT INPUTS AND OUTPUTS**
- **ON-CHIP ROW-SELECT COUNTER**
- **ASCII ENCODED**

ABSOLUTE MAXIMUM RATINGS – (Above which useful life may be impaired)

Storage Temperature T_S	−65° to +150°C
Operating Temperature T_A	0°C to +70°C
Voltage on any Pin Relative to V_{SS}	−20 V to +0.3 V

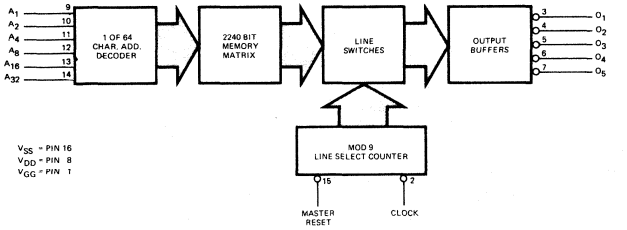
APPLICATIONS:
CRT Displays
Billboard Displays
LED Matrix Displays

LOGIC SYMBOL



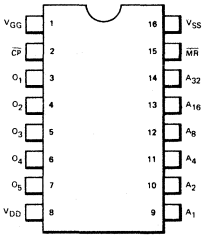
V_{SS} = PIN 16
V_{DD} = PIN 8
V_{GG} = PIN 1

LOGIC BLOCK DIAGRAM



V_{SS} = PIN 16
V_{DD} = PIN 8
V_{GG} = PIN 1

CONNECTION DIAGRAM
(TOP VIEW)



FAIRCHILD SEMICONDUCTOR

OPERATIONAL DESCRIPTION – A MASTER RESET pulse (≅GND) is required to set the Modulo 9 counter to the first state. A 6-bit binary word present at the address inputs is decoded to select 1 of 64 characters in the memory. Information, representing the first row of the character, will be available at the five outputs the next clock time after the MASTER RESET goes HIGH (≅V_{SS}). The next 6 rows of the character are sequentially selected by the counter. The last state of the counter, like the first state, clamps the outputs HIGH (≅V_{SS}) which provides 2 space blanking between lines. The counter dead ends at the last state and the outputs will remain HIGH (≅V_{SS}) providing blanking, until another MASTER RESET pulse is provided.

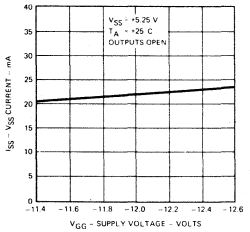
D C ELECTRICAL CHARACTERISTICS – Standard Operating Conditions (unless otherwise specified)
V_{SS} = +5 V ±5%, V_{GG} = −12 V ±5%, V_{DD} = 0 V, 0°C ≤ T_A ≤ 70°C

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
V_{IH}	Input HIGH Voltage	2.0		V_{SS}	Volts	V_{SS} = V_{CC} = +4.75 V (Note 1)
		2.5		V_{SS}	Volts	V_{SS} = V_{CC} = +5.25 V
V_{IL}	Input LOW Voltage	V_{GG}	0	0.55	Volts	Note 1
V_{OH}	Output HIGH Voltage	2.4	3.5	V_{SS}	Volts	I_{OH} = −0.5 mA
V_{OL}	Output LOW Voltage	0	0.3	0.4	Volts	I_{OL} = 2.4 mA
I_{IL}	Input Leakage Current			1.0	μA	V_{IN} = −13 V (Note 1)
C_{IN}	Input Capacitance		5.0	10	pF	f = 1 MHz, 0 V Bias (Note 1)
I_{SS}	V_{SS} Supply Current		23	28	mA	V_{SS} = +5.25 V, V_{GG} = −12.6 V, Outputs Open
I_{GG}	V_{GG} Supply Current		23	28	mA	V_{SS} = +5.25 V, V_{GG} = 12.6 V, Outputs Open
P_D	Power Dissipation		410	500	mW	

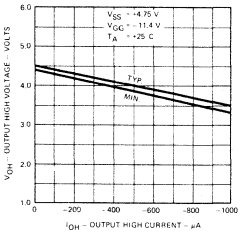
NOTE 1: Inputs include Character Address, Count Control, Clock, and Master Reset.

TYPICAL ELECTRICAL CHARACTERISTICS

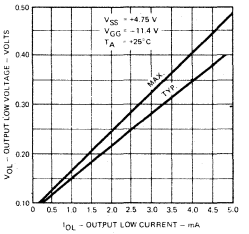
SUPPLY CURRENT VERSUS SUPPLY VOLTAGE



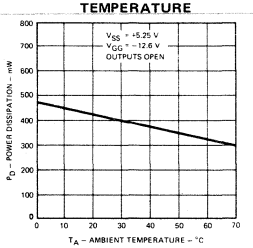
OUTPUT HIGH VOLTAGE VERSUS OUTPUT HIGH CURRENT



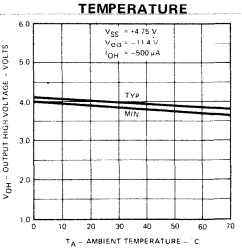
OUTPUT LOW VOLTAGE VERSUS OUTPUT LOW CURRENT



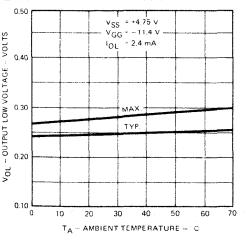
POWER DISSIPATION VERSUS TEMPERATURE



OUTPUT HIGH VOLTAGE VERSUS TEMPERATURE



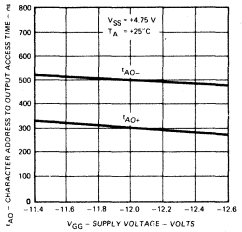
OUTPUT LOW VOLTAGE VERSUS TEMPERATURE



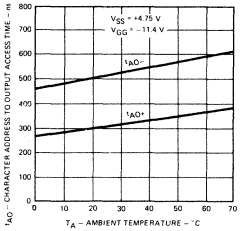
A C ELECTRICAL CHARACTERISTICS – Standard Operating Conditions (unless otherwise specified)
V_{SS} = +5 V ±5%, V_{GG} = –12 V ±5%, V_{DD} = 0 V, T_A = 0°C to +70°C, C_L = 10 pF

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
f	Clock Frequency	0		500	kHz	
$t_{\phi w}$	Clock Pulse Width	1.0			μs	
t_r, t_f	Clock Rise and Fall Time			2.0	μs	
t_{RW}	Reset Pulse Width	500			ns	
t_{CRD}	Clock to Reset Time Delay	200			ns	
t_{AO}	Character Address to Output Time Delay		500	625	ns	Figure 1 & 2
t_{CO}	Clock to Output Time Delay			2.0	μs	Figure 1 & 3
t_{RO}	Reset to Output Time Delay			2.0	μs	Figure 1 & 4

CHARACTER ADDRESS TO OUTPUT ACCESS TIME VERSUS SUPPLY VOLTAGE



CHARACTER ADDRESS TO OUTPUT ACCESS TIME VERSUS AMBIENT TEMPERATURE



ACCESS TIME TEST CIRCUIT

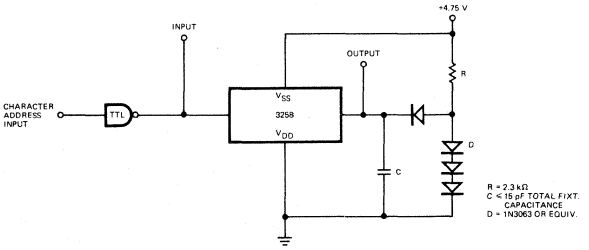


Fig. 1

TIMING DIAGRAMS

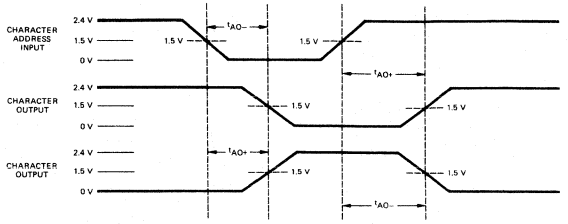


Fig. 2

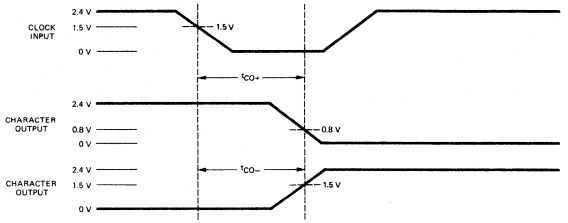


Fig. 3

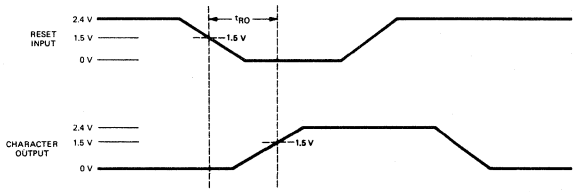
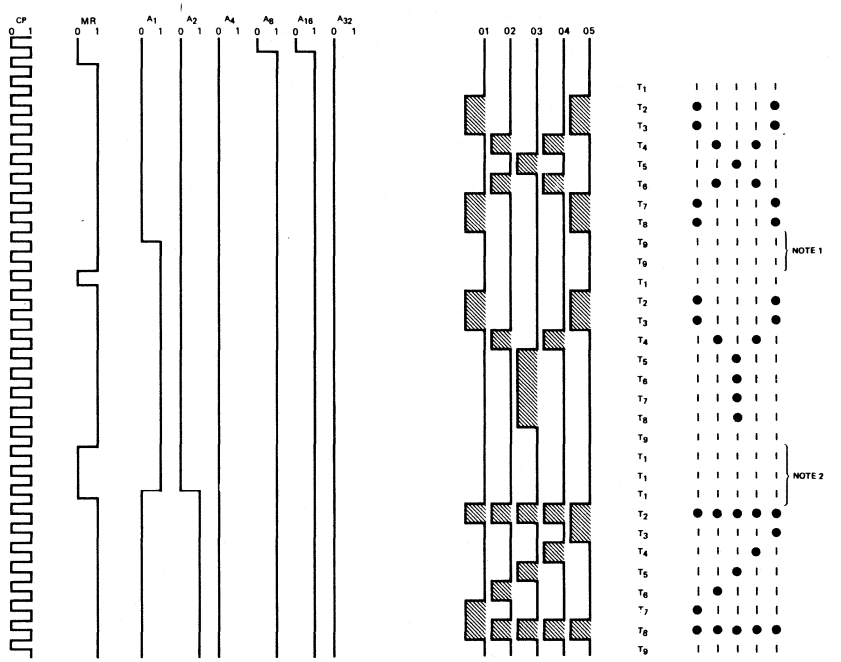


Fig. 4

GLOSSARY OF TERMS

1. V_{SS} The most positive voltage applied to the device.
2. V_{GG} The most negative voltage applied to the device.
3. V_{DD} The next most negative voltage applied to the device.
4. t_{CRD} Clock to reset time delay – reset must return to a logical HIGH within the period t_{CRD}, before a positive to negative clock transition to insure character output levels during that clock time.
5. t_{AO} The time for a character output to change logic levels after a character input changes logic levels.
6. t_{CO} Time for a character output to change logic levels after the clock input reaches a logic LOW level.
7. t_{RO} Time for a character output to reach a logic HIGH after reset reaches a logic LOW.

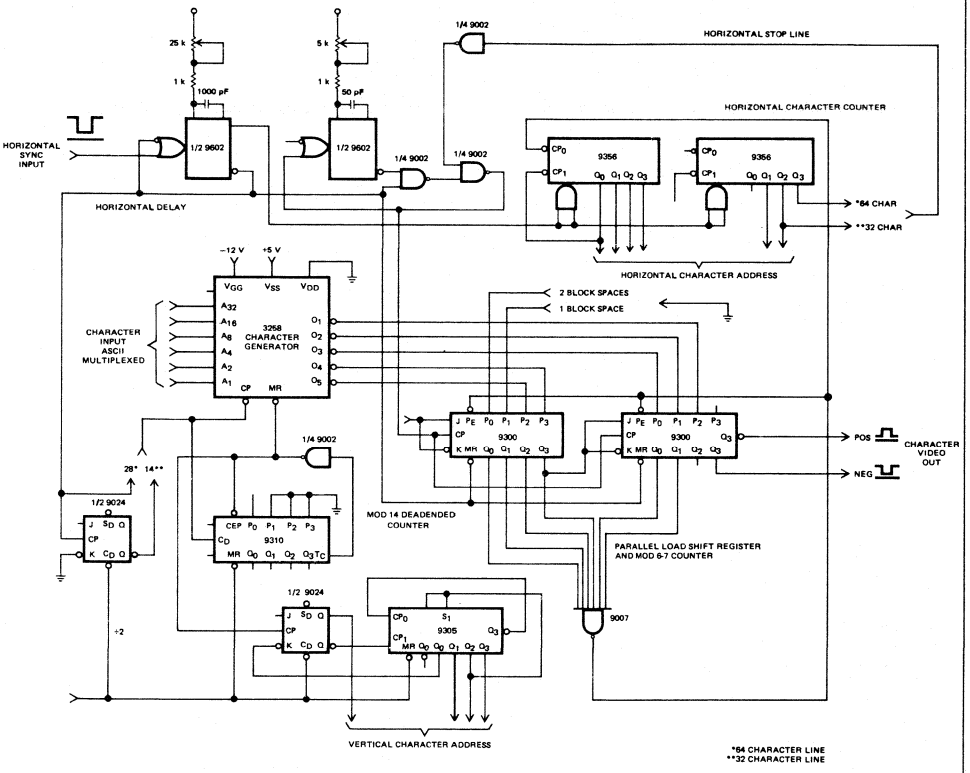
FUNCTIONAL TIMING DIAGRAM



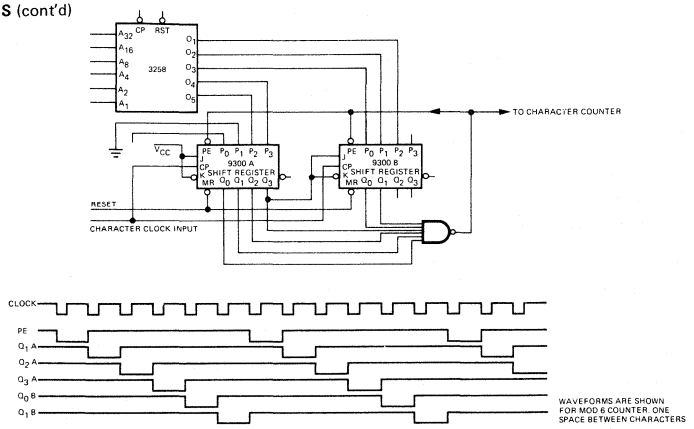
NOTES:
1. Counter dead ends at last state.
2. Counter is reset to first state.

APPLICATIONS

HORIZONTAL RASTER SCAN CHARACTER GENERATOR



APPLICATIONS (cont'd)



OPERATION:

The two 9300 registers and the 9008, eight-input gate combine to form the character clock counter and the parallel to serial converter required for the outputs of the 3258 character generator.

When all the gate inputs are high, the gate output is low which enables the parallel load (PE) of the shift registers. On the next clock pulse, positive edge after PE goes low, the contents of the 3258 character generator and the LOW on P_0 (A) are transferred into the registers. This LOW is shifted down the registers followed by all HIGH's from the JK input. On reaching Q_2 (B) all the outputs to the gates are once again high, therefore reloading the shift registers again. The modulo count of the system can easily be changed to Modulo 7 by loading in a zero on P_0 (A).

The shift counter is reset at the beginning of each horizontal raster line to ensure that it has the correct time phase.

ORDERING INFORMATION

Order A7K3258191 for character font shown.

Additional character fonts are available on request. The 3258 is programmed on IBM cards or IBM coding forms in the coding format shown below:

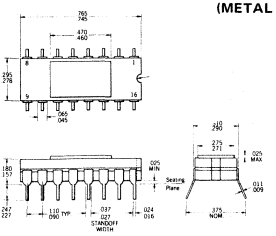
A logical "1" = A more positive voltage nominally +5 V
A logical "0" = A more negative voltage nominally 0 V

The character must be defined by a logical "0". The background by a logical "1". Each character is programmed on one IBM card or a single line on the coding form.

COLUMN NUMBER	DESCRIPTION
6,7,8,9,10,11	Character address input code. The most significant bit (A32) is in Column 11.
22,23,24,25,26	The top line of the character addressed. The most significant bit (05) is in Column 26.
28,29,30,31,32	The next line of the character addressed. The most significant bit (05) is in Column 32.
34,35,36,37,38	The next line of the character addressed. The most significant bit (05) is in Column 38.
40,41,42,43,44	The next line of the character addressed. The most significant bit (05) is in Column 44.
46,47,48,49,50	The next line of the character addressed. The most significant bit (05) is in Column 50.
52,53,54,55,56	The next line of the character addressed. The most significant bit (05) is in Column 56.
58,59,60,61,62	The bottom line of the character addressed. The most significant bit (05) is in Column 62.
73,74,75,76,77,78,79,80	Coding these columns is not essential and may be used for card identification purpose.

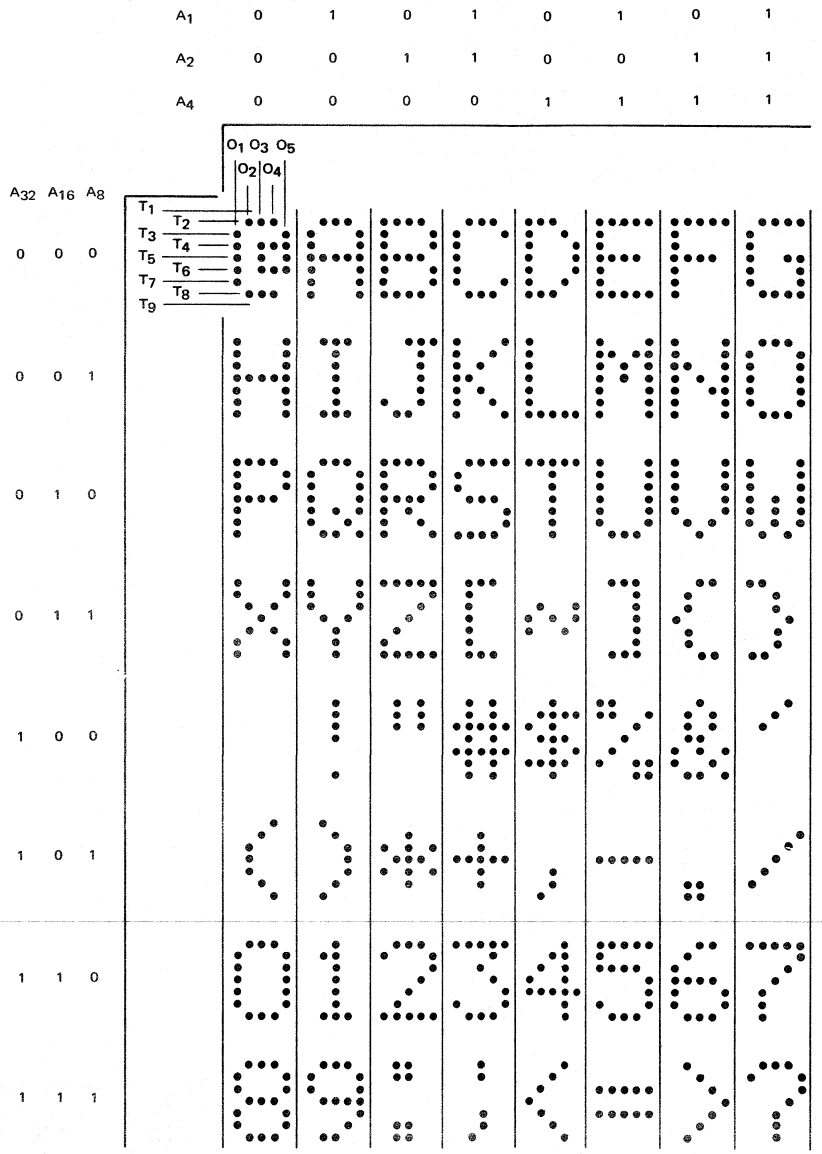
PACKAGE INFORMATION

16 LEAD DUAL IN-LINE (METAL CAP)



NOTES
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" misalignment to facilitate insertion.
Board-drilling dimensions should equal your practice for .010 inch diameter lead
Leads are gold-plated kovar
Package weight is 1.3 grams

3258 CHARACTER FONT



3303

DUAL 25-BIT DYNAMIC SHIFT REGISTER

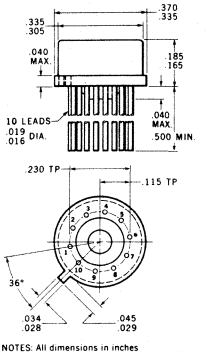
MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 3303 is a dual 25-bit dynamic shift register. It is a monolithic integrated circuit utilizing Planar* II, P-Channel enhancement mode MOS technology. A two phase clock is used to reduce power consumption and increase speed.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Clock Voltages ($V_{\phi_1} = V_{\phi_2}$)	−30 V to +0.3 V
Data Input Voltage (V_{in})	−30 V to +0.3 V
Supply Voltage	−30 V to +0.3 V
Storage Temperature	−65°C to +150°C
Operating Temperature (330314X)	−55°C to +85°C
Operating Temperature (330319X)	0°C to +70°C

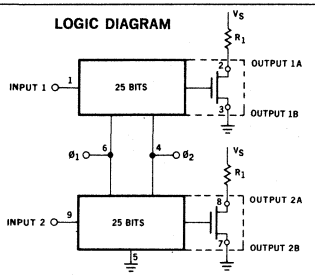
PHYSICAL DIMENSIONS
(In accordance with JEDEC TO−100)



NOTES: All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.02 grams

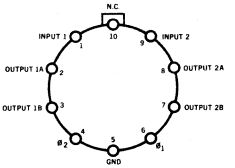
ORDER PART NOS. A5F330314X
A5F330319X

LOGIC DIAGRAM



The output device requires an external resistor (R_1), ground and power supply (V_S) and can be used either as an inverter or source follower (inverter shown).

CONNECTION DIAGRAM



TOP VIEW

NOTE:
(1) These ratings are limiting values above which the serviceability of the device may be impaired.

Electrical Characteristics on Page 2

*Planar is a patented Fairchild process.

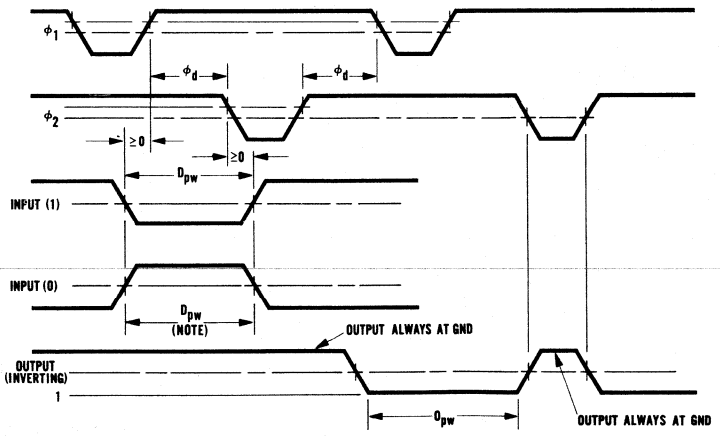
FAIRCHILD
SEMICONDUCTOR

FAIRCHILD MOS INTEGRATED CIRCUIT 3303

ELECTRICAL CHARACTERISTICS
STANDARD CONDITIONS (unless otherwise specified)
Load . . . 10 MΩ and 10 pF
$V_s = -15\ V \pm 1.0\ V$, $V_{\phi} = -27\ V \pm 1.0\ V$
$R_l = 20\ k\Omega$, $T_A = -55°C$ to $+85°C$ or $0°C$ to $+70°C$

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
ϕ_1, ϕ_2	Clock Repetition Rate	10		500	kHz	
ϕ_{1w}, ϕ_{2w}	Clock Pulse Width	0.4		45	μs	
ϕ_d	Clock Delay	0.4			μs	
V_{ϕ}	Clock Pulse Amplitude					
	"0" Level	0		−0.5	Volts	
	"1" Level	−26		−28	Volts	
	Clock Pulse Rise and Fall Time (10% - 90%)			100	ns	
V_{in}	Data Input Logic Levels					
	Logic "0"	0		−2.0	Volts	
	Logic "1"	−9.0			Volts	$\phi_1 = 0.4\ \mu s$
D_{pw}	Data Pulse Width	200			ns	$\phi_2 = 0.4\ \mu s$
V_o	Output Logic Levels					
	Logic "0"			−1.0	Volts	
	Logic "1"	−10			Volts	
	Output Fall Time			550	ns	
O_{pw}	Output Pulse Width	1.0			μs	
R_o	Output Impedance to Ground			1000	Ω	
I_{CL}	Clock Input Leakage Current			100	μA	$V_{\phi} = -26\ V$
	Data Input Capacitance		4.0		pF	$V_{\phi} = 0\ V$
	Clock Input Capacitance		20		pF	$V_{\phi} = 0\ V$
	Fan In			1.0		
	Fan Out			5.0		

TYPICAL WAVEFORMS



Note: $D_{PW} \geq \phi_d$ if input data is "0"

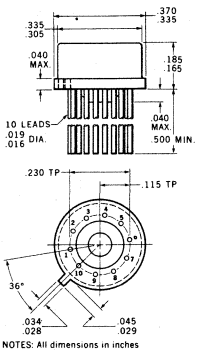
3304
DUAL 16-BIT STATIC SHIFT REGISTER
MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 3304 is a Dual 16-Bit Static Shift Register. It is a monolithic integrated circuit utilizing Planar II*, P-Channel Enhancement Mode MOS Technology. It is designed to operate on a two phase clock in delay line or in serial binary or BCD data storage applications. For DC storage conditions, it is important that ϕ_1 is a logic "0" and ϕ_2 is a logic "1".

ABSOLUTE MAXIMUM RATINGS (Note 1)

Drain Voltage (V_{DD})	−30 V to +0.3 V
Gate Voltage (V_{GG})	−30 V to +0.3 V
Clock and Data Input Voltages	−30 V to +0.3 V
Storage Temperature	−55°C to +150°C
Operating Temperature Range	−55°C to +85°C
	0°C to +70°C
Power Dissipation at $T_A = 25°C$	200 mW

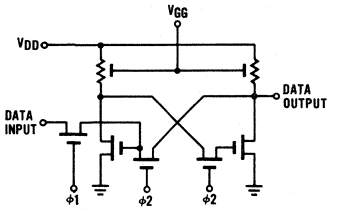
PHYSICAL DIMENSIONS
(In accordance with JEDEC TO−100)



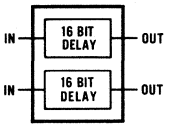
NOTES: All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.02 grams

ORDER PART # A5F330414X (−55°C to +85°C)
ORDER PART # A5F330419X (0°C to +70°C)

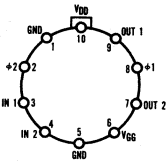
SCHEMATIC DIAGRAM
(ONE BIT)



BLOCK DIAGRAM



CONNECTION DIAGRAM
TOP VIEW



NOTE:
(1) These ratings are limiting values above which the serviceability of the device may be impaired.

*Planar is a patented Fairchild process.

FAIRCHILD
SEMICONDUCTOR

MOS INTEGRATED CIRCUIT 3304

ELECTRICAL CHARACTERISTICS

(V_{DD} = −13 Volts ±1 Volt, V_{GG} = −27 Volts ± 1 Volt, Load = 10 MΩ and 10 pF, T_A = −55°C to +85°C, unless otherwise specified)

CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Clock Repetition Rate	D.C.		1.0	MHz	
Clock Pulse Widths					
ϕ_1 pw	0.4		10	μs	See Figure 1
ϕ_2 pw	0.4			μs	See Figure 1
Clock Delay (ϕd)	0.01		10	μs	See Figure 1
Clock Pulse Rise and Fall Time (10% to 90%)			5.0	μs	See Figure 1
Clock Pulse Logic Levels (ϕ_1 & ϕ_2)					
Logic "0"			−2.0	Volts	
Logic "1"	−26		−28	Volts	
Clock Pulse Input Capacitance (ϕ_1 & ϕ_2)		4.0		pF	$\phi_1 = \phi_2$ = 0 Volt
Data Pulse Width (Dpw)	0.4			μs	
Data Input Capacitance		2.0		pF	V_{IN} = 0 Volt
Data Input Logic Levels					
Logic "0"			−2.0	Volts	
Logic "1"	−9.0			Volts	
Data Input Leakage Current			1.0	μA	V_{IN} = −20 Volts
Clock Input Leakage Current			100	μA	V_{IN} = −26 Volts
Clock (ϕ_2) Input Impedance	60			kΩ	ϕ_1 = −26 Volts ϕ_2 = 0 Volt
Output Logic Levels					
Logic "0"		−0.5	−1.0	Volts	
Logic "1"	−10	−11		Volts	
Output Impedance to Ground		2.0	3.0	kΩ	Output at Logic "0"
Output Drive Capability	−5.0			Volts	R_L = 4.0 kΩ to Ground
Power Supply Current Drain V_{DD}			10	mA	V_{DD} = −13 Volts
Power Supply Current Drain V_{GG}			2.0	mA	V_{GG} = −27 Volts

TIMING DIAGRAMS

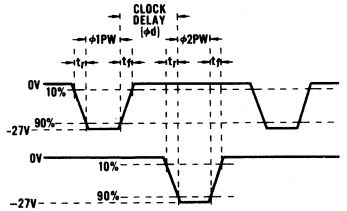


Figure 1

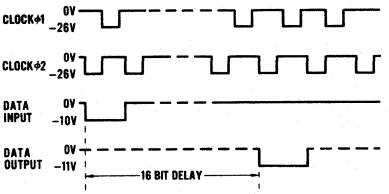
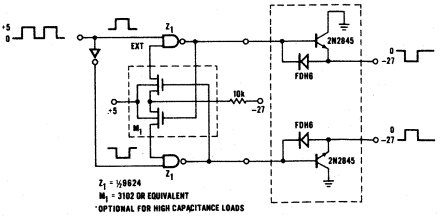


Figure 2



2 PHASE-NON-OVERLAPPING CLOCK DRIVER

3305/6
64-BIT 1Ø STATIC SHIFT REGISTER
MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 3305/6 is a 64-bit 1ϕ static shift register. The 3305 is a Quad 16 in a DIP package and the 3306 is a Dual 16, Single 32 in a TO-100 package. It is a monolithic integrated circuit utilizing Planar II*, P-channel Enhancement Mode Technology.

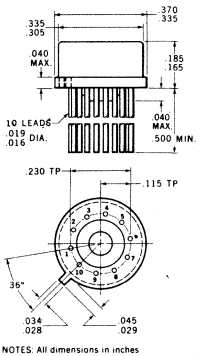
FEATURES:
- **SINGLE PHASE CLOCK**
- **LOW POWER CONSUMPTION — LESS THAN 3 mW/BIT**
- **HIGH SPEED OPERATION — DC TO 1.0 MHz**

APPLICATIONS:
Delay line and binary or BCD storage in:
- **Calculators**
- **Peripheral Equipment**
- **Data Acquisition**
- **Telemetry**
- **Computers and Business Machines**
- **Machine Control**

ABSOLUTE MAXIMUM RATINGS (Note 1)

Drain Voltage (V_{DD})	−30 V to +0.3 V
Gate Voltage (V_{GG})	−30 V to +0.3 V
Clock and Data Input Voltages	−30 V to +0.3 V
Storage Temperature	−55°C to +150°C
Operating Temperature Range	−55°C to +85°C
Power Dissipation at $T_A = 25°C$	300 mW

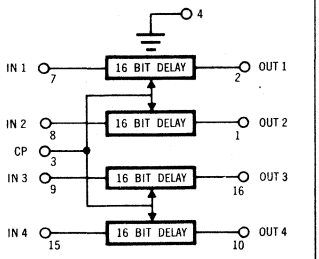
PHYSICAL DIMENSIONS
(In accordance with JEDEC TO−100)



NOTES: All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.02 grams

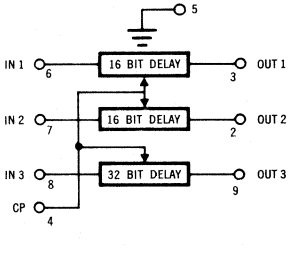
ORDER PART NO. A5F330614X

3305 BLOCK DIAGRAM



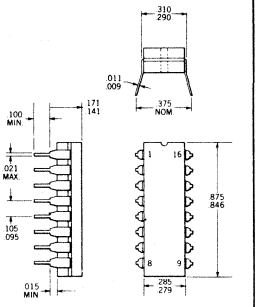
V_{GG} pin 12, V_{DD} pin 13

3306 BLOCK DIAGRAM



V_{GG} pin 10
V_{DD} pin 1
Gnd pin 5

PHYSICAL DIMENSIONS



ORDER PART NO. A6J330514X

*Planar is a patented Fairchild process.

FAIRCHILD
SEMICONDUCTOR

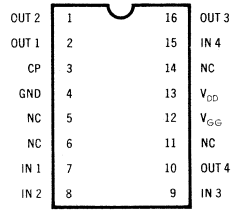
FAIRCHILD MOS INTEGRATED CIRCUIT 3305/6

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V_{GG} = -27 \pm 2$ V, $V_{DD} = -13 \pm 2$ V, unless otherwise specified)

SYMBOL	CHARACTERISTICS		MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
	Power Consumption			200		mW	
	Operating Frequency		d.c.		1.0	MHz	$V_{GG} = -27$ V
V_{CP}	Clock Pulse Amplitude	"0" level			−2.0	Volts	
		"1" level	−9.0			Volts	
W_{CP}	Clock Pulse Width		0.3		100	μs	
	Clock Pulse Rise and Fall Time				10	μs	
	Clock Capacitance			8.0		pF	$V_{CP} = 0$ V
I_{CL}	Clock Leakage Current				−1.0	μA	$V_{CP} = -20$ V
V_{IL}	Input Amplitude	"0" level			−2.0	Volts	
V_{IH}		"1" level	−9.0			Volts	
C_{in}	Input Capacitance			2.5		pF	$V_{in} = 0$ V
I_{IL}	Input Leakage Current				−1.0	μA	$V_{in} = -20$ V
V_{OL}	Output Levels	"0" level			−1.0	Volts	$I_{out} = -10$ μA
V_{OH}		"1" level	−10			Volts	$I_{out} = -10$ μA
t_{df}	Time Delay Fall			0.4	0.5	μs	$V_{GG} = -27$ V
t_{dr}	Time Delay-Rise			0.4	0.5	μs	$V_{GG} = -27$ V

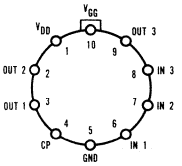
3305 CONNECTION DIAGRAM

TOP VIEW

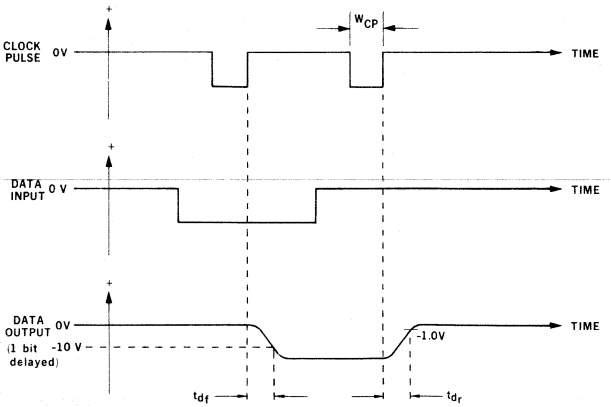


3306 CONNECTION DIAGRAM

TOP VIEW



TIMING DIAGRAM



3307

DUAL 100-BIT STATIC SHIFT REGISTER

MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 3307 is a Dual 100-Bit Static Shift Register with independent Inputs and Outputs. It is a monolithic integrated circuit utilizing Planar II*, P-Channel Enhancement Mode MOS Technology. It is designed to operate on a two phase clock in delay line or in serial binary or BCD data storage application. For DC storage conditions, it is important that ϕ_1 is a logic "0" and ϕ_2 is a logic "1".

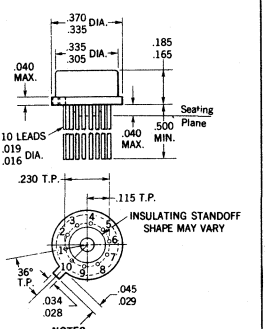
ABSOLUTE MAXIMUM RATINGS (Note 1)

Drain Voltage (V_{DD})	−30 V to +0.3 V
Gate Voltage (V_{GG})	−30 V to +0.3 V
Clock and Data Input Voltages	−30 V to +0.3 V
Storage Temperature	−55°C to +150°C
Operating Temperature Range	−55°C to +85°C
	0°C to +70°C
Power Dissipation at $T_A = 25°C$	350 mW

ORDER INFORMATION

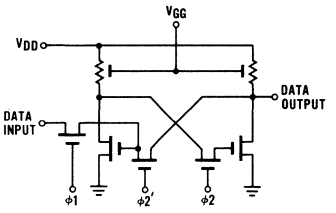
A5F3307141 (−55°C to +85°C, 1.0 MHz operation)
A5F3307192 (0°C to +70°C, 0.5 MHz operation)

PHYSICAL DIMENSIONS
(In accordance with JEDEC TO-100)

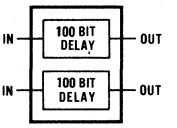


NOTES:
All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.32 grams
Lead 5 is connected to case

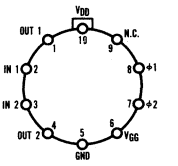
SCHEMATIC DIAGRAM
(ONE BIT)



BLOCK DIAGRAM



CONNECTION DIAGRAM
TOP VIEW



NOTE:
(1) These ratings are limiting values above which the serviceability of the device may be impaired.

*Planar is a patented Fairchild process.

FAIRCHILD
SEMICONDUCTOR

FAIRCHILD MOS INTEGRATED CIRCUIT 3307

ELECTRICAL CHARACTERISTICS *See Figure 1

DEVICE TYPE	TEMPERATURE RANGE	CLOCK REPETITION RATE	CLOCK PULSE WIDTH* ϕ_1 PW MIN.	ϕ_1 PW MAX.	ϕ_2 PW MIN.	ϕ_2 PW MAX.	DATA PULSE WIDTH*
3307141	−55°C to +85°C	DC to 1.0 MHz	0.4 μs	10 μs	0.4 μs	∞	0.4 μs
3307192	0°C to +70°C	DC to 0.5 MHz	0.8 μs	10 μs	0.8 μs	∞	0.8 μs

(V_{DD} = −13 Volts ±1 Volt, V_{GG} = −27 Volts ±2 Volts, Load = 10 MΩ and 10 pF, T_A = −55°C to +85°C, unless otherwise specified, for all types)

CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Clock Delay (ϕd)	0.01		10	μs	See Figure 1
Clock Pulse Rise and Fall Time (10% to 90%)			5.0	μs	See Figure 1
Clock Pulse Logic Levels (ϕ_1 & ϕ_2)					
Logic "0"			−2.0	Volts	
Logic "1"	−25	−27	−29	Volts	
Clock Pulse Input Capacitance (ϕ_1)		15		pF	$\phi_1 = \phi_2$ = 0 Volt
(ϕ_2)		25		pF	$\phi_1 = \phi_2$ = 0 Volt
Propagation Delay Time from Clock ϕ_2 to Data Output ($t_{pd\,1}$ & $t_{pd\,0}$)		300	450	ns	See Figure 1
Data Input Capacitance		3.0		pF	V_{IN} = 0 Volt
Data Input Logic Levels					
Logic "0"			−2.0	Volts	
Logic "1"	−9.0			Volts	
Data Input Leakage Current			0.5	μA	V_{IN} = −15 Volts
Clock Input Leakage Current			100	μA	V_{IN} = −26 Volts
Clock (ϕ_2) Input Impedance	50	100		kΩ	ϕ_1 = −26 Volts, ϕ_2 = 0 Volt
Output Logic Levels					
Logic "0"		−0.5	−1.0	Volts	
Logic "1"	−10	−11		Volts	
Output Impedance to Ground		2.0	3.0	kΩ	Output at Logic "0"
Output Drive Capability (Logic "1")	−1.5	−1.75		mA	R_L = 4.0 kΩ to Ground
Power Supply Current Drain V_{DD}		15	23	mA	V_{DD} = −13 Volts
Power Supply Current Drain V_{GG}		1.0	2.0	mA	V_{GG} = −27 Volts

TIMING DIAGRAMS

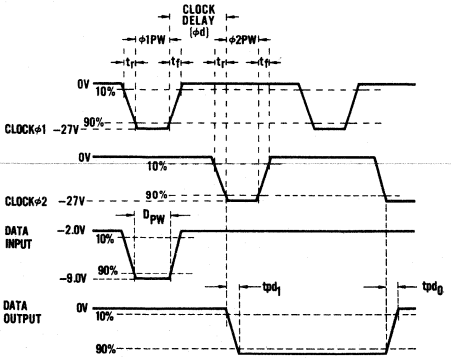


Figure 1

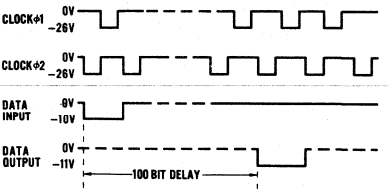


Figure 2

3325

QUAD 64-BIT DYNAMIC SHIFT REGISTER

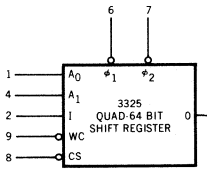
FAIRCHILD SILICON GATE MOS INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The 3325 contains four individual MOS two-phase dynamic shift registers of 64-bits each. It is a monolithic P-channel-enhancement-mode integrated circuit which is fabricated using low threshold SILICON GATE TECHNOLOGY. All inputs are protected against static charge through diode protection. The 3325 is bipolar-compatible; it can be driven and drive bipolar integrated circuits ($TT_{\mu}L$, $DT_{\mu}L$) directly without using interface level converters.

FEATURES:

- **SILICON GATE TECHNOLOGY**
- **DIRECT BIPOLAR COMPATIBILITY**
- **35 pF TYP. CLOCKLINE CAPACITANCE**
- **0.45 mW/BIT POWER DISSIPATION (TYP. AT 30% DUTY CYCLE)**
- **COMPLETE DECODING, MULTIPLEXING, CHIP SELECTION**
- **OUTPUT PUSH-PULL CIRCUITRY**
- **INPUT OVERVOLTAGE PROTECTION**
- **10 LEAD TO-100 PACKAGE**

LOGIC SYMBOL



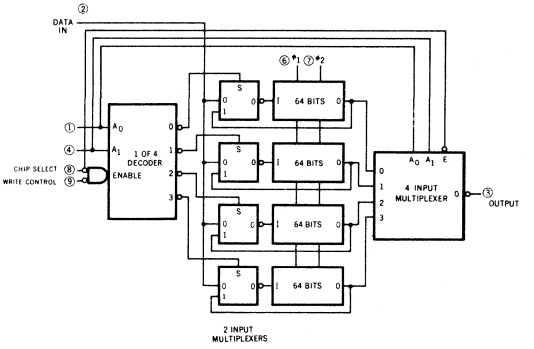
V_{DD} = PIN 10
V_{SS} = PIN 5

ABSOLUTE MAXIMUM RATINGS (above which useful life may be impaired) Note 1

Supply Voltage (V_{DD})	−20 V to +0.3 V
Clock Input Voltage	−20 V to +0.3 V
All Data Input (data line, address chip select and write control) Voltages	−10 V to +0.3 V
Storage Temperature	−55°C to +150°C
Operating Temperature	0°C to +70°C

Note 1: All voltages are measured with V_{SS} @ GND.

LOGIC DIAGRAM



"1" Most Positive Voltage
"0" Most Negative Voltage

OUTPUT LEVEL			
Chip Select		Input	Output
1	Chip Not Selected	1	1
		0	1
0	Chip Selected	1	1
		0	0

LOOP NO.	ADDRESS		WRITE CONTROL	
	A_0	A_1	Write	Recirculate
1	0	0	0	1
2	0	1	0	1
3	1	0	0	1
4	1	1	0	1

ORDER PART NO. A5F332519X

FAIRCHILD SEMICONDUCTOR

FUNCTIONAL DESCRIPTION — The 3325 contains four 64-bit two phase dynamic shift registers with complete input decoding, multiplexing, output selection and push-pull output driver circuitry. One out of four shift registers is selected by addressing two ADDRESS lines A_0 and A_1. Any one of the four registers recirculates continuously if no new data is being written in. Old information is being erased automatically if new data is entering into the shift register. While one shift register is selected for either "read" or "write", the other three recirculate continuously. Logical "0" of WRITE CONTROL is defined as writing; while logical "1" as reading and recirculating. When WRITE CONTROL line is at logic "1", all four shift registers are in the recirculating mode. When the WRITE CONTROL line is at logic "0" only the addressed shift register can receive new data while the other three shift registers recirculate. Chip is selected for the normal operation when CHIP SELECT is set at logical "0". When CHIP SELECT is at logical "1", the output voltage goes to logical "1" and information is being recirculated on all four shift registers.

Writing in of data is accomplished by simultaneously selecting CHIP SELECT at "0", WRITE CONTROL at "0", ADDRESS lines, and applying data at input. When WRITE CONTROL is at "1", data appears at output and recirculates, and no data can enter the shift register.
Data is entering the shift register when clock ϕ_1 is going to a logical "0". Data is appearing at the output when clock ϕ_2 is going to a logical "0".
For operation, the most positive voltage is defined as logical "1" and the most negative voltage as logical "0" level.

D.C. ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V_{DD} = -12\ V \pm 10\%$, $V_{SS} = 5.0\ V \pm 10\%$, Load = one TTμL load with $I_L = 1.6$ mA)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
$V\phi_H$	Clock Pulse "1" Voltage Level	$V_{SS} - 1.0$		V_{SS}	Volts	
$V\phi_L$	Clock Pulse "0" Voltage Level		$V_{DD} + 2.0$		Volts	
V_{IH}	Data Input Logic "1" Level	$V_{SS} - 1.0$		V_{SS}	Volts	
V_{IL}	Data Input Logic "0" Level	-1.0		0.8	Volts	
V_{OH}	Output Voltage "1" Level	$V_{SS} - 0.6$		V_{SS}	Volts	
V_{OL}	Output Voltage "0" Level			0.4	Volts	
I_L	Leakage Current					
	Clock Input Leakage Current		50	500	nA	@ −15 Volts } all other pins at ground
	Data Input (data, chip select, write control, address) Leakage Current		50	500	nA	@ −15 Volts } all other pins at ground
	Output Leakage Current		50	500	nA	@ −15 Volts } all other pins at ground
R_P	Input Pullup Resistance	3.5	5.0	10	kohms	$V_{SS} = +5.0\ V$, $V_{DD} = -12\ V$, $V_{IN} = +0.4\ V$
I_{DD}	Power Supply Current Drain		6.0	10	mA	$V_{SS} = +5.5\ V$, $V_{DD} = -13.2\ V$, Clock Amplitude = +4.5 to −12 V, Clock Duty Cycle = 30%
P_D	Power Dissipation		115	190	mW	

A.C. ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V_{DD} = -12$ Volts ± 10%, $V_{SS} = +5.0$ Volts ±10%, Load = one TTμL load with $I_L = 1.6$ mA)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
ϕ_1, ϕ_2	Clock Repetition Rate	0.001	1		MHz	
ϕ_{1w}, ϕ_{2w}	Clock Pulse Width	0.30		10	μs	
$t\phi_r$	Clock Pulse Rise Time		100		ns	
$t\phi_f$	Clock Pulse Fall Time		100		ns	
t_{pd+}, t_{pd-}	Output Delay Times		40		ns	
t_{AD1}	Address Lead Time to ϕ_1 when Writing		20		ns	
t_{AD2}	Address Lead Time to ϕ_2 when Reading		20		ns	
t_{WC}	Write Control Lead to ϕ_1		20		ns	
t_{DA}	Data Lead Time to ϕ_1		10		ns	
C_{IN}	Input Capacitance					
	Clock Input Capacitance		35		pF	$V\phi = V_{SS}$, f = 1 MHz
	Data Input Capacitance		3.5		pF	$V\phi = V_{SS}$, f = 1 MHz

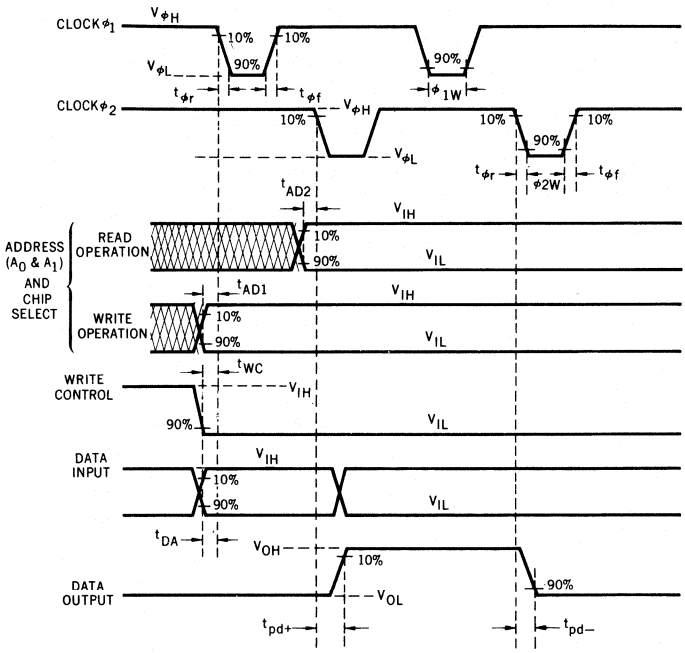
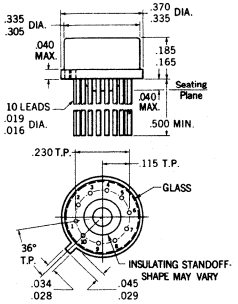


Fig. 1
TIMING DIAGRAM

PACKAGE INFORMATION

PHYSICAL DIMENSIONS

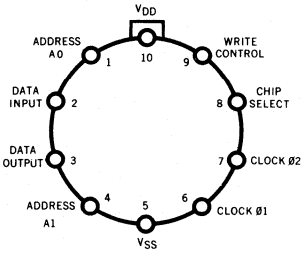
In accordance with
JEDEC (TO-100) outline



NOTES:
All dimensions in inches
Leads are gold-plated kovar
Package weight is 1.32 gram
Lead No. 5 is connected to case

CONNECTION DIAGRAM

(TOP VIEW)



3326
TRIPLE 66-BIT DYNAMIC SHIFT REGISTER
FAIRCHILD MOS INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The 3326 contains three independent two-phase dynamic shift registers of 66-bits each. It is a MOS P-channel-enhancement-mode monolithic integrated circuit. Each shift register has independent input and output but power supply and clock lines are common. The inputs are protected against static charge through diode protection. The 3326 can be driven and drive both MOS and bipolar integrated circuits (TTμL, DTμL). See Bipolar Interface configurations on Page. 4.

FUNCTIONAL DESCRIPTION — Each of the three shift register outputs is open drain. The output is delayed 66-bit times from the input and is inverted. The shift registers can be cascaded but each output must be connected to an external power supply through a pull-up resistor. Data is entering the shift register when clock ϕ_1 is going to a Logical "1". Data is appearing at the output when clock ϕ_2 is going to a logical "1". Logic "1" is the most negative voltage and logic "0" is the most positive voltage.

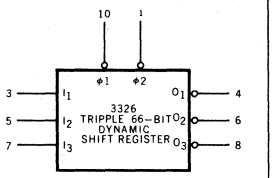
FEATURES:
- **3 MHz OPERATION GUARANTEED**
- **BIPOLAR COMPATIBILITY**
- **INPUT OVERVOLTAGE PROTECTION**
- **10 LEAD TO-100 PACKAGE**

ABSOLUTE MAXIMUM RATINGS (Above which useful life may be impaired) (Note 1)

Drain Voltage (V_{DD})	−30 V to +0.3 V
Data and Clock Input Voltage	−30 V to +0.3 V
Data Output	−30 V to +0.3 V
Storage Temperature	−55°C to +150°C
Operating Temperature	−55°C to +85°C

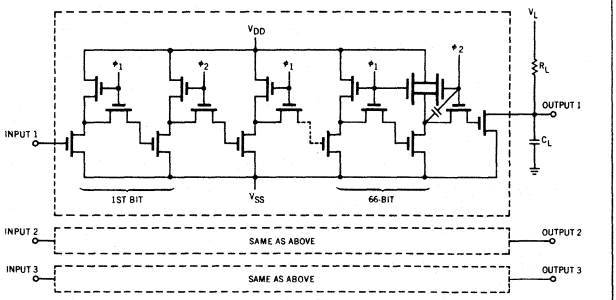
Note 1: All voltages are referenced with pin 9 @ GND.

LOGIC SYMBOL

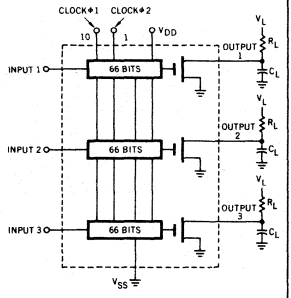


V_{SS} = PIN 9
V_{DD} = PIN 2

SCHEMATIC DIAGRAM



BLOCK DIAGRAM



Each output device requires an external pullup resistor R_L and power supply V_L.

ORDER PART NO. A5E332614X

FAIRCHILD SEMICONDUCTOR

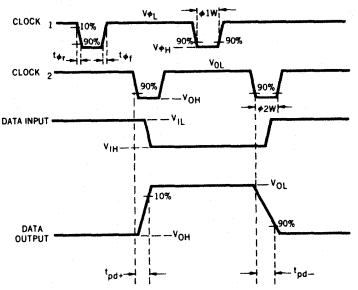
D.C. ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V_{DD} = -13\ V \pm 10\%$, $V_{SS} = GND$, Clock Amplitude = $-24\ V$ to $-27\ V$ $R_L = 8\ k\Omega \pm 10\%$, $V_L = -13\ V \pm 10\%$, $C_L = 20\ pF$)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
	Clock Pulse Amplitude					
V_{OL}	Logic "0" Level	0		−2.0	Volts	
V_{OH}	Logic "1" Level			−27	Volts	
	Data Input Voltage Level					
V_{IL}	Logic "0"	0		−3.0	Volts	
V_{IH}	Logic "1"	−9.0			Volts	
	Output Voltage Level					
V_{OL}	Logic "0"		−1.2	−2.0	Volts	
V_{OH}	Logic "1"		−12.5	V_L	Volts	
I_L	Leakage Current					
	Clock Input Leakage Current			10	μA	at −27 V
	Data Input Leakage Current			0.5	μA	at −13 V
	Output Leakage Current			0.5	μA	at −13 V
I_{DD}	Power Supply Current Drain		8.0	14	mA	$V_{DD} = -13\ V$ Clock Amplitude = −27 V Clock Duty Cycle = 20%
P_D	Power Dissipation		105	180	mW	

A.C. ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V_{DD} = -13\ V \pm 10\%$, $V_{SS} = GND$, Clock Voltages = $-24\ V$ to $-27\ V$ Loading Conditions $R_L = 8\ k\Omega \pm 10\%$, $C_L = 20\ pF$, $V_L = -13\ V \pm 10\%$)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
ϕ_1, ϕ_2	Clock Repetition Rate	0.001		3.0	MHz	
ϕ_{1w}, ϕ_{2w}	Clock Pulse Width	0.15		50	μs	
$t\phi_r, t\phi_f$	Clock Pulse Rise and Fall Times		100		ns	
t_{pd+}	Output Delay Time		50		ns	
t_{pd-}	Output Delay Time		200		ns	SEE NOTE 3
C_{IN}	Input Capacitance					
	Clock Input Capacitance		35	50	pF	
	Data Input Capacitance		3.5	5.0	pF	

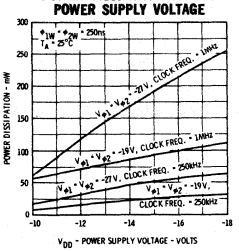
TYPICAL WAVEFORMS



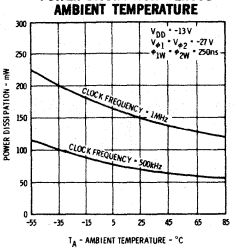
Note 3: Output delay time t_{pd-} is essentially determined by the output load time constant $R_L C_L$.

TYPICAL ELECTRICAL CHARACTERISTICS

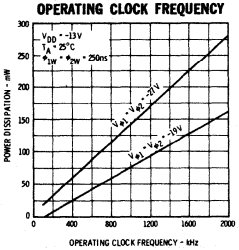
POWER DISSIPATION VERSUS POWER SUPPLY VOLTAGE



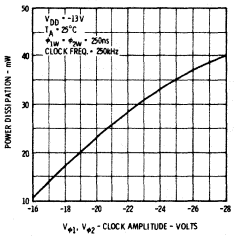
POWER DISSIPATION VERSUS AMBIENT TEMPERATURE



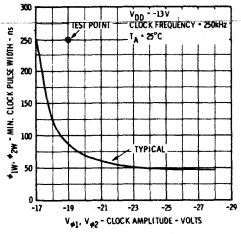
POWER DISSIPATION VERSUS OPERATING CLOCK FREQUENCY



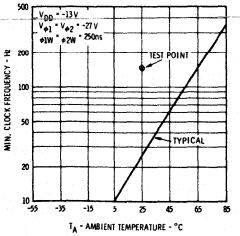
POWER DISSIPATION VERSUS CLOCK AMPLITUDE



MINIMUM CLOCK PULSE WIDTH VERSUS CLOCK AMPLITUDE



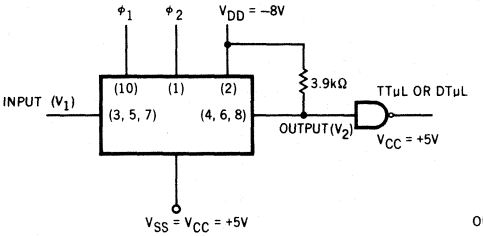
MINIMUM CLOCK FREQUENCY VERSUS TEMPERATURE



BIPOLAR INTERFACE

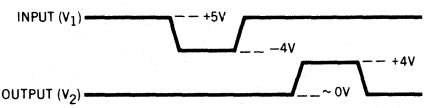
(A). OUTPUT COMPATABILITY

The 3326 can drive bipolar integrated circuits (TTμL, DTμL, etc.) directly without using additional interface circuitry. One scheme is shown below:



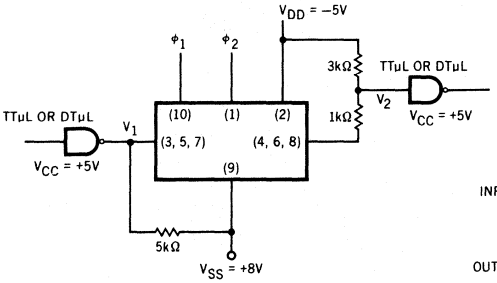
Clock amplitude $V\phi_1$, $V\phi_2 = +5$ V to -19 V.

Clock pulse width ϕ_{1w}, $\phi_{2w} \geq 150$ ns.



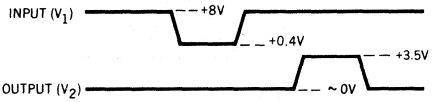
(B). INPUT/OUTPUT BIPOLAR COMPATABILITY

For both input and output compatibility with bipolar integrated circuits (TTμL, DTμL) the following circuit scheme is suggested:



Clock amplitude $V\phi_1$, $V\phi_2 = +8$ V to -16 V.

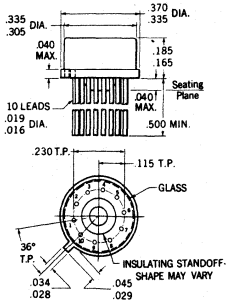
Clock pulse width ϕ_{1w}, $\phi_{2w} \geq 150$ ns.



PACKAGE INFORMATION

PHYSICAL DIMENSIONS

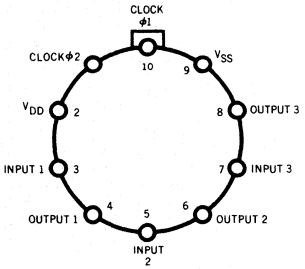
In accordance with JEDEC (TO-100) outline



NOTES:
All dimensions in inches
Leads are gold-plated kovar
Package weight is 1.32 gram
NO leads connected to case

CONNECTION DIAGRAM

(TOP VIEW)



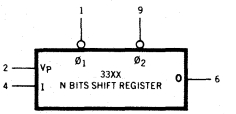
3329 (512-BIT . 3330 (480-BIT) . 3331 (500-BIT)
DYNAMIC SHIFT REGISTERS
FAIRCHILD SILICON GATE MOS INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The 3329, 3330 and 3331 are single 512-bit, 480-bit and 500-bit respectively, two-phase dynamic shift registers. They are monolithic integrated circuits utilizing P-channel enhancement mode SILICON GATE MOS technology. An on-chip input resistor allows direct bipolar compatibility by tying the V_P pin to V_{DD}. The output buffer is capable of driving both low level MOS and bipolar loads directly without addition of an external resistor.

FUNCTIONAL DESCRIPTION — The 3329, 30 and 31 are straight "pipe line" two phase dynamic shift registers. The functions ϕ_1 and ϕ_2 are non-overlapping and negative as illustrated in Figure 1. Data is accepted at the input when ϕ_1 is negative and data is available at the output after negative going transition of ϕ_2. The input is connected by a MOS transistor to V_{SS}; this transistor acts as an externally controlled pull-up resistor allowing complete TTμL compatibility. The output stage is push-pull, and can sink 1 TTμL load to V_{DD} (1.6 mA at 0.4 V). Bipolar compatible operation is achieved by connecting V_{SS} to +5.0 V, V_{DD} to 0 V, and V_{GG} to −12 V, with V_P, the control pin to the input pull-up resistor tied to V_{DD}.

- **DIRECT BIPOLAR COMPATIBILITY**
- **2 MHz OPERATION GUARANTEED (TYPICALLY FROM 1 kHz TO 4 MHz)**
- **45 pF CLOCKLINE CAPACITANCE (MAX.)**
- **0.5 mW/BIT POWER DISSIPATION (MAX) AT 2 MHz**
- **INPUT OVERVOLTAGE PROTECTION**
- **10 LEAD TO-100 PACKAGE**

LOGIC SYMBOL



XX	N
29	512
30	480
31	500

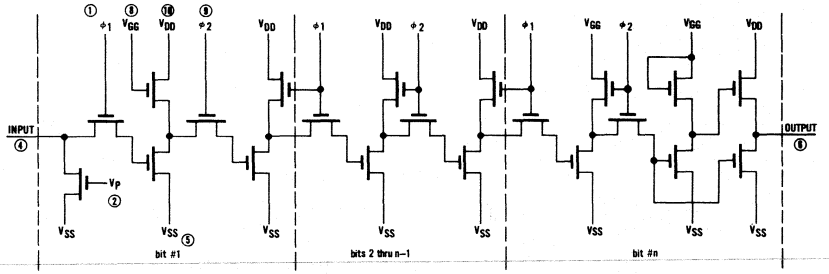
V_{SS} = PIN 5
V_{DD} = PIN 10
V_{GG} = PIN 8

ABSOLUTE MAXIMUM RATINGS, (above which the useful life may be impaired)

All Inputs Including ϕ_1, ϕ_2 and V_P (Notes 1 & 3)	−24 V to +0.3 V
V_{GG} (Note 3)	−24 V to +0.3 V
V_{DD} and Output (Note 3)	−7.0 V to +0.3 V
Output Current when Output is low (Note 2)	10 mA
Storage Temperature	−55°C to +150°C
Operating Temperature	0°C to +70°C

Note 1: V_P must be tied to V_{SS} if data input is between −7 V and −24 V.
Note 2: Low logic level is most negative level and high logic level is most positive level.
Note 3: All voltages with respect to V_{SS}.

SCHEMATIC DIAGRAM



ORDER INFORMATION A5F332919X for 512-Bit Shift Register A5F333019X for 480-Bit Shift Register A5F333119X for 500-Bit Shift Register
Using the "basic cells" of this family and Computer Aided Design techniques, customized Shift Register lengths, other than above, can be easily obtained upon request.

FAIRCHILD
SEMICONDUCTOR

D.C. CHARACTERISTICS ($T_A = 0°C$ to $+70°C$, $V_{SS} = 5.0\ V \pm 10\%$, $V_{DD} = 0\ V$, $V_{GG} = -12\ V \pm 10\%$)

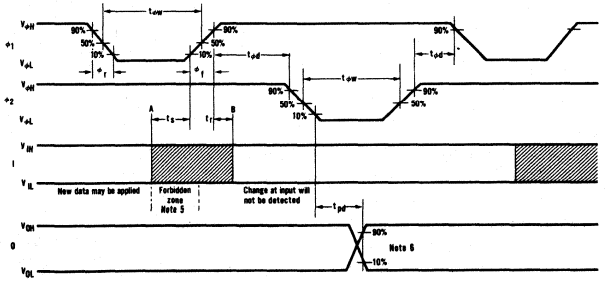
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
V_{OH}	Output High Voltage	$V_{SS} - 0.6$		V_{SS}	Volts	$I_{OH} = -0.5\ mA$
V_{OL}	Output Low Voltage	0	0.24	0.4	Volts	$I_{OL} = 1.6\ mA$
V_{IH}	Input High Voltage	$V_{SS} - 1.0$			Volts	
V_{IL}	Input Low Voltage	V_{GG}		0.85	Volts	$V_P = V_{SS}$ if V_I is negative
I_{IH}	Input High Load Current	0.17			mA	$V_I = V_{SS} - 1$, $V_P = V_{DD}$
I_{IL}	Input Low Load Current		1.0	1.60	mA	$V_I = 0.4\ V$, $V_P = V_{DD}$
I_{IL}	Input Low Load Current			1.0	μA	$V_I = -5.0\ V$, $V_P = V_{SS}$, $T_A = 25°C$
$V\phi_H$	Clock Input High Voltage	$V_{SS} - 1.0$		V_{SS}	Volts	
$V\phi_L$	Clock Input Low Voltage	−6.5		−4.5	Volts	
$I\phi_L$	Clock Input Leakage			1.0	μA	$V\phi = -10\ V$, $T_A = 25°C$
R_{OH}	Impedance of Output High		0.7	1.0	kohms	$V_{OUT} = V_{SS} - 0.5\ V$
R_{OL}	Impedance of Output Low		150	250	ohms	$V_{OUT} = V_{OL}$
I_{GG}	V_{GG} Current		−2.4	−3.0	mA	$V_{SS} = 5.5\ V$, $V_{GG} = -13.2\ V$
I_{DD}	V_{DD} Current		− 28	−35	mA	$V\phi_L = -6.5\ V$
I_{SS}	V_{SS} Current		30.4	38	mA	$T_A = 25°C$, f = 2.0 MHz
P_D	Power Dissipation		200	250	mW	$t\phi_w = 200\ ns$

A.C. CHARACTERISTICS ($T_A = 0°C$ to $+70°C$, $V_{SS} = 5.0\ V \pm 10\%$, $V_{DD} = 0\ V$, $V_{GG} = -12\ V \pm 10\%$) (See Fig. 1)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
$t\phi_w$	Clock Pulse Width	0.2		100	μs	Note 4
$t\phi_d$	Time Between Clocks	0		100	μs	Note 4
ϕ_r, ϕ_f	Clock Rise & Fall Times (10% - 90%)			1.0	μs	
$C\phi$	Clock Capacitance (Each clockline)			45	pF	$V\phi = V_{SS}$, f = 1.0 MHz
f	Operating Frequency	0.01		2.0	MHz	
t_s	Input Set Up Time			100	ns	
t_r	Input Release Time	0			ns	
t_{pd+}	Delay from ϕ_2 to High Level at Output			150	ns	$C_L = 10\ pF$, Load = 1 TTμL Input
t_{pd-}	Delay from ϕ_2 to Low Level at Output			150	ns	$C_L = 10\ pF$, Load = 1 TTμL Input

Note 4: Maximum cycle time ($t\phi_{w1} + t\phi_{d1,2} + t\phi_{w2} + t\phi_{d2,1}$) = 100 μs.

Fig. 1 **TIMING DIAGRAM**

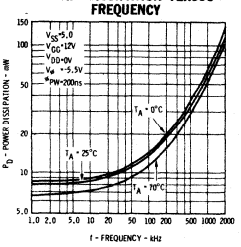


Note 5: A and B define a window during which the input to the shift register is setting up. If the input data changes during this window, the change may or may not be detected. To avoid this ambiguous operation, the input data must remain good between A and B.

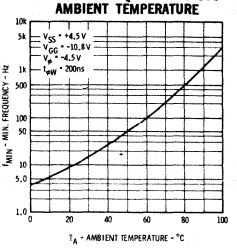
Note 6: The outputs remain good until a new output appears.

TYPICAL ELECTRICAL CHARACTERISTICS

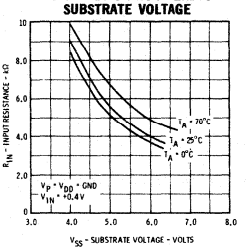
POWER DISSIPATION VERSUS FREQUENCY



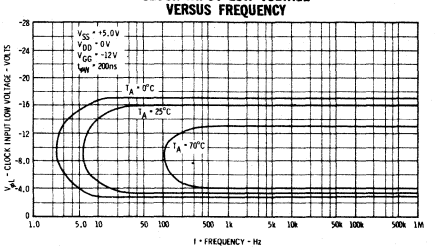
MINIMUM FREQUENCY VERSUS AMBIENT TEMPERATURE



INPUT RESISTANCE VERSUS SUBSTRATE VOLTAGE



CLOCK INPUT LOW VOLTAGE VERSUS FREQUENCY



APPLICATIONS

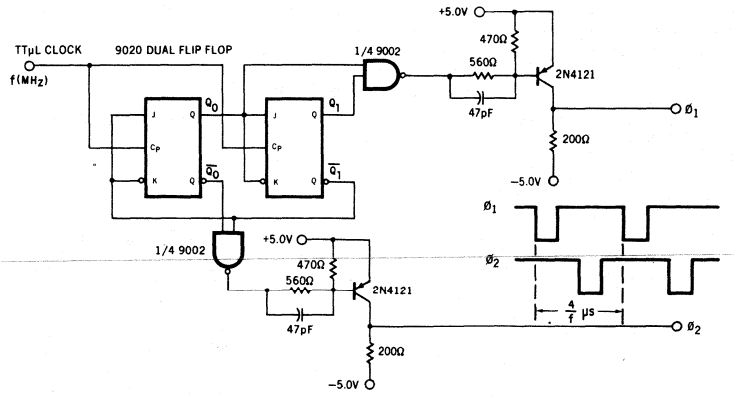


Fig. 2

TWO-PHASE NON-OVERLAPPING CLOCK GENERATOR

The counter states 11 and 00 are decoded to produce −5 V clock pulses.

APPLICATIONS

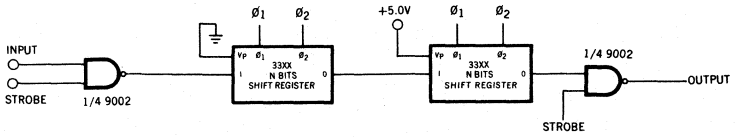


Fig. 3

SHIFT REGISTER INTERFACE

The shift register inputs may be connected directly to a TTμL or DTμL output if V_P is tied to ground. If the input is to be driven by a MOS output, V_P is tied to V_{SS}. The output can drive TTμL or DTμL directly. No external components are required.

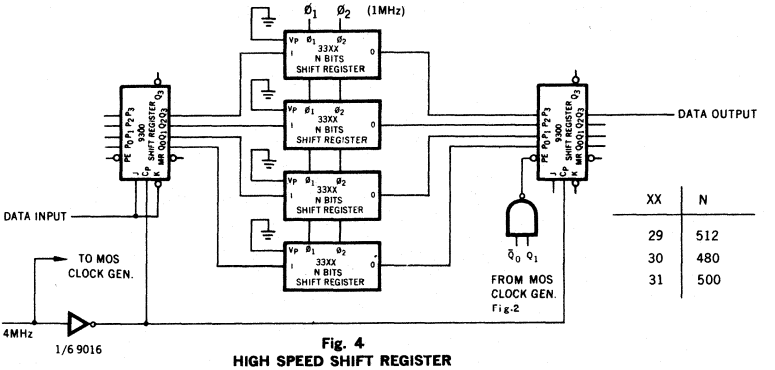


Fig. 4

HIGH SPEED SHIFT REGISTER

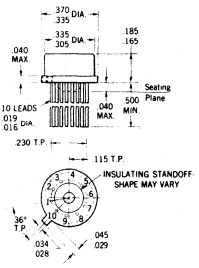
Four shift registers may be connected as shown in the figure above to simulate one long high speed shift register. The 9300 MSI shift register on the left is used as a serial to parallel converter. Data is clocked into the 9300 at four times the clock rate of the silicon gate shift registers. When four bits have been clocked in, they are loaded into the four long shift registers. At the output of the silicon gate registers, another 9300 is used to re-serialize the data at the higher clock rate. Because the 9300's add several bits of delay, the system illustrated looks like a high speed 4N + 5 bit register, where N is the length of each of the silicon gate registers.

Note that the clock period of the 9300's must be greater than the input set up time on the silicon gate registers.

PACKAGE INFORMATION

PHYSICAL DIMENSIONS

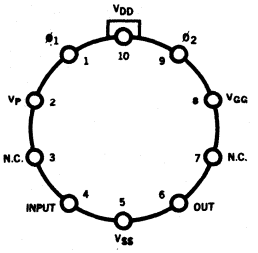
In accordance with JEDEC (TO-100) outline



NOTES:
All dimensions in inches
Leads are gold-plated kovar
Lead No. 5 internally connected to case
Package weight is 1.32 grams

CONNECTION DIAGRAM

(TOP VIEW)



3333

TRIPLE 64-BIT DYNAMIC SHIFT REGISTER

FAIRCHILD MOS INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The 3333 is a high threshold MOS dynamic shift register fabricated using Micromosaic Design Approach. The integrated circuit contains three individual 64-Bit, 2-phase dynamic shift registers, each with a tap at the 48th bit and a separate phase 1 clock input. The phase 2 clock is common to all three registers.

Data is written into a register during its phase 1 time. Data outputs change during phase 2 time.

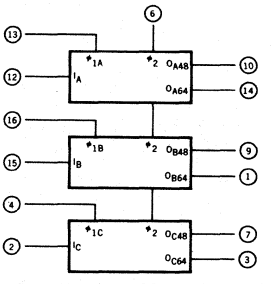
All data inputs have full diode protection. All clock inputs have partial diode protection. Outputs are through uncommitted transistor to V_{SS}. With a pull-up resistor to V_{DD}, the logic levels are the true form of the input delayed by 48 or 64 clock times.

ABSOLUTE MAXIMUM RATINGS (Above which useful life may be impaired) See Note 1

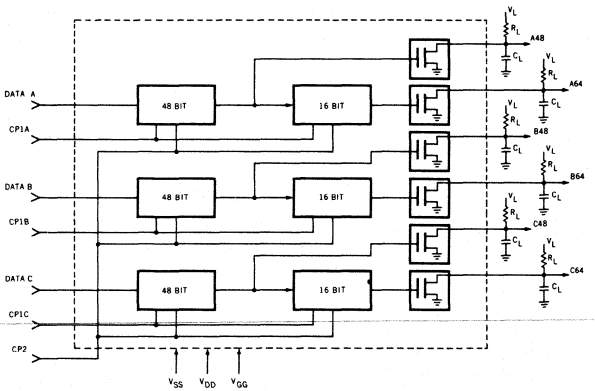
V_{DD} Supply Voltage	+0.3 V to −15 V
V_{GG} Supply Voltage	+0.3 V to −32 V
Clock Input Voltage	+0.3 V to −32 V
Data Input Voltage	+0.3 V to −15 V
Storage Temperature	−55°C to +150°C
Operating Temperature	0°C to +70°C
Power Dissipation (All clock inputs = −30 V, T_A = 25°C, V_{DD} = −15 V, V_{GG} = −30 V)	750 mW

Note 1: All voltages are with respect to V_{SS}.

LOGIC SYMBOL



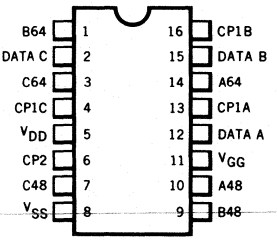
BLOCK DIAGRAM



Note: The output device requires an external pull-up Resistor, R_L, and Power Supply, V_L.

CONNECTION DIAGRAM

(TOP VIEW)



ORDER PART NO. A7K333319X

FAIRCHILD SEMICONDUCTOR

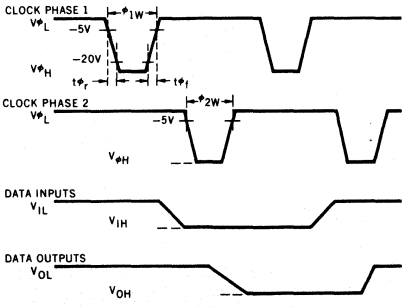
D.C. ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V_{DD} = -10\,V$ to $-15\,V$, $V_{GG} = -24\,V$ to $-32\,V$, $V_{SS} = 0\,V$, $V_L = V_{DD}$, $R_L = 20\,k\Omega \pm 5\%$)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
	Clock Pulse Amplitude					
$V_{\phi L}$	Logic "0" Level	0		−2.0	Volts	
$V_{\phi H}$	Logic "1" Level	−24.0		−32.0	Volts	
	Data Input Voltages					
V_{IL}	Logic "0" Level	0		−2.0	Volts	
V_{IH}	Logic "1" Level	−9.0		−15.0	Volts	
	Data Output Voltages					
V_{OL}	Logic "0" Level	0		−1.0	Volts	
V_{OH}	Logic "1" Level	$V_L - 1$		V_L	Volts	
I_L	Leakage Current					
	Clock Input			0.5	μA	@ −30 V
	Data Input			0.1	μA	@ −15 V
I_{DD}	Power Supply Current			−12.5	mA	$V_{DD} = -15\,V$ $V_{GG} = -30\,V$ Clock Amplitude −30 V Duty Cycle Per Phase 25%
Z_O	Output Impedance to V_{SS}	0.7		2.0	kΩ	$V_{out} = -1.5\,V$

A.C. ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V_{DD} = -10\,V$ to $-15\,V$, $V_{GG} = -24\,V$ to $-32\,V$, $V_{SS} = 0\,V$, $V_L = V_{DD}$, $R_L = 20\,k\Omega \pm 5\%$, $C_L = 15\,pF$
Clock Amplitude $V_{\phi L} = 0\,V$ to $-2\,V$, $V_{\phi H} = -24\,V$ to $-32\,V$

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
ϕ_1, ϕ_2	Clock Repetition Rate	0.01		1.0	MHz	ϕmin is with $\phi_w = 1\,\mu s$; ϕmax is with $\phi_w = 0.30\,\mu s$ and $t\phi_r = t\phi_f$ <40ns
ϕ_{1w}	Phase 1 Pulse Width	0.15	1.0		μs	
ϕ_{2w}	Phase 2 Pulse Width	0.25	1.0		μs	
$t\phi_r, t\phi_f$	Clock Pulse Rise and Fall Times		100 100		ns ns	
C_{IN}	Input Capacitance					
	Clock Phase 1			20	pF	
	Clock Phase 2			60	pF	
	Data		3.0		pF	

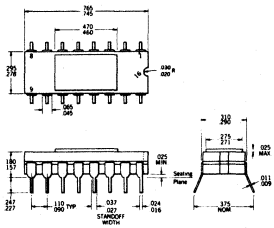
TYPICAL WAVEFORMS



Note: Output rise time from V_{OL} to V_{OH} is determined by the time constant R_L and C_L.

PACKAGE INFORMATION

PHYSICAL DIMENSIONS



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are gold-plated kovar
Lead No. 8 is internally grounded

3383

256-BIT DYNAMIC SHIFT REGISTER WITH RECIRCULATE

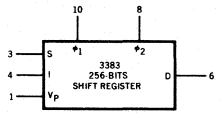
FAIRCHILD SILICON GATE MOS INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The 3383 is a single, 256-bit, two-phase, dynamic shift register. It is a monolithic integrated circuit utilizing P-channel enhancement mode SILICON GATE MOS technology. A data-select pin (pin 3) allows data to be either entered externally or recirculated from the device output without external wiring. On-chip input resistors allow direct bipolar compatibility by tying the V_P pin to V_{DD}. The output buffer is capable of driving both MOS and bipolar loads directly without addition of an external resistor.

FEATURES:

- **DIRECT BIPOLAR COMPATIBILITY**
- **2 MHz OPERATION**
- **25 pF CLOCKLINE CAPACITANCE**
- **0.6 wW/BIT MAX. POWER DISSIPATION AT 2 MHz**
- **INPUT OVER VOLTAGE PROTECTION**
- **10 LEAD TO-100 PACKAGING**

LOGIC SYMBOL



V_{SS} = PIN 5
V_{DD} = PIN 9
V_{GG} = PIN 7

ABSOLUTE MAXIMUM RATINGS (Above which useful life may be impaired)

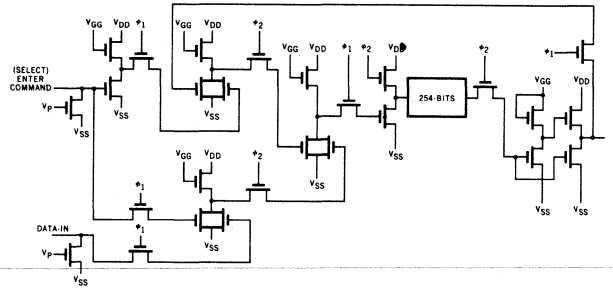
All Inputs [ϕ_1, ϕ_2, V_P, Input, Select] (Notes 1 & 3)	−24 V to +0.3 V
V_{GG} (Note 3)	−24 V to +0.3 V
V_{DD} and Data Output (Note 3)	−7.0 V to +0.3 V
Output Low Current (Note 2)	10 mA
Storage Temperature	−55°C to +150°C
Operating Temperature	0°C to +70°C

Note 1. V_P must be tied to V_{SS} if data input or select is between −7.0 V and −24 V.

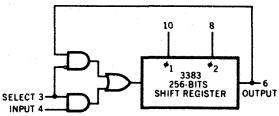
2. Low logic level is the most negative level and high logic level is the most positive level.

3. All Voltages with respect to V_{SS}.

SCHEMATIC DIAGRAM



LOGIC DIAGRAM



ORDER PART NO. A5F338319X

Using the "basic cells" of this family and Computer Aided Design techniques, customized Shift Register lengths, other than above, can be easily obtained upon request.

FAIRCHILD
SEMICONDUCTOR

FUNCTIONAL DESCRIPTION — The 3383 is a straight "pipeline" two phase dynamic shift register with a recirculate control. The clock functions ϕ_1 and ϕ_2 are non-overlapping negative pulses as illustrated in Figure 1. Data is accepted on the input and select lines when ϕ_1 is negative and data is available at the output when ϕ_2 is negative. The data-in and select lines are connected by an MOS transistor to V_{SS}; these transistors act as externally controlled pull up resistors allowing complete TTμL compatibility. The output stage is push-pull and can sink one TTμL load to V_{DD} (1.6 mA at 0.4 V). Bipolar compatible operation is achieved by connecting V_{SS} to +5.0 V, V_{DD} to 0 V, and V_{GG} to −12 V, with V_P, the control pin to the pull-up resistors, tied to V_{DD}. For driving the input with MOS, the V_P pin should be connected to V_{SS}.

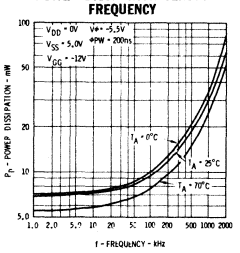
D.C. CHARACTERISTICS ($T_A = 0°C$ to $+70°C$, $V_{SS} = +5.0$ V ±10%, $V_{DD} = 0$ V, $V_{GG} = -12.0$ V ±10%)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	V_{SS} −0.6		V_{SS}	Volts	$V_{SS} = +4.5$ V, $I_{OH} = -0.5$ mA
V_{OL}	Output Low Voltage	0	.24	+0.4	Volts	$V_{SS} = +5.5$ V, $I_{OL} = 1.6$ mA
$V_{IH\ (VSH)}$*	Input (Select) High Voltage	V_{SS} −1		V_{SS}	Volts	$V_P = V_{SS}$ if V_{IH} is negative
$V_{IL\ (VSL)}$*	Input (Select) Low Voltage	V_{GG}		+0.85	Volts	
$I_{IH\ (ISH)}$*	Input (Select) Load Current	0.17			mA	$V_I = V_{SS} - 1$, $V_P = V_{DD}$
$I_{IL\ (ISL)}$*	Input (Select) Load Current		1.0	1.6	mA	$V_I = +0.4$ V, $V_P = V_{DD}$
$I_{IL\ (ISL)}$	Input (Select) Load Current			1.0	μA	$V_I = -5$ V, $V_P = V_{SS}$, $T_A = 25°C$
V_{OH}	Clock Input High Voltage	V_{SS} −1		V_{SS}	Volts	
V_{OL}	Clock Input Low Voltage	−6.5		−4.5	Volts	
I_{OL}	Clock Input Leakage			1.0	μA	$V\phi = -10$ V, $T_A = 25°C$
R_{OH}	Output Impedance		0.7	1.0	kOhms	$V_O = V_{SS} - 0.5$ V
R_{OL}	Output Impedance		150	250	Ohms	$V_O = V_{OL}$
I_{GG}	V_{GG} Current		−2.4	−3.0	mA	$V_{SS} = +5.5$ V
I_{DD}	V_{DD} Current		−14.0	−18.0	mA	$V_{GG} = -13.2$ V
I_{SS}	V_{SS} Current		16.4	+21.0	mA	$V_{OL} = -6.5$ V
P_D	Power Dissipation		125	155	mW	$T_A = +25°C$, f = 2.0 MHz $t\phi_w = 200$ ns

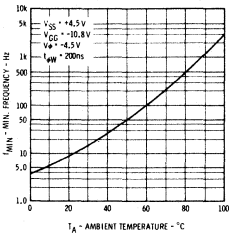
*All input voltages and currents pertain also to the data select pin.

TYPICAL ELECTRICAL CHARACTERISTICS

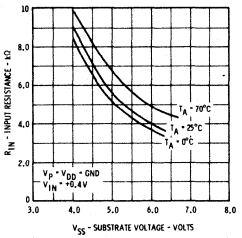
POWER DISSIPATION VERSUS FREQUENCY



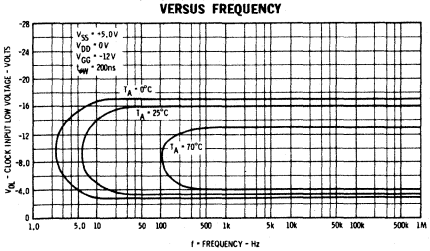
MINIMUM FREQUENCY VERSUS AMBIENT TEMPERATURE



INPUT RESISTANCE VERSUS SUBSTRATE VOLTAGE



CLOCK INPUT LOW VOLTAGE VERSUS FREQUENCY



A.C. CHARACTERISTICS ($T_A = 0°C$ to $+70°C$, $V_{SS} = +5.0\,V \pm 10\%$, $V_{DD} = 0\,V$, $V_{GG} = -12.0\,V \pm 10\%$) (SEE FIGURE 1)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
$t\phi_w$	Clock Pulse Width	0.2		100	μs	Note 4
$t\phi_D$	Time Between Clocks	0		100	μs	Note 4
ϕ_r, ϕ_f	Clock Rise and Fall Times (10% - 90%)			1.0	μs	
$C\phi$	Clock Capacitance (Each Clock Line)			25	pF	$V\phi = V_{SS}$, f = 1 MHz
t_s**	Data Set-Up Time			100	ns	
t_r**	Data Release Time	0			ns	
t_{pd+}	Delay from ϕ_2 to V_{OH}			150	ns	C_L = 10 pF
t_{pd-}	Delay from ϕ_2 to V_{OL}			150	ns	Load = 1 TTμL Input
f	Max. Operating Frequency	.010		2.0	MHz	

**All input timing conditions also pertain to the data select pin.

Note 4: Maximum cycle time ($t\phi_{w1} + t\phi_{D1,2} + t\phi_{w2} + t\phi_{D2,1}$) = 100 μs

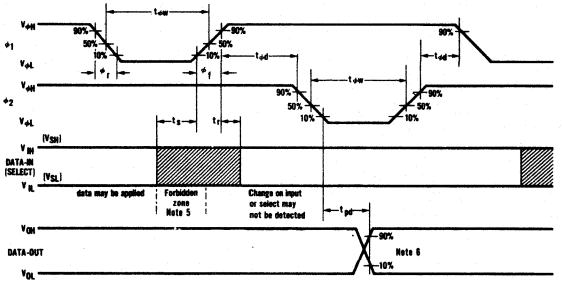


Fig. 1 — TIMING DIAGRAM

Note 5: A and B define a window during which the input to the shift register is setting up. If input or select data changes during this window, the change may or may not be detected. To avoid this ambiguous operation, information must remain good between A and B.

Note 6: The outputs remain good until a new output appears.

APPLICATIONS

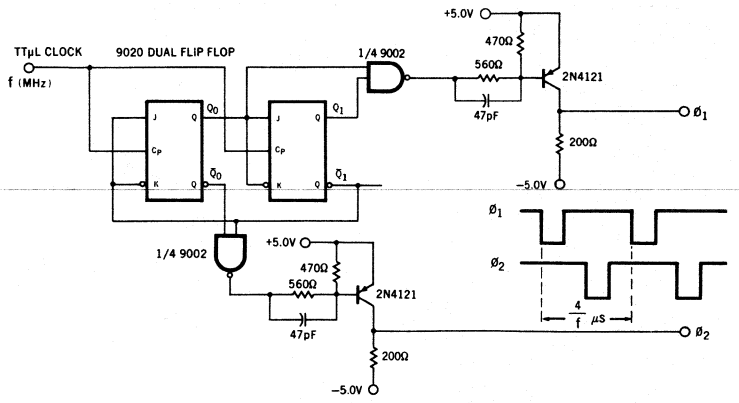


Fig. 2 — TWO-PHASE NON-OVERLAPPING CLOCK GENERATOR

The counter states 11 and 00 are decoded to produce −5 V clock pulses.

APPLICATIONS

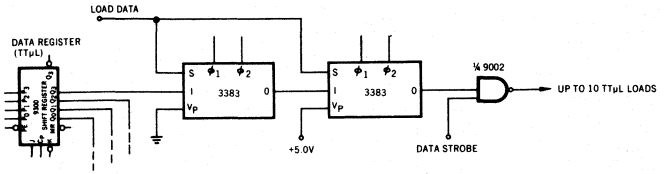


Fig. 3 — SHIFT REGISTER INTERFACE

The shift register inputs may be connected directly to a TTμL or DTμL output if V_P is tied to ground (V_{DD}). If the inputs are to be driven by a Silicon Gate MOS output, V_P is tied to V_{SS}. The output can drive TTμL or DTμL directly without external components.

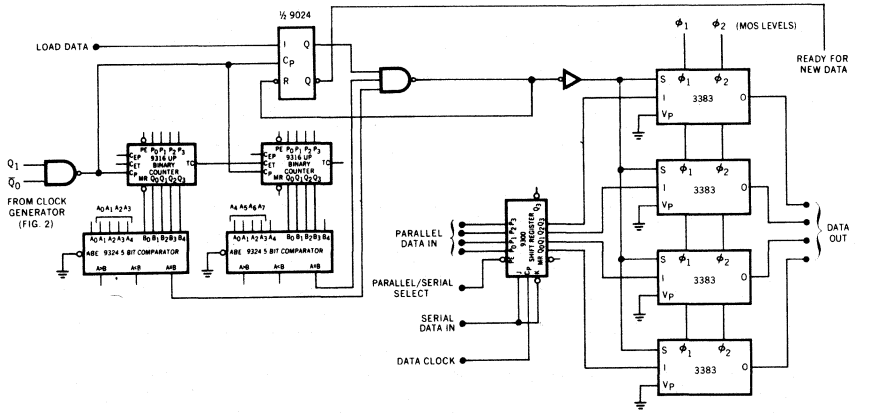
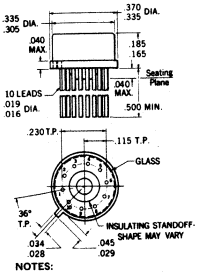


Fig. 4 — 256WX4B SEQUENTIAL MEMORY

256 four-bit words are stored in the shift registers. The two 9316's keep track of address locations in the shift registers. New data is loaded into the 9300 data register, either in serial or parallel. When the data is ready in the 9300, the "Data Ready" line is made high for one cycle, setting the 9024 flip-flop. The address for the new data is applied at A_0 - A_7 on the comparator. When the address comes up on the counters, the shift register select input switches to accept the new data, and the data flip-flop is reset.

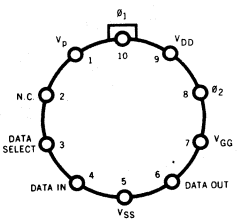
PACKAGE INFORMATION

PHYSICAL DIMENSIONS
In accordance with JEDEC (TO-100) outline



NOTES:
All dimensions in inches
Leads are gold-plated kovar
Package weight is 1.32 gram
Lead No. 5 is connected to case

CONNECTION DIAGRAM
(TOP VIEW)



3501
1024-BIT STATIC READ-ONLY MEMORY
MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 3501 is a 1024-bit read-only memory in a 128 word by 8 bit format. It is a MOS monolithic integrated circuit utilizing P-channel enhancement mode technology. The fixed program memory is specified by the customer and customized by modifying one mask in the fabrication process. This results in a fast turn-around, low cost custom memory.

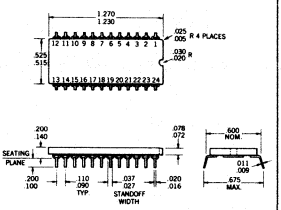
FEATURES:
- **CHIP SELECT**
- **ACCESS TIME — 3.6 μs**
- **STATIC OPERATION**
- **LOW POWER CONSUMPTION — 150 mW TYP.**
- **BIPOLAR COMPATIBLE OUTPUTS**

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

All Voltages and Data Input Lines	−30 V to +0.3 V
Power Dissipation	250 mW
Storage Temperature	−55°C to +150°C
Operating Temperature	−55°C to +85°C 0°C to +70°C

APPLICATIONS:
- Micro Programming
- Code Conversion
- Table Lookup
- Control Logic

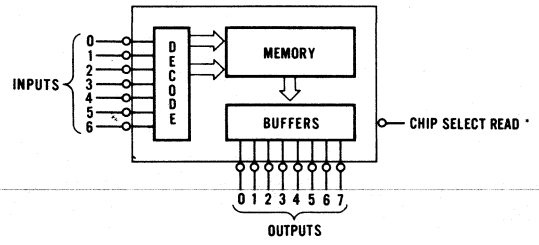
PHYSICAL DIMENSION



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .600" centers. They are purposely shipped with "positive" misalignment to facilitate insertion
Leads are gold-plated kovar
Package weight is 4.1 grams
Lead No. 12 is internally grounded

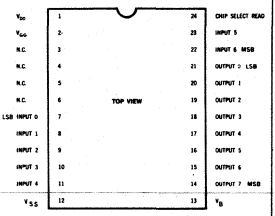
ORDER PART NO. A6G350114X (—55°C to +85°C)
A6G350119X (0°C to +70°C)

LOGIC DIAGRAM (MIL STD 806B)



*WHEN CHIP SELECT READ IS AT GROUND THE OUTPUTS ARE FLOATING.

PIN CONFIGURATION



FAIRCHILD
SEMICONDUCTOR

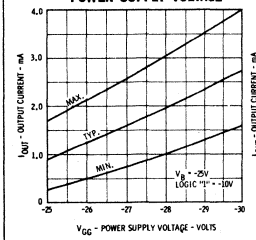
ELECTRICAL CHARACTERISTICS STANDARD CONDITIONS (unless otherwise specified) Note 3
$V_{DD} = -13\ V \pm 1\ V$, $V_{GG} = -27\ V \pm 2\ V$, $V_B = -27\ V \pm 2\ V$, $V_{SS} = 0\ V$ (Gnd), $0 \leq T_A \leq 70°C$ (Note 8)

CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Input Logic Levels					
Logic 0	0		−2.0	Volts	
Logic 1	−9.0			Volts	
Input Capacitance		7.0		pF	Note 5
Input Leakage			1.0	μA	$V_{IN} = -15\ V$, Note 6
Output Logic Levels					
Logic 0	0		−1.0	Volts	$I_L = -10\ \mu A$
Logic 1	−10			Volts	$I_L = +10\ \mu A$
Access Time					
t_{pd-} (to −10 V)		2.3	3.1	μs	$R_L = 1\ M\Omega$, $C_L = 10\ pF$
t_{pd+} (to −1 V)		3.6	4.25	μs	Note 2, 4, Fig. 1
Chip Select Time					
Enable t_e (to −10 V)		1.9	3.6	μs	$R_L = 1\ M\Omega$, $C_L = 10\ pF$
Disable t_{de} (to −1 V)		2.9	4.5	μs	Note 2, 4, Fig. 1
Output Current					
Logic 0	.15	.24			$V_{OUT} = -1.0\ V$ (forced), Note 7
Logic 1	.30	.85			$V_{OUT} = -10\ V$ (forced), Note 7
Output Leakage			−1.0	μA	$V_{OUT} = -15\ V$
Output Capacitance		5.0		pF	Note 5
Supply Current Drain					
I_{DD}			6.5	mA	$V_{DD} = -14\ V$, $V_{GG} = -29\ V$
I_{GG}			4.0	mA	Note 2
Power Consumption		150	215	mW	Note 1, 2

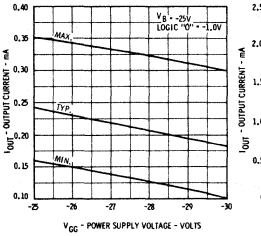
NOTES:
(1) Exclusive of I_B (load current)
(2) $T_A = +25°C$
(3) Fairchild will furnish complete test spec's upon request
(4) Sample tested
(5) Guaranteed by design
(6) Address and chip select inputs, all pins grounded except the one under test
(7) $V_{DD} = -12\ V$, $V_{GG} = -25\ V$ (worst case condition of measurement)
(8) Consult the factory for −55°C to +85°C and −55°C to +125°C operation, performance, parameter limits etc.

ELECTRICAL CHARACTERISTICS

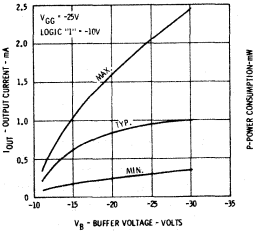
OUTPUT CURRENT VERSUS POWER SUPPLY VOLTAGE



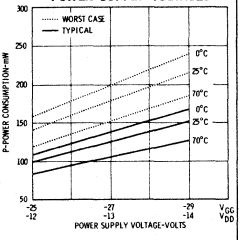
OUTPUT CURRENT VERSUS POWER SUPPLY VOLTAGE



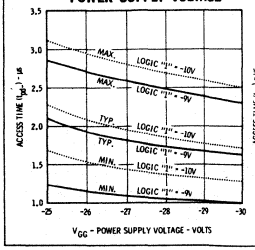
OUTPUT CURRENT VERSUS BUFFER VOLTAGE



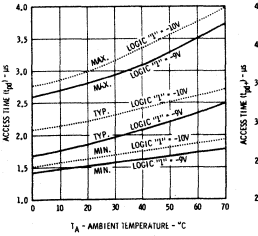
POWER CONSUMPTION VERSUS POWER SUPPLY VOLTAGES



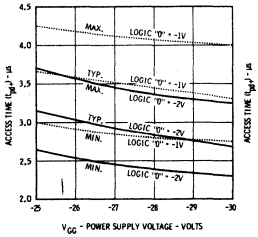
ACCESS TIME (t_{pd-}) VERSUS POWER SUPPLY VOLTAGE



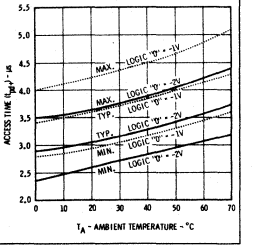
ACCESS TIME (t_{pd-}) VERSUS AMBIENT TEMPERATURE



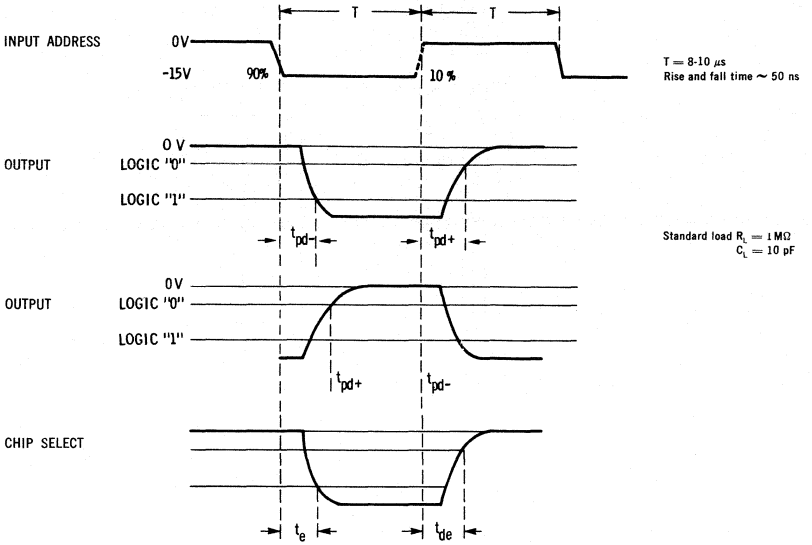
ACCESS TIME (t_{pd+}) VERSUS POWER SUPPLY VOLTAGE



ACCESS TIME (t_{pd+}) VERSUS AMBIENT TEMPERATURE



TYPICAL TIMING DIAGRAM



NOTE: The logic "0", "1" levels may be taken to be (−1 V, −10 V) or (−2 V, −9 V) respectively. Both versions are reflected in the graphs. Guaranteed limits are at −1 V and −10 V.

Fig. 1 — ACCESS AND CHIP SELECT TIMES

GLOSSARY OF TERMS

V_{GG} The most negative voltage applied to the device
V_{DD} An intermediate negative voltage applied to the device
V_B The voltage applied to the output buffers
V_{SS} The most positive voltage, applied to the device (substrate)

ACCESS TIME:
The delay time from the −9 V level (or the −2 V level respectively) of the input square wave to a valid output level reflecting the new logic state (see timing diagram) under standard load conditions ($R_L = 1\,M\Omega$, $C_L = 10$ pF).

CHIP SELECT TIME:
The delay time from a valid chip select input to a valid OR-wired output of the selected device under standard load conditions.

CUSTOM BIT PATTERN ORDERING PROCEDURE

To order a custom bit pattern matrix

1. Customer will be furnished a Read-Only Memory Coding Form from Fairchild representative. This form, when completed, will list each input and output bit pattern. From this information Fairchild will generate a Truth Table print out for verification, a custom mask, and a final test program for each custom device, or
2. Customer will provide Fairchild with a Truth Table in the Coding Form format, or
3. Customer will provide Fairchild with prepunched computer cards in the coding form format.

Fig. 2 — TYPICAL EXPANDED MEMORY
(CONNECTION FOR 256 WORDS BY 8 BITS)

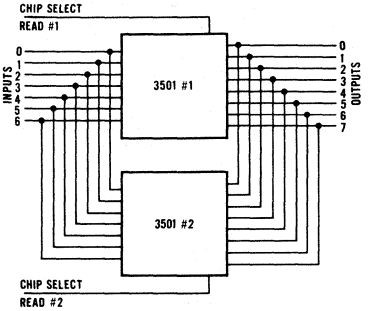
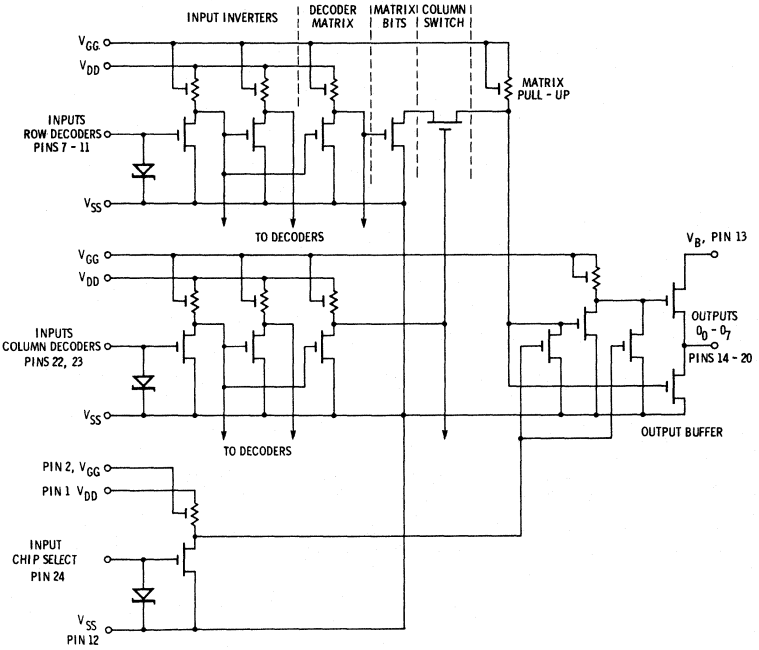


Fig. 3 — REPRESENTATIVE SCHEMATIC DIAGRAM



3512

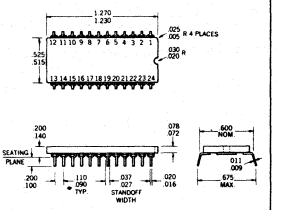
2048-BIT STATIC READ-ONLY MEMORY

SILICON GATE INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 3512 is a 2048-bit ROM manufactured with the Silicon Gate technology. The 8-line input address is decoded on chip to one of 256 possible 8-bit output words. No clocks are required as this is a static ROM. Typical access time when driving one DTL or TTL load is 500 ns. Four Chip Select inputs and a wired-OR output capability enable this device to be used in a 32K ROM system with no external components. An internal MOS pull-up resistor can be activated when the 3512 inputs are driven from a DTL or TTL source.

PHYSICAL DIMENSIONS

24 Lead Array Package



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .600" centers. They are purposely shipped with "positive" misalignment to facilitate insertion
Leads are gold-plated kovar
Package weight is 4.1 grams

FEATURES:

- Interfaces Directly with DTL/TTL — No External Components
- 500 ns Typical Access Time
- 4-Bit Programmable Chip Select Code
- Wired-OR Capability on Outputs

APPLICATIONS:

- Code Conversion
- Microprogramming
- Table Look-Up
- Control Logic

ABSOLUTE MAXIMUM RATINGS:

Voltage on Any Pin (V_{SS} = GND)	-25 V to +0.3 V
Storage Temperature	-65°C to +150°C
Operating Temperature	0°C to +70°C

FAIRCHILD
SEMICONDUCTOR

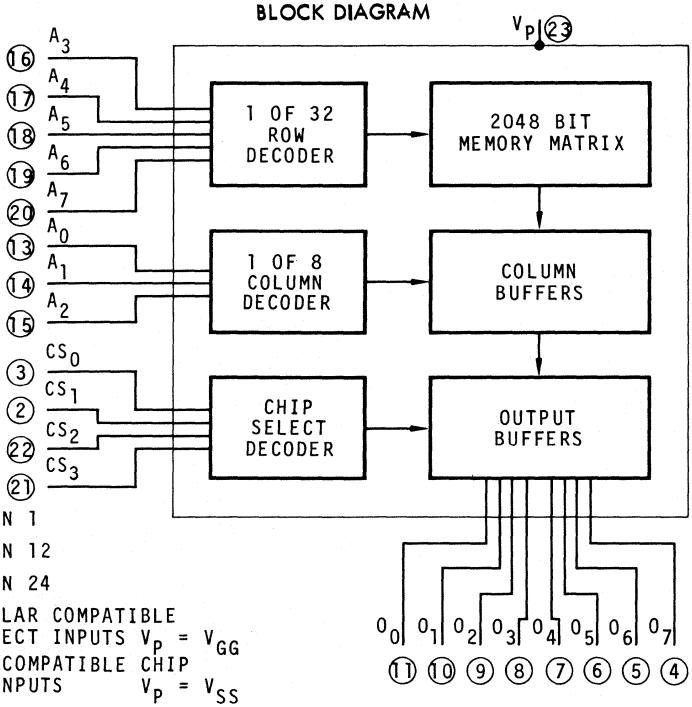
ELECTRICAL CHARACTERISTICS: Standard Test Conditions (unless otherwise specified).

V_{SS} = +5 V ± 5%, V_{GG} = -12 V ± 5%, V_{DD} = 0 V, T_A = 0°C to 70°C

Symbol	CHARACTERISTICS	MIN	TYP	MAX	Units	CONDITIONS
V_{IH}	Input High Voltage	V_{SS} - 1*		V_{SS}	Volts	Driven by DTL/TTL
V_{IL}	Input Low Voltage	V_{GG}		0.85	Volts	Driven by DTL/TTL
V_{OH}	Output High Voltage	2.4	3.0	V_{SS}	Volts	One DTL/TTL Load
V_{OH}	Output High Voltage	V_{SS}-0.5		V_{SS}	Volts	MOS Load
V_{OL}	Output Low Voltage	0	0.3	0.4	Volts	One DTL/TTL or MOS Load
T_A	Access Time		500		ns	One DTL/TTL or MOS Load
P	Power Consumption		575		mW	One DTL/TTL or MOS Load

* The usage of the internal pull-up (which is optional to the user) will automatically pull V_{IH} to a value of (V_{SS} - 1) when the device is driven by DTL/TTL.

BLOCK DIAGRAM



V_{GG} = PIN 1
V_{DD} = PIN 12
V_{SS} = PIN 24
FOR BIPOLAR COMPATIBLE CHIP SELECT INPUTS $V_P = V_{GG}$
FOR MOS COMPATIBLE CHIP SELECT INPUTS $V_P = V_{SS}$

3513

2560-BIT READ ONLY MEMORY

FAIRCHILD SILICON GATE MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The 3513 is a mask programmable, static, Read Only Memory, organized 256 words by ten bits. Both inputs and outputs are compatible with bipolar logic devices. There is also a customer programmable 3-bit chip select which allows simple expansion of the system. The 3513 is fabricated with p-channel enhancement mode SILICON GATE MOS technology.

FUNCTIONAL DESCRIPTION – The 3513 decodes an 8-bit address (A_0–A_7) into 256 addresses, each of which access ten bits of stored information. The first three bits of the input address turn on one of eight column switches to each of the ten matrix segments containing the stored information for each output bit. The remaining addresses (A_3 through A_7) select the row (1 of 32) which contains the specific bits. Logic levels and loading rules for inputs and outputs (O_0 through O_9) are much the same as normal bipolar rules, subject to some restrictions. These rules are given in the TTL interface explanation on page 5. Because the active level of the chip select inputs (CS_0 through CS_2) may be programmed with a custom pattern for use in multichip memories. When the chip is not selected, the output goes to a high impedance state thereby allowing "OR" tying.

V_{DD} serves as both an output buffer reference and matrix pull-up supply, some care must be exercised in maintaining relative voltage levels when using the device in systems with other than V_{DD} as ground reference.

FEATURES

- **INTERFACE DIRECTLY WITH TTL – NO EXTERNAL COMPONENTS**
- **500 ns TYPICAL ACCESS TIME**
- **3-BIT PROGRAMMABLE CHIP SELECT CODE**
- **WIRED-OR CAPABILITY ON OUTPUTS**

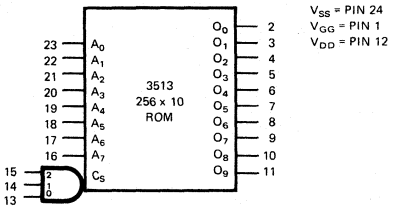
APPLICATIONS

- Code Conversion
- MICRO Programming
- Table Lookup
- Control Logic

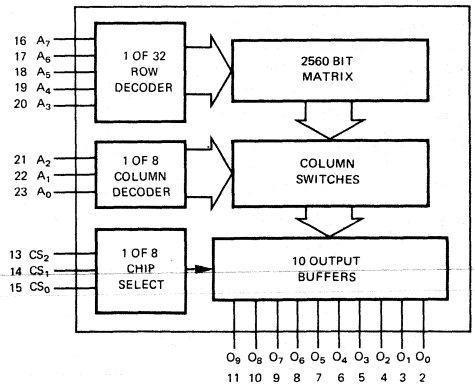
ABSOLUTE MAXIMUM RATINGS

Storage Temperature (T_S)	−55°C to +150°C
Operating Temperature (T_A)	0°C to +70°C
Voltage on Any Pin Relative to V_{SS}	−25 V to +0.3 V

3513 LOGIC SYMBOL



3513 LOGIC BLOCK DIAGRAM



FAIRCHILD
SEMICONDUCTOR

D C ELECTRICAL CHARACTERISTICS

Standard Conditions (Unless otherwise specified) V_{SS} = +5 V ±0.25 V, V_{GG} = −12 V ±0.60 V, V_{DD} = 0V T_A = 0°C to 70°C

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
V_{IH}	Input High Voltage	2.0		V_{SS}	V	V_{SS} = V_{CC} = +4.75 V
V_{IH}	Input High Voltage	2.5		V_{SS}	V	V_{SS} = V_{CC} = +5.25 V
V_{IL}	Input Low Voltage	V_{GG}		0.55	V	
V_{OH}	Output High Voltage	2.4		V_{SS}	V	I_{OH} = −90 μA
V_{OL}	Output Low Voltage	0		0.15	V	I_{OL} = 10 μA
V_{OL}	Output Low Voltage	0		0.40	V	I_{OL} = 2.4 mA
I_{RA}	Input Leakage			1.0	μA	V_{IN} = −10 V, Notes 1 and 3
I_{RO}	Output Leakage			1.0	μA	V_{OUT} = −6 V, Notes 1 and 3
C_O	Output Capacitance			15	pF	V_O = V_{OH}, Note 2
C_I	Input Capacitance			8.0	pF	V_I = V_{IH}, Note 2
I_{GG}	V_{GG} Current		39	57	mA	
I_{DD}	V_{DD} Current		1.0	3.0	mA	Output Open
I_{SS}	V_{SS} Current		40	60	mA	
P_C	Power Consumption		680	1070	mW	See Fig. 3

NOTES:

1. All pins at zero volts except that under test.
2. This parameter not tested but guaranteed by design.
3. Chip not selected.

A C ELECTRICAL CHARACTERISTICS

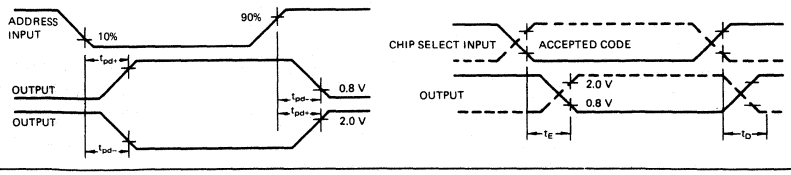
Standard Conditions (Unless otherwise specified) V_{SS} = +5 V ±0.25 V, V_{GG} = −12 V ±0.60 V, V_{DD} = 0V T_A = 0°C to 70°C

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
t_{pd+}	Access Time from Address to Output High	200	500	850	ns	Notes 4 and 5
t_{pd-}	Access Time from Address to Output Low	200	500	850	ns	Notes 4 and 5
t_E	Chip Select Enable to Output	200	500	850	ns	Note 5
t_D	Chip Select Disable to Output Disable	200	500	850	ns	Note 5

NOTES:

4. A standard load of one TTL. See TTL interface section.
5. See timing diagram and characteristic curves.

TIMING DIAGRAM



TYPICAL ELECTRICAL CHARACTERISTICS

Fig. 1
ACCESS TIME VERSUS SUPPLY VOLTAGE

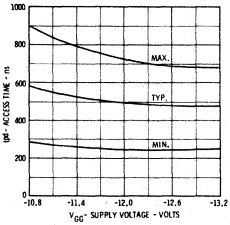


Fig. 2
ACCESS TIME VERSUS AMBIENT TEMPERATURE

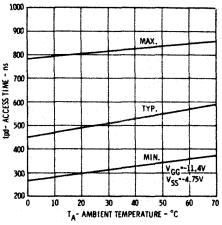


Fig. 3
SUPPLY CURRENT VERSUS AMBIENT TEMPERATURE

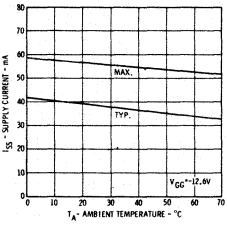


Fig. 4
ACCESS TIME VERSUS LOAD CAPACITANCE

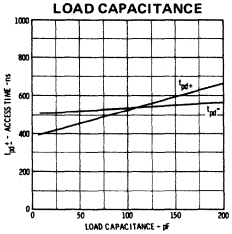


Fig. 5
OUTPUT HIGH VOLTAGE VERSUS OUTPUT CURRENT

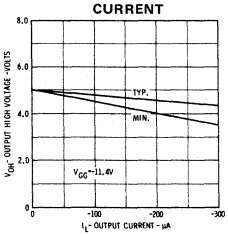


Fig. 6
OUTPUT LOW VOLTAGE VERSUS OUTPUT CURRENT

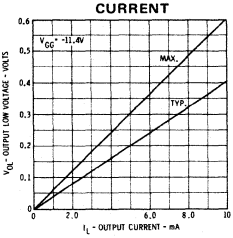


Fig. 7
SUPPLY CURRENT VERSUS SUPPLY VOLTAGE

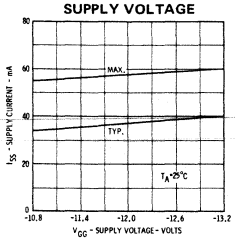


Fig. 8
OUTPUT HIGH VOLTAGE VERSUS AMBIENT TEMPERATURE

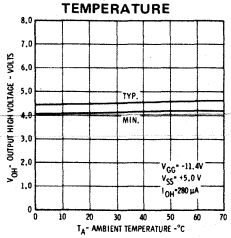
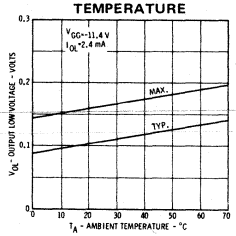


Fig. 9
OUTPUT LOW VOLTAGE VERSUS AMBIENT TEMPERATURE



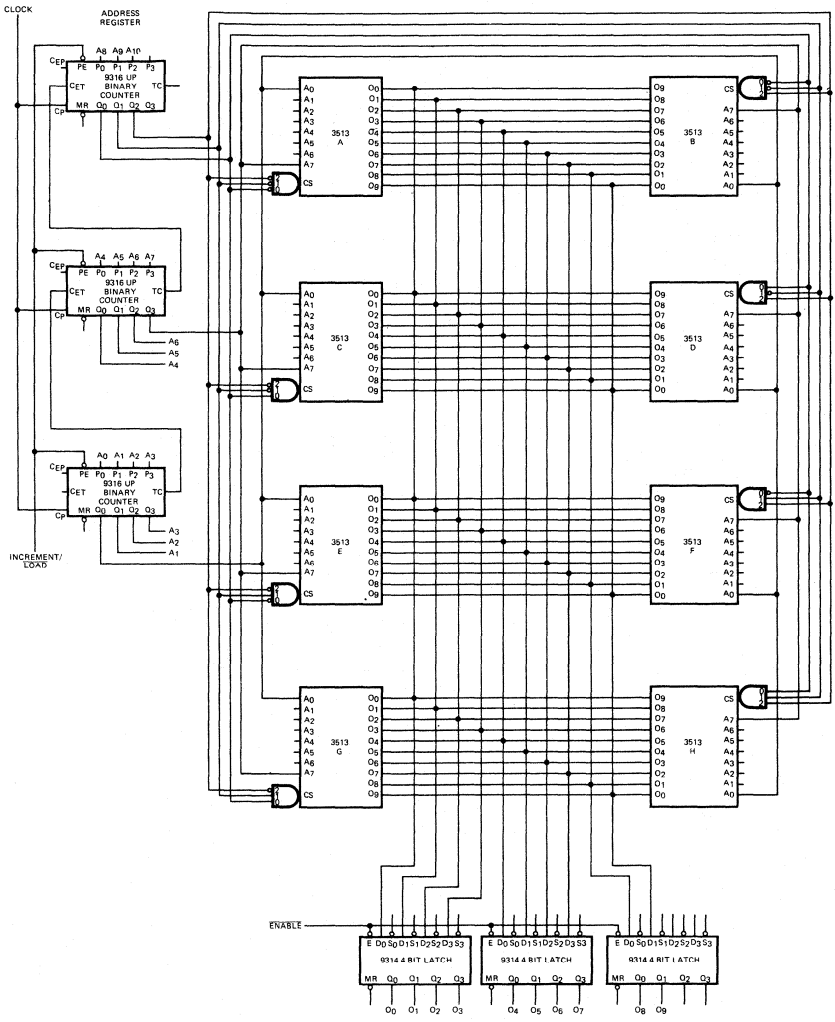


Fig. 10 2K BY 10 BIT READ ONLY MEMORY SYSTEM

This 2048 word by 10-bit system uses eight 3513 ROM's. The address is stored in the 9316 counters. New addresses may be obtained by parallel loading the counters or by incrementing the current address. Chip selects 0, 1, and 2 have been programmed on the devices to decode three bits of the address. The configuration shown follows the pin-out of the devices. Layout is simplified by turning over the right hand column so that all the outputs lie between the devices, as shown. The O_9 output on the right side corresponds to the O_0 output on the left side. The wire OR'ed data outputs can be connected directly to the inputs of the TTL MSI 9314 four bit latch.

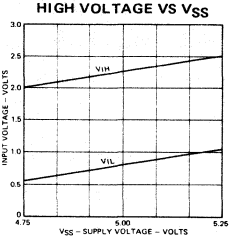
TTL INTERFACE

Both inputs and outputs may be interfaced with TTL, DTL and LPTTL without the use of external components or logic signals. Some constraints must be added to the normal TTL loading rules to insure a 400 mV noise margin while maintaining sufficient drive to the MOS. The need for these constraints arises primarily from the fact that MOS circuits are referenced to the positive supply (V_{SS}) while TTL circuits are referenced to the negative supply (Gnd). The constraints have been chosen to minimize their effect on application flexibility, but are not the only tradeoffs possible. The rules and their explanation are as follows:

1. Supply Voltages are ±5%. The input trip point of the MOS device directly tracks V_{SS}. As can be seen from Figure 11. V_{OH} could be specified as (V_{SS}–2.75V) and V_{OL} as (V_{SS}–4.2V). The choice of definition has been made to emphasize bipolar compatibility. The five percent restriction on V_{SS} insures sufficient drive for the MOS device in the low supply, high output low voltage condition. The five percent restriction on the V_{GG} supply insures sufficient current sinking capability at the MOS outputs.
2. V_{CC} and V_{SS} are common. For bipolar compatibility the input trip point of this device has been made less positive by circuit means, but still tracks the V_{SS} supply. The output high voltage of all bipolar logic devices under consideration also track their positive supply. This constraint was made to take maximum advantage of the nature of the circuits.
3. A bipolar gate driving MOS device may not drive more than 2 bipolar gates. This constraint reduces the sink current which the bipolar circuit must handle and thereby reduces the maximum output low voltage to 150 mV. This allows noise margin to be 500 mV – 150 mV = 400 mV.
4. An MOS output is limited to a maximum of one bipolar gate. MOS drivers may not have both an MOS and a bipolar load. If 400 mV noise margin is to be kept, the current sinking capability of the MOS device is limited to one TTL load in order to meet the TTL maximum zero rating of 400 mV. A maximum zero level of 150 mV must be met when driving another MOS device If 400 mV of noise margin is required. If, however, 400 mV of noise margin is not necessary (in cases of adjacent devices), many more MOS devices can be driven subject to access time versus load capacitance dependency. (See Figure 4.)

Fig. 11

MINIMUM INPUT HIGH VOLTAGE VS V_{SS}



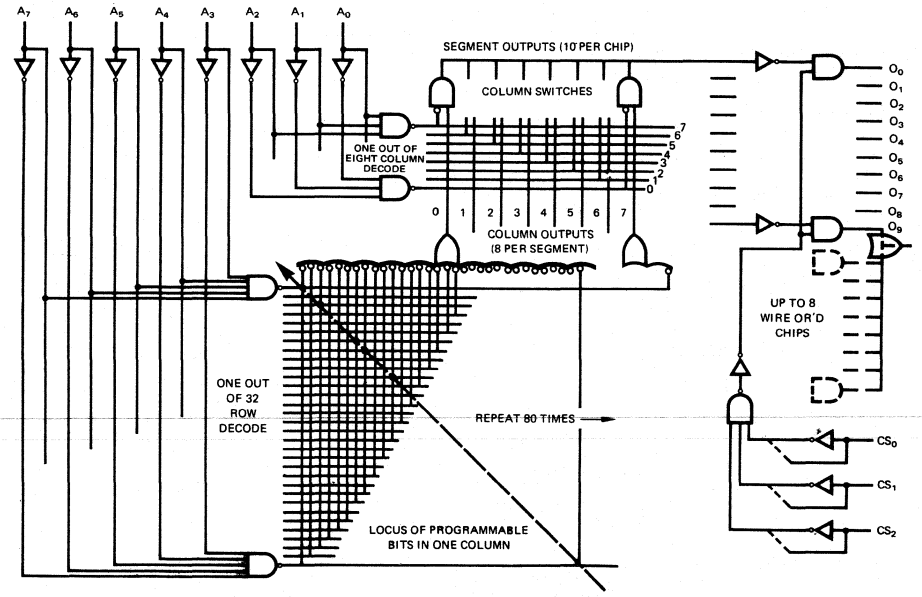


Fig. 12. 3513 ABBREVIATED LOGIC DIAGRAM

ORDERING INFORMATION – The 3513 is programmed on IBM cards or IBM coding forms in the format shown below.

A logical "1" = a more positive voltage (normally +5 V)
A logical "0" = a more negative voltage (normally 0 V)

FIRST CARD

Column Number	Description
29	CS_2 input required to select chip
31	CS_1 input required to select chip
33	CS_0 input required to select chip

REMAINING 256 CARDS

Column Number	Description
10, 12, 14, 16, 18, 20, 22, 24	Address input pattern. The most significant bit (A_7) is in column 10.
40, 42, 44, 46, 48, 50, 52, 54	Output pattern. The most significant bit (O_9) is in column 40.
73, 74, 75, 76, 77, 78, 79, 80	Coding these columns is not essential but may be used for card identification purpose

ORDER PART NO. A7C351319X

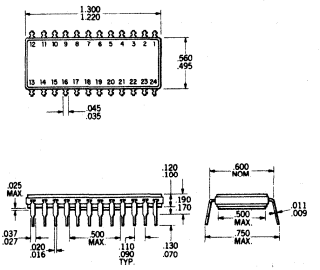
GLOSSARY OF TERMS

1. V_{SS}: The most positive voltage applied to the device.
2. V_{GG}: The most negative voltage applied to the device.
3. V_{DD}: The next most negative voltage applied to the device.
4. Address access time:
   t_{pd+} – The time delay from an address input high or low state to an output high state.
   t_{pd-} – The time delay from an address input high or low state to an output low state.
5. Chip enable time t_E: The time delay from Valid Code at chip select inputs to an output high or low state.
6. Chip disable time t_D: The time delay from removal of a valid chip select input code to a high state of the output with a standard TTL load (see note 4).
7. T_A: Still air ambient temperature.

PACKAGE INFORMATION

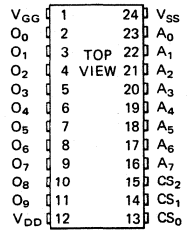
PHYSICAL DIMENSIONS

7C – 24 LEAD DUAL-IN-LINE



NOTES: All dimensions in inches
Leads are intended for insertion in hole rows on .600" centers. They are purposely shipped with "positive" misalignment to facilitate insertion
Base, cap and leads are gold-plated kovar
Package weight is 5.2 grams

CONNECTION DIAGRAM



512 x 1 RANDOM ACCESS MEMORY

FAIRCHILD SILICON GATE MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The 3532 is a 512 words by 1 bit non-destructive-read-out static Random Access Memory. It uses static circuitry for its memory cells. The decoding and sensing are accomplished by dynamic circuitry, thus resulting in low peripheral power consumption. This product is manufactured using p-channel enhancement mode SILICON GATE TECHNOLOGY.

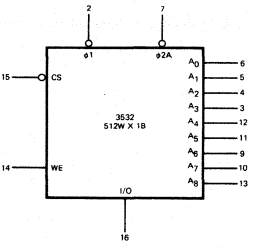
FEATURES

- **LOW POWER DISSIPATION – TYPICAL** { **0.3 mW/BIT – (OPERATING)** / **30 μW/BIT – (STANDBY)**
- **BIPOLAR COMPATIBLE (WITH EXTERNAL RESISTORS)**
- **WRITE/READ CYCLE TIME – 600 ns/1 μs**
- **STATIC MEMORY CELLS**
- **WIRE-OR CAPABILITY**
- **FULLY DECODED**
- **16 PIN DIP**
- **INPUT PROTECTION**

ABSOLUTE MAXIMUM RATINGS (above which useful life may be impaired)

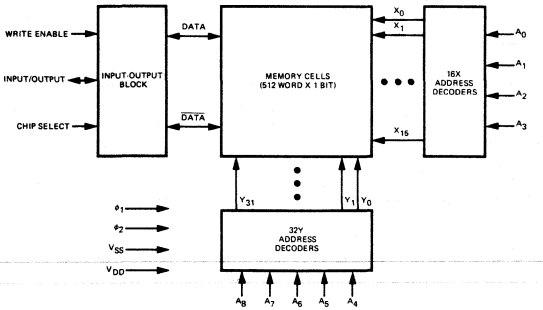
Storage Temperature	−65°C to +150°C
Operating Temperature	0°C to +70°C
All pins except I/O (V_{SS} = GND)	−24 V to +0.3 V
I/O Pin	−13 V to +0.3 V

LOGIC SYMBOL



V_{DD} = Pin 1
V_{SS} = Pin 8

BLOCK DIAGRAM



FAIRCHILD SEMICONDUCTOR

OPERATION – The 3532 is designed for easy system implementation. All logic signals (not including the clocks) are bipolar compatible with external pull up resistors. For the on-chip peripheral circuitry (address decoding and input-output), a two-phase clock system (ϕ_1 and ϕ_2) is required. However, because of the static nature of the memory cells, the two clocks can be turned off indefinitely during the standby condition and power consumption of the device would then be reduced considerably. To facilitate system expansion, data input and output of the device, which share one common device pin (I/O), have "Wire-Or" capability.

For WRITE OPERATION, the I/O pin is unconditionally precharged to a "Low" level when ϕ_1 clock is on. After ϕ_1 clock is off, the voltage level of the I/O pin will either remain "Low", if the system input signal (DI) is "Low", or, after some internal delay, will change to a "High", if the system data input signal (DI) is "High". After the ϕ_2 clock is on and after some internal delay, data input information will be "stored" into the addressed memory cell. (See figures of "TIMING" and "MULTICHIP MEMORY PLANE".)

For READ OPERATION the I/O pin is also unconditionally precharged to a "Low" level when ϕ_1 clock is on. The voltage level of the I/O pin will then remain "Low" until ϕ_2 is turned on. After ϕ_2 clock is on and after some internal delay; the stored logic level will define the output state. (See figures of "TIMING" and "MULTICHIP MEMORY PLANE".)

For memory system implementation, several 3532 packages can be "or-tied" and each of the "or-tied" packages can be either "selected" or "inhibited" with the chip select (CS) signal as shown in the figure of "MULTICHIP MEMORY PLANE". Interface of the I/O pin with system data input (DI) and system data output (DO) is also shown in the figure. During "read" operation, the "write" driver connected to the I/O pin must be inhibited.

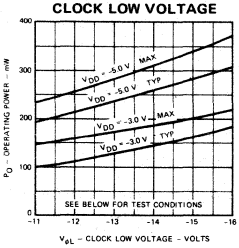
Appropriate timing for the two clocks and the logic signals is shown in the "TIMING" diagram.

DC CHARACTERISTICS (T_A = 0°C to 75°C, V_{SS} = +5.0V ±5%; V_{DD} = –3 V ±10%, unless otherwise specified)

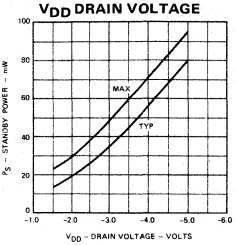
SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
$V_{\phi L}$	Clock "LOW" Voltage	–160		–13.5	Volts	
$V_{\phi H}$	Clock "HIGH" Voltage	V_{SS} – 1.0		V_{SS}	Volts	
V_{IL}	Input "LOW" Voltage			+0.8	Volts	
V_{IH}	Input "HIGH" Voltage	V_{SS} – 1.0		V_{SS} + 0.3	Volts	
V_{OL}	Output "LOW" Voltage			+0.40	Volts	One TTL and 680Ω Resistor to V_{SS}
V_{OH}	Output "HIGH" Voltage	2.4			Volts	
$I_{DD\phi 1}$	V_{DD} Supply Current, ϕ_1 ON		27	35	mA	$V_{\phi 1}$ = –16 V (DC); $V_{\phi 2}$ = +4.5 V (DC) I/O Pin Tied to +0.4 V
$I_{DD\phi 2}$	V_{DD} Supply Current, ϕ_2 ON		5.5	8.0	mA	$V_{\phi 1}$ = +4.5 V (DC); $V_{\phi 2}$ = –16 V (DC)
I_{DDS1}	V_{DD} Supply Current, Standby Condition 1 } See Note 4 of Timing		4.8	6.5	mA	$V_{\phi 1} = V_{\phi 2}$ = +4.5V
I_{DDS2}	V_{DD} Supply Current, Standby Condition 2 } See Note 4 of Timing		2.5	3.5	mA	$V_{\phi 1} = V_{\phi 2}$ = +4.5 V; V_{DD} = –1.5 V
I_{DDO}	Average V_{DD} Supply Current, Operating Condition		23.0	28.5	mA	(i) $V_{\phi L}$ = –16V; $V_{\phi H}$ = +4.5 V (ii) $t_{\phi 1}$ = 130 ns; $t_{\phi D1}$ = 150 ns $t_{\phi 2}$ = 280 ns; $t_{\phi D2}$ = 40 ns (iii) Alternating Write-Read Operations (iv) Alternating "High-Low" data Pattern for Write Operation
P_{DDO}	Average Operating Power		180	230	mW	
I_S	Output Sink Current	9.0	11.5	14	mA	$V_{\phi L}$ = –16 V; $V_{\phi H}$ = +4.5 V; V_{OUT} = 0.40 V
I_{IN}	Input Leakage Current			1.0	μA	$V_{SS} - V_{IN}$ = 6.0 V

DC CHARACTERISTIC CURVES

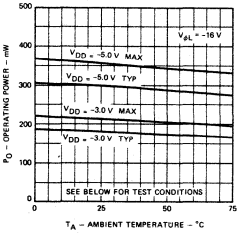
OPERATING POWER VERSUS* CLOCK LOW VOLTAGE



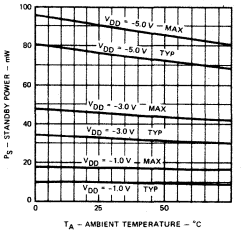
STANDBY POWER VERSUS V_{DD} DRAIN VOLTAGE



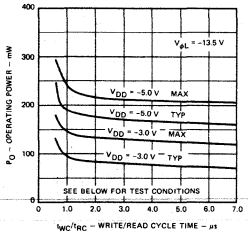
OPERATING POWER VERSUS* AMBIENT TEMPERATURE



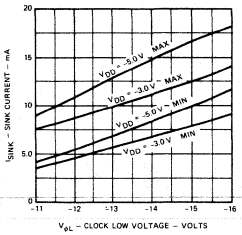
STANDBY POWER VERSUS AMBIENT TEMPERATURE



OPERATING POWER VERSUS* WRITE/READ CYCLE TIME



OUTPUT SINK CURRENT VERSUS CLOCK LOW VOLTAGE



OPERATING POWER TEST CONDITIONS

$t_{\phi 1}$ = 130 ns, $t_{\phi D1}$ = 150 ns, $t_{\phi s}$ = 280 ns, $t_{\phi D2}$ = 40 ns

Alternating Write/Read Operation (50% Write Time and Read Time)

R_L adjusted to V_{OL} = +0.40 V

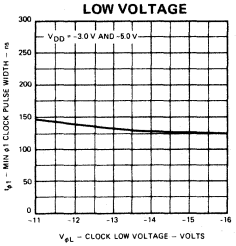
*Alternating "HIGH — LOW" data pattern for write operation.

AC CHARACTERISTICS (T_A = 0°C to 75°C, V_{SS} = +5.0 V ±5%; V_{DD} = −3 V ±10%, unless otherwise specified)

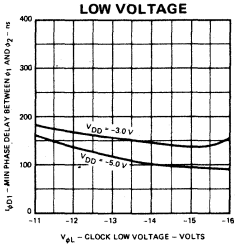
SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
C_ϕ	Clock Capacitance		50	65	pF	
C_{DI}	Data Input Capacitance		5.0	7.0	pF	Measuring frequency = 1 MHz
C_{ADD}	Address Capacitance		3.0	5.0	pF	All other device pins grounded
C_{CS}	Chip Select Capacitance		3.0	5.0	pF	
C_{WE}	Write Enable Capacitance		4.5	6.0	pF	
CLASS A (A7K353219A)						
$t_{\phi r}$	Clock Rise Time, 10% to 90%	0.04		1	μs	
$t_{\phi f}$	Clock Fall Time, 10% to 90%	0.02		1	μs	
$t_{\phi 1}$	ϕ_1 Clock Pulse Width	0.13		10	μs	
$t_{\phi 2}$	ϕ_2 Clock Pulse Width	0.28		10	μs	$V_{\phi L}$ = −13.5 V
$t_{\phi D1}$	Phase Delay Between ϕ_1 and ϕ_2	0.15		10	μs	$V_{\phi H}$ = +4.5 V
$t_{\phi D2}$	Phase Delay Between ϕ_2 and ϕ_1	40			ns	$t_{\phi r} = t_{\phi f} \cong 40$ ns
t_{OD}	Output Delay			270	ns	C_L = 45 pF, R_L = 680Ω and
t_{WC}	Write Cycle Time (= $t_{\phi 1} + t_{\phi D1} + t_{\phi 2} + t_{\phi D2}$)			600	ns	1 TTL Load
t_{RA}	Read Access Time (= $t_{\phi 1} + t_{\phi D1} + t_{OD}$)			550	ns	
t_S	Input Set Up Time	130			ns	
t_H	Address Hold Time	30			ns	

ELECTRICAL CHARACTERISTICS

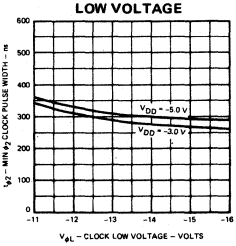
MINIMUM ϕ_1 CLOCK PULSE WIDTH VERSUS CLOCK LOW VOLTAGE



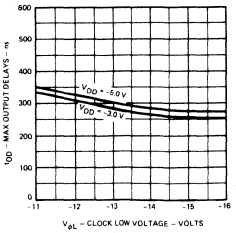
MINIMUM PHASE DELAY BETWEEN ϕ_1 AND ϕ_2 VERSUS CLOCK LOW VOLTAGE



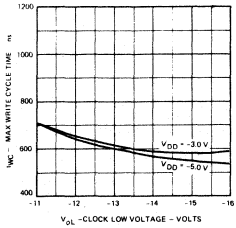
MINIMUM ϕ_2 CLOCK PULSE WIDTH VERSUS CLOCK LOW VOLTAGE



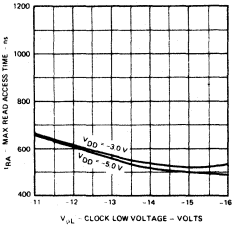
MAXIMUM OUTPUT DELAY VERSUS CLOCK LOW VOLTAGE



MAXIMUM WRITE CYCLE TIME VERSUS CLOCK LOW VOLTAGE



MAXIMUM READ ACCESS TIME VERSUS CLOCK LOW VOLTAGE

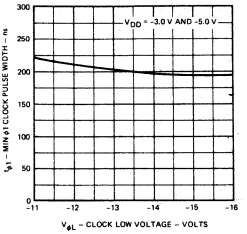


CLASS B (A7K353219B)

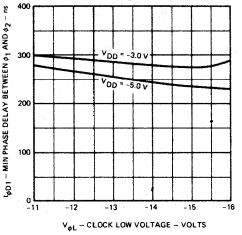
SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
$t_{\phi r}$	Clock Rise Time, 10% to 90%	0.04		1	μs	
$t_{\phi f}$	Clock Fall Time, 10% to 90%	0.02		1	μs	
$t_{\phi 1}$	ϕ_1 Clock Pulse Width	0.2		10	μs	
$t_{\phi 2}$	ϕ_2 Clock Pulse Width	0.46		10	μs	
$t_{\phi D1}$	Phase Delay Between ϕ_1 and ϕ_2	0.28		10	μs	$V_{\phi L}$ = −13.5 V $V_{\phi L}$ = +4.5 V
$t_{\phi D2}$	Phase Delay Between ϕ_2 and ϕ_1	60			ns	$t_{\phi r} = t_{\phi f} \cong 40$ ns
t_{OD}	Output Delay			440	ns	C_L = 45 pF, R_L = 680Ω and
t_{WC}	Write Cycle Time (= $t_{\phi 1} + t_{\phi D1} + t_{\phi 2} + t_{\phi D2}$)			1.0	μs	1 TTL Load
t_{RA}	Read Access Time (= $t_{\phi 1} + t_{\phi D1} + t_{OD}$)			920	ns	
t_s	Input Set Up Time	200			ns	
t_H	Address Hold Time	30			ns	

ELECTRICAL CHARACTERISTICS

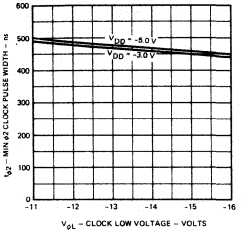
MINIMUM ϕ_1 CLOCK PULSE WIDTH VERSUS CLOCK LOW VOLTAGE



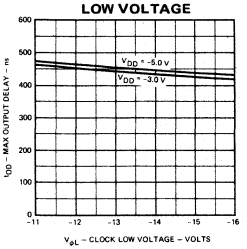
MINIMUM PHASE DELAY BETWEEN ϕ_1 AND ϕ_2 VERSUS CLOCK LOW VOLTAGE



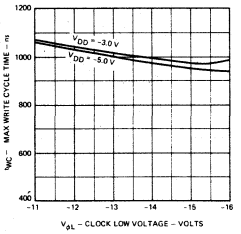
MINIMUM ϕ_2 CLOCK PULSE WIDTH VERSUS CLOCK LOW VOLTAGE



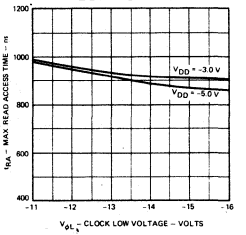
MAXIMUM OUTPUT DELAY VERSUS CLOCK LOW VOLTAGE



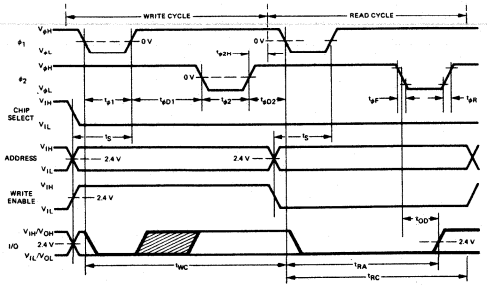
MAXIMUM WRITE CYCLE TIME VERSUS CLOCK LOW VOLTAGE



MAXIMUM READ ACCESS TIME VERSUS CLOCK LOW VOLTAGE

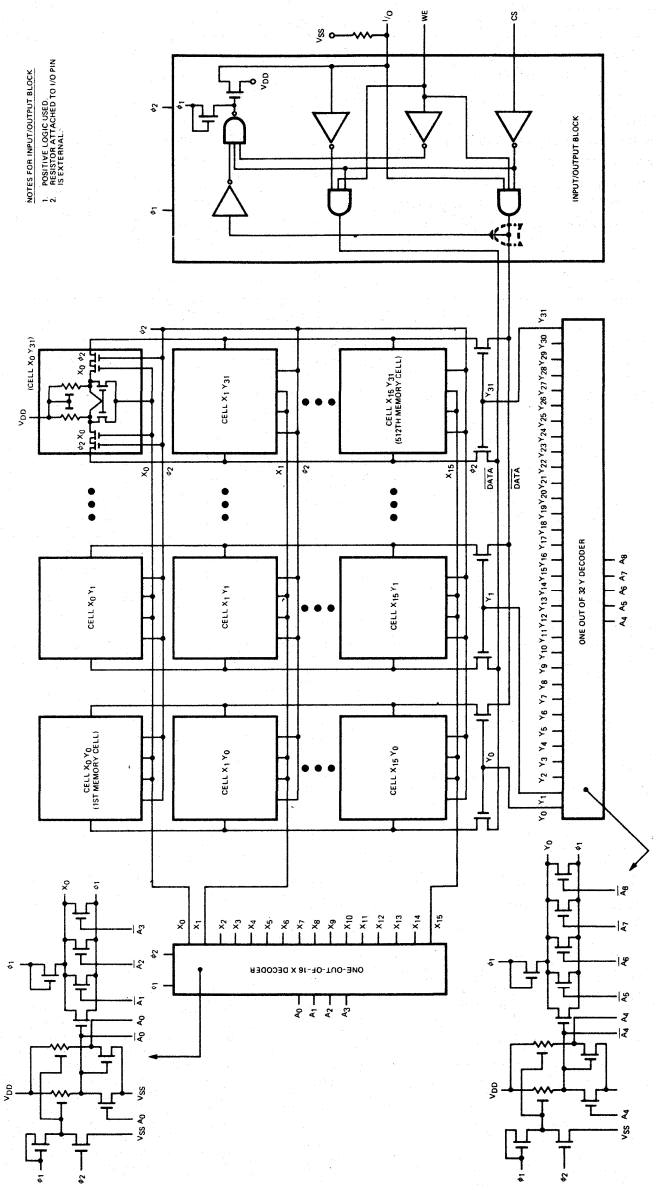


TIMING DIAGRAM

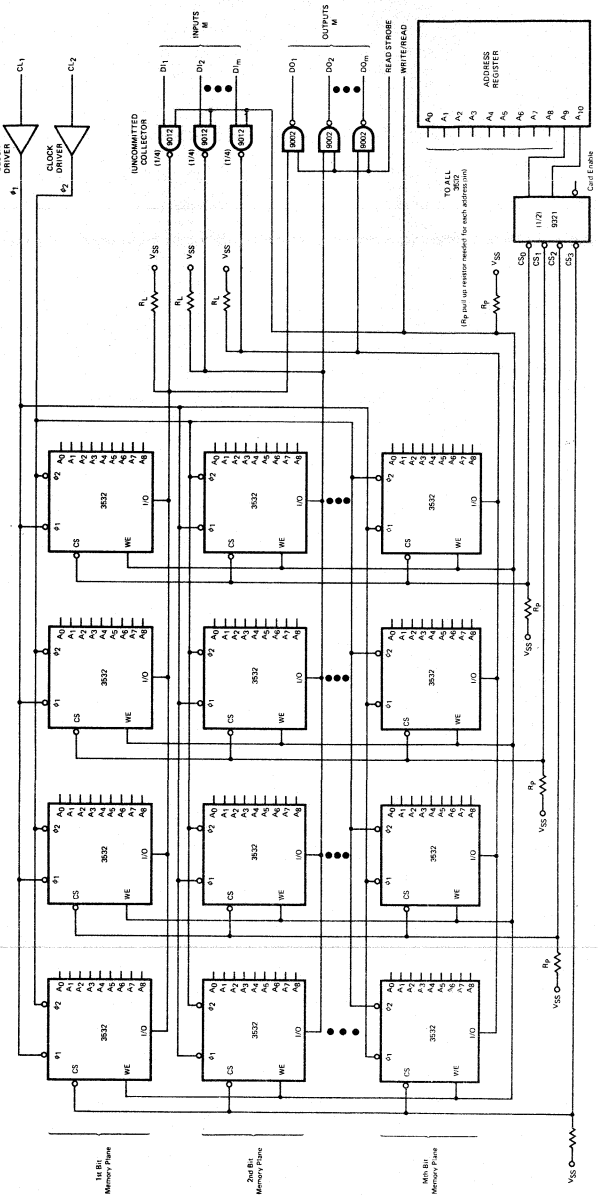


NOTES:
1. Data input driver must be disabled during read.
2. Output is an MOS device returned to V_{DD}.
3. For I/O waveform, thick line shows levels controlled by the memory itself while thin line indicates appropriate input levels. Whenever ϕ_1 is "ON" ($V_{\phi L}$), I/O voltage level will be pulled down to "Low" regardless of Write or Read Cycle. Shaded area indicates RC delay determined by output capacitance, output impedance and external pull up resistance.
4. During "Standby", data information for individual cells will not be lost even if V_{DD} is decreased to −1.5 V. Accordingly, standby power can be reduced if V_{DD} power supply is reduced to −1.5 V during standby condition.

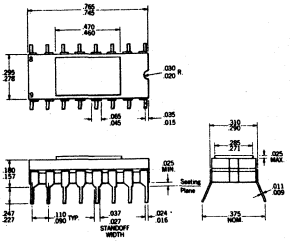
LOGIC-CIRCUIT SCHEMATIC DIAGRAM



MULTICHIP MEMORY PLANE
(2048 WORD BY M BITS)



PACKAGE INFORMATION



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are gold-plated kovar

ORDER PART NOS.: A7K353219A (600 ns t_{WC})
A7K353219B (1 μs t_{WC})

3534/1103
FULLY DECODED 1024–BIT RANDOM ACCESS DYNAMIC MEMORY
FAIRCHILD SILICON GATE MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The 3534 is a fully decoded 1024 X 1 dynamic Random Access Memory, especially suited for main memory applications. The circuitry is designed for maximum speed and low standby power dissipation. Unlike other memories, the 3534 does not have critical clock overlap requirements. Furthermore, the write cycle can be of the same duration as the read cycle. Readout is non-destructive and the data out line may be OR tied for ease of expansion. Exercise of the 32 row addresses is required for refresh every two milliseconds. This product is manufactured using p-channel enhancement mode silicon gate technology.

- **FULLY DECODED**
- **NO CLOCK OVERLAPPING REQUIRED**
- **NO CRITICAL "WRITE" TIMING REQUIRED**
- **ACCESS TIME – 300 ns max**
- **CYCLE TIME – 480 ns max**
- **REFRESH PERIOD – 2 ms**
- **EQUAL "READ" AND "WRITE" CYCLE TIME CAPABILITY**
- **CHIP ENABLE FOR EXPANSION**
- **"OR" TIE CAPABILITY**
- **18-LEAD DUAL IN-LINE PACKAGE**
- **STANDBY POWER – 2mW MAX**

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Operating Temperature	0°C to +70°C
All Pins (V_{SS} = GND)	–24 V to +0.3 V

ORDER PART NO. : A7T3534192/1103

BLOCK DIAGRAM

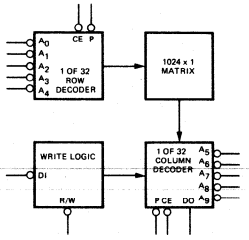
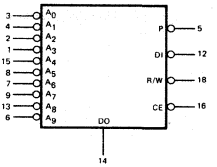


Fig. 3

LOGIC SYMBOL



V_{BB} - Pin 10
V_{SS} - Pin 17
V_{DD} - Pin 11

Fig. 1

CONNECTION DIAGRAM
DIP (TOP VIEW)

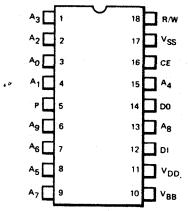


Fig. 2

FAIRCHILD
SEMICONDUCTOR

FUNCTIONAL DESCRIPTION – The block diagram (Figure 3) indicates the functions of various inputs and output. Inputs A_0 through A_9 select the memory cell to be accessed during a particular cycle. Precharge (P) powers the access circuitry and array columns. Chip Enable (CE) activates the row drivers and data input-output circuitry. Read/Write (R/W) enables the write circuitry of the chip if the chip has been selected by CE. Data-In (DI) determines whether a HIGH or LOW level is written into the cell during the write time. V_{SS}, V_{BB} and V_{DD} are dc bias supplies. The circuit diagram (Figure 13) indicates in greater detail the circuits used for the various functions.

When CE is positive ($\overline{CE}$ is negative) and Precharge goes negative, the column precharge enable switches are turned on and allow precharging of the columns. All row address decoders, except half of the column decoders (determined by A_8), are also charged LOW. Addresses must then stabilize and all but one row decoder and one column decoder will be pulled HIGH. A_8 is redundantly decoded and ANDed with the load device of the column decoders such that only 16 of the 32 decoders draw power when Precharge is LOW. This reduces the power dissipation of the column decoders.

When all the decoders are stabilized, Precharge can go HIGH and imposes no critical Precharge and Chip Enable timing requirement. The only requirement is that Precharge remain in the negative state long enough to precharge the columns and to power up the decoders and address inverters. Chip Enable drives one of 32 rows that is selected by the row decoders, thus selecting all 32 cells in that row. The cells are cross coupled latches with no load devices. Depending on the state of the bit (HIGH or LOW), one of the columns will be discharged and the other one remains charged. The charge stored on the columns refresh the storage node in the cell. This is due to charge sharing between column capacitance and the storage node. Since the capacitance of the column is much larger than the capacitance of the storage node, the storage node voltage is refreshed almost to the same voltage as the precharged column. Also, due to the regenerative action and the fact that the cell is being refreshed while accessed, the access time of the memory is short, consistent and insensitive to time between refresh.

The column and write switches selected by the row decoders and Read/Write direct data in and out of the selected column. Because of the nature of the cell, data is inverted on chip. The inverter, however, consumes power only when Read/Write is (LOW).

Since no refresh amplifiers are necessary, the Read/Write timing is not critical (see Write Cycle timing diagram), and need not be a pulse.

The timing diagrams show three basic cycles; Read, Write and Read/Write. As shown, the Read and Write cycles are the same length and the Read/Write cycle is somewhat longer. It is apparent that the critical times are minimized in order to facilitate ease of system implementation.

When all R/W, CE and P are all positive, there will only be leakage current flowing through V_{DD} thus reducing standby power to practically zero.

DC CHARACTERISTICS (V_{SS} = 16 V ±5%, $V_{BB} - V_{SS}$ = 3.5 V±0.5 V, V_{DD} = 0V, T_A = 0°C to 70°C) Note 1

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
I_{RI}	Input Leakage Current			1.0	µA	V_{IN} = 0 V
I_{RO}	Output Leakage Current			1.0	µA	V_{OUT} = 0 V
I_{BB}	V_{BB} Supply Current			100	µA	
I_{DD1}	Supply Current During Precharge		37	56	mA	Note 2
I_{DD2}	Supply Current During Overlap		38	59	mA	Note 2
I_{DD3}	Supply Current During Chip Enable		5.5	11	mA	P = V_{SS}, CE = 0 V T_A = 25°C
I_{DD4}	Supply Current Between Chip Enable and Precharge (Standby Current) Note 3			100	µA	R/W = V_{SS}, P = V_{SS} CE = V_{SS}, T_A = 25°C
I_{DD5}	Write Circuit Supply Current (Note 5)			4.0	mA	P = V_{SS}, CE = V_{SS} R/W = V_{DD}, DI = VDD
I_{DD}AVG	Average Supply Current (Notes 4 & 6)		17	25	mA	Cycle Time = 580 ns t_P = 190 ns, T_A = 25°C
V_{IL1}	Input Voltage LOW (A_0 thru A_9 and DI)	V_{SS} – 17		V_{SS} – 14.2	Volts	T_A = 0°C
V_{IL2}	Input Voltage LOW (A_0 thru A_9 and DI)	V_{SS} – 17		V_{SS} – 14.5	Volts	T_A = 70°C
V_{IL3}	Input Voltage LOW ($\overline{P}$, $\overline{CE}$ and $\overline{R/W}$ Inputs)	V_{SS} – 17		V_{SS} – 14.7	Volts	T_A = 0°C
V_{IL4}	Input Voltage LOW (P, CE and R/W Inputs)	V_{SS} – 17		V_{SS} – 15.0	Volts	T_A = 70°C
V_{IH1}	Input Voltage HIGH (All Inputs)	V_{SS} – 1.0		V_{SS} + 1.0	Volts	T_A = 0°C
V_{IH2}	Input Voltage HIGH (All Inputs)	V_{SS} – 0.7		V_{SS} + 1.0	Volts	T_A = 70°C
I_{OH1}	Output Current HIGH	0.6	0.9	4.0	mA	T_A = 25°C, R_L = 100Ω
I_{OH2}	Output Current HIGH	0.5	0.8	4.0	mA	T_A = 70°C, R_L = 100Ω
I_{OL}	Output Current LOW			10	µA	
V_{OH1}	Output Voltage HIGH	60	90	400	mV	T_A = 25°C, R_L = 100Ω
V_{OH2}	Output Voltage HIGH	50	80	400	mV	T_A = 70°C, R_L = 100Ω

AC CHARACTERISTICS (T_A = 0°C to 70°C, V_{SS} = 16 V ±5%, V_{BB} – V_{SS} = 3.5V±.5V, V_{DD} = 0 V, t_{rise} = t_{fall} = 20 ns)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
	READ, WRITE, AND READ/WRITE CYCLE					
t_{ref}	Time Between Refresh Cycles			2.0	ms	
t_{AC}	Address to Chip Enable Time	115			ns	
t_{CA}	Chip Enable to Address Time	20			ns	
t_{PC}	Precharge to Chip Enable Time	125			ns	
t_{CP}	Chip Enable to Precharge Delay	85			ns	
t_{AP}	Address to Precharge Time	115			ns	
	READ CYCLE					
t_{RC}	Read Cycle Time	480			ns	
t_P	Precharge Width	150			ns	
t_C	Chip Enable Width	190			ns	
t_{CO}	Chip Enable to Output Delay			165	ns	
t_{ACC1}	Address to Output Access	300			ns	R_L = 100 Ω, C_L = 100 pF
t_{ACC2}	Precharge to Output Access	310			ns	R_L = 100 Ω, C_L = 100 pF
	WRITE CYCLE					
t_{WCY}	Write Cycle	480			ns	
t_{CW}	Chip Enable to End of Write	150			ns	
t_{WP}	Write Pulse Width	80			ns	
t_{DW}	Data Set Up Time	105			ns	Note 7
t_{DH}	Data Hold Time	10			ns	Note 7
t_W	Write Setup Time	80			ns	
	READ/WRITE CYCLE					
t_{RWC}	Read/Write Cycle	580			ns	Note 8
	CAPACITANCE					
C_{AD}	Address Capacitance		5.0	7.0	pF	V_{IN} = V_{SS}, V_{BB} = V_{SS} + 3
C_{PR}	Precharge Capacitance		15	18	pF	V_{IN} = V_{SS}, V_{BB} = V_{SS} + 3
C_{CE}	Chip Enable Capacitance		15	18	pF	V_{IN} = V_{SS}, V_{BB} = V_{SS} + 3
C_{RW}	Read/Write Capacitance		11	15	pF	V_{IN} = V_{SS}, V_{BB} = V_{SS} + 3
C_{IN1}	Data Input Capacitance		4.0	5.0	pF	CE = 0 V
C_{IN2}	Data Input Capacitance		2.0	4.0	pF	CE = V_{SS}
C_{OUT}	Data Output Capacitance		2.0	3.0	pF	V_{OUT} = 0 V

NOTES:
(1) V_{BB} supply should be applied at or before V_{SS}.
(2) A_0 through A_9 = 0, P = 0 V, T_A = 25°C. CE = V_{SS} for I_{DD1} and CE = 0 V for I_{DD2}.

(3) Total standby power for chip is: $(V_{SS} - V_{DD})\left(I_{DD4} + \frac{t_P}{t_{ref}} I_{DD1} + \frac{t_C}{t_{ref}} I_{DD3}\right)$

(4) This parameter is tested on a sample basis.
(5) I_{DD5} will be drawn only when both R/W and DI are LOW.

(6) $I_{DDAVG} = \left[\frac{t_P}{t_{cycle}} I_{DD1} + \frac{t_C}{t_{cycle}} I_{DD3} + \frac{t_{cycle} - t_C - t_P}{t_{cycle}}\right] I_{DD4}$

(7) t_{DW} and t_{DH} are referenced to the rising (positive going) edge of CE or R/W, whichever occurs first.

(8) 580 ns read/write cycle time assumes a T_{DOW} of 65 ns. This is to allow for changing of data if data is ready. This cycle time can be shorter by 65 ns. If longer T_{DOW} is required, the cycle time will increase proportionately.

ELECTRICAL CHARACTERISTICS

SUPPLY CURRENT DURING PRECHARGE VERSUS AMBIENT TEMPERATURE

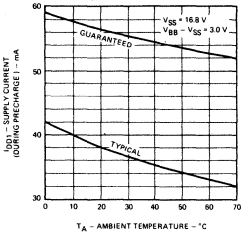


Fig. 4

SUPPLY CURRENT DURING OVERLAP VERSUS AMBIENT TEMPERATURE

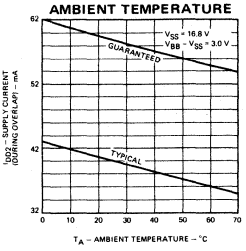


Fig. 5

SUPPLY CURRENT DURING CHIP ENABLE VERSUS AMBIENT TEMPERATURE

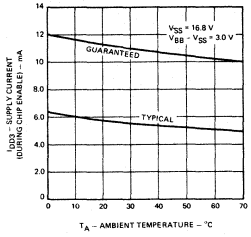


Fig. 6

SUPPLY CURRENT VERSUS TIME

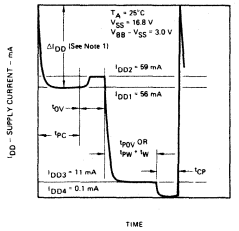


Fig. 7

(see Notes 1,2,3)

OUTPUT CURRENT HIGH VERSUS SUPPLY VOLTAGE

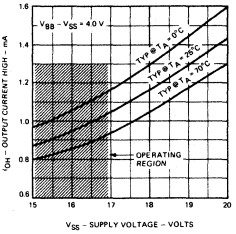


Fig. 8

AVERAGE SUPPLY CURRENT VERSUS SUPPLY VOLTAGE

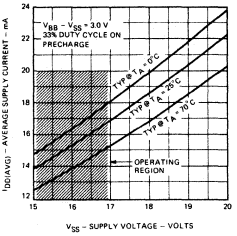


Fig. 9

GLOSSARY OF TERMS

P	Precharge
CE	Chip Enable
R/W	Read/Write
DI	Data In
DO	Data Out
V_{BB}	Substrate Bias
V_{SS}	Positive Circuit Bias
V_{DD}	Negative Circuit Bias
A_n	Single Bit of the Access Address.

NOTES: (Refer to Fig. 7)

1. ΔI_{DD} is due to charging of internal device node capacitance at precharge.
2. These values are taken from a single pulse measurement.
3. t_{0V} is not a required parameter, but when it occurs, current will be drawn as shown above.

READ CYCLE

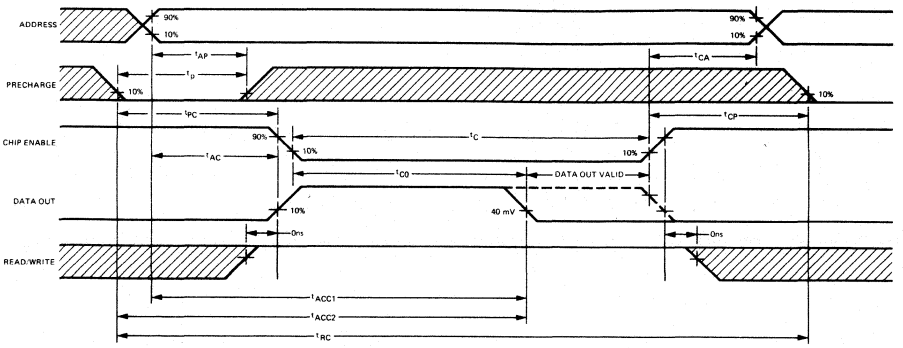


Fig. 10

WRITE CYCLE

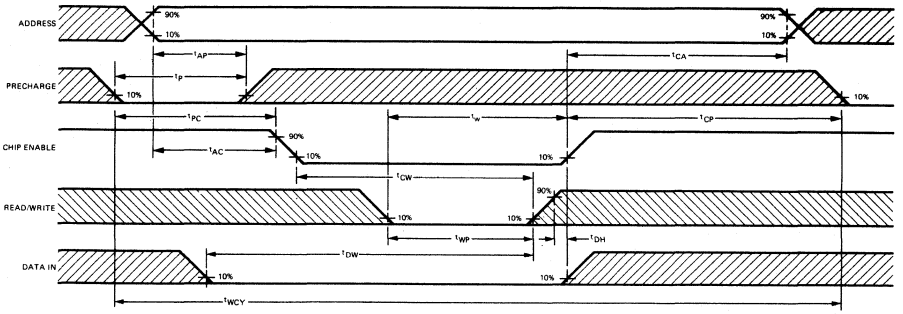


Fig. 11

READ/WRITE CYCLE

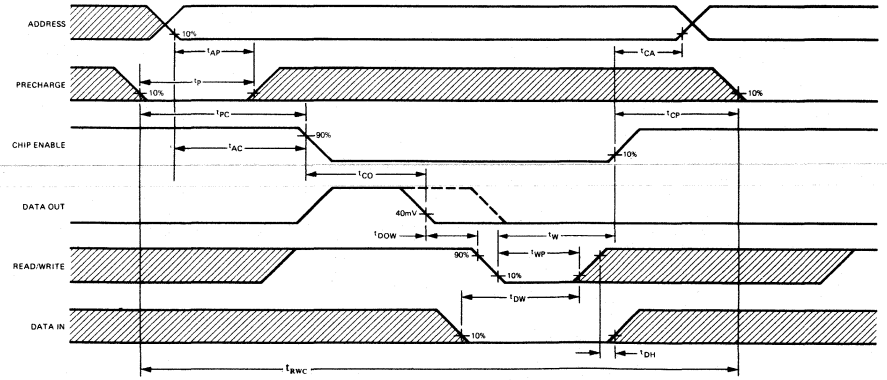


Fig. 12

PARTIAL SCHEMATIC DIAGRAM

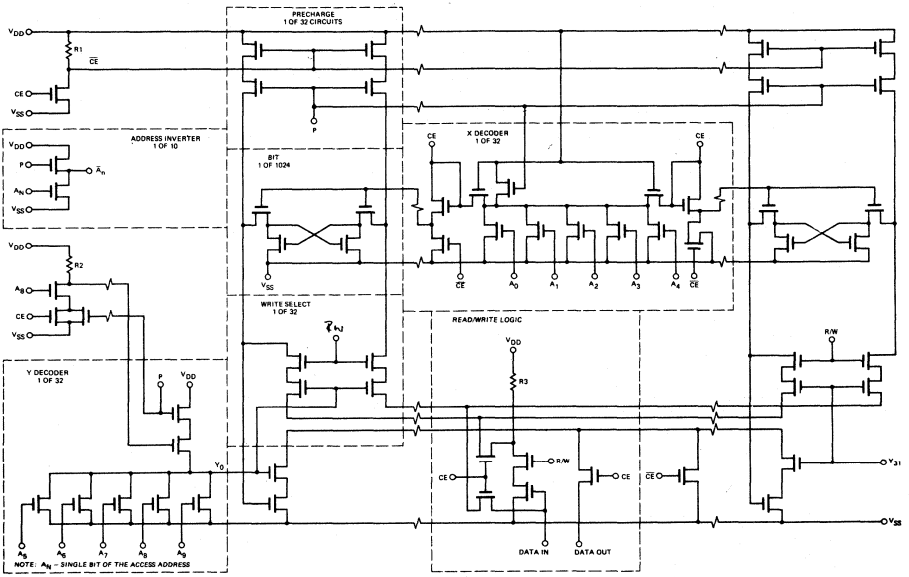
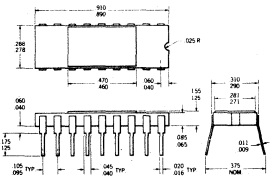


Fig. 13

PACKAGE INFORMATION



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" misalignment to facilitate insertion.
Board-drilling dimensions should equal your practice for .020" diameter lead
Leads are gold-plated kovar
Package weight is 1.3 grams

3584

2048-BIT (512 × 4) STATIC READ-ONLY MEMORY

MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION—The 3584 is a high threshold MOS static 512 word by 4-bit read only memory. The customer specifies the program to be stored in the memory and one mask is modified in the fabrication process to implement the code. The device incorporates binary decoding of the address and open drain data outputs. There is a chip select input to facilitate expansion. The 3584 is in a 24 pin DIP package.

FEATURES:

- **CHIP SELECT INPUT**
- **1.25 μs ACCESS TIME**
- **STATIC OPERATION**
- **WIRED-OR CAPABILITY**
- **OPEN DRAIN OUTPUTS**

APPLICATIONS

- **MICRO PROGRAMMING**
- **CODE CONVERSION**
- **TABLE LOOKUP**
- **CONTROL LOGIC**

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired.)

All Voltage and Data Input Lines (V_{SS} = 0V)	−30V to +0.3V
Power Dissipation	1000 mW
Storage Temperature	−55°C to +150°C
Operating Temperature	0°C to +70°C

Logic convention—MIL-806B is used throughout this data sheet. A LOW is the more negative logic level, and a HIGH is the more positive (≈ V_{SS}).
A small circle at the input to any element indicates that the relatively low (L) input signal activates the function.

BLOCK DIAGRAM

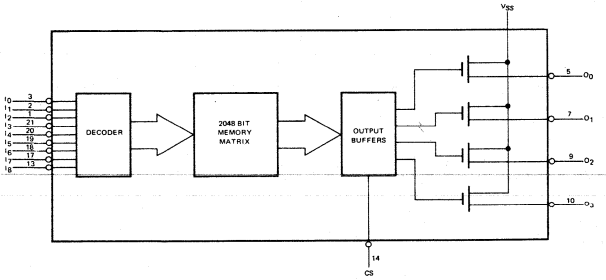
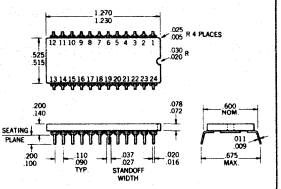


Fig. 4

PHYSICAL DIMENSIONS



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .600" centers. They are purposely shipped with "positive" misalignment to facilitate insertion
Leads are gold-plated kovar
Package weight is 4.1 grams
Lead No. 12 is connected to substrate

ORDER PART NO.
A6G358419X (0°C to 70°C)

Fig. 1

LOGIC SYMBOL

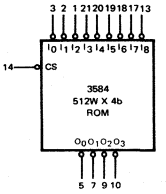


Fig. 2

PIN CONFIGURATION

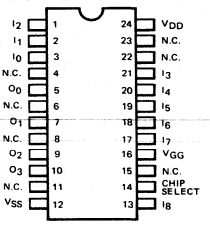


Fig. 3

FAIRCHILD SEMICONDUCTOR

FUNCTIONAL DESCRIPTION—A nine bit address applied to inputs I_0 to I_8 is decoded to select 4 bits from the 2048 bit memory matrix. These four bits go through an output buffer circuit and drive the gates of open drain transistors. If the chip select input is HIGH, the output drivers are off and the four open drain output transistors are off, effectively isolating the output pins. If the chip select is LOW, the output drivers are enabled. The data from the memory matrix then either turns on the output transistors, pulling the outputs up to V_{SS}, or turns off the output transistors, allowing the outputs to be pulled down to a negative level by external resistors.

The outputs of several 3584 ROM's may be tied together, as shown in Figure 13.

ELECTRICAL CHARACTERISTICS (V_{SS} = 0V, V_{DD} = −12V ±10%, V_{GG} = −24V ±10%, T_A = 0°C to 70°C)

SYMBOL	CHARACTERISTIC	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	CONDITIONS
V_{OH}	Output High Voltage	−1.0		0	Volts	I_{OH} = 0.5 mA
V_{OL}	Output Low Voltage			−10	Volts	I_{OL} = 0 (NOTE 2)
V_{IH}	Input High Voltage	−2.0			Volts	
V_{IL}	Input Low Voltage			−9.0	Volts	
C_I	Input Capacitance		10		pF	
C_O	Output Capacitance		6.0		pF	
I_{IL}	Input Leakage Current			5.0	μA	V_{IN} = −15 V All pins at V_{SS} except pin under test, T_A = 25°C
R_{ON}	Output Impedance to V_{SS} When Output is on.		1.0	2.0	kΩ	V_O = −1.0V
R_{OFF}	Output Impedance to V_{SS} When Output is Off	500	1.0		MΩ	V_O = −10V (No load)
I_{DD}	V_{DD} Supply Current		1.0	2.0	mA	
I_{GG}	V_{GG} Supply Current		12	20	mA	
P_D	Power Dissipation		300	500	mW	T_A = 25°C

A.C. CHARACTERISTICS (V_{SS} = 0V, V_{DD} = −12V ±10%, V_{GG} = −24V ±10%, T_A = 25°C) (Note 1)

SYMBOL	CHARACTERISTIC	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	CONDITIONS (Note 2)
t_{pd+}	Address to Output High Delay		1.25	2.0	μs	Fig. 6
t_{pd-}	Address to Output Low Delay		1.25	2.0	μs	Fig. 6
t_e	Chip Select to Output High Delay (Chip Selected)		0.8	1.0	μs	Fig. 5
t_{de}	Chip Select to Output Low Delay (Chip Not Selected)		0.8	1.0	μs	Fig. 5

NOTES:

1. Delay times are determined by internal delays plus the time required to charge C_L to V_{OH} or V_{OL}. Total times are heavily dependent on R_L and C_L.
2. R_L = 22 kΩ to −12 V C_L = 20 pF to V_{SS}.

TIMING DIAGRAM
(WAVEFORM DRAWINGS NOT TO SCALE FOR CLARITY)

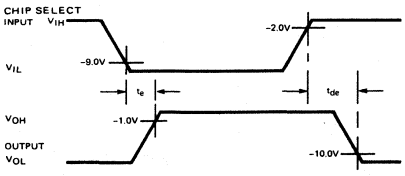


Fig. 5 - CHIP SELECT TO OUTPUT DELAY
Addressed such that the output device is on

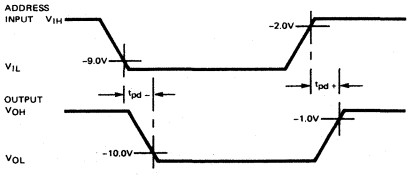


Fig. 6 - ADDRESS TO OUTPUT DELAY

TYPICAL ELECTRICAL CHARACTERISTICS

POWER DISSIPATION VERSUS SUPPLY VOLTAGE

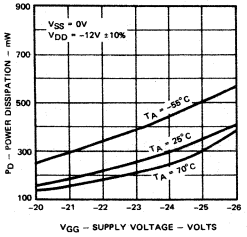


Fig. 7

SUPPLY CURRENT VERSUS SUPPLY VOLTAGE

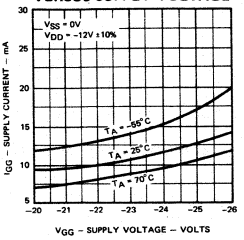


Fig. 8

ACCESS TIME VERSUS SUPPLY VOLTAGE

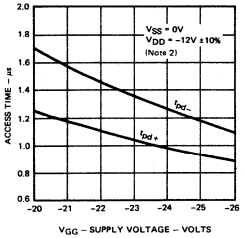


Fig. 9

ACCESS TIME VERSUS AMBIENT TEMPERATURE

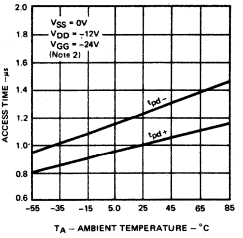


Fig. 10

APPLICATIONS

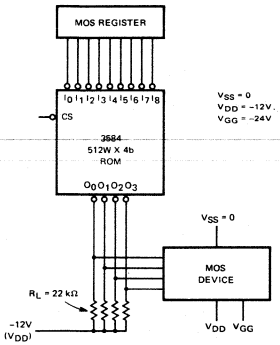


Fig. 11 - INTERFACE WITH OTHER HIGH THRESHOLD MOS

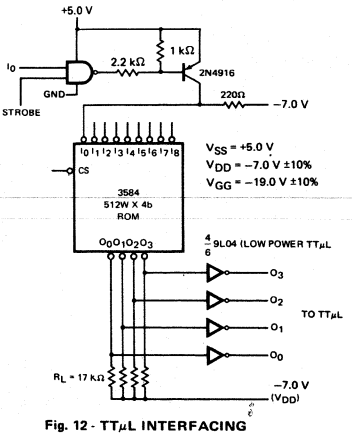


Fig. 12 - TTµL INTERFACING

APPLICATIONS

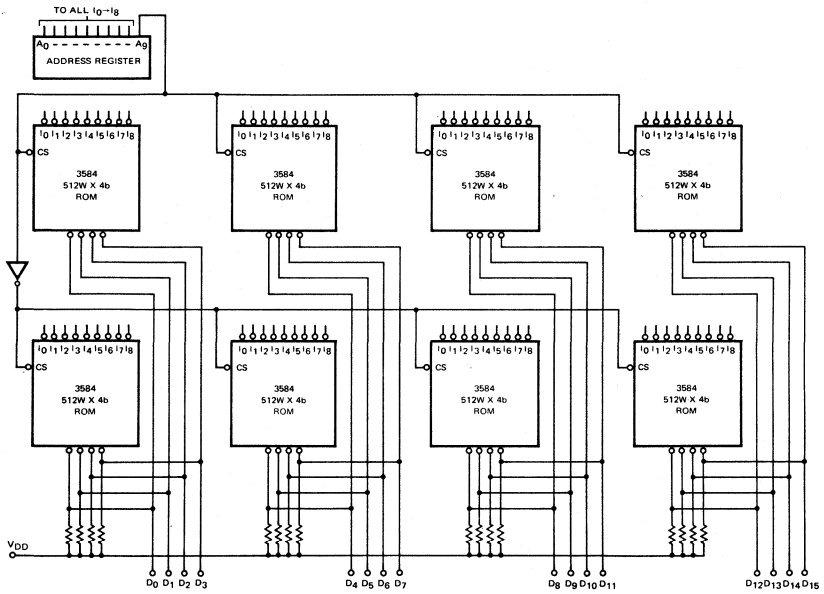


Fig. 13 - 1024 BY 16 BIT ROM USING THE 3584

GLOSSARY OF TERMS

1. V_{GG} The most negative voltage applied to the device.
2. V_{DD} An intermediate negative voltage applied to the device.
3. V_{SS} The most positive voltage applied to the device. Device substrate.
4. ADDRESS ACCESS TIME
   - t_{pd-} The delay between the time an address has changed its logical state and the output has changed from a V_{OH} to a V_{OL}.
   - t_{pd+} The delay between the time an address has changed its logical state and the output has changed from a logical 1 to a logical 0.
5. CHIP ENABLE ACCESS TIME
   - t_e The delay between the time the chip enable input reaches a logical 1 and the output reaches a logical 0.
   - t_{de} The delay between the time the chip enable input reaches a logical 0 and the output reaches a logical 1.
6. OUTPUT RESISTANCE
   - R_{ON} The amount of resistance measured from the output to V_{SS} when the output is at a logical 0 and V_O is equal to –1.0V.
   - R_{OFF} The amount of resistance measured from the output to V_{SS} when the output is at a logical 1 and V_O is equal to –10V.

CUSTOM BIT PATTERN ORDERING PROCEDURE

To order a custom bit pattern matrix

1. Customer will be furnished a Read-Only Memory Coding Form from Fairchild or a Fairchild representative. This form, when completed, will list each input and output bit pattern. From this information Fairchild will generate a Truth Table print out for verification, a custom mask and a final test program for each custom device, or
2. Customer will provide Fairchild with a Truth Table in the Coding Form format, or
3. Customer will provide Fairchild with prepunched computer cards in the coding Form format. A ZERO is a high and a ONE is a low.

3700

MOS MONOLITHIC 4-CHANNEL SWITCH

MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 3700 is a four-channel multiplex switch with all channel blanking. It is a monolithic integrated circuit utilizing Planar* II, P-Channel enhancement mode MOS technology. Control logic has been included on the chip to make the 3700 NPN bipolar compatible. The HLLDTμL 9112 High Level Hex Inverter can be used to directly interface the 3700 with TTμL logic levels. This device is intended for use in A/D Converters, Multiplexing, Analog or Digital Data Transmission Systems, and other airborne or ground instrumentation signal routing applications.

FEATURES:

- **BIPOLAR COMPATIBLE INPUT LOGIC LEVELS**
- **HIGH ON/OFF RATIO**
- **ALL CHANNEL BLANKING CONTROL**
- **PLANAR II STABILITY**
- **INPUT GATE PROTECTION**
- **LOW LEAKAGE CURRENT**
- **ZERO OFFSET VOLTAGE**

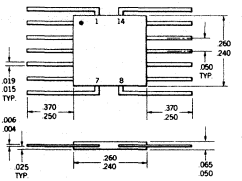
ABSOLUTE MAXIMUM RATINGS (Notes 1 and 2)

Storage Temperature		−65°C to +150°C
Operating Temperature	A3I370011X	−55°C to +125°C
	A3I370019X	0°C to +70°C
Positive Voltage on Any Pin		+0.3 V
Negative Voltage on Digital and Analog Input pins		
Analog Output pins		−30 V
Negative Voltage on V_{DD} and V_{GG} pins		
A3I3700112/192		−50 V
A3I3700113/193		−35 V
Total Power Dissipation in package (T_A = 25°C)		200 mW

ORDERING INFORMATION — The 3700 is available for use in two signal ranges. (See electrical characteristics for supply voltage requirements.)

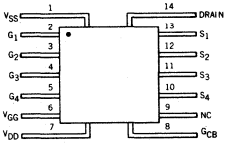
+5.0 to −5.0 volts signal applications, Order A3I3700112/192
0 to +5.0 volts signal applications, Order A3I3700113/193

PHYSICAL DIMENSIONS
In accordance with
JEDEC (TO-86) Outline

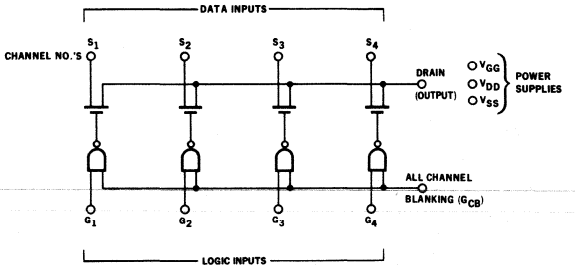


NOTES:
All dimensions in inches
Leads are gold-plated kovar
Package weight is 0.26 gram

PIN CONFIGURATION



LOGIC DIAGRAM



NOTES:
(1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.
(2) Voltage ratings are all referenced to pin 1 (V_{SS}).

*Planar is a patented Fairchild process.

FAIRCHILD
SEMICONDUCTOR

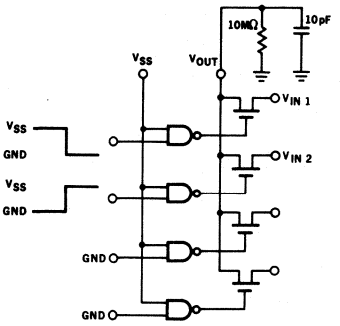
ELECTRICAL CHARACTERISTICS

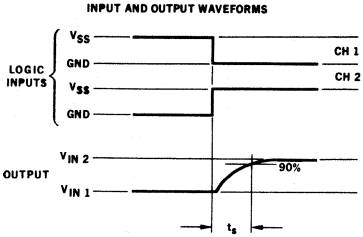
FOR 3700112/192: $-5.0\ V < V_{OUT} < +5.0\ V$, $T_A = 25°C$, $V_{DD} = V_{GG} = -35\ V \pm 10\%$, $V_{SS} = +8.0\ V \pm 10\%$ unless otherwise specified.

FOR 3700113/193: $0\ V \leq V_{OUT} \leq +5.0\ V$, $T_A = 25°C$, $V_{DD} = V_{GG} = -21\ V \pm 10\%$, $V_{SS} = +8.0\ V \pm 10\%$ unless otherwise specified.

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS	
R_{ON}	Channel "ON" Resistance			270	Ω	$V_{OUT} = V_{SS}$	$I_{OUT} = -100\ \mu A$
	A3I3700112			400	Ω	$V_{OUT} = -5.0\ V$	$I_{OUT} = -100\ \mu A$
	A3I3700113			400	Ω	$V_{OUT} = 0\ V$	$I_{OUT} = -100\ \mu A$
	A3I3700192			600	Ω	$V_{OUT} = -5.0\ V$	$I_{OUT} = -100\ \mu A$
	A3I3700193			600	Ω	$V_{OUT} = 0\ V$	$I_{OUT} = -100\ \mu A$
	A3I3700112 @ +125°C			650	Ω	$V_{OUT} = -5.0\ V$	$I_{OUT} = -100\ \mu A$
	A3I3700113 @ +125°C			650	Ω	$V_{OUT} = 0\ V$	$I_{OUT} = -100\ \mu A$
R_{OFF}	Channel "OFF" Resistance	1.5			GΩ	$V_{SS} - V_{OUT} = 15\ V$	V_G = Gnd
	A3I3700112/113 @ +125°C	2.1			MΩ	$V_{SS} - V_{OUT} = 15\ V$	V_G = Gnd
I_{LO}	Output Leakage Current						
	A3I3700112/113			2.0	nA	$V_{SS} - V_{OUT} = +15\ V$	V_G = Gnd
	A3I3700192/193			10	nA	$V_{SS} - V_{OUT} = +15\ V$	V_G = Gnd
	A3I3700112/113 @ +125°C			700	nA	$V_{SS} - V_{OUT} = +15\ V$	V_G = Gnd
I_{LI}	Data Input Leakage Current			1.5	nA	$V_{SS} - V_{IN} = 15\ V$	V_G = Gnd
	A3I3700112/113 @ +125°C			200	nA	$V_{SS} - V_{IN} = 15\ V$	V_G = Gnd
V_{IH}	Logic Gate Input "1" Level	V_{SS} - 1.5		V_{SS}	V		
V_{IL}	Logic Gate Input "0" Level	V_{SS} - 7.5		V_{SS} - 30	V		
t_s	Channel Switching Time (see Fig. 1)		1.0		μs		
C_{db}	Output Capacitance		25		pF	$V_{SS} - V_{OUT} = 0\ V$	f = 1.0 MHz
C_{is}	Data Input Capacitance		9.0		pF	$V_{SS} - V_{IN} = 0\ V$	f = 1.0 MHz
C_{ig}	Logic Input Capacitance		3.5		pF	$V_{SS} - V_G = 0\ V$	f = 1.0 MHz
C_{it}	Channel Blanking Input Capacitance		10		pF	$V_{SS} - V_G = 0\ V$	f = 1.0 MHz

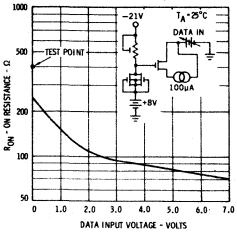
FIG. 1
SWITCHING TIME TEST CIRCUIT



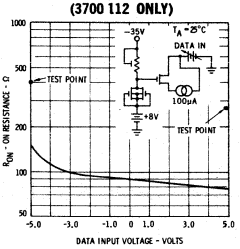


TYPICAL CHARACTERISTICS

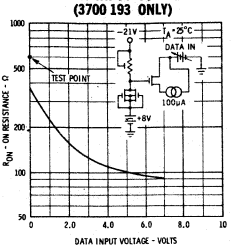
ON RESISTANCE VERSUS DATA INPUT VOLTAGE (3700 113 ONLY)



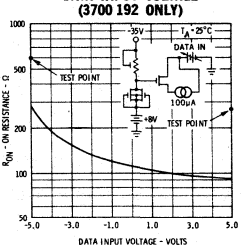
ON RESISTANCE VERSUS DATA INPUT VOLTAGE (3700 112 ONLY)



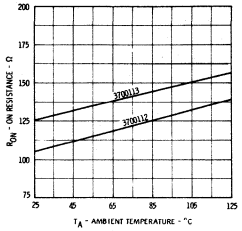
ON RESISTANCE VERSUS DATA INPUT VOLTAGE (3700 193 ONLY)



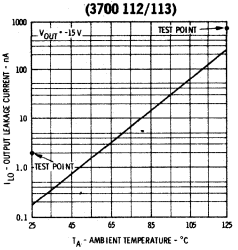
ON RESISTANCE VERSUS DATA INPUT VOLTAGE (3700 192 ONLY)



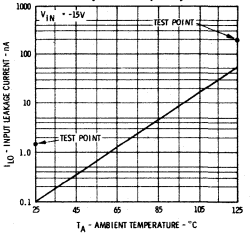
ON RESISTANCE VERSUS AMBIENT TEMPERATURE

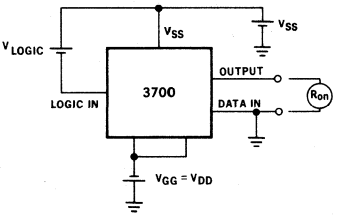


OUTPUT LEAKAGE CURRENT VERSUS AMBIENT TEMPERATURE (3700 112/113)



DATA INPUT LEAKAGE CURRENT VERSUS AMBIENT TEMPERATURE (3700 112/113)





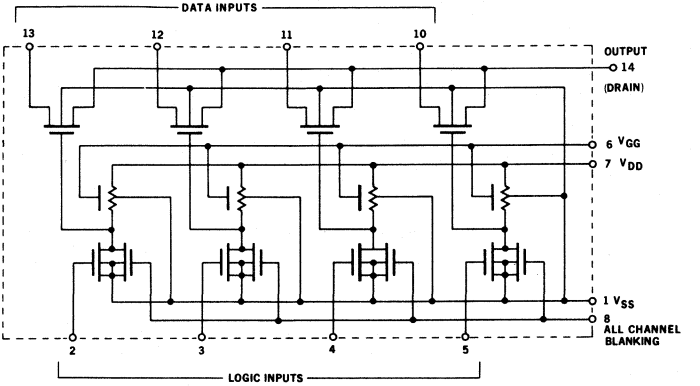
Voltage levels between semiconductor electrodes are normally referenced to one of the electrodes. In MOS, this electrode is the Substrate (body). The voltages can be translated to an equivalent level and referenced to another electrode. In order to measure the ON resistance of the data channel accurately, the data input is at ground potential and all other terminals are changed correspondingly to test worst case conditions.

The following sets of bias conditions are equivalent

	Condition 1	Condition 2	Condition 3
Data in	+5.0 V	−3.0 V	0 V
V_{SS}	+8.0 V	0 V	+3.0 V
$V_{DD} = V_{GG}$	−21 V	−29 V	−26 V
Logic in			
1 Level	+7.0 V	−1.0 V	+2.0 V
0 Level	+1.5 V	−6.5 V	−3.5 V

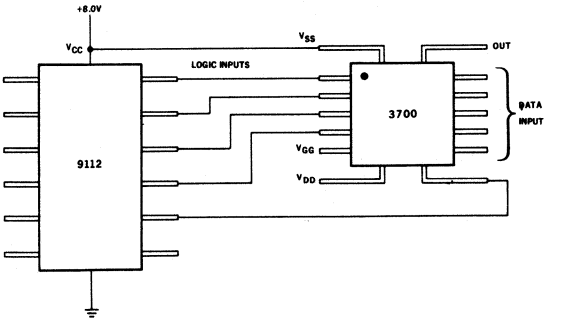
The logic input levels are V_{SS} - 30 V < "0" level < V_{SS} - 7.5 V to turn a data channel off
V_{SS} - 1.5 V < "1" level < V_{SS} to turn a data channel on.

SCHEMATIC DIAGRAM



TYPICAL CIRCUIT CONFIGURATION

Typical circuit configuration showing the 3700 driven by bipolar Diode-Transistor Logic such as the Fairchild HLLDTμL 9112.



3701
MOS MONOLITHIC 6-CHANNEL SWITCH
MOS INTEGRATED CIRCUIT

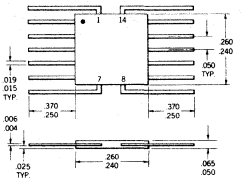
GENERAL DESCRIPTION — The 3701 is a P-channel enhancement mode Monolithic MOS six-channel, single output switch. This device can be used as a basic switching element for airborne or ground instrumentation, telemetry or other signal routing applications.

FEATURES
- **GATE PROTECTION**
- **ZERO OFFSET VOLTAGE**
- **LOW LEAKAGE CURRENT**
- **GUARANTEED OPERATIONS OVER —55°C TO +125°C**
- **PLANAR* II STABILITY**

ABSOLUTE MAXIMUM RATINGS (Note 1)

Storage Temperature		−65°C to +150°C
Operating Temperature	A3I370111X	−55°C to +125°C
	A3I370119X	0°C to +70°C
Power Dissipation at +25°C		200 mW
Positive Voltage on any pin ($V_{BODY} = 0$)		+0.3 Volt
Negative Gate Voltage ($V_{BODY} = 0$)		−35 Volts
Negative Source or Drain Voltage ($V_{BODY} = 0$)		−30 Volts

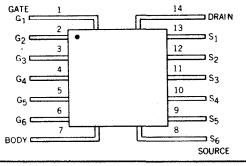
PHYSICAL DIMENSIONS
In accordance with
JEDEC (TO-86) Outline



NOTES:
All dimensions in inches
Leads are gold-plated kovar
Package weight is 0.26 gram

ORDER PART NO. A3I370111X/19X

PIN CONFIGURATION



ELECTRICAL CHARACTERISTICS ($V_{BODY} = 0$ Volt, $T_A = 25°C$ unless otherwise specified)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
R_{ON}	Channel "ON" Resistance					
	A3I370111X		210	375	Ω	$V_S = 0$ V, $V_G = -30$ V, $I_D = -100$ μA
	A3I370111X (125°C)		310	550	Ω	$V_S = 0$ V, $V_G = -30$ V, $I_D = -100$ μA
	A3I370119X		300	500	Ω	$V_S = 0$ V, $V_G = -30$ V, $I_D = -100$ μA
R_{OFF}	Channel "OFF" Resistance					
	A3I370111X	10	200		GΩ	$V_D = -20$ V, $V_G = 0$, $V_S = 0$ V
	A3I370111X (125°C)	100	250		MΩ	$V_D = -20$ V, $V_G = 0$, $V_S = 0$ V
	A3I370119X	4.0	200		GΩ	$V_D = -20$ V, $V_G = 0$, $V_S = 0$ V
$V_{GS(TH)}$	Gate Threshold Voltage			−5.5	Volts	$V_S = 0$ V, $V_G = V_D$, $I_D = -10$ μA
I_{SL}	Input Leakage					
	A3I370111X			1.0	nA	$V_S = -20$ V, $V_D = 0$ V, $V_G = 0$ V
	A3I370111X (125°C)			150	nA	$V_S = -20$ V, $V_D = 0$ V, $V_G = 0$ V
	A3I370119X			1.0	nA	$V_S = -20$ V, $V_D = 0$ V, $V_G = 0$ V

*Planar is a patented Fairchild process.

NOTE:
(1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.

FAIRCHILD
SEMICONDUCTOR

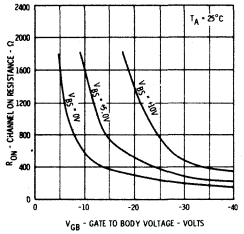
FAIRCHILD MOS INTEGRATED CIRCUIT 3701

ELECTRICAL CHARACTERISTICS (V_{BODY} = 0 Volt, T_A = 25°C unless otherwise specified)

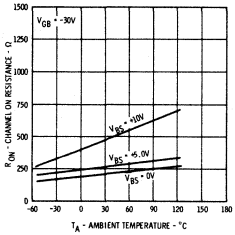
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
I_{DL}	Output Leakage					
	A3I370111X			2.0	nA	$V_D = -20$ V, $V_S = V_G = 0$ V
	A3I370111X (125°C)			200	nA	$V_D = -20$ V, $V_S = V_G = 0$ V
	A3I370119X			5.0	nA	$V_D = -20$ V, $V_S = V_G = 0$ V
I_{GL}	Gate Leakage			1.0	nA	$V_G = -20$ V, $V_D = V_S = 0$ V
C_S	Input Capacitance		4.0		pF	$V_S = 0$ V, $V_D = 0$ V, $V_G = 0$ V
C_S	Input Capacitance		3.0		pF	$V_S = -10$ V, $V_D = 0$ V, $V_G = 0$ V
C_D	Output Capacitance		13		pF	$V_S = 0$ V, $V_D = 0$ V, $V_G = 0$ V
C_D	Output Capacitance		7.0		pF	$V_S = 0$ V, $V_D = -10$ V, $V_G = 0$ V
C_G	Gate Capacitance		4.0		pF	$V_S = 0$ V, $V_D = 0$ V, $V_G = 0$ V
C_{GS} or C_{GD}	Gate-Source or Gate-Drain Capacitance		1.0		pF	$V_S = 0$ V, $V_D = 0$ V, $V_G = 0$ V

A3I370111X

TYPICAL CHANNEL ON RESISTANCE VERSUS GATE TO BODY VOLTAGE WITH BODY TO SOURCE VOLTAGE AS PARAMETER

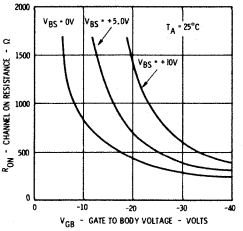


TYPICAL CHANNEL ON RESISTANCE VERSUS AMBIENT TEMPERATURE WITH BODY TO SOURCE VOLTAGE AS PARAMETER

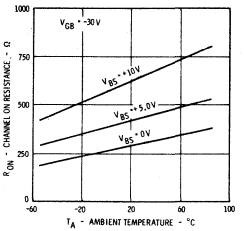


A3I370119X

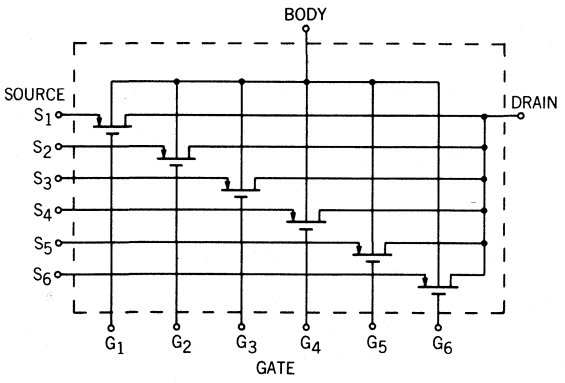
TYPICAL CHANNEL ON RESISTANCE VERSUS GATE TO BODY VOLTAGE WITH BODY TO SOURCE VOLTAGE AS PARAMETER



TYPICAL CHANNEL ON RESISTANCE VERSUS AMBIENT TEMPERATURE WITH BODY TO SOURCE VOLTAGE AS PARAMETER



SCHEMATIC DIAGRAM



3705

MOS MONOLITHIC 8-CHANNEL MULTIPLEX SWITCH

MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 3705 is an eight-channel multiplex switch with output enable control and one-out-of-eight decoder included on the chip. It is a monolithic integrated circuit utilizing Planar* II, P-channel enhancement Mode MOS technology. The logic input lines of the 3705 are NPN bipolar compatible and can be used directly with CCSL 5.0 volt logic levels with no level-shifting interface required. This device is intended for use in A/D converters, multiplexing in analog or digital data transmission systems, and other airborne or ground instrumentation signal routing applications.

FEATURES

- **CCSL COMPATIBLE INPUT LOGIC LEVELS**
- **ONE-OUT-OF-EIGHT DECODER ON THE CHIP**
- **HIGH ON/OFF RATIO**
- **OUTPUT ENABLE CONTROL**
- **PLANAR II STABILITY**
- **INPUT GATE PROTECTION**
- **LOW LEAKAGE CURRENT**
- **ZERO OFFSET VOLTAGE**

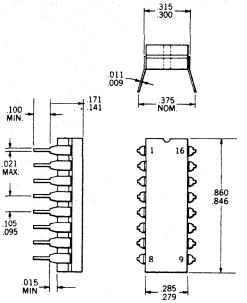
ABSOLUTE MAXIMUM RATINGS (Notes 1 and 2)

Storage Temperature	−65°C to +150°C
Operating Temperature	−55°C to +85°C
Positive Voltage on any pin	+0.3 V
Negative Voltage on digital and analog input pins	−35 V
Negative Voltage on analog output pins	−35 V
Negative Voltage on V_{DD} pin	−35 V
Total power dissipation in package (T_A = 25°C)	200 mW

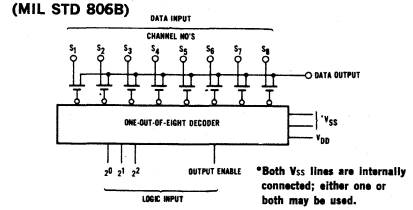
ORDERING INFORMATION — The 3705 is available for use in two signal ranges

−5.0 to +5.0 volts signal applications, Order A6J3705142
0 to +5.0 volts signal applications, Order A6J3705143

PHYSICAL DIMENSIONS
16 Lead Dual In-Line



SYMBOLIC DIAGRAM
(MIL STD 806B)

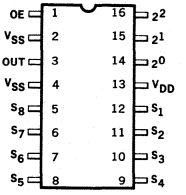


***Both V_{SS} lines are internally connected; either one or both may be used.**

TRUTH TABLE

LOGIC INPUTS				CHANNEL
2^0	2^1	2^2	OE	'ON'
L	L	L	H	S_1
H	L	L	H	S_2
L	H	L	H	S_3
H	H	L	H	S_4
L	L	H	H	S_5
H	L	H	H	S_6
L	H	H	H	S_7
H	H	H	H	S_8
X	X	X	L	OFF

PIN CONFIGURATION
(16 lead DIP)



TOP VIEW

NOTES:

(1) These ratings are limiting values above which the serviceability of the device may be impaired.
(2) Voltage ratings are all referenced to pins 2 and 4 (V_{SS}).

*Planar is a patented Fairchild process.

FAIRCHILD
SEMICONDUCTOR

FAIRCHILD MOS INTEGRATED CIRCUIT 3705

ELECTRICAL CHARACTERISTICS

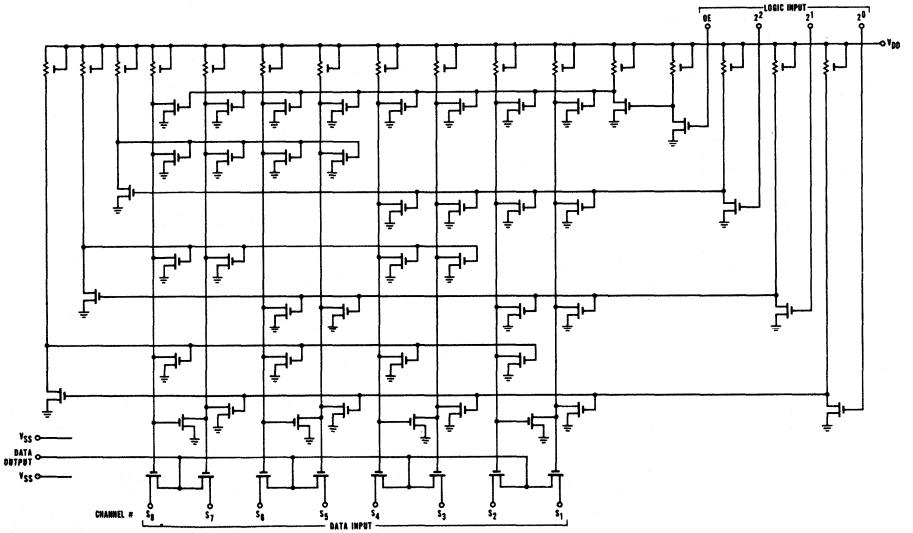
For 3705142: $-5.0\ V < V_{OUT} < +5.0\ V$, $T_A = 25°C$, $-20\ V < V_{DD} < -24\ V$, $5.0\ V < V_{SS} < 7.0\ V$ unless otherwise specified

For 3705143: $0\ V < V_{OUT} < +5.0\ V$, $T_A = 25°C$, $-20\ V < V_{DD} < -24\ V$, $5.0\ V < V_{SS} < 7.0\ V$ unless otherwise specified

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
R_{ON}	Data Channel "ON" Resistance					
	142		250	400	Ω	$V_{OUT} = -5.0\ V$, $I_{OUT} = -100\ \mu A$
	143		190	350	Ω	$V_{OUT} = 0\ V$, $I_{OUT} = -100\ \mu A$
R_{OFF}	Data Channel "OFF" Resistance	1.5			GΩ	$V_{SS} - V_{OUT} = 15\ V$
I_{LO}	Output Leakage Current			10	nA	$V_{SS} - V_{OUT} = 15\ V$
$I_{LO}(85°C)$	Output Leakage Current			500	nA	$V_{SS} - V_{OUT} = 15\ V$
I_{LDI}	Data Input Leakage Current					
	142			3.0	nA	$V_{SS} - V_{IN} = 15\ V$
	143			2.0	nA	$V_{SS} - V_{IN} = 10\ V$
I_{LI}	Logic Input Leakage Current			1.0	μA	$V_{SS} - V_{LOGIC\text{-}IN} = 15\ V$
*V_{IL}	Logic Gate Input "Low" Level	V_{DD}		+0.2	V	
*V_{IH}	Logic Gate Input "High" Level	$V_{SS} - 1.5$		V_{SS}	V	
t_S	Channel Switching Time (See Fig. 1)		1.0		μS	
C_{db}	Output Capacitance		40		pF	$V_{SS} - V_{OUT} = 0\ V$, $f = 1.0\ MHz$
C_{is}	Data Input Capacitance		7.5		pF	$V_{SS} - V_{IN} = 0\ V$, $f = 1.0\ MHz$
C_{ig}	Logic Input Capacitance		5.5		pF	$V_{SS} - V_{LOGIC\text{-}IN} = 0\ V$, $f = 1.0\ MHz$
P_D	Power Dissipation		130	175	mW	$V_{DD} = -31\ V$, $V_{SS} = 0\ V$

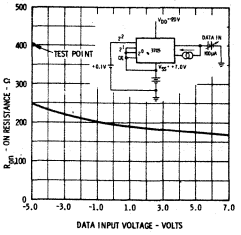
*When driven by CCSL elements, avoid excessive D.C. loading of CCSL elements to insure 3705 logic levels under maximum fan-out conditions.

SCHEMATIC DIAGRAM

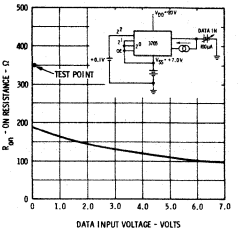


TYPICAL DEVICE CHARACTERISTICS

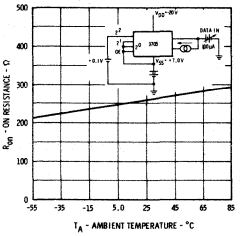
ON RESISTANCE VERSUS DATA INPUT VOLTAGE (3705 142 ONLY)



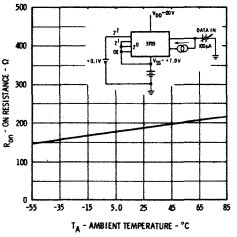
ON RESISTANCE VERSUS DATA INPUT VOLTAGE (3705 143 ONLY)



ON RESISTANCE VERSUS AMBIENT TEMPERATURE (3705 142 ONLY)



ON RESISTANCE VERSUS AMBIENT TEMPERATURE (3705 143 ONLY)



OUTPUT LEAKAGE CURRENT VERSUS AMBIENT TEMPERATURE

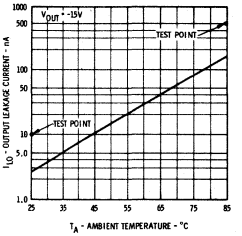
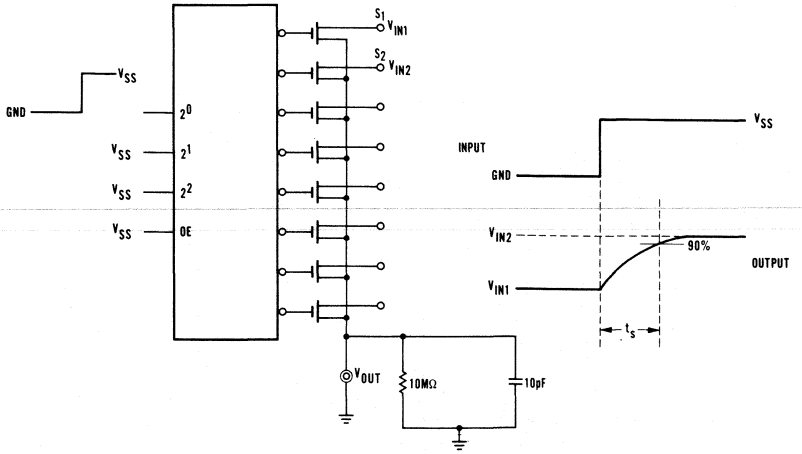
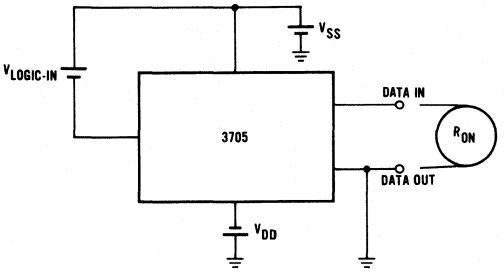


FIG. 1

SWITCHING TIME TEST CIRCUIT



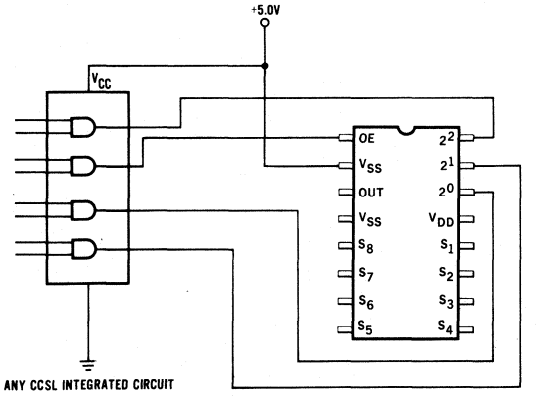


Voltage levels between semiconductor electrodes are normally referenced to one of the electrodes. In MOS, this electrode is the substrate (body or V_{SS}). The voltages can be translated to an equivalent level and referenced to another electrode. In order to measure the 'ON' resistance of the data channel accurately, the data output is at ground potential and all other terminals are changed correspondingly to test worst case conditions.

The following sets of bias conditions are equivalent:

	CONDITION 1	CONDITION 2
DATA IN	+5.0 V	0 V
V_{SS}	+7.0 V	+2.0 V
V_{DD}	−20 V	−25 V
LOGIC IN		
"Low" Level	+0.2 V	−4.8 V
"High" Level	+5.5 V	+0.5 V

TYPICAL CONTROL CIRCUIT



3708

SGOS MONOLITHIC 8-CHANNEL MULTIPLEX SWITCH

SILICON-GATE OXIDE SEMICONDUCTOR INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 3708 is an eight-channel multiplex switch with output enable control and one-out-of-eight decoder included on the chip. It is a monolithic integrated circuit utilizing Planar* II, P-channel enhancement mode silicon gate technology. The logic input lines of the 3708 are NPN bipolar compatible and can be used directly with CCSL 5.0 volt logic levels with no level-shifting interface required. This device is intended for use in A/D converters, multiplexing in analog or digital data transmission systems, and other airborne or ground instrumentation signal routing applications.

FEATURES

- **CCSL COMPATIBLE INPUT LOGIC LEVELS**
- **ONE-OUT-OF-EIGHT DECODER ON THE CHIP**
- **HIGH ON/OFF RATIO**
- **OUTPUT ENABLE CONTROL**
- **PLANAR II STABILITY**
- **INPUT GATE PROTECTION**
- **LOW LEAKAGE CURRENT**
- **ZERO OFFSET VOLTAGE**
- **FAST SWITCHING TIME 0.8 μs (TYP) AT $T_A = +85°C$**

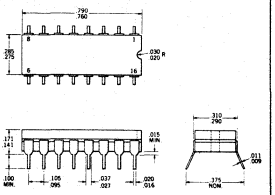
ABSOLUTE MAXIMUM RATINGS (Notes 1 and 2)

Storage Temperature	−65°C to +150°C
Operating Temperature	−55°C to +85°C
Positive Voltage on any pin	+0.3 V
Negative Voltage on digital and analog input pins	−30 V
and analog output pins	−30 V
Negative Voltage on V_{DD} pin	−30 V
Total power dissipation in package ($T_A = 25°C$)	200 mW

ORDERING INFORMATION — The 3708 is available for use in two signal ranges

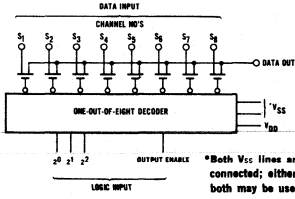
−5.0 to +5.0 volts signal applications, Order A6J3708142
0 to +5.0 volts signal applications, Order A6J3708143

PHYSICAL DIMENSIONS
16 Lead Dual In-Line



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" misalignment to facilitate insertion.
Board-drilling dimensions should equal your practice for .020 inch diameter lead.
Leads are gold-plated Kovar.
Package weight is 0.9 gram.

SYMBOLIC DIAGRAM
(MIL STD 806B)

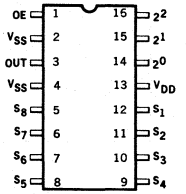


*Both V_{SS} lines are internally connected; either one or both may be used.

CCSL TRUTH TABLE

LOGIC INPUTS				CHANNEL
2^0	2^1	2^2	OE	'ON'
L	L	L	H	S_1
H	L	L	H	S_2
L	H	L	H	S_3
H	H	L	H	S_4
L	L	H	H	S_5
H	L	H	H	S_6
L	H	H	H	S_7
H	H	H	H	S_8
X	X	X	L	OFF

PIN CONFIGURATION
(16 lead DIP)



TOP VIEW

NOTES:
(1) These ratings are limiting values above which the serviceability of the device may be impaired.
(2) Voltage ratings are all referenced to pins 2 and 4 (V_{SS}).

*Planar is a patented Fairchild process.

FAIRCHILD
SEMICONDUCTOR

FAIRCHILD FIELD EFFECT INTEGRATED CIRCUIT 3708

ELECTRICAL CHARACTERISTICS

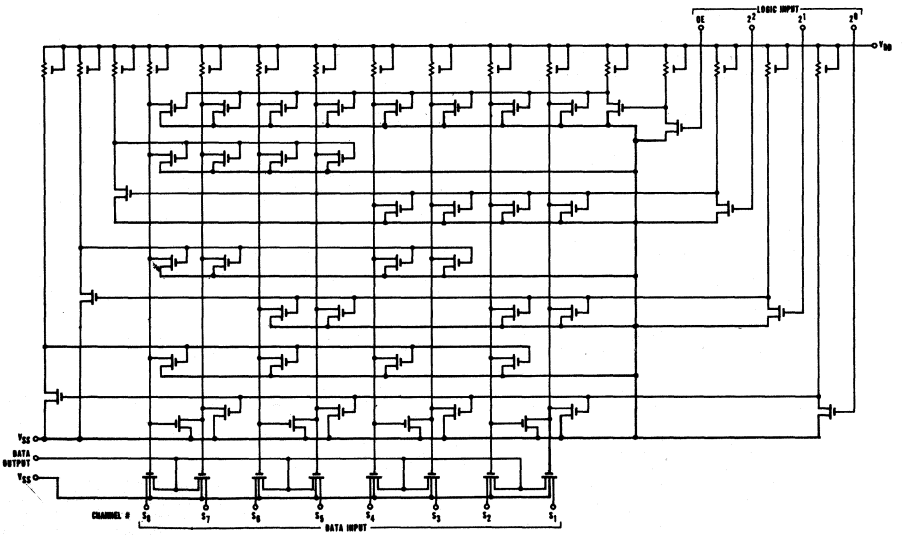
For 3708142: $-5.0\ V < V_{OUT} < +5.0\ V$, $T_A = 25°C$, $-18\ V < V_{DD} < -20\ V$, $5.0\ V < V_{SS} < 6.0\ V$ unless otherwise specified

For 3708143: $0\ V < V_{OUT} < +5.0\ V$, $T_A = 25°C$, $-18\ V < V_{DD} < -20\ V$, $5.0\ V < V_{SS} < 6.0\ V$ unless otherwise specified

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
R_{ON}	Data Channel "ON" Resistance					
	142		250	400	Ω	$V_{OUT} = -5.0\ V$, $I_{OUT} = -100\ \mu A$
	143		190	350	Ω	$V_{OUT} = 0\ V$, $I_{OUT} = -100\ \mu A$
R_{ON}	Data Channel "ON" Resistance		125		Ω	$V_{DD} = -20\ V$, $V_{SS} = +5.0\ V$, $I_{OUT} = -100\ \mu A$
R_{OFF}	Data Channel "OFF" Resistance	1.5	5.0		GΩ	$V_{SS} - V_{OUT} = 15\ V$
I_{LO}	Output Leakage Current		2.0	10	nA	$V_{SS} - V_{OUT} = 15\ V$
$I_{LO}(85°C)$	Output Leakage Current		100	500	nA	$V_{SS} - V_{OUT} = 15\ V$
I_{LDI}	Data Input Leakage Current					
	142			3.0	nA	$V_{SS} - V_{IN} = 15\ V$
	143			2.0	nA	$V_{SS} - V_{IN} = 10\ V$
I_{LI}	Logic Input Leakage Current			1.0	μA	$V_{SS} - V_{LOGIC\text{-}IN} = 15\ V$
*V_{IL}	Logic Gate Input "Low" Level	V_{DD}		+0.2	V	
*V_{IH}	Logic Gate Input "High" Level	$V_{SS} - 1.5$		V_{SS}	V	
t_S	Channel Switching Time (See Fig. 1)		0.45		μs	
$t_S(85°C)$	Channel Switching Time (See Fig. 1)		0.8	1.5	μs	
t_d	Channel Switching Time (See Fig. 1)		1.0	2.5	μs	
C_{db}	Output Capacitance		25		pF	$V_{SS} - V_{OUT} = 0\ V$, $f = 1.0\ MHz$
C_{is}	Data Input Capacitance		4.5		pF	$V_{SS} - V_{IN} = 0\ V$, $f = 1.0\ MHz$
C_{ig}	Logic Input Capacitance		3.0	175	pF	$V_{SS} - V_{LOGIC\text{-}IN} = 0\ V$, $f = 1.0\ MHz$
P_D	Power Dissipation		130		mW	$V_{DD} = -26\ V$, $V_{SS} = 0\ V$

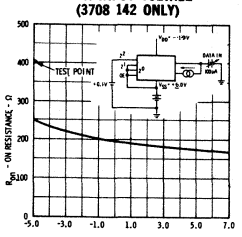
*When driven by CCSL elements, avoid excessive D.C. loading of CCSL elements to insure 3708 logic levels under maximum fan-out conditions. Analog input signal swing should not exceed V_{SS} (= V_{CC}).

SCHEMATIC DIAGRAM

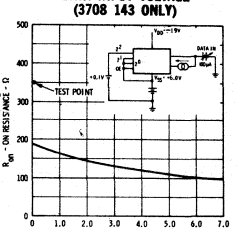


TYPICAL DEVICE CHARACTERISTICS

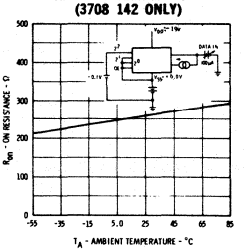
ON RESISTANCE VERSUS DATA INPUT VOLTAGE (3708 142 ONLY)



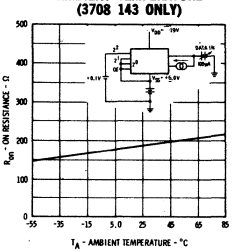
ON RESISTANCE VERSUS DATA INPUT VOLTAGE (3708 143 ONLY)



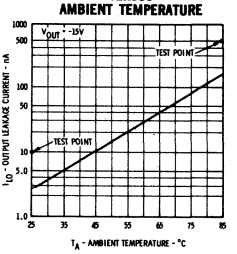
ON RESISTANCE VERSUS AMBIENT TEMPERATURE (3708 142 ONLY)



ON RESISTANCE VERSUS AMBIENT TEMPERATURE (3708 143 ONLY)



OUTPUT LEAKAGE CURRENT VERSUS AMBIENT TEMPERATURE



SWITCHING TIME VERSUS AMBIENT TEMPERATURE

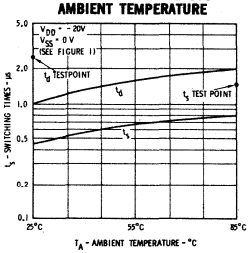
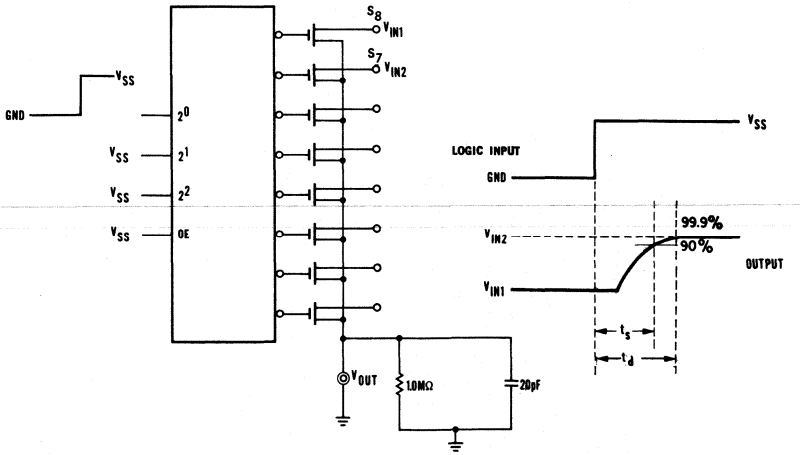
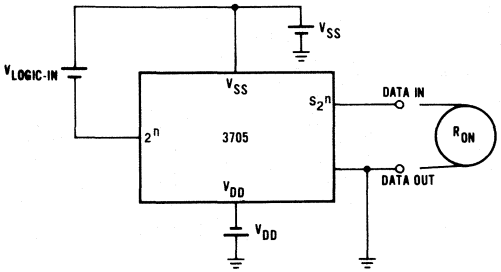


FIG. 1

SWITCHING TIME TEST CIRCUIT



FAIRCHILD FIELD EFFECT INTEGRATED CIRCUIT 3708

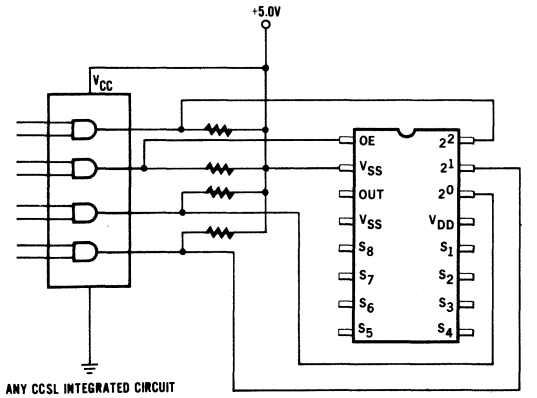


Voltage levels between semiconductor electrodes are normally referenced to one of the electrodes. In MOS, this electrode is the substrate (body or V_{SS}). The voltages can be translated to an equivalent level and referenced to another electrode. In order to measure the 'ON' resistance of the data channel accurately, the data output is at ground potential and all other terminals are changed correspondingly to test worst case conditions.

The following sets of power supplies are equivalent:

	CONDITION 1	CONDITION 2
DATA IN	+5.0 V	0 V
V_{SS}	+6.0 V	+1.0 V
V_{DD}	−18 V	−23 V
LOGIC IN		
"Low" Level	+0.2 V	−4.8 V
"High" Level	+5.5 V	+0.5 V

TYPICAL CONTROL CIRCUIT



3750
10-BIT D/A CONVERTER
MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 3750 is a monolithic MOS/LSI ten bit digital to analog converter using P-channel enhancement mode MOS technology. The digital word can be entered serially or in parallel. If desired, the word is available in serial form through an output buffer in either an 8 or 10 bit format. The converter output data is available thru 10 single pole double throw (SPDT) MOS switches. The holding register retains the state of the previous digital input word and drives the output switches. Transfer gates are used to isolate the holding register from the input register while new data is being entered. The 'on' resistance of the MOS switches is weighted to provide the necessary accuracy and stability for a ten bit conversion.

FEATURES

- **8 AND 10 BIT DATA LENGTHS**
- **SERIAL AND PARALLEL OPERATION**
- **250 kHz SERIAL BIT RATE**
- **500 kHz PARALLEL WORD RATE**
- **250 Ω TYPICAL 'ON' RESISTANCE OF TWO MSB's**
- **500 Ω TYPICAL 'ON' RESISTANCE OF REMAINING EIGHT BITS**
- **110 mW POWER DISSIPATION**
- **ZERO AND FULL SCALE CALIBRATION LOGIC**

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

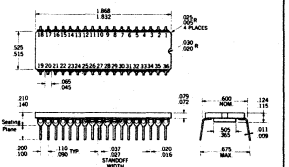
Input Voltages	−30 to +0.3 Volts
Power Supply	−29 Volts
Storage Temperature	−55°C to +150°C
Operation Temperature	−55°C to +85°C
	0°C to +70°C

APPLICATIONS

D/A Converters
- Telemetry
- Analog data plotters
- Industrial process control
- Servo systems

PHYSICAL DIMENSION

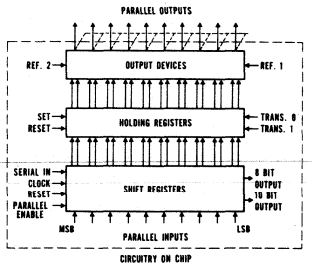
36 PIN
DUAL IN-LINE PACKAGE



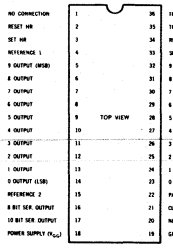
NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .600" centers. They are purposely shipped with "positive" misalignment to facilitate insertion
Leads are gold-plated kovar
Package weight is 6.0 grams

ORDER PART NO. A6H375014X (−55°C to +85°C)
A6H375019X (0°C to +70°C)

BLOCK DIAGRAM



PIN CONFIGURATION



FAIRCHILD
SEMICONDUCTOR

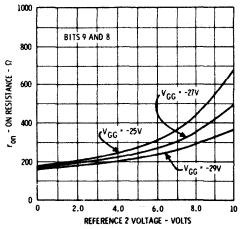
FAIRCHILD MOS INTEGRATED CIRCUIT 3750

ELECTRICAL CHARACTERISTICS $V_{GG} = -27 \pm 2.0$ Volts, $R_L = 10$ MΩ, $C_L = 10$ pF (unless otherwise specified)

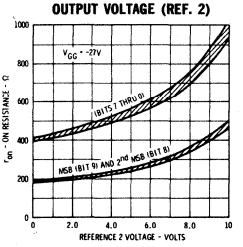
SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
	Logic Inputs					
	"0"	0		−2.0	Volts	
	"1"	−9.0		−30	Volts	
	Logic Outputs					
	"0"	0		−1.0	Volts	
	"1"	−10		−30	Volts	
	Clock					
	Amplitude	−9.0		−30	Volts	
	Width	1.0		10	μs	
f_{max}	Frequency					
	Serial	DC		250	kHz	
	Parallel	DC		500	kHz	
r_{on}	MOS Switches					
	"9"	150	250	500	ohms	$V_{REF} = -5.0$ V
	"8"	150	250	500	ohms	$V_{GG} = -27$ V
	"7" thru "0"	325	550	1000	ohms	
Δr_{on}	Switch Mismatch					
	"9"		70	150	ohms	$V_{REF_2} = -5.0$ V
	"8"		70	150	ohms	$V_{REF_1} = 0$ V
	"7" thru "0"		120	250	ohms	
t_{df}	Serial Delay,		0.6		μs	
t_f	rise and fall		0.2		μs	
t_{dr}	times		0.5		μs	
t_r			0.5		μs	
t_{df}	Parallel Delay,		0.55		μs	
t_f	rise and fall		0.35		μs	
t_{dr}	times		0.4		μs	
t_r			0.3		μs	
C_{in}	Data and Control Input Capacitance		7.0		pF	
I_{max}	Power Supply Current Drain		4.5	7.0	mA	$V_{GG} = -27$ V
P_{max}	Power Dissipation		120	190	mW	$V_{GG} = -27$ V
	Temperature Coefficient of Switches		0.3		%/°C	
	Temperature Coefficient Tracking		0.03		%/°C	
I_{LX}	Input Leakage Current			5.0	μA	$V_{in} = -20$ V
t_{dd}	Data Delay Time	250			ns	

TYPICAL ELECTRICAL CHARACTERISTICS

ON RESISTANCE VERSUS POWER SUPPLY VOLTAGE (V_{GG}) OUTPUT VOLTAGE (REF. 2)

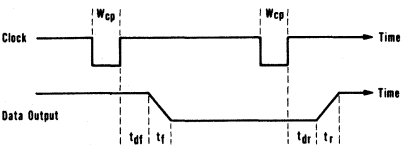


ON RESISTANCE VERSUS OUTPUT VOLTAGE (REF. 2)

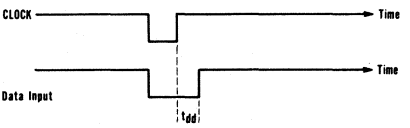


TIMING DIAGRAM

OUTPUT DELAY, RISE AND FALL TIMES



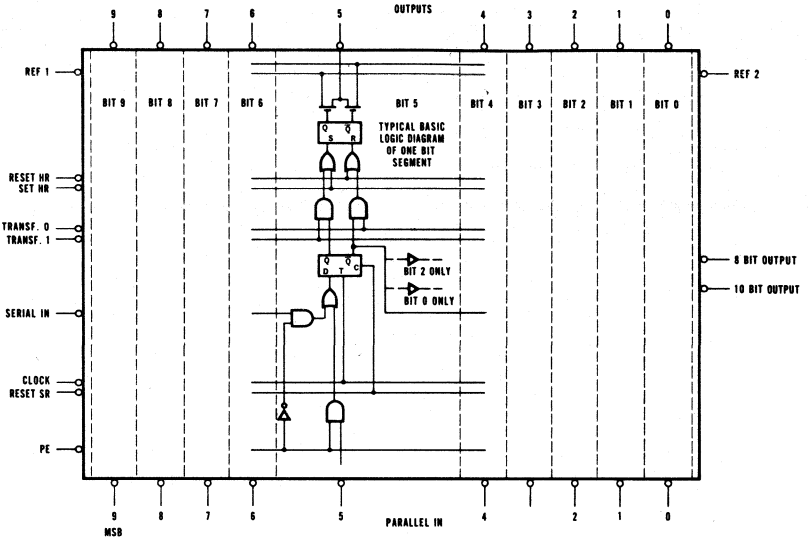
DATA BIT TIMING



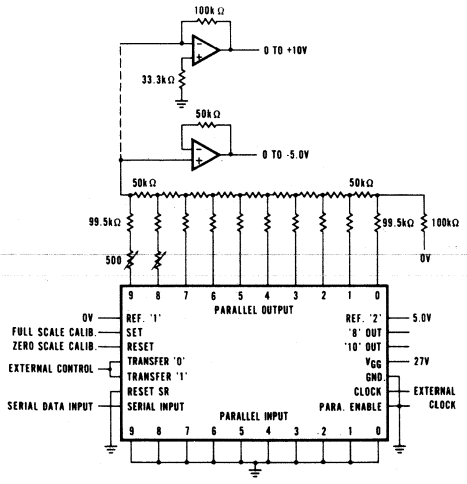
TIMING DIAGRAMS

FAIRCHILD MOS INTEGRATED CIRCUIT 3750

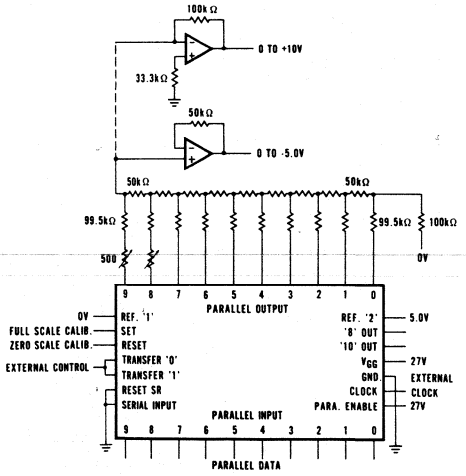
LOGIC DIAGRAM

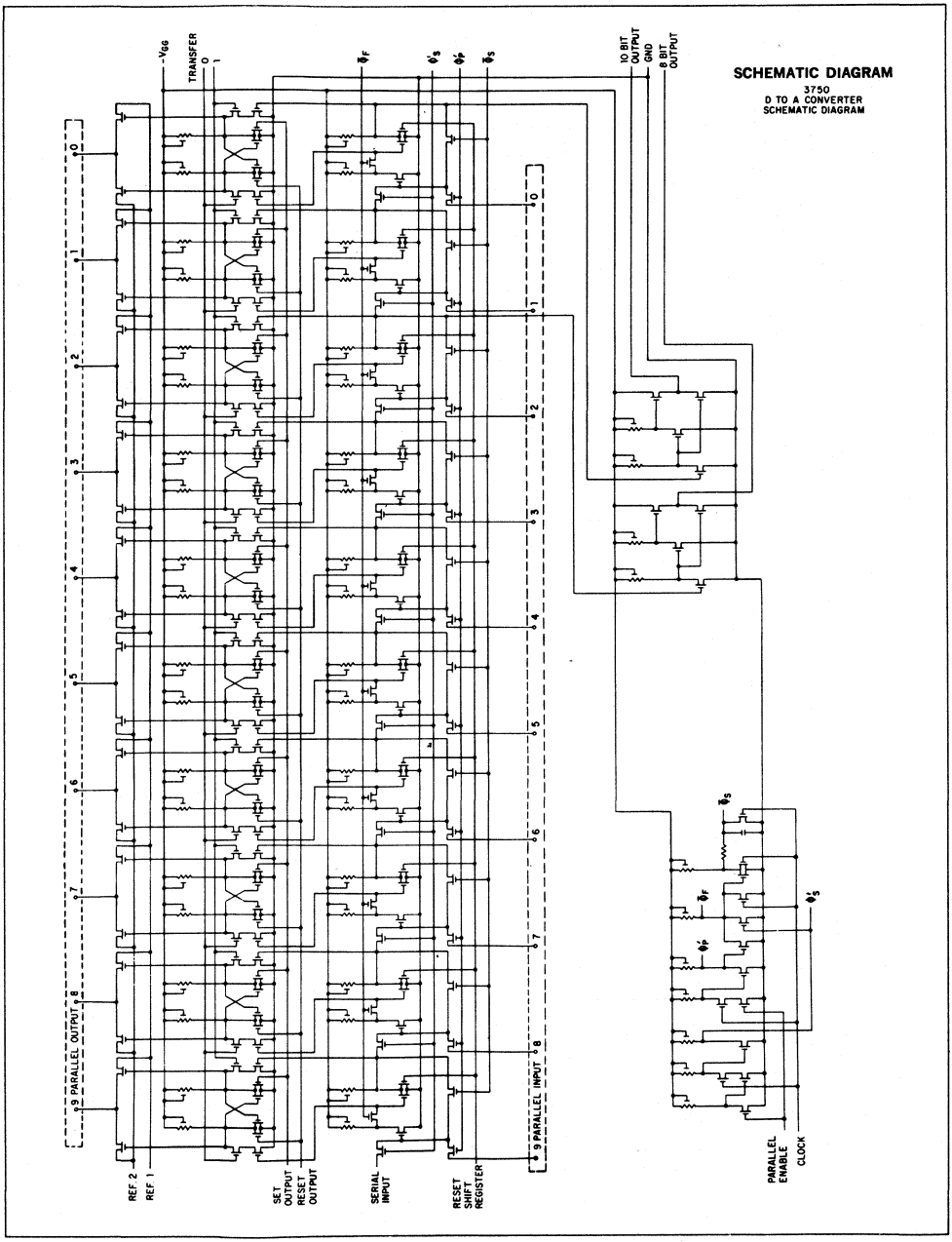


SERIAL OPERATION



PARALLEL OPERATION




SCHEMATIC DIAGRAM
3750
D TO A CONVERTER
SCHEMATIC DIAGRAM
-VGG
TRANSFER
0
1
10 BIT OUTPUT
GND
8 BIT OUTPUT
PARALLEL OUTPUT
PARALLEL INPUT
REF. 2
REF. 1
SET OUTPUT
RESET OUTPUT
SERIAL INPUT
RESET SHIFT REGISTER
PARALLEL ENABLE
CLOCK

3751
12-BIT A/D CONVERTER
MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 3751 is a twelve bit analog to digital converter using P channel enhancement mode MOS/LSI technology. The conversion is accomplished by the successive approximation technique. The word length is variable for eight, nine, ten or twelve bits by applying a DC potential to each of two control pins. The 3751 provides all the A/D system control functions such as: master timing, automatic start and recycle, and RZ or NRZ format control. By choosing the appropriate ladder network, the output will be in either a binary or binary coded decimal digital format.

FEATURES

- **8, 9, 10, OR 12 BIT WORD LENGTH**
- **RZ OR NRZ DIGITAL FORMAT**
- **COMPLETE LOGIC AND SYSTEM TIMING CIRCUITS INCLUDED ON THE CHIP**
- **BCD OVERVOLTAGE FLAG**
- **200 Ω TYPICAL "ON" RESISTANCE FOR THE TWO MSB**
- **500 Ω TYPICAL "ON" RESISTANCE FOR THE REMAINING TEN SWITCHES**
- **150 mW POWER DISSIPATION**
- **AUTOMATIC RESTART CIRCUITS**

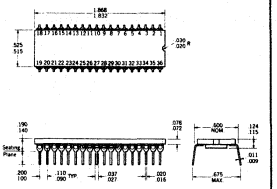
ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Input Voltages	−30 to +0.3 Volts
Power Supply	−30 Volts
Storage Temperature	−55°C to +150°C
Operation Temperature	−55°C to +85°C

APPLICATIONS

A/D Converters
Three Digit DVM's
Telemetry
Industrial Control
Computer Interface

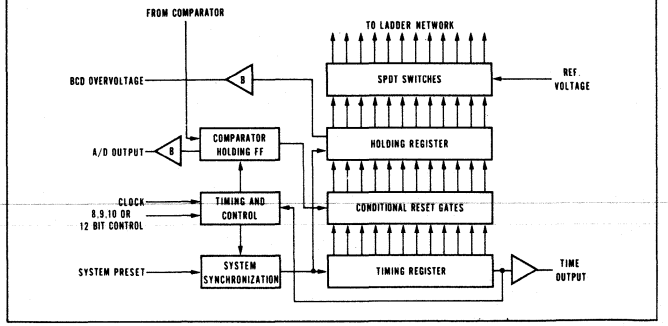
PHYSICAL DIMENSIONS
36 PIN
DUAL IN-LINE PACKAGE



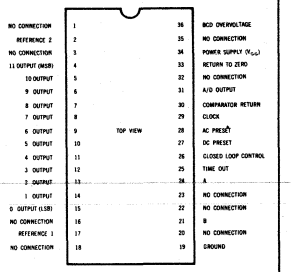
NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .600" centers. They are purposely shipped with "positive" misalignment to facilitate insertion
Leads are gold-plated Kovar
Package weight is 6.0 grams

ORDER PART NO. A6H375114X

BLOCK DIAGRAM



PIN CONFIGURATION



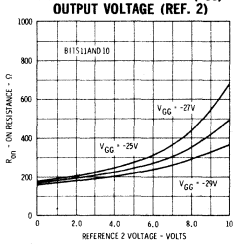
FAIRCHILD
SEMICONDUCTOR

ELECTRICAL CHARACTERISTICS ($V_{GG} = -27 \pm 2.0$ Volts, $R_L = 10$ MΩ, $C_L = 10$ pF unless otherwise specified)

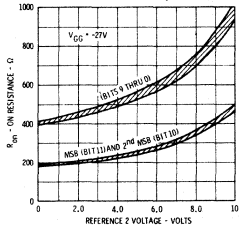
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
	Logic Inputs					
	"0"	0		−2.0	Volts	
	"1"	−9.0		−30	Volts	
	Logic Outputs					
	"0"	0		−1.0	Volts	
	"1"	−10		−30	Volts	
W_{cp}	Clock					
	Amplitude	−9.0		−30	Volts	
	Width	1.0		10	μs	
f_{max}	Bit Frequency	DC		250	kHz	
R_{ON}	MOS Switches					
	"11"	150	250	500	Ω	
	"10"	150	250	500	Ω	
	"9" thru "0"	325	550	1000	Ω	
ΔR_{ON}	Switch Mismatch					
	"11"		70	150	Ω	
	"10"		70	150	Ω	
	"9" thru "0"		120	250	Ω	
C_{IN}	Data and Control Input Capacitance		7.0		pF	
I_{max}	Power Supply Current Drain		4.5	7.0	mA	$V_{GG} = -27$ V
P_{max}	Power Dissipation		120	190	mW	$V_{GG} = -27$ V
	Temperature Coefficient of Switches		0.3		%/°C	
	Temperature Coefficient of Tracking		0.03		%/°C	
I_{LX}	Input Leakage Current			5.0	μA	$V_{IN} = -20$ V
	Analog Switch Delay,					
t_{df}	rise and fall times		0.7		μs	
t_f	(10% to 90% points)		0.5		μs	$V_{GG} = -27$ V
t_{dr}			1.1		μs	
t_r			0.25		μs	

TYPICAL ELECTRICAL CHARACTERISTICS

ON RESISTANCE VERSUS POWER SUPPLY VOLTAGE (V_{GG}) OUTPUT VOLTAGE (REF. 2)

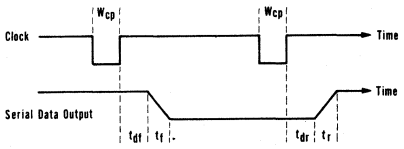


ON RESISTANCE VERSUS OUTPUT VOLTAGE (REF. 2)



TIMING DIAGRAM

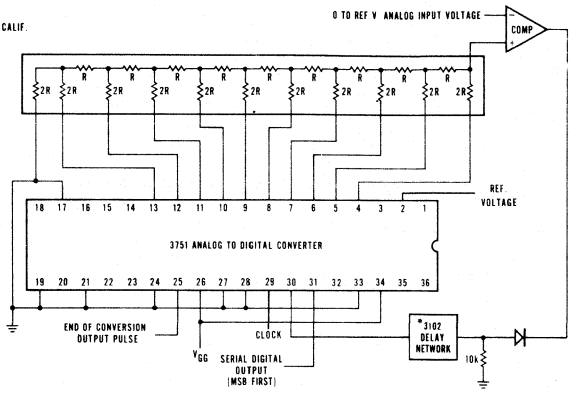
OUTPUT DELAY, RISE AND FALL TIMES



TEN BIT A/D CONVERTER

NO. OF BITS	R VALUE
8	12.5k
9	25k
10	50k
12	200k

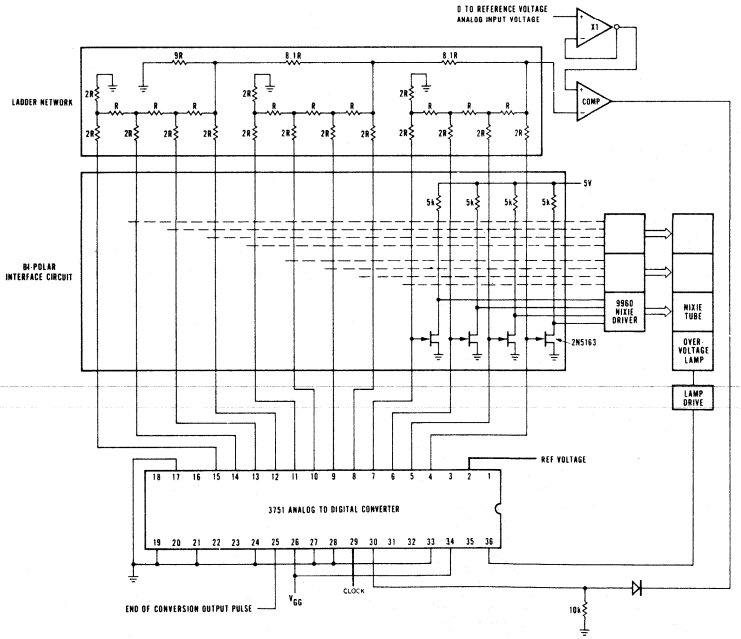
LADDER NETWORK MFGR'S
NEGADYNE CORP., ROCHESTER, N.Y.
ANGSTROM PRECISION INC., VAN NUYS, CALIF.



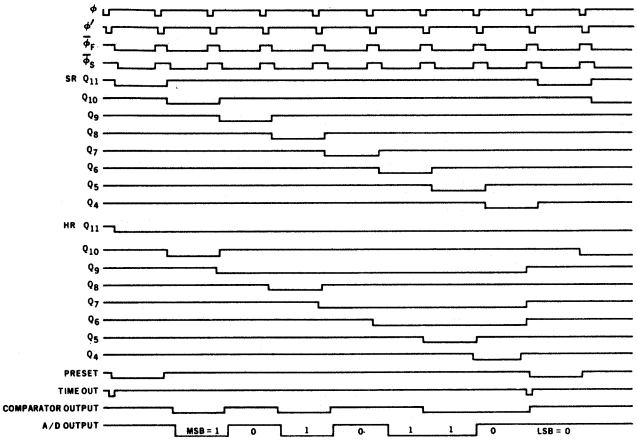
When the serial digital output is used, a delay network is required between the comparator output and the converter as shown. This is to inhibit any change of the comparator return signal at the input of the converter during a clock pulse.

*Dual 3102 as Type D Flip-Flop

THREE DIGIT BCD A/D CONVERTER



TYPICAL TIMING DIAGRAM



8 BIT FORMAT
ANALOG INPUT = −3.369 V = 10101100
REFERENCE VOLTAGE = −5.000 V
FIGURE 3

DESCRIPTION OF PIN FUNCTION

PIN NO.

24, 21 — A, B: These two pins are connected as shown in the truth table below to control the length of the digital word.

	8	9	10	12
A	1	0	1	0
B	1	1	0	0

25 — TIME OUT: A synchronous pulse with the clock is applied at this output at the end of each conversion. This pulse may be used to step a multiplexer or otherwise notify the system of the readiness of the A/D to start another conversion.

26 — CLOSED LOOP CONTROL: A '1' voltage level continuously applied to this input will put the A/D in an automatic mode of operation. The time output pulse is internally gated to cause a preset at the end of each conversion and initiate a new conversion. The automatic start circuitry presets the circuit and restarts the conversion if a bit has been dropped in this mode of operation.

27 — D.C. PRESET: A '1' voltage level applied to this input will cause an immediate preset and the unit will stay preset until this input is returned to a '0' voltage level.

28 — A.C. PRESET: When a '1' level is applied to this input, the A/D is preset on the next clock pulse. The unit will continue to be preset on each clock pulse until the '1' level is removed from the input.

31 — A/D OUTPUT: The serial digital conversion is available at this pin in a most significant bit (MSB) first format. The data output is delayed by one bit time.

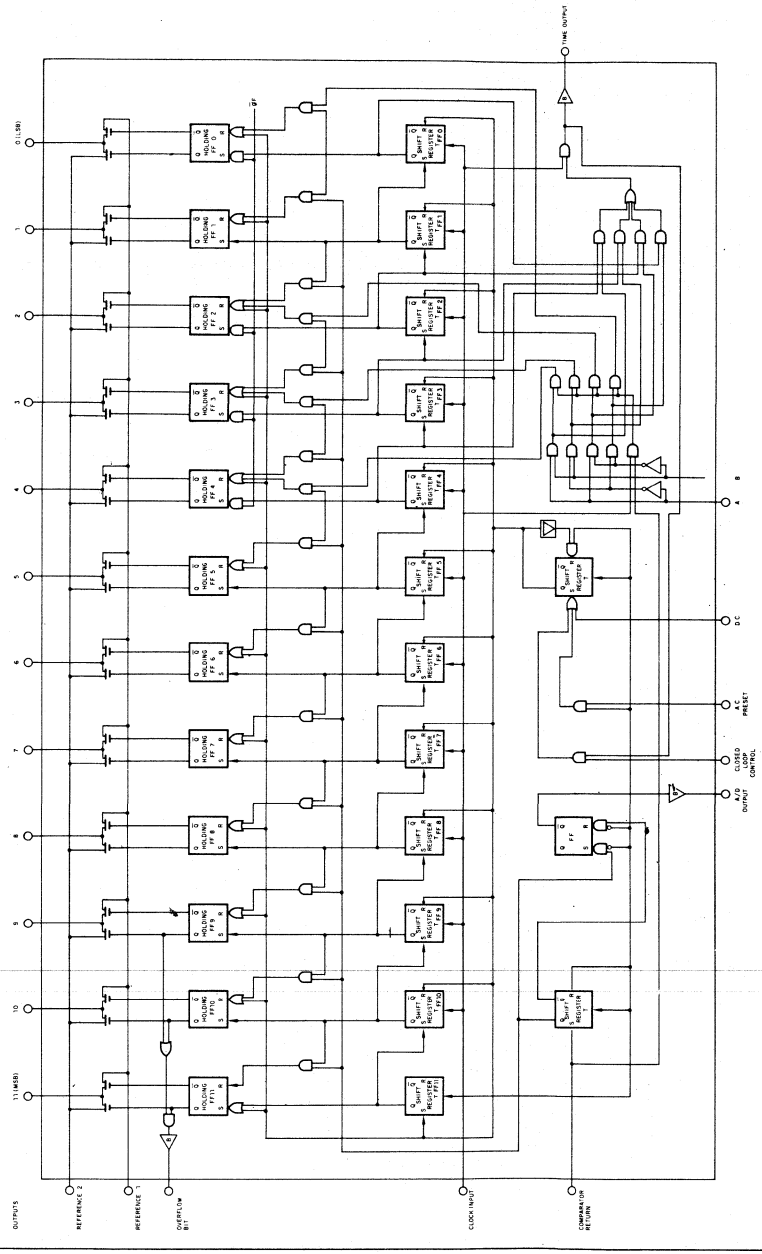
36 — BCD OVERVOLTAGE: This output is used when a three digit analog to binary coded decimal (BCD) conversion is being made. If the binary equivalent of the most significant digit is greater than 9, a '1' voltage level is applied on this output.

33 — RETURN-TO-ZERO: This input modifies the digital code format from non-return-to-zero (NRZ) to return-to-zero (RZ) if used. When tied to the clock line, the digital output will return to zero during each clock pulse. The RZ duty cycle can be varied by controlling the length of time that a '1' level is applied to this input.

30 — COMPARATOR RETURN: The comparator output should be connected to this input. The input must be prevented from going positive with respect to substrate (ground). The output SPDT MOS switches are successively toggled to the reference voltage. This input will cause these switches to be conditionally reset if the ladder network output voltage is greater than the signal voltage.

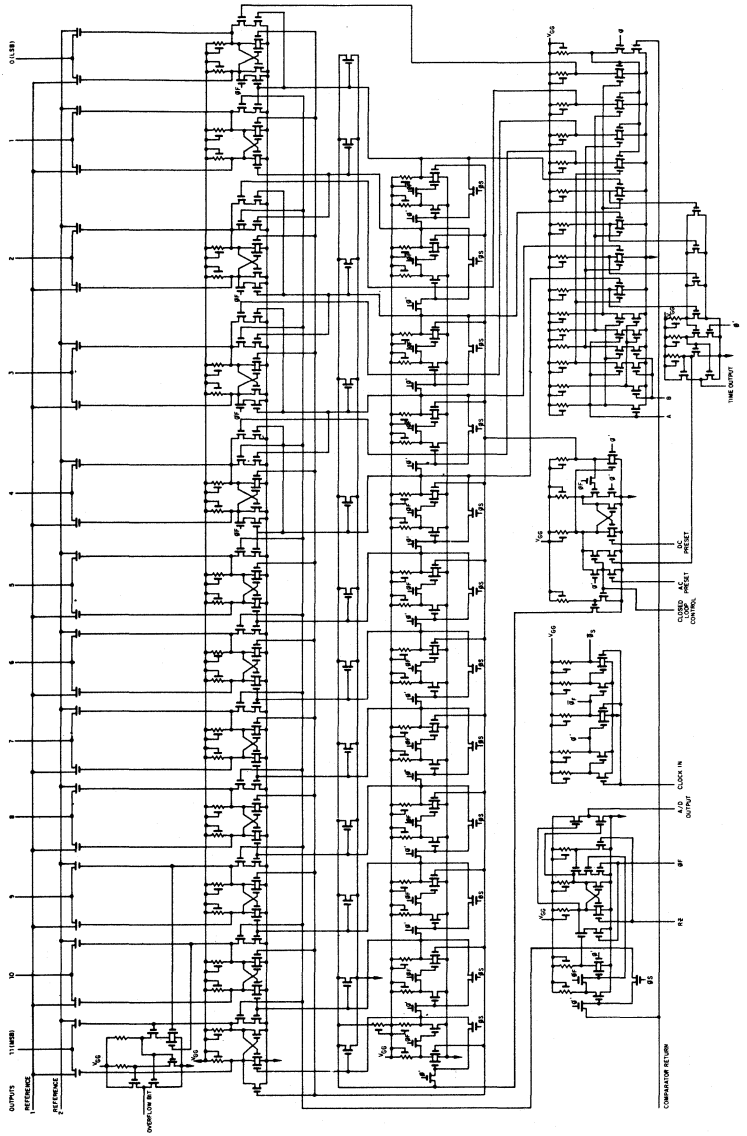
2, 17 — REFERENCES 1 & 2: Reference 1 is normally connected to ground and reference 2 to −5.0 volts. However, they may each be connected anywhere between 0 and −5.0 volts D.C. for special applications.

LOGIC BLOCK DIAGRAM



NOTE: Polarity indicators (0) external to the solid box conform to MIL-STD-806B where 0 indicates the less positive state is active. Internal to the box and in the remainder of this data sheet conventional MOS polarities are used, where HI = "1" ≈ −10 V and LO = "0" ≈ Gnd.

SCHEMATIC DIAGRAM



3800
8-BIT PARALLEL ACCUMULATOR
MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 3800 is a LSI-MOS integrated circuit containing approximately 200 gates. It functions as an eight bit slice of an arithmetic unit, which may be connected to form any word length. It is capable of parallel addition and subtraction, and by simultaneously shifting the sum or difference right or left, multiplication and division algorithms. A direct subtraction capability eliminates the need for the usual carry input to the LSB during subtraction, thus allowing operands to be located anywhere in the truly variable word length accumulator. The parallel data organization of the 3800 improves speed and greatly reduces the amount of random control logic when compared to the same function performed serially.

FEATURES

- **DIRECT SUBTRACTION USED TO PROVIDE VARIABLE WORD LENGTH CAPABILITY**
- **STROBED OUTPUTS FOR HARD WIRE COMMON BUS SYSTEMS**
- **DC TO 200 kHz ADD AND SHIFT RATE**
- **3.0 μs, 8 STAGE CARRY PROPAGATION TIME**
- **LOW POWER — 180 mW**

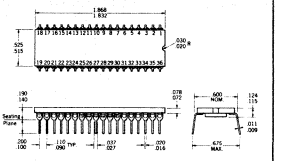
APPLICATIONS

Basic Accumulator Block
Index Register
>, =, < Comparator
General Logic Control
Up-Down Counter
Divide By N Counter

ABSOLUTE MAXIMUM RATINGS

Input Voltages	−30 V to +0.3 V
V_{GG} and V_{DD} Supply Lines	−30 V to +0.3 V
Storage Temperature	−55°C to +150°C
Operating Temperature	−55°C to +85°C

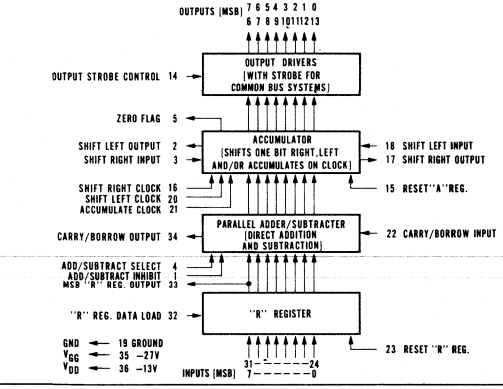
PHYSICAL DIMENSIONS
36-Pin
Dual In-Line Package



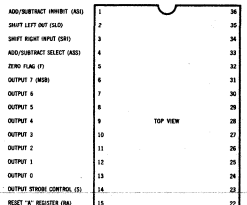
NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .600" centers. They are purposely shipped with "positive" misalignment to facilitate insertion
Leads are gold-plated kovar
Package weight is 6.0 grams

ORDER PART NO. A6H380014X (−55°C to +85°C)
A6H380019X (0°C to 70°C)

BLOCK DIAGRAM



PIN CONFIGURATION



FAIRCHILD
SEMICONDUCTOR

FAIRCHILD MOS INTEGRATED CIRCUIT 3800

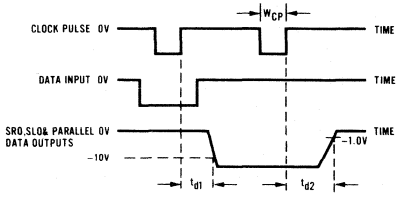
ELECTRICAL CHARACTERISTICS $V_{GG} = -27\ V \pm 1\ V$, $V_{DD} = -13\ V \pm 1\ V$, $R_L = 10\ M\Omega$, $C_L = 10\ pF$ (unless otherwise specified)

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
	Logic inputs					
	Logic "0"	0		−2.0	Volts	$V_{GG} = -27\ V$
	Logic "1"	−10		−30	Volts	$V_{GG} = -27\ V$
	Clocks					
	Amplitude	−10		−30	Volts	
	Width	1.0		10	μs	
	Shift frequency	DC		300	kHz	
	Shift & add frequency	DC		200	kHz	
	Delay Times					
t_{CB}	8 stage carry		3.0	5.0	μs	See Figure 1
t_{d1} & t_{d2}	Output delay		1.0	3.0	μs	See Figure 1
I_{LX}	Input leakage current			5.0	μA	$V_{IN} = -20\ V$
	Logic outputs					
	Logic "0"	0	−0.5	−1.0	Volts	
	Logic "1"	−11	−12		Volts	
	Logic "1"	−10	−11		Volts	$R_L = 40\ k\Omega$
	Supply current drain					
	V_{DD}			7.0	mA	$V_{GG} = -27\ V$, $V_{DD} = -13\ V$
	V_{GG}			5.0	mA	$V_{GG} = -27\ V$, $V_{DD} = -13\ V$
	Network dissipation		180		mW	

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	FUNCTION
1	Add/subtract inhibit	ASI	When ASI is a logic "1", no addition or subtraction will occur when the ACC, SRC or SLC clock are pulsed. The accumulator register will shift right or left normally however. The carry/borrow through line is not affected, allowing numbers to be shifted and compared when the subtract mode is selected.
2	Shift left output	SLO	SLO is the MSB output of the ACC and may be connected directly to the SLI input of the next eight bit section of the accumulator. Shift and add function normally.
3	Shift right input	SRI	SRI accepts the SRO output of a higher order, 8 bit slice. Shift and add function normally.
4	Add/Subtract select	ASS	When ASS is a logic "1", addition is performed, and when ASS is a logic "0", subtraction is performed.
5	Zero flag	F	The zero flag output is a logic "1" only if the accumulator register contains all zeros. This output is independent of the strobe control.
6-13	Outputs	7-0	When the strobe control STR is a logic "0", all outputs represent the contents of the accumulator register.
14	Output strobe control	STR	When STR is a logic "1", all parallel outputs, 0-7, are disconnected from the power and ground lines allowing them to float. Thus several similar outputs may be hard wired together for a common buss system.
15	Reset Accum. register	RA	When RA = logic "1", the accumulator is reset to zero. This asynchronous signal overrides all others.
16	Shift right clock	SRC	Pulsing the SRC with a logic "1" shifts the contents of the accumulator one bit position to the right. If the add/subtract controls are enabled, the sum or difference of the accumulator register and the "R" register is shifted one bit to the right and written into the accumulator.
17	Shift right output	SRO	SRO is the LSB end of the 8 bit accumulator and may be connected directly to the SRI of an adjacent 8 bit slice.
18	Shift left input	SLI	The SLI accepts the SLO output from a lower order, 8 bit slice.
19	Ground	GND	Circuit common and substrate ground are both connected to this pin.
20	Shift left clock	SLC	Pulsing the SLC with a logic "1" shifts the contents of the accumulator one bit position to the left. If the add/subtract controls are enabled, the sum or difference of the accumulator and the "R" register is shifted one bit to the right and written into the accumulator.
21	Accumulate clock	AC	Pulsing the AC input adds the contents of the accumulator and the "R" register if ASS = logic "1". The "R" register is subtracted from the accumulator if ASS = "0". If ASI = "1", no action occurs.
22	Carry/borrow input	CBI	A logic "1" on CBI enters a carry or borrow into the LSB position of the add/subtract logic.
23	Reset "R" register	RR	Placing a logic "1" on RR asynchronously resets the "R" register.
24-31	Inputs	0-7	Inputs are entered into the "R" register asynchronously when RL is activated.
32	"R" register data load	RL	When RL is a logic "1", data presented at the inputs are loaded into the "R" register. RL may be permanently a logic "1", effectively bypassing the R register during normal operation. Note that RR overrides the data inputs regardless of the load command.
33	MSB "R" register output	MSB	It shows the MSB of the "R" register. When the "R" register is used to temporarily hold operands during multiply, divide, etc., the MSB output indicates the sign of the stored operand.
34	Carry/borrow output	CBO	The CBO is the asynchronous carry or borrow output from the MSB of the add/subtract logic. It is not affected by the ASI control.
35	V_{GG} power supply	V_{GG}	−27 V supply.
36	V_{DD} power supply	V_{DD}	−13 V supply.

SHIFT COMMAND TIMING DIAGRAM



CARRY/BORROW 8 STAGE PROPAGATION TIME

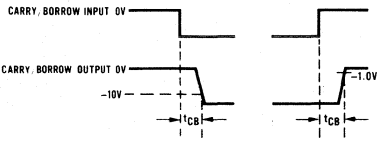
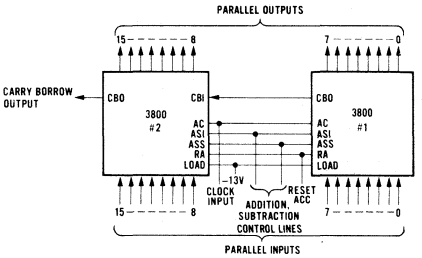


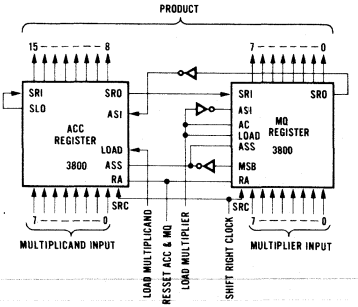
FIGURE 1

STANDARD CONNECTIONS FOR ADDITION AND SUBTRACTION



SIXTEEN BIT PARALLEL ADDITION (SUBTRACTION)*: The addition (subtraction) operation begins by resetting the accumulator, then transferring the augend (subtrahend) through the "R" register into the accumulator by pulsing the AC clock line. The operation is completed by loading the addend (minuend) into or through the "R" register, then adding (or subtracting if ASS = logic "0") it from the accumulator by again pulsing the AC clock. Multiple addition and subtraction or combinations of both operations may be performed by repeating the last operation. Thus a running total may be kept in the accumulator.

STANDARD CONNECTIONS FOR MULTIPLICATION

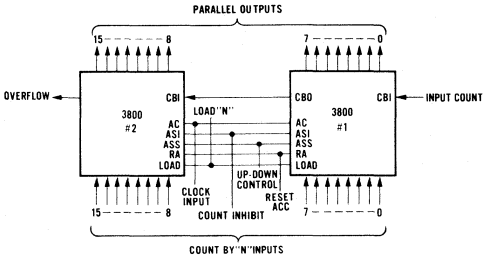


MULTIPLICATION: The multiplication operation, shown above, begins by clearing the ACC and MQ registers, then loading the multiplier into the MQ "R" register. If the MSB of the MQ's "R" register is a "1", ie. the multiplier is negative, the ACC and MQ subtract lines are enabled before the multiplier is transferred into the MQ. Thus the multiplier in the MQ is always positive. However, the multiplicand, which has been loaded into the ACC "R" register for temporary storage, will be subtracted from the partial product in the ACC if the multiplier was negative. The multiplicand is added to or subtracted from the partial product and shifted one bit to the right each time the LSB of the MQ register is a "1". If it is a "0", only a shift right occurs. Neither the multiplicand nor the resulting product require any further sign corrections as the answers will automatically be in two's complement.

DIVISION: The division algorithm is similar to the multiply and is described in detail in The Logic of Computer Arithmetic by Flores. The most straightforward way to perform division is to convert both the divisor and dividend to sign magnitude numbers the same way the multiplier was converted in multiplication. Then proceed through a successive subtraction division. The resulting positive quotient must however then be corrected to two's complement rotation if the signs of the dividend and the divisor were not the same.

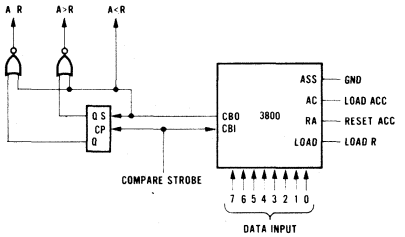
NOTES: 1. Input logic levels may be selected by referring to the list of Pin Function Descriptions.
2. All unused input or control pins should be grounded.
3. All operands are in two's complement notation.
4. All diagrams are BASIC BLOCK DIAGRAMS and no electrical levels are indicated. See Logic Diagram for correct 806B notation.

APPLICATIONS



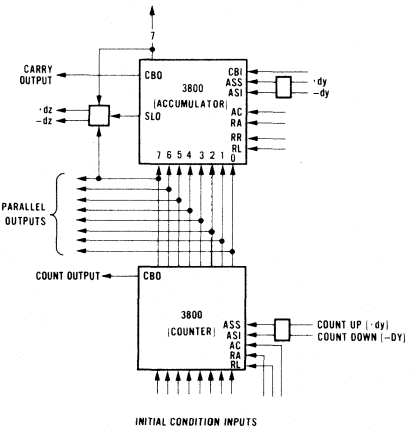
UP-DOWN COUNTER

SIXTEEN STAGE UP-DOWN COUNTER: Operation begins by resetting the registers and enabling ASS, which determines the count direction. Counting by one may be accomplished by enabling CBI or INPUT "0". To count by n, set n into the "R" register.



L, = > COMPARATOR

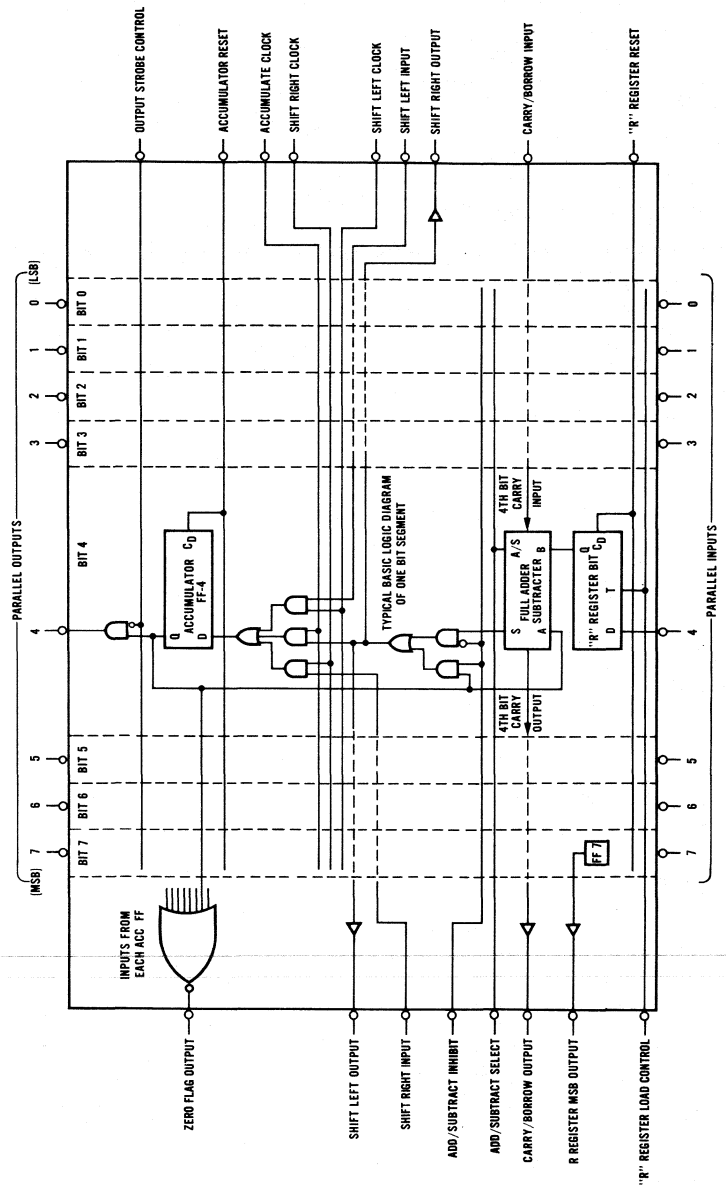
COMPARE OPERATION: To compare two numbers, simply insert the first into a previously cleared accumulator by pulsing AC. Enabling the subtract control will immediately indicate whether R>A, as a borrow output will appear. If the borrow output follows a pulse on the borrow input, the numbers are equal. If neither, then R<A. The logic is shown above.



DDA CONNECTIONS

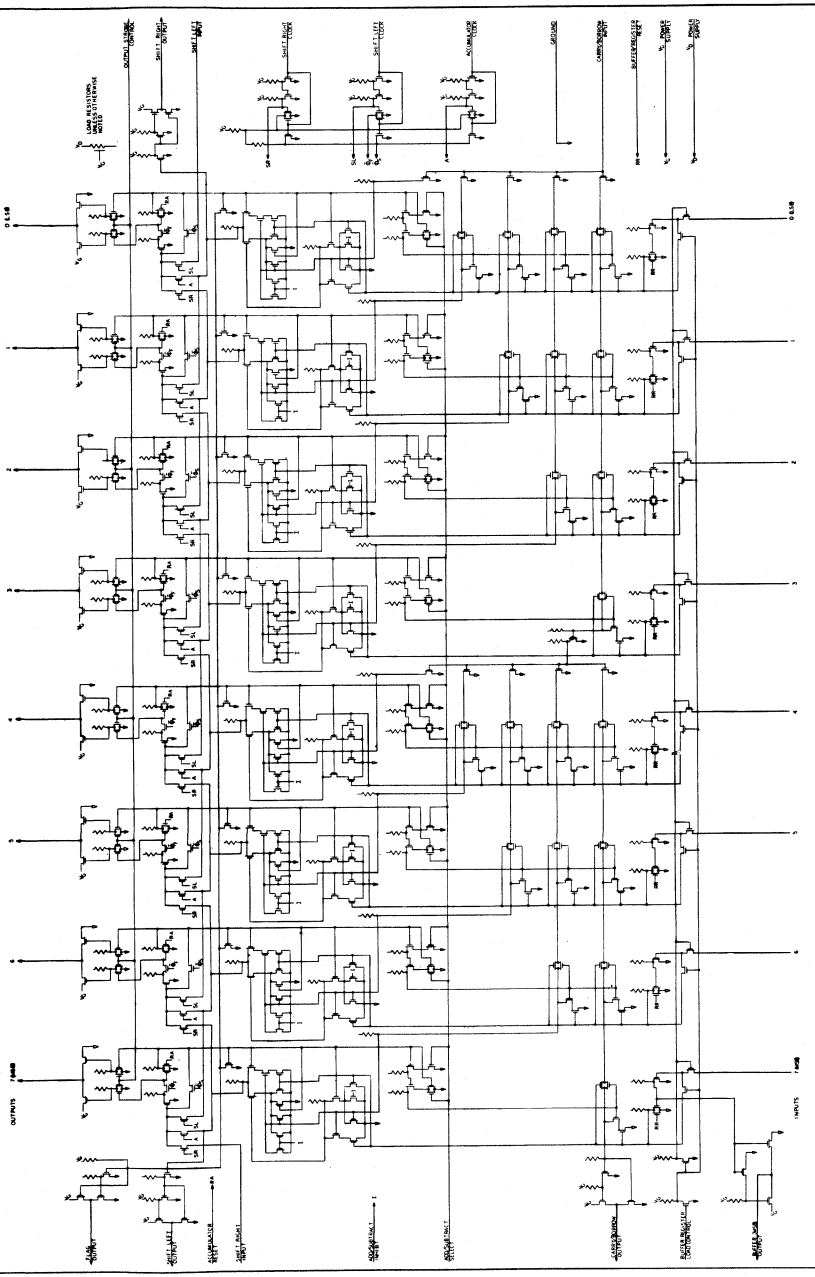
The DDA shown above utilizes one 3800 for a remainder register and a second 3800 for a y accumulator counter.

LOGIC BLOCK DIAGRAM



NOTE: Polarity indicators (0) external to the solid box conform to MIL-STD-806B where 0 indicates the less positive state is active. Internal to the box and in the remainder of this data sheet conventional MOS polarities are used, where HI = "1" ≈ −10 V and LO = "0" ≈ Gnd.

SCHEMATIC DIAGRAM



3801

10-BIT SERIAL/PARALLEL-PARALLEL/SERIAL CONVERTER

MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 3801 is a monolithic MOS/LSI ten bit serial/parallel - parallel/serial converter utilizing P-Channel Enhancement mode MOS technology. The device has the capability of serial or parallel input and serial or parallel output. A holding register included on the chip is isolated from the shift register by transfer gates. In serial to parallel applications data may be stored in the holding register while new data is being entered into the shift register.

FEATURES

- **8 AND 10 BIT SERIAL OUTPUT**
- **250 kHz SERIAL TO PARALLEL OPERATION**
- **500 kHz PARALLEL TO PARALLEL OPERATION**
- **120 mW POWER DISSIPATION**
- **INPUT GATE PROTECTION**
- **SET AND RESET OF HOLDING REGISTER**
- **OUTPUT STROBE CONTROL**
- **SINGLE PHASE CLOCK**
- **RESET OF SERIAL REGISTER**

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

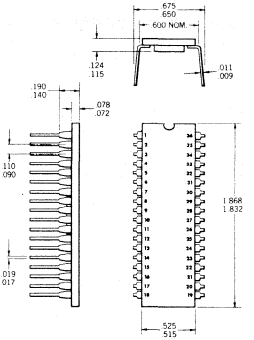
Input Voltages	−30 to +0.3 Volts
Power Supply	−30 Volts
Storage Temperature	−55°C to +150°C
Operation Temperature (A6H380114X)	−55°C to +85°C
(A6H380119X)	0°C to +70°C

APPLICATIONS

Serial and Parallel Data Conversion in

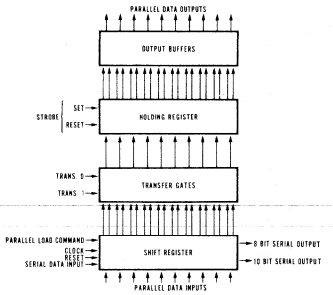
- Process Control
- Data Terminals
- Computer Peripheral Equipment
- Data Acquisition

PHYSICAL DIMENSION
36 PIN
DUAL IN-LINE PACKAGE

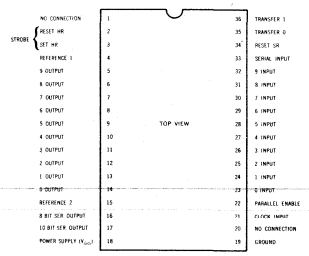


ORDER PART NO. A6H380114X
A6H380119X

BLOCK DIAGRAM



PIN CONFIGURATION



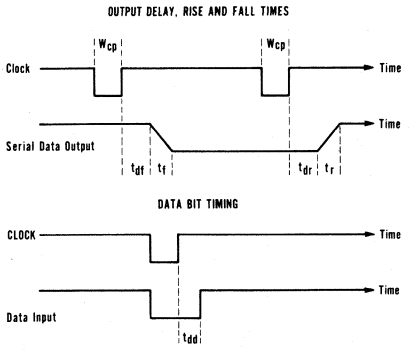
FAIRCHILD
SEMICONDUCTOR

FAIRCHILD MOS INTEGRATED CIRCUIT 3801

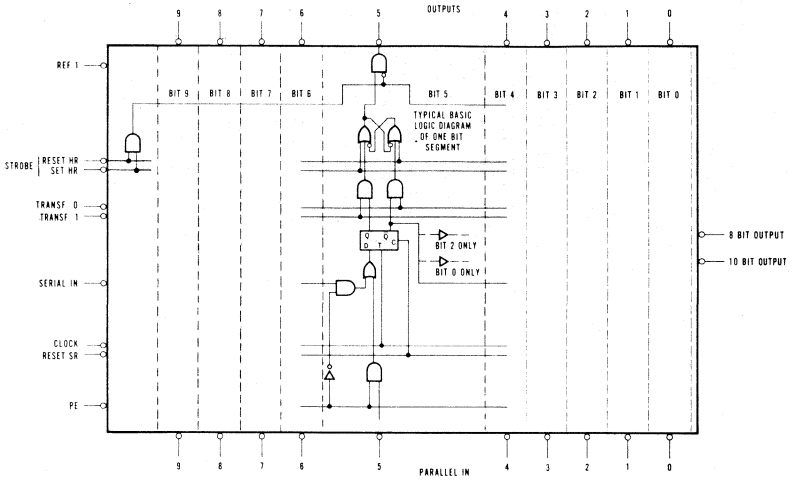
ELECTRICAL CHARACTERISTICS ($V_{GG} = -27 \pm 2.0$ Volts, $R_L = 10M\Omega$, $C_L = 10$ pF unless otherwise specified)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
	Logic Inputs					
	"0"	0		−2.0	Volts	
	"1"	−9.0		−30	Volts	
	Logic Outputs					
	"0"	0		−1.0	Volts	
	"1"	−10	−11		Volts	$R_L = 40$ kΩ
	"1"	−11	−12		Volts	
	Clock					
	Amplitude	−9.0		−30	Volts	
	Width	1.0		10	μs	
f_{max}	Frequency					
	Serial	DC		250	kHz	
	Parallel	DC		500	kHz	
t_{df}	Serial Delay,		0.6		μs	
t_f	rise and fall		0.2		μs	
t_{dr}	times		0.5		μs	
t_r			0.5		μs	
t_{df}	Parallel Delay,		0.55		μs	
t_f	rise and fall		0.35		μs	
t_{dr}	times		0.4		μs	
t_r			0.3		μs	
C_{in}	Data and Control Input Capacitance		7.0		pF	
I_{max}	Power Supply Current Drain		4.5	7.0	mA	$V_{GG} = -27$ V
P_{max}	Power Dissipation		120	190	mW	$V_{GG} = -27$ V
I_{LX}	Input Leakage Current			5.0	μA	$V_{in} = -20$ V
t_{dd}	Data Delay Time	250			ns	

TIMING DIAGRAM

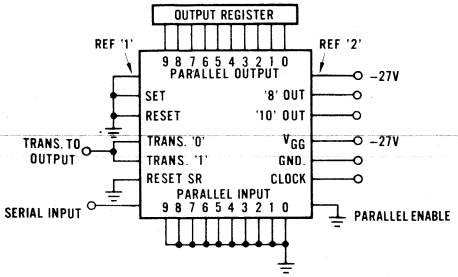


LOGIC DIAGRAM

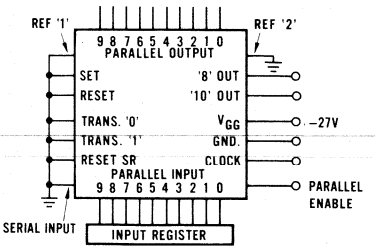


APPLICATIONS (Basic Logic Representation)

SERIAL TO PARALLEL CONVERTER



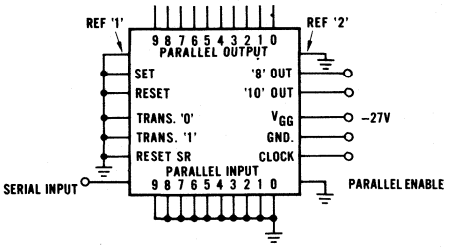
PARALLEL TO SERIAL CONVERTER



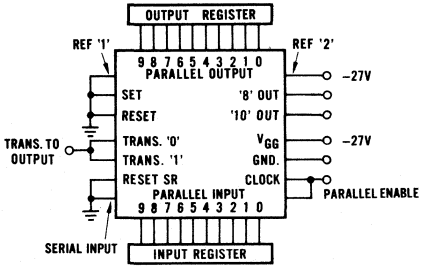
APPLICATIONS

(Basic Logic Representation)

SERIAL TO SERIAL BUFFER REGISTER



PARALLEL TO PARALLEL BUFFER REGISTER



MOS Applications

ADVANCES IN LSI USING SILICON GATE TECHNOLOGY

INTRODUCTION

Silicon gate technology is superior to conventional metal gate (MOS) technology in many respects for manufacturing complex, high density, monolithic digital subsystems. During the next several years this new technology will undoubtedly replace the original technology in the production of such subsystems. Numerous custom and standard product devices illustrating the device/circuit/subsystems advantages of silicon gate technology have already been designed and transferred to production at Fairchild. These devices offer greater functional capability, higher speed and lower power dissipation. This report considers briefly the salient features of the silicon gate process and of the devices and circuit structures produced by this process. The relative merits of the new technology versus the old also are compared in detail.

THE SILICON GATE PROCESS

Processing of silicon gate devices consists of five masking steps, or six steps if a double masking step is required to open up the contact holes. The first mask is used to cut through a thermally grown field oxide to open up the source-drain (P+) and gate areas of the circuit. After regrowth of the gate oxide and deposition of polysilicon, a silicon gate mask is used to define the gate electrode and the polysilicon interconnection line segments. The silicon gate itself is subsequently used as a mask to define the source and drain regions (See Figure 1), and is doped with P+ dopant during the source-drain predeposition and diffusion steps. Following this, a layer of oxide is vapor deposited on the wafer, and the contact mask is used to open up contacts on the source, drain, and polysilicon areas that are subsequently to be connected to metal interconnects. The contact etch may be accomplished with either one or two masking steps depending on how well dimensions can be controlled during the etch cycle. After the metal layer is placed on the wafer and defined by the metal mask, a layer of topside vapox is deposited and the fifth and final mask is used to open up the bonding pads.

FAIRCHILD
SEMICONDUCTOR

The principal differences between the silicon gate process and conventional metal gate processes are:

1. The gate oxide is grown under conditions which are not influenced by other processing requirements, such as diffusion times, etc.

2. The oxide is immediately covered by the polysilicon layer and is never thereafter exposed to additional processing steps (photoresist and etch).

3. The channel area is defined by the gate, resulting in a self-aligned structure.

4. There may be one less masking step in the silicon gate process if a single contact mask step is used.

5. High temperature processing can be accomplished after the device formation is completed, thus permitting nitride passivation.

THE SILICON GATE DEVICE

Typical transistor cross-sections of devices fabricated with metal gate technology and with silicon gate technology are illustrated in Figure 2. The most obvious feature of the silicon gate device is that the transistor is approximately one-half as large in cross-section as its metal gate equivalent. This is due to the self-alignment of the gate to the source and drain regions, and to the fact that no provision is needed for metal-to-metal separations such as those required between the gate and the source and drain contacts in metal gate devices. The reduced transistor size permits fabrication of devices equivalent in impedance to larger metal gate devices, but with smaller gate capacitances. Or if desired, the transistor channel width may be increased somewhat to produce lower impedance transistors which are suitably small for high density circuitry, and which have gate capacitances approximately as large as the higher impedance metal gate devices. In this case, geometrically smaller, lower impedance load resistors may be used in ratio-type logic circuits, to improve transient performance. Since the logic voltage supplies for silicon gate devices are typically ground and +5v (compared to ground and -12v for metal gate circuits), silicon gate load resistors could be as much as five or six times smaller than metal gate load resistors without increasing power dissipation (power per gate is approximately equal to V_{DD}^2/R_L). Silicon gate resistors usually are designed to have one-half to one-third the impedance of their metal gate equivalents. Thus the improved speed of silicon gate circuits is obtained in conjunction with reduced power dissipation.

Another factor contributing to the reduced size of silicon gate devices is the fact that source and drain contact holes are made in one processing step and need only be aligned with the P+ source and drain diffusions. In the thick oxide metal gate technology, the contact mask must be aligned to contact areas previously defined during the gate mask step, and thus some allowance is generally incorporated into the second mask to ensure alignment to the first. Thus the cumulative contact areas are larger in metal gate devices than in silicon gate devices.

In addition to the reduced impedances of silicon gate transistors and

load resistors discussed above, the total capacitive loads on internal nodes also are reduced in silicon gate circuits, further improving performance. Figure 3 shows profiles of typical interconnection segments for metal gate and silicon gate circuits. The first layer of interconnection in the metal gate circuit is made in P+ diffusion line segments, while polysilicon strips accomplish this function in silicon gate circuits. In either technology, the metal-to-substrate and the crossover capacitances are essentially identical. But the diffusion capacitance is approximately three times larger than the polysilicon-to-substrate capacitance. This means that for equal-length runs of metal and either diffusion or polysilicon on a given node, the silicon gate circuit has approximately half the capacitive load due to interconnect lines compared with the metal gate circuit. Techniques which try to minimize the total length of diffusion interconnect on a given node in metal gate circuits introduce area inefficiencies by utilizing long and circuitous metal interconnections.

The brief discussion and figures presented above are intended to describe the devices and circuit structures produced with silicon gate technology, using metal gate devices for reference. The following paragraphs contain detailed comparisons of the two technologies in terms of devices, circuits, and reliability. Some indications of the ultimate systems performance advantages, reliability improvements and cost reductions to be realized with silicon gate technology are summarized in the conclusion.

COMPARISON OF TECHNOLOGIES

Metal gate technology may be used to produce either high threshold circuits (on < 111 > orientation starting material) or low threshold circuits (on < 100 > material). The high threshold circuits (with V_{DD} in the vicinity of -12 volts and V_{GG} near -27 volts) are the most common types available today. Low threshold circuits operating with bipolar voltage supplies (+5 volts and ground) as well as with negative 12 volt or 15 volt supplies also are built, although these circuits usually offer inferior performance in comparison to their high threshold counterparts.

Like the low threshold metal gate circuits, silicon gate devices are designed to operate with +5, ground, and -12-volt supplies, but with improved rather than derated performance. In the outline that follows, ratio-type silicon gate circuits are compared to equivalent metal gate structures produced on either < 111 > or < 100 > substrate material. Such circuit structures are used in Fairchild's Micromosaic™ array cell families and in numerous shift register, ROM, and RAM applications. The comparisons made also are valid for ratioless circuit structures that can be produced using either manufacturing process.

I. TRANSISTORS

A. DEVICE CHARACTERISTICS:

Silicon Gate Technology	Metal Gate Technology
1. Threshold voltage in the range $1.5 \leq V_{TO} \leq 2.0v$ on < 111 > starting material.	1. Threshold voltage in the range $1.8 \leq V_{TO} \leq 2.6v$ on < 100 > and 2.8 to 4.5 on < 111 > starting material.
2. Minimum transistor overdrive voltage for 5v ± 10% logic voltage supply is 4.5V - 2.0v = 2.5 volt.	2. Minimum transistor overdrive voltage for 5v ± 10% logic voltage supply is 4.5v - 2.6v = 1.9 volt.
3. Channel mobility, $\bar{\mu}$, is reduced from the zero field value by a surface field of E_S = 5v/1300 Å. The minimum strength of this field minimizes mobility reduction with voltage.	3. Channel mobility, $\bar{\mu}$, for high threshold circuits is reduced by E_S = 12v/1100 Å and by E_S = 5V/1100 Å for low threshold circuits. In both cases, the fields exceed those encountered in silicon gate devices.
4. Self-aligned structure minimizes gate oxide area by eliminating mask overlaps. Overlap capacitances are small (lateral diffusion depth only) and predictable (always the same) at approximately 0.8μ. Miller capacitance and gate-to-drain coupling are minimized by reduced overlaps.	4. Overlaps are required to ensure channel continuity to source and drain during fabrication. Overlap capacitances are large (lateral diffusion plus alignment tolerance) and vary by a factor of two from nominal to worst case as alignment changes. Worst case may be as high as 5μ with only 0.1 mil mask misalignment. Large overlaps make Miller and coupling capacitances large, thus amplifying the effect of the parasitics.
5. Transistor cross sections are determined by channel length and contact areas, resulting in minimum device sizes of approximately 1.6 mils in cross-section, using standard mask dimensions and tolerances.	5. Transistor cross-sections are determined by channel length, two metal-to-metal separations, and contact areas which must accommodate successive masking steps during processing resulting in minimum of 2.8-mil cross-sections, using standard dimensions.
6. Shallow diffusion profiles (~1μ) permit greater control of channel lengths. This	6. Deep diffusion profiles (1.5 - 2.5μ) result during gate oxidation and introduce

plus reduced circuit voltages permit shorter source-to-drain channel lengths (0.1 mil minimum), and thus higher gain.	potentially greater variation in channel length. On high voltage < 111 > parts, long channel lengths (.15 mil minimum after processing) are required to prevent reach through breakdown. Variation in the diffusion profiles of deep junctions must be accounted for in the device design.
7. Large capacitors may be generated when required using field effect structures without relying on parasitics to provide capacitance.	7. Large capacitors may be generated using field effect structures. Overlap capacitances add to total node capacitances, reducing the size of any separate capacitor structures that may be required.

B. EFFECTS OF DEVICE CHARACTERISTICS:

Silicon Gate Technology	Metal Gate Technology
1. Transistors have high gain, and therefore low impedance, due to high mobility, low V_{TO}, and short channel lengths.	1. Transistors have lower gain due to higher V_{TO}, longer channel lengths, and, in the case of high threshold parts, lower mobility because of stronger gate-to-channel fields.
2. Low impedance transistors can sink large (TTL) currents in output buffers and discharge large load capacitances rapidly, both internally and when driving off chip. Typical devices with 5-volt gate drive have 7.5 Kohms per square in the channel area.	2. Voltage level imcompatibility prevents direct output interfacing of high level MOS and bipolar devices without at least some additional external components. Low voltage < 100 > devices with 5-volt gate drive have in excess of 10 Kohms per square in the channel area, necessitating large driver devices to sink bipolar currents.
3. Low impedance (30-40 Kohm) load resistors are built which increases the speed of an average logic gate to 30 nsec per picofarad of load. Typical resistors occupy approximately 0.6 mil^2.	3. Resistors of 50-100 Kohms occupying 1.2 mil^2 are required to limit the size of the transistors. Typical gate speeds of 50 ns per picofarad result on high threshold < 111 > circuits. Average gate delays of 75 nsec per picofarad are realized on < 100 > devices.

4. DC noise immunity is greater than 0.7v under usual worst case conditions for 0°C to 70°C temperatures.	4. DC noise immunity typically exceeds 1v, even for the full temperature range of -55° to +125°C for high voltage parts, and is 0.6v for low voltage devices for $0°C \leq T_A \leq 70°C$.
5. The operating logic level voltage of 5 volts leads to power dissipation of typically 0.5 mw per "on" gate.	5. Power dissipation with high voltage MOS circuits is 1.6 mw per "on" gate, and 0.3 mw per "on" gate for the slower low threshold circuits.
6. Reduced transistor gate area, even for lower impedance devices, presents lower input capacitance as load.	6. Input capacitance of transistors is approximately twice as large as that of an electrically equivalent silicon gate device, due to overlap requirements and longer channel lengths.
7. Bipolar interfacing at outputs is direct since buffers sink TTL currents.	7. Output interfacing circuits (pull-up resistors, etc.) are required to enable high or low threshold devices to drive standard bipolar circuits.
8. Low thresholds permit direct interfacing with bipolar circuits at inputs. On chip pull-ups, may be used when needed.	8. High threshold circuits cannot be interfaced directly to standard bipolar IC's at inputs. Low threshold circuits interface directly with bipolar IC's at inputs, but, since the worst case overdrive voltage is less than 2v, the transistors are necessarily large and noise immunity is minimized.

II. ON CHIP INTERCONNECTION

A. STRUCTURES AND CHARACTERISTICS

Silicon Gate Technology	Metal Gate Technology
1. Two levels of interconnection, isolated above the substrate, are available.	1. One level of interconnection isolated above the substrate is available.

2. Polysilicon interconnection capacitance is 0.11 pF for a typical 10-mil interconnection line segment.	2. Diffusion interconnection capacitance, which is used for the second layer of interconnection, is 0.30 pF for a typical 10-mil interconnection line segment of equal line width.
3. P+ diffusion can be used occasionally to provide a "third" layer of interconnection, although it cannot cross under the polysilicon layer. Limited use minimizes introduction of large capacitances, but permits flexibility in design.	3. Present technologies are limited to two layers of interconnection, metal and diffusion.
4. Metal interconnect segments may pass over active regions of devices. Capacitive coupling is minimum and does not affect performance of properly designed ratio-type circuitry.	4. Interconnections may not pass over active device areas.
5. Polysilicon interconnect lines have 20-80 Ohms/square series impedance.	5. P+ diffusions typically have 100-300 Ohms/square impedance.
6. Crossover capacitances (metal-to-polysilicon, metal-to-P+) are determined by coincident interconnection areas and approximately a half micron dielectric. Typical capacitances are less than 0.01 pF.	6. Crossover Capacitance (metal to P+ diffusion) is through a 1μ oxide, which results in a lower capacitance per unit area. Typical capacitances are approximately 0.005 pF, smaller than the silicon gate crossover capacitance.
7. Large butting contacts (.12 to .18 mil^2) are required to connect diffusion to polysilicon.	7. No butting contacts are required since metal crosses over P+ diffusions. Contacts are typically 0.08 to 0.09 $mils^2$.

B. EFFECT OF INTERCONNECTION CHARACTERISTICS

Silicon Gate Technology	Metal Gate Technology
1. The low capacitance per unit area of polysilicon results in substantial reduction of total interconnection capacitance.	1. P+ diffusion causes interconnection capacitance to be large and voltage dependent. Note that the diffusion capacitance is smallest in value when reverse biased, as when "holding at one level", so that the nonlinearity adversely affects circuit performance.
2. Low polysilicon series resistance allows long extensions of gate runs to distribute signals. Series RC time constants in the distribution net are minimum due to low ohms per square and small capacitances.	2. P+ diffusion runs can introduce large RC time constants in signal distribution nets, causing deterioration of pulse characteristics.
3. Total interconnection area is minimized by unrestricted use of polysilicon interconnection line segments and the distribution of metal interconnects over active devices.	3. Interconnection areas are larger than necessary due to the preferred use of metal interconnects and the resultant routing problems. Also, interconnections are not allowed to pass over device areas.
4. Butting contacts are rarely used in grid-oriented interconnection systems, such as those used in logic circuits, because contacts are made between metal and polysilicon or metal and diffusion. Few butting contacts are used inside logic "cells" because polysilicon is used to route intracell signals. Butting contacts can cause area inefficiencies if carelessly employed in design.	4. No butting contacts are used in metal gate devices. Interconnection contacts occupy minimum areas, similar to the large majority of contacts in silicon gate circuits.

III. CHIP AREA

A. ACTIVE AREA COMPONENTS

Silicon Gate Technology	Metal Gate Technology
1. Small transistors result in compact circuit structures.	1. Larger transistors and resistors adversely affect packing density.
2. Total interconnection areas are reduced by the use of polysilicon interconnects and by distribution of metal over active areas, as outlined above.	2. Interconnection areas are larger than for silicon gate as outlined above.
3. Small capacitive loads permit use of small geometry devices without sacrificing performance.	3. For large capacitive loads, transistor and resistor geometries must be large to produce the low impedance devices necessary for suitable transient performance.
4. Contacts between metal and polysilicon or between metal and P+ diffusion are similar in size to contacts in the metal gate technology (0.08 to 0.09 mil^2).	4. Contacts to change levels between metal and diffusion are typically 0.08 to 0.09 mil^2 minimum.

B. EFFECTS OF ACTIVE-AREA COMPONENTS ON CHIP SIZE

Silicon Gate Technology	Metal Gate Technology
1. For a given frequency of operation, small transistors may be used to drive small capacitive loads. Power dissipation is minimized and chip area is conserved.	1. Larger transistors and resistors, required to drive larger capacitive loads, dissipate greater power.
2. Serial organization of logic may minimize the gate count, and therefore chip size, without sacrificing performance because the individual gates have greater drive and are faster. The resulting minimization in chip size further minimizes interconnection capacitance, thus further enhancing circuit performance.	2. Often, parallel logic organizations are required to meet system speeds, thus increasing the gate count with no increase in functional capability, and increasing chip size, which further increases capacitive loads.

3. Chip sizes are minimized for a given logic function, or more gates may be placed on a single chip because of improved packing density. 300-400-gate general purpose logic arrays are reasonable.	3. Large chips are necessary to accommodate 200-gates of random, general purpose logic.
4. Smaller circuits with smaller areas of P+ diffusion and gate oxide offer higher percentage yields and more gross die per wafer. Die costs are reduced and manufacturing capacity is increased accordingly.	4. Circuits with large, thin oxide areas and large areas of P+ diffusions statistically yield a lower percentage. In addition, the gross die per wafer are reduced as circuit area increases.

IV. DEVICE FABRICATION

A. WAFER PROCESSING CONSIDERATIONS

Silicon Gate Technology	Metal Gate Technology
1. Five or six masking steps are required including one for topside passivation.	1. Six masking steps are required including topside mask.
2. The gate oxide is grown independently of other processing considerations, is immediately covered with polysilicon, and is never subsequently exposed to additional processing.	2. The gate oxide is grown as the P+ diffusions are being driven in. The oxide layer is subsequently covered with photoresist, which must remain intact during the contact etch step.
3. Doping of the polysilicon layer is accomplished during the source-drain predep and diffusion. Anomalous threshold variations due to introduction of dopant into the gate oxide do not occur during controlled processing.	3. No doping of the metal gate is required.
4. Lower voltage signals on circuits with < lll > starting material permit the use of thinner field oxides.	4. Field oxides must withstand 30v logic signals and clocks on < lll > circuits, thus requiring thicker oxides (See Figure 2 for typical cross sections).

5. The polysilicon gate can withstand high temperature processing, such as that required for deposition of a silicon nitride layer for passivation after the transistor has been formed.	5. The metal gate device cannot be subjected to high temperature processing after the transistors are made, which limits the type of post-transistor processing that may be employed.
6. The polysilicon layer is an additional layer added to the basic MOS structure, which represents in some instances, and additional processing burden.	6. The basic MOS structure has a P+ layer, gate oxide, field oxide and the metal layer. A fifth layer is often, if not generally, used beneath the metal gate to prevent instability.

B. EFFECTS OF WAFER PROCESSING

Silicon Gate Technology	Metal Gate Technology
1. The fact that the 1300 Å gate oxide is not exposed to photoresist and etching minimizes the occurance of pinholes, and this enhances yields.	1. The 1100 Å gate oxide can develop pinholes during the contact mask operation, which is a common device failure mode.
2. The doped gate electrode accounts for the 1.5 to 2.0-volt range of V_{TO} on < 111 > starting material. Reliability studies have identified no long term instability of devices manufactured with doped electrodes. Reliability data is not nearly as extensive as that available for metal gate. Experiments are under way.	2. The aluminum-silicon work function increases the device threshold by approximately 1.1 volts over that of silicon gate circuits. The millions of device hours of reliability data gathered to date exceed the data available for silicon gate devices.
3. Thinner field oxides minimize the topographical irregularities of the surface and contribute to higher resolution and higher yield metal processing. The maximum metal step is less than 1μ.	3. Because the contact mask must align to the contact cut made during the gate masking operation, staircasing tolerances must be used to avoid steep steps at the cost of area. If this is done, the maximum metal step is approximately 1μ.

4. A passivation layer, such as silicon nitride, which is currently under development, will effectively seal the device from outside environments and will enable manufacturers to use plastic or other forms of low cost packages.	4. Without effective passivation, hermetic packages are required and devices are subject to contamination during wafer sort and assembly operations. At best, post assembly processing is required to ensure reliability.
5. The polysilicon layer may or may not represent an additional layer compared with a metal gate device. Its use, however, in covering the gate oxide from the beginning of the process eliminates the need for a multiple-layer dielectric beneath the gate electrode.	5. Multilayer gate oxides are optional, but generally used, making the processing equal on this issue.
6. P+ diffusion area is minimized because diffusion is not used extensively for interconnections.	6. P+ diffusions are used for interconnects and can contribute both to yield loss due to junction failures, and performance loss due to increased capacitance.

CONCLUSION: DESIGN WITH SGT COMPONENTS

The detailed comparison of the silicon gate and metal gate technologies outlined above thoroughly defines the relative merits of the two approaches from the manufacturing and the device characteristic viewpoints. A summary of the major circuit-oriented advantages of the silicon gate technology includes the following:

1. The self-aligned gate electrode results in reduced transistor area primarily because mask alignment tolerances are eliminated and because the transistor has one less metal strip and one less metal-to-metal separation.

2. Transistors have low on-impedances due to low threshold voltage, high carrier mobility, and shorter channel lengths. Low load resistors are used to improve performance.

3. Transistor gate capacitances are reduced because of small device area and small overlaps.

4. The polysilicon layer may be used as a second layer interconnection. Capacitances of polysilicon runs are only one-third as large as depletion capacitances for diffused P+ interconnections.

5. Reduced load capacitances on internal nodes permit the use of small circuit structures with reduced power dissipation without sacrificing performance, or conversely, with improved performance using typical device geometries.

6. Output devices can be designed to drive bipolar circuits directly without extra power supplies or external components.

The ultimate comparison, however, is the measure of the utility of the resulting devices in the systems constructed with them. The concluding remarks of this report summarize the systems advantages offered by devices manufactured with the silicon gate process.

1. Smaller circuit structures result in packing density improvements of 50% and more over metal gate MOS circuits in general purpose logic applications.

2. Improved transient performance is realized coincidentally with reduced power dissipation, so that today's general purpose logic circuits operate with 2 to 3 MHz systems clocks with average power dissipations of 0.3 milliwatt per gate. More regular structures, such as shift registers, can be designed to operate at speeds greater than this. This amounts to a five or six-to-one improvement in the speed x power product over metal gate circuits.

3. Bipolar compatibility of SGT circuits is accomplished by using +5 volt and ground power supplies and by direct interfacing at input and output data terminals. This compatibility, resulting from low device thresholds, permits mixing bipolar and SGT components in systems without expensive interfacing.

4. Peripheral circuits for SGT circuits, such as clock drivers, are easier to build because of reduced amplitudes and reduced drive requirements, even at high levels of performance. Logic level clocks are often used, either directly or indirectly, as in the case of dynamic circuits with on-chip clock signal processing.

5. Because of these features, systems implemented with SGT components have fewer chips and fewer chip types compared to metal gate MOS systems, as well as reduced peripheral circuitry. The end result is minimum system development and manufacturing costs.

Undoubtedly, LSI technology is a major step forward in the reduction of circuit components costs (whether one counts transistors, simple gates, or complex functions), and prices equivalent to four or five cents a gate are not uncommon in today's market. While this is impressive in itself, an even greater systems advantage inherent in LSI is the fact that the interconnection for all the gates contained on a given chip is implemented during the batch-fabrication manufacture of the circuits. As an example, a 200-gate array of general purpose logic is equivalent to about 40 packages of bipolar IC's. At 14 pins per package, the bipolar circuits have 560 pins to be inserted and assembled in a system. If one assumes the commonly used cost of seven cents per package pin to assemble components into a system, assembly cost of the 40-package system is nearly $40. Thus, the savings offered by LSI (even with today's depressed prices for bipolar gates) are not only obvious, but also compelling.

In addition, the reduction in semiconductor part types, the decrease in the number of printed circuit cards in a system, the reduced component documentation, and the decrease in the volume of incoming inspection testing at the user's plant are significant advantages of large scale integration. The silicon gate technology leads to a greater level of integration, thereby resulting in further cost improvements for system implementation.

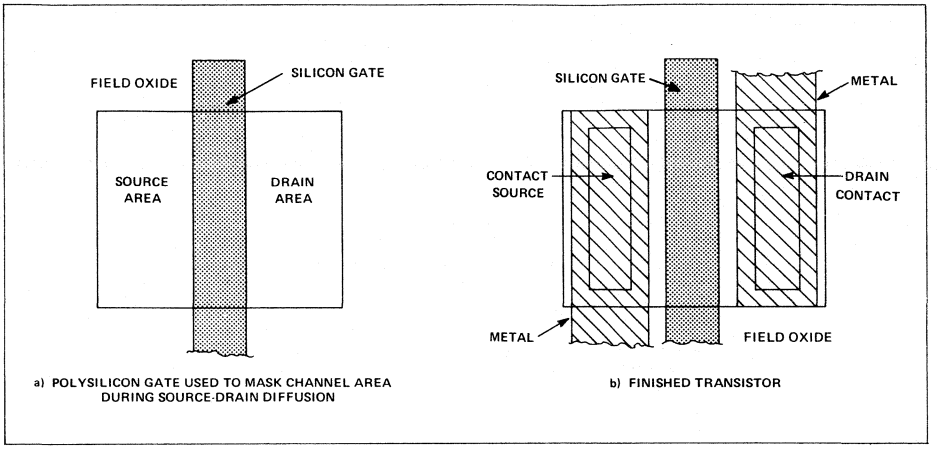


FIGURE 1: TOP VIEWS OF A SILICON GATE TRANSISTOR

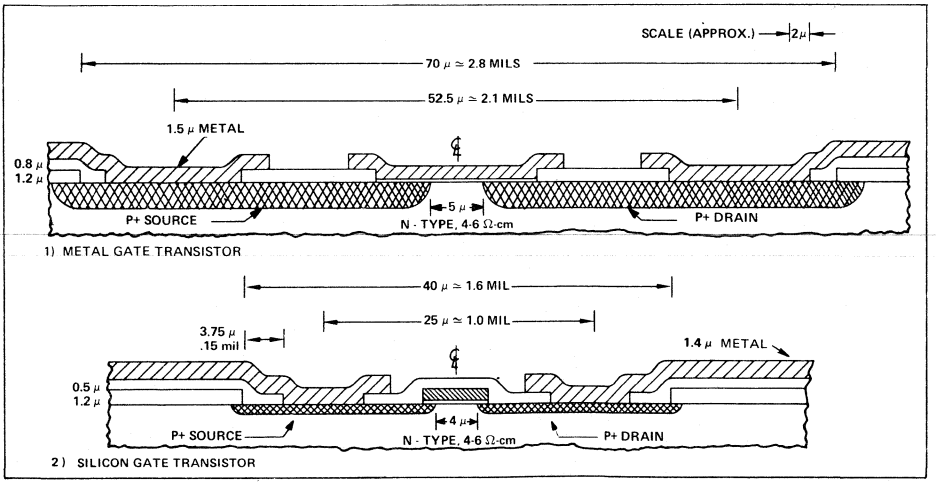


FIGURE 2: TRANSISTOR CROSS SECTIONS. COMPLETED STRUCTURES BEFORE T.S.V.

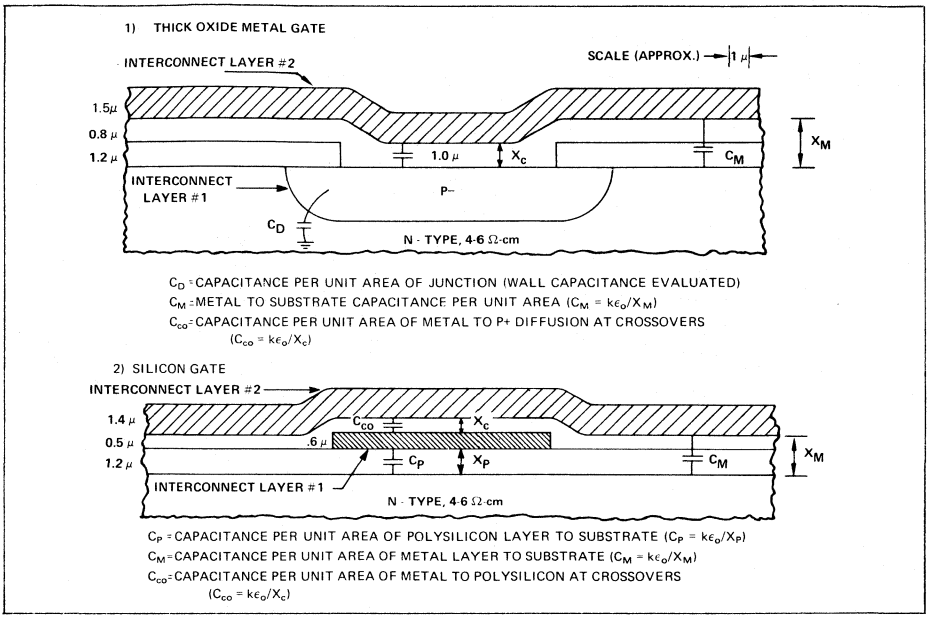


FIGURE 3: INTERCONNECTION SEGMENTS AND CAPACITANCE COMPONENTS

PARTITIONING LOGIC SYSTEMS FOR 3400 MICROMOSAIC

The 3400 Series Micromosaic™ array in digital systems can replace as many as 200 conventional gates (approximately 70 DTL packages) with one device, thereby substantially reducing costs and space requirements. This paper describes techniques, using the 3400 Micromosaic™ array, for partitioning a digital system into a configuration that optimizes performance and cost savings.

Partitioning a logic system is not a new design problem. To illustrate: Assume that a logic system of 150 packages has been implemented using standard MSI parts. These 150 packages must be placed on 4 1/2" x 4 1/2", two-sided PC cards with 44 pins. Up to 15 packages may be placed on a card. Ideally, it would be desirable to partition the logic system into 10 identical cards, thus reducing design, manufacturing, and inventory costs and associated problems considerably. However, in practice one usually partitions the system into 10 cards, which may or may not be identical. Since each card must contain an average of 15 packages and be limited to no more than 44 pins, this 10-card partitioning is not always easy.

Partitioning usually consists of finding groups of $\leq$16 DIP's that have a high package-to -external-pin ratio when separated from the rest of the system. Some of these groups may be significantly smaller than 16 packages. By rearranging and combining these groups, one can define a total of 10 groups so that no group has more than 16 packages and 44 external pins. If 10 of these groups cannot be found, it is then necessary to either increase the number of groups (cards) or modify the logic design.

Designing with the 3400 Micromosaic™ family requires partitioning similar to that described above; the packages are analogous to functional building blocks (cells) and the PC cards are analogous to MOS chips (3400 arrays). There are, however, significant differences.

LOGIC CONVERSION

Often, a logic design that is going to be implemented with 3400, has previously been adapted to another logic family, i.e., Fairchild TTμL. Before detailed partitioning begins, the logic must be adapted to the 3400 cell set. The cell set is specified in a brochure entitled "Micromosaic Arrays ... An MOS Approach to Custom LSI." As can be seen in Figure 1, a direct conversion may waste silicon area. In this example, the direct conversion (Figure 1B) represents about 20% more area, twice the power and twice the propogation delay than the reduced conversion (Figure 1C). The symbology of Figure 1 is consistent

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with MIL STD 806-B; thus, if the three diagrams were considered as "black boxes", they would all respond with the same polarity of voltages. Note that in terms of voltage polarity a TTμL NAND gate in Figure 1A is equivalent to an MOS NOR gate in Figure 1B or 1C.

Finding the optimum conversion from a given complex logic diagram to the 3400 cell set may require a great effort. However, once the designer is familiar with the cell set, it is easy for him to bring about significant reductions in both silicon area and the number of chips.

PARTITIONING BASED ON CHIP SIZE AND PACKAGE PINS

The following information enables the designer to partition his system on a basis of chip size and pin count. At present, the optimum chip size (minimum cost per gate) is in the range of 100 mils side to 130 mils/side. With chips>100 mils/side, the cost per gate tends to increase because of decreased gate-to-pin ratio and increased number of chips per system. With chips > 130 mils/side, the cost per gate tends to increase because of lower yields per wafer. Available packages are:

16 pin DIP* and Flatpak
24 pin DIP and Flatpak
36 pin DIP and Flatpak
50 pin DIP and Flatpak

Figure 2 shows the approximate chip size as a function of total horizontal cell length (complexity). The curves represent the equation $L = W \cdot H + 20$, where:

L = outside chip dimensions (assuming square chip)
W = cumulative cell width
H = cell height + intercell wiring space
  = 24 for difficult interconnections
  = 20 for moderate interconnections
  = 16 for simple interconnections
20 = space allowed for pads on all 4 sides of chip

*Max chip size = 90 mils x 120 mils in 16 pin DIP

The entering arguments are estimated difficulty of interconnection and horizontal cell width (W). For random logic which has no counters or registers, use difficult interconnection curve, (Figure 2). (A 3400 where H ≥ 24 mils is extremely rare.) For logic which is "typical" including some random logic, counters and registers, use the "moderate interconnection" curve. (Most of the logic examined falls close to this curve.) For logic that is highly regular, such as long shift registers, ripple counters and a nominal amount of control logic use the "simple interconnection" curve.

To determine W, total the horizontal length of the cells to be placed on the chip, using Table 1 to obtain individual cell lengths.

EXAMPLE: LOGIC OF FIGURE 1C

CELL	NUMBER	CELL WIDTH	TOTALS
NAND 2	1	3	3
NOR 3	1	4	4
NOR 4	2	5	10
NOR 5	1	6	6
EXP 3	1	4	4
EXP	1	3	3
INV	2	2.5	5
		TOTAL CELL WIDTH	35

For an actual array, the total cell length would be in the range of Figure 2.

LOGIC CHANGES FOR MORE EFFICIENT PARTITIONING

It is often desirable (economical) to add a nominal amount of logic to reduce the interchip wiring (number of pins) to a tolerable level. A few such approaches are listed below. Some of these approaches are utilized only after preliminary partitioning has commenced while others are designed in before partitioning begins:

1. Single rail transfer between chips: If both polarities of a signal are needed at the

destination chip(s), invert the signal at each destination chip where necessary, rather than bringing both wires off the originating chip.

2. Local decoding: If many decodes of a counter must be used on other chips, decode at the destination chips instead of decoding on the counter chip and distributing these numerous signals between chips.
3. Efficient counters: Use minimum flip-flop counters where condition 2 exists (avoid Johnson and ring counters).
4. Signal bussing: Interchip signals which are not used at the same time, may be bussed together.
5. Bit slicing: Partition a processor by bit(s) rather than by function(s). (See Figure 3.)
6. Serial data transfer: Data is transmitted between chips in serial form.
7. Conceptual design change:
   a. Use time multiplexing - This is an extension of #4.
   b. Other - This is probably the most significant factor in reducing the number of pins and the most difficult to describe. Each functional requirement must be considered uniquely with conceptual approaches which lead to pin reduction and do not lead to excessive logic complexity.

SUMMARY

Efficient logic design and partitioning of Micromosaic arrays will result in the minimum cost and turnaround time to implement a function.

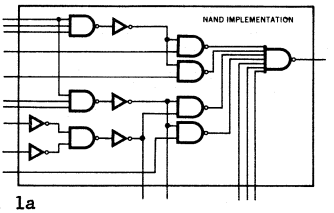

FIG. 1a

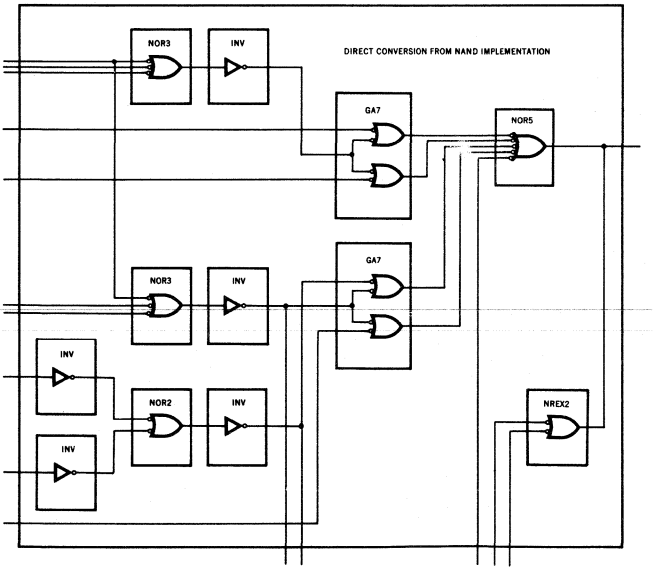

FIG. 1b

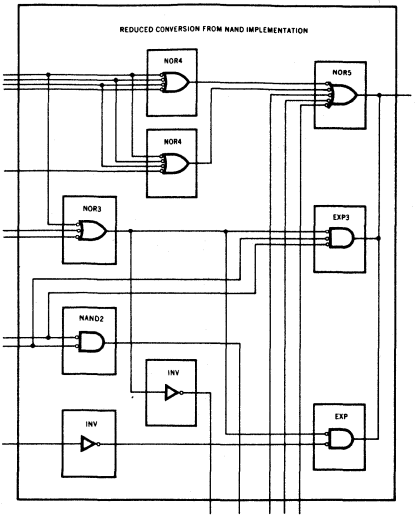

FIG. 1c Complexity (cell area), power and propagation time of 1B is much greater than that of 1c.

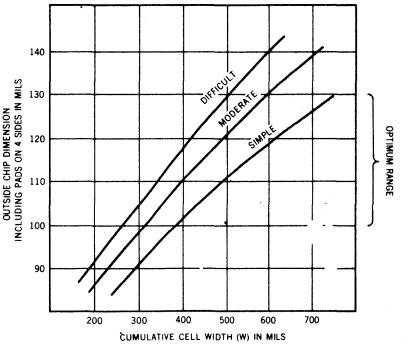

FIG. 2 Chip size as a function of cell length and complexity of intra-chip connections.

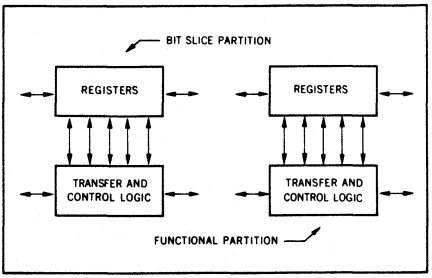

FIG. 3 A processor may be bit sliced, producing a number of identical parts if the number of bits (word length) is larger. If the number of vertical paths, bit slicing also will require fewer interconnections.

TABLE 1

CELL TYPE	LENGTH (MILS)	CELL TYPE	LENGTH (MILS)
BBUF	8	GA6	6
BUF	6	GA7	5
BA	11	GA8	7
CG	16	HPI	3
EXP	3	INV	2.5
DNOR2	6	LRS	7
EXP3	4	MPI	3
FRS1	13	NAND2	3
FRS2	11	NAND3	4
FRS3	11	NOR2	3
FT1	13	NOR3	4
FT2	11	NOR4	5
GA1	5	NOR5	6
GA2	5	NREX2	3
GA3	6	NREX3	3
GA4	6	OUT	6
GA5	6	PD	2
		PDO	5

AB-182 HORIZONTAL RASTER SCAN VIDEO NUMERIC GENERATOR

Video character generators are being used a great deal for computer terminal readouts, television titles, stock market reports, time, etc., where the input information is in digital form such as from a keyboard or telephone line. These systems tend to use specialized read-only memories for the character generation which can be quite complex. This particular approach provides a low-cost 16-character video generator (Figure 1) which operates with standard television raster scan systems. An additional advantage is that the numerics can be superimposed over a video picture.

Digital BCD outputs from many available instruments such as DVMs or frequency counters are easily connected to the video numeric generator for a single composite readout. The data need only be converted to a video format signal and it can be distributed to several monitors through a standard coaxial cable.

The circuit provides 16-horizontal characters and 12 vertical characters -- 192 total -- and can readily display any lesser number. Each character is formed on a five-dot horizontal by seven-dot vertical matrix occupying 14 horizontal scanning lines. This provides an easy-to-read numeral from a normal viewing distance. Spacing is two video lines vertically and the equivalent of two* dot spaces horizontally.

The heart of this numeric generator is a 3255 or 3256 silicon gate character generator. This consists of a counter, column decode switch and a 560-bit read only memory (Figure 2). This ROM more than handles the dot matrix requirements of 540 dots (5 X 7 X 16). Figure 3 best explains the operation.

Requirements of the generator as as follows:

Negative going horizontal and vertical synchronization pulses, either from the monitor or derived from the composite video signal (Figure 4).

*This applies to the 3256. The 3255 spacing is one dot space horizontally.

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+5 volts for the logic and -12 volts for the silicon gate device bias.

Binary Coded Decimal (BCD) multiplexed information and a method for mixing the numeric information into the video system.

The operation outlined here references Figures 5 and 6. Figure 5 is a block diagram; Figure 6 is the circuit schematic. The horizontal delay one-shot and vertical delay counter are used to locate the numbers in a viewable area of the display. The end of the horizontal delay pulse from "A" starts keyed astable multivibrator "B" for the high frequency horizontal clock. The multivibrator operation is explained in Figure 7. The output of the astable multivibrator has a pulse duration of only 40 ns so it is fed through divide-by-2 JK flip-flop "C" (Q_0) to obtain symmetrical clock drive for the 3256 character generator "J." As there is no terminal count output on the 3256 column counters it is necessary to recount the clock pulses to count the characters using "C." The character counter "D" counts 16 and activates the stop JK flip-flop "E" and stops the astable multivibrator. All of the horizontal counters are reset when one-shot "A" is activated by the horizontal sync pulse.

The vertical sync pulse resets all of the vertical counters. At the end of this pulse, the JK flip-flop "H" divides horizontal sync by two. This feeds vertical delay counter "G" which counts until terminal count (TC), 15 pulses (or 30 horizontal sync pulses) later. Terminal count then goes high and is inverted and fed back to the count enable parallel (CEP) input of "G," stopping the count. Gate "G3" is now open allowing horizontal sync divide-by-two for line counter "H" to operate. When the vertical character counter "I" reaches 12 counts it operates stop flip-flop "L," blocking gate "G3" for any further pulses. Vertical sync resets the vertical counter and the operation repeats.

The number of characters displayed is reduced by connecting the vertical and horizontal stop flip-flops to the appropriate positions on the character counters. For example, the display of eight characters horizontally requires that stop flip-flop "E" be connected to $\overline{Q}_2$ of "D." Similarly, to obtain a single line vertically, the stop flip-flop "L" is connected directly to $\overline{Q}_3$ of line counter "H." (Counter "I" is not required for this application.)

Numerous methods may be used to enter input information into the video numeric generator. The use of input multiplexers is the most direct. Several input multiplexing systems are covered in the following publications.

APP 160 - Applications of the 9301 Decoder
APP 161 - 9300 Shift Register
APP 167 - MSI 9308 Dual 4-bit Latch
APP 170 - Applications of the 9311 1-out-of-16 Decoder
APP 181 - The 9309 and 9312 Multiplexers
APP 182 - The MSI 9328 Dual 8-bit Shift Register

Copies of these publications are available from Fairchild Semiconductor, Distribution Services, PO Box 880, Mountain View, California 94040.

Order Part Number A7K325519X or A7K325619X.

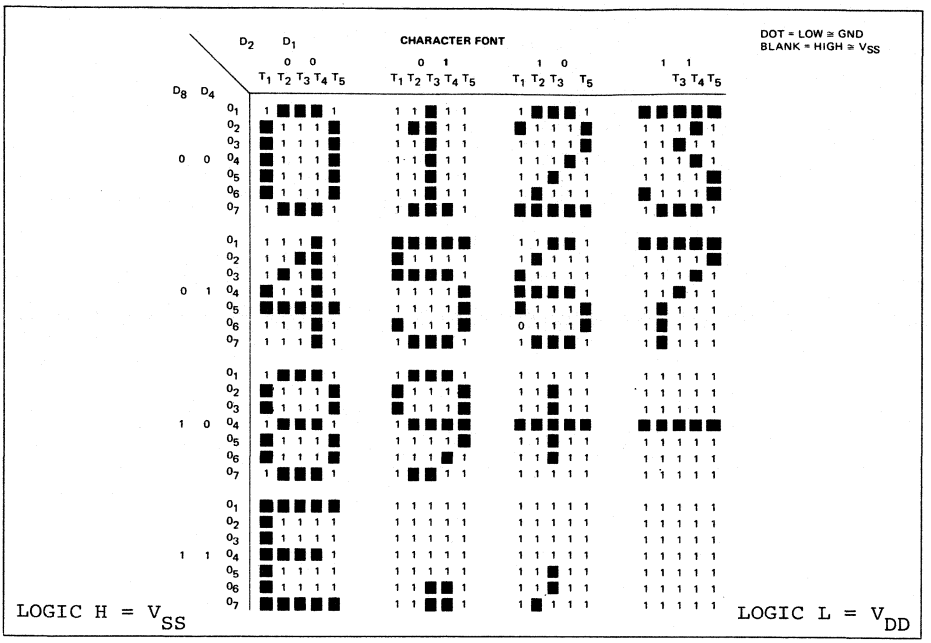

Figure 1. Character Font.

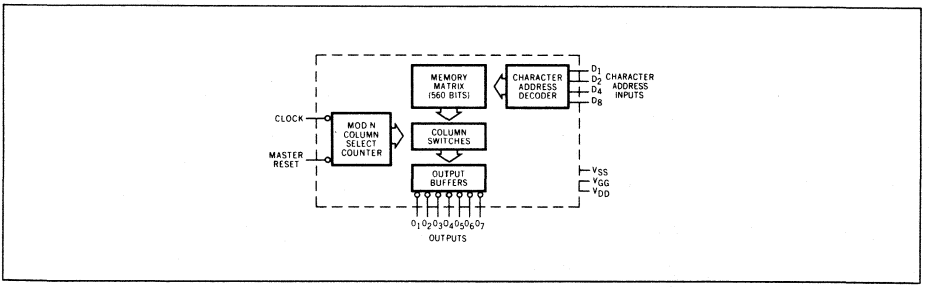

Figure 2. Block Diagram 3255 and 3256.

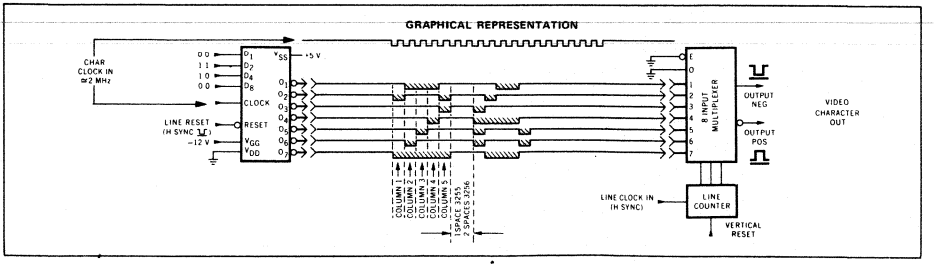

Figure 3. Graphic Representation of Waveforms for Numerals 2 and 6.

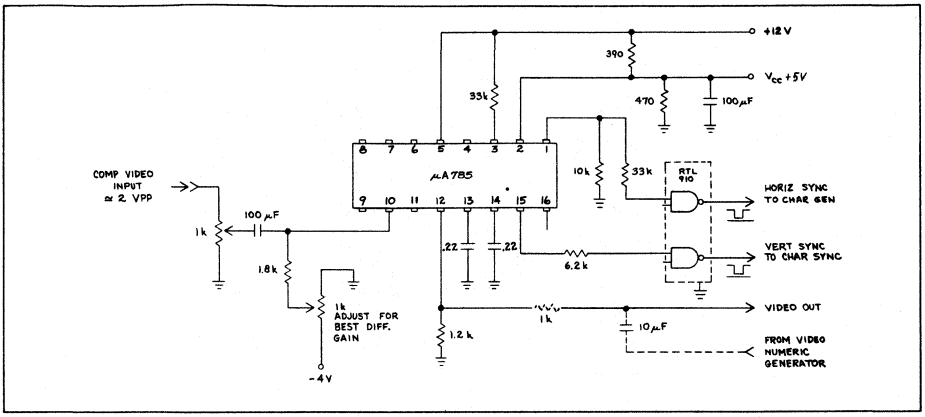

Figure 4. Interface Circuit for Character Generators and a Standard Composite Video Signal.

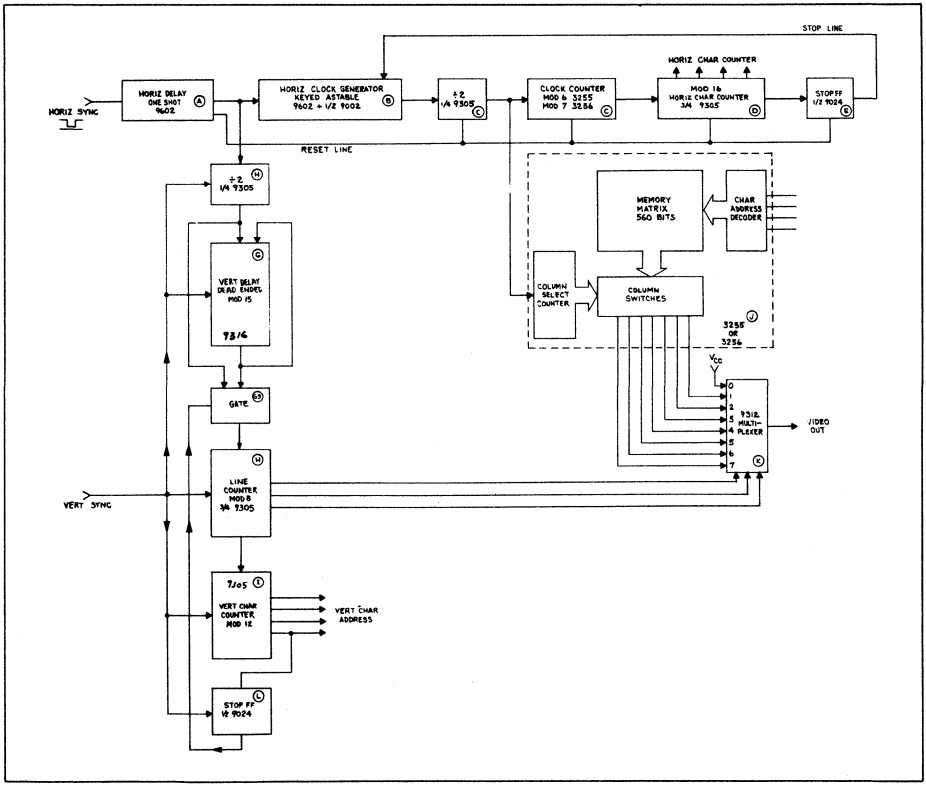

Figure 5. Video Numeric Generator Block Diagram.

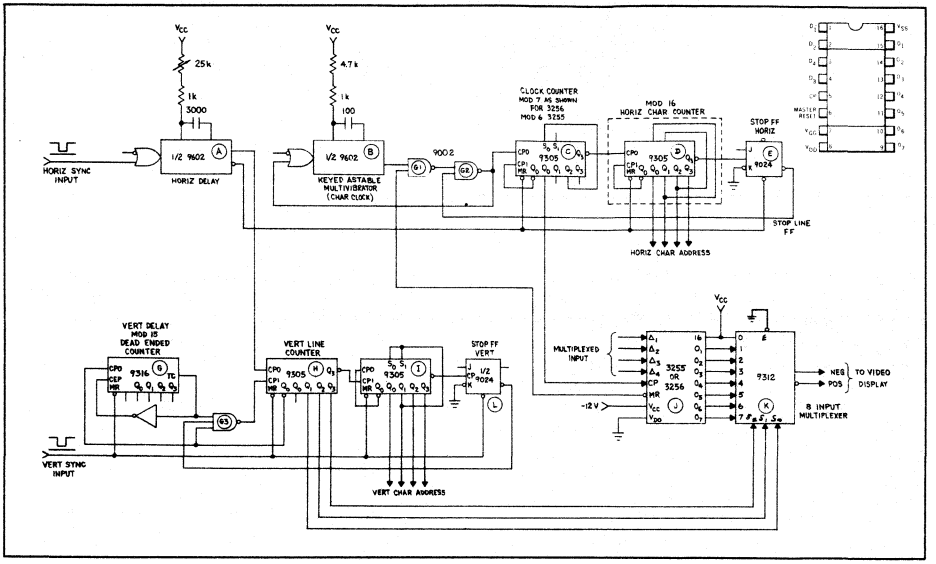

Figure 6. Video Numeric Generator Using the 3255 and 3256 Produces up to 192 Characters in 12 Horizontal Rows of 16 Each.

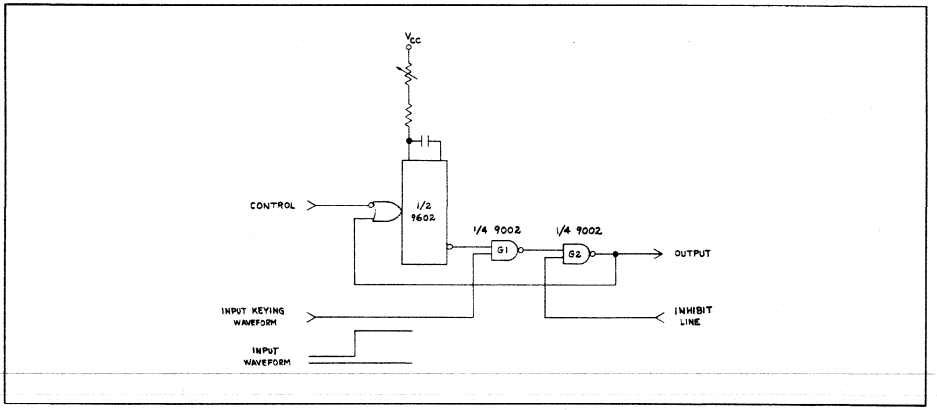

Figure 7. Horizontal Clock Keyed Astable Multivibrator.

The horizontal clock generator is only active during the period of the numeric display. Operation starts when the input waveform goes positive (low to high) with both inhibit and control lines high. The positive going edge triggers the one-shot and since both gates in the feedback loop are open, the astable multivibrator action commences. The operation is stopped by bringing either the inhibit line or control line low. An advantage of this type of keyed astable is that the duration of the first pulse is the same as the duration of successive pulses.

EFFICIENT UTILIZATION OF THE 3400 MICROMOSAIC ARRAY CELL SET

This application brief presents design information which will allow more efficient design of 3400 Micromosaic Arrays. The use of 3400 cells is analogous to that of a standard IC family, with the exception that 3400 Micromosaic offers a wider selection and provides more numerous ways of implementing a function. Normally, the method using the least silicon area is the most desirable, but other factors such as pin count, propagation delay, or power dissipation may be influential in the design. Schematics and logic diagrams for the cells are available in the brochure entitled: "Micromosaic Arrays...An MOS Approach to LSI" and will not be repeated here.

LOGIC SYMBOLS and EQUIVALENTS

The symbols used for the 3400 cell set are in accordance with MIL-STD-806B. The terms AND, OR, NAND, NOR, ONE, and ZERO are defined as follows:

ONE = the most negative logic level

ZERO = the most positive logic level

a NAND output = ZERO if and only if all inputs = ONE

a NOR output = ZERO if and only if any input = ONE

an AND output = ONE if and only if all inputs = ONE

an OR output = ONE if and only if any inputs = ONE

The designer may use either of two symbols to indicate an AND function or OR function (with or without inversion) as shown in Figure 1.

Since the most negative voltage is logic ONE (so called "negative logic"), the series connection is called the NAND, the parallel connection the NOR, and the common source the "wired AND." Throughout this Brief, the symbols used will be selected for maximum clarity.

SINGLE FUNCTION CELLS

The NAND and NOR gates, along with the dimensionally similar expanders (no load resistors), form the single function cells. In general, these cells are input-output limited so that a three input NOR has the same area as a three input NAND, even though the NAND transistors are larger. The ability to mix NAND's and NOR's has the obvious

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advantage of directly forming the AND or OR function in either logic polarity. (A NOR gate may generate the AND function, a NAND gate may generate the OR function). Using combinations of NAND gates and NOR gates reduces the chip area by reducing the required number of inverters, and often increase the speed by reducing the signal propagation path.

The number of inputs to a NOR gate is effectively unlimited; NOR gates having ≤ 5 inputs may be implemented directly with GA7, NOR2, NOR3, NOR and NOR5 cells. A NOR gate having > 5 inputs may be implemented with a combination of one or more PD, NREX2, and NREX3 cells. (See Figure 2).

The number of inputs to a NAND gate is limited to 3, which is determined by the ON resistance of the input transistors. (NAND2 and NAND3 cells). The effective number of inputs to a NAND gate may be increased by using a NAND gate with a NOR gate. (See Figure 3). Note that opposite polarity signals are required for the NOR gate.

When the speed of the standard gates is insufficient, higher power (and subsequently faster) gates must be used. The high speed cells consist of the HPI (inverter), HPN2 (2-input NOR), PDX(single input expander), and HPEX2 (2-input expander). Figure 4 illustrates a high speed function implemented with these cells.

COMPLEX FUNCTION CELLS

The complex function cells provide a superior "gate-to-pin-ratio" over the single function elements; thus offering significant savings in area. These cells are designed to perform many common Boolean functions such as sum of products, product of sums, binary additions, etc.

The Binary Adder (BA) element accepts inputs A, B and Carry In and produces Sum and Carry in complemented form. If the inputs are complemented, the sum and carry will be true. For additional applications for an adder of this type, see Fairchild's "Application of The CCSL 9304 Dual Adder," Application Bulletin 163, by Clive Ghest.

The GA1 cell may be used either as a product of sums generator or as a sum of products generator. When generating a product of sums, the output is inverted and when generating a sum of products, the inputs must be inverted. (See Figure 5).

After a logic function has been initially implemented with the 3400 cell set, further improvement is usually possible by replacing combinations of simple function cells with complex function cells. Figure 6 shows some combinations of simple function cells which may be replaced by GA1 cells, depending on polarity requirements of input and output signals.

Frequently, latches and flip-flops are controlled by sums of products in the form $A \cdot B + C \cdot D$. This function is particularly adaptable to the GA1, provided the opposite polarity of A, B, C and D are available.

It may be desirable to generate the inverted sum of products. Depending on the function, the GA1 may be used to generate the function.

If, for example, the complement of the function $F = AC + \underline{A}D + BC + BD$ is desired, it may be implemented as shown in Figure 7.

The GA2 cell may also be used, either as a product of sums generator or a sum of products generator. When generating the sum of products, the output is

inverted, and when generating the product of sums, the inputs are inverted. (See Figure 8) Note that the GA2 generates the dual function of the GA1.

It is often desirable to generate a non inverted sum of products. Depending on the function, the GA2 may be used to generate the function. If, for example, the function F = AC + AD + BC + BD is desired, it may be implemented as shown in Figure 9.

As with the GA1 cell, the GA2 cell may replace combinations of existing simple function cells. Figure 10 shows some combinations of simple function cells which may be replaced by GA2 cells, depending on the polarity requirements of input and output signals.

Since the GA3 cell is merely an expansion of the GA2 cell, it may be treated similarly. It may be used to generate a sum of 3 products instead of 2 products as with the GA2. Figure 11 shows the generation of a non-inverted sum of products; Figure 12 shows an inverted sum of products.

The GA4 cell is functionally identical to the GA2 cell with an output inverter. It is used where both polarities of the output function are required. Note that the function may occasionally be generated in more than one way (Figure 13).

The GA5 cell forms the function $(A1 + A2)(\overline{B1 \cdot B2})$ at output Z1. When A1 and B1 are commoned and A2 and B2 are commoned, the Exclusive OR (Not Compare) function is generated at Z1 -- with inverted inputs, the GA5 becomes a half adder with Z1 equal to sum, Z2 equal to carry. If the Exclusive OR (or Compare) function is required and both true and complemented inputs are available, the GA1 or GA2 will more economically generate the function.

The GA6 generates the function $(A1 \cdot A2) + (\overline{B1 + B2})$ at output Z1. When A1 and B1 are commoned and A2 and B2 are commoned, Compare (not Exclusive OR) function is generated at Z1--this corresponds to Z1 being the inverted sum, Z2 the inverted carry of a half adder. If both true and complemented inputs are available, the compare function may be more economically generated by Ga1 or GA2. Note that GA6 generated the dual function of GA5.

The GA8 cell is similar to the GA2, differing only by the number of inputs to the NAND gates. Its use is also similar to that of the GA2 and therefore will not be covered in detail. Figure 14 shows an implementation of the function with an inverted output using the GA8 cell.

The PD, EXP and EXP3 cells may be connected to the output of any of the previously discussed cells to form more complex functions. The resulting output will equal the true function generated by the previously discussed cell ANDED with the true function generated by the PD, EXP, or EXP3 cell (see Figure 15).

The number of expanders which may be commoned is limited by interconnection resistance and capacitance. Generally up to four may be commoned easily -- above that number expansion using gating techniques may be required.

SEQUENTIAL FUNCTION CELLS

This classification includes flip-flops, latchs, dynamic shift register cells and a clock generator.

The LRS and LRS2 are simple gated latchs; the LRS2 is similar to the LRS except for an additional direct reset input. The LRS

latchs may be controlled at their output by the use of expander elements, frequently this results in area, propagation time and power savings. Figure 16 is an example.

Latches may also be implemented with cell types other than LRS elements for special applications, as shown in Figure 17.

The FRS1 consists of a master slave flip-flop made up of two latches. The master latch is logically identical to an LRS2; the slave is a dual of an LRS2. With CPA and CPB commoned, the master is sensitive to the S and R inputs when the clock is true. When CP is false, the master is latched and not sensitive to the S and R inputs. The slave switches to the same state as the master as CP goes false. If both S and R inputs are true as CP goes false, the output state of the flip-flop will be arbitrary.

Separate CLEAR DIRECT inputs are provided to the master and the slave. Normally, the two inputs CDA and CDB are commoned, but this is not always necessary. When CDA is true, the master will reset. The master will assume an ambiguous state when S, CPA and CDA are true. This ambiguity is resolved as soon as either CDP, CPA or S return false. While the ambiguity exists, it is not manifested at the outputs since the slave is not sensitive to the master. Note also that, if CDA and S return false simultaneously, a hazard exists and the slave will assume the arbitrary state of the master. If CPA and CPB are commoned do not return CDA and CP to false simultaneously, unless it is known that S is false or CDB remains true. Direct clearing may be accomplished by using CDA only, the outputs are influenced by CDA when CP is false. Direct clearing may also be accomplished by using CDB only. When CP is false, CDB will reset the slave; but, if CDB is removed before CP returns true, the outputs will again follow the master. If CDB is removed after CP returns true, the outputs will remain reset.

When the FRS1 changes state, the output going from 0 to 1 changes before the other output can change from 1 to 0. The exception to this occurs when CDB causes the Q output to change to 0 before the QN output changes to 1.

The FRS2 consists of two latches: the master is equivalent to an LRS2, and the slave is equivalent to an LRS. Since both the master and slave are sensitive to their inputs when their respective clock inputs are true, in order to function as a master slave flip-flop, the clocks must never be true simultaneously.

Unlike the FRS1, the FRS2 has a CLEAR DIRECT (CD) input provided to the master only. The master will, therefore, respond identically to the input combination and sequences described for the master of the FRS1. The outputs Q and QN are influenced by CD when CPN is true.

Note when the FRS2 changes state, the output going from 1 to 0 changes before the other output can change from 0 to 1.

The FRS3 is quite similar to the FRS2. The differences are simple but significant:

1) There is no CLEAR DIRECT (CD)
2) CPA and CPB are commoned internally (CP)
3) The QN node is accessable for adding a CLEAR DIRECT with a PD cell or a more complex RESET function with one or more EXP cells.

To obtain more powerful logic functions of the FRS flip-flops, additional gating must be used as shown in Figure 18.

The FT1 cell is logically identical to an FRS1 with the Q output connected to the R input, and the QN output connected to the S input. The analysis of the FRS1 also applies to the FT1.

The FT2 cell is logically identical to an FRS2 with the Q output connected to the R input, the QN output connected to the S input and the QMN access node not available for expansion. The analysis of the FRS2 also applies to the FT2.

The FT flip-flops are used pricipally as ripple counters. The input signal is applied to the least significant flip-flop, the following stages obtain their clocks from the previous stage as shown in Figure 19.

To guarantee an asynchronous reset of the FT2 flip-flops counter shown in Figure 19, CPN must go true while the clear input is true. Since the two phase flip-flops are 2 mils shorter than the single phase flip-flops, long ripple counters from a single phase source may use FT2 flip-flop for an overall saving. An FT1 is used for the first stage, and a NOR gate late used to guarantee non-overlapping inputs to the second state; see Figure 20. Note that the counter will reset independently of clock inputs because of the master and slave clear-direct inputs to the FT1.

The purpose of the CG cell is to provide clocks for the masters and slaves of FRS2, FRS3, and FT2 flip-flops. The C and CN outputs are never true simultaneously; that is, during a transition the output going from 1 to 0 changes before the other output can change from 0 to 1.

When the output drive of the CG is not necessary, area may be saved by implementing a 2-phase clock generator with simple function cells as shown in Figure 21. Note that a gated clock is also easily generated. (Figure 22).

When FRS2 or FRS3 flip-flops are used as a shift register, a novel clock generator may be implemented to simplify the CLEAR DIRECT or SET DIRECT logic as shown in Figure 23.

A comparison table of the master-slave flip-flops is shown in Table 1.

Master-slave flip-flops are subject to a phenomenon known as "ones-catching." This may be described as the master being set or reset by a momentary true input (on the R or S input) which has gone back to zero before the clock goes false. Consider the example of Figure 24.

This circuit is intended to apply a set input when A = B = 0. If different propagation paths, etc., cause both A and B to be momentarily false while CP is true long enough to set the master, (assume the R input is zero) the flip-flop will be set--in spite of the fact that the S input was false when CP went false.

Use of good design practices will guard against ones catching:

1) Use synchronous techniques so that signals change only as a result of the 1 to 0 clock transitions.

2) Insure that gating delays are small enough so that inputs to flip-flops are stable before the 0 to 1 clock transition. This may

also be accomplished by adjusting clock duty cycle.

3) Insure that R = $\bar{S}$ by using the flip-flop as a "D" flip-flop.

The SR1 is a two-phase dynamic shift register stage. Within its frequency range (minimum frequency 10 KHz) it is logically equivalent to a D flip-flop; however, its outputs cannot be used without the use of an SRB cell. The logic symbol and schematic are shown in Figure 25.

The SRB cell is a two-phase dynamic shift register buffer element. It is intended to be used as an interface from an SR1 cell to any of the static cells. It accepts the Q output from an SR1 cell and converts it to Q and $\bar{Q}$ outputs. It is logically similar to a gated D latch, Figure 26.

CONCLUSION

The 3400 Micromosaic building blocks provided by the 3400 cell set permit the development of a very efficient design in terms of function-per-chip area. A brute force implementation of a logic function using only NOR gates may be reduced as much as 20% simply by replacing some of these gates by other cell combinations. The flexible flip-flops with their access points also increase the efficiency. The key to efficient logic design with the 3400 cell set is familiarization with the cells and their numerous functions.

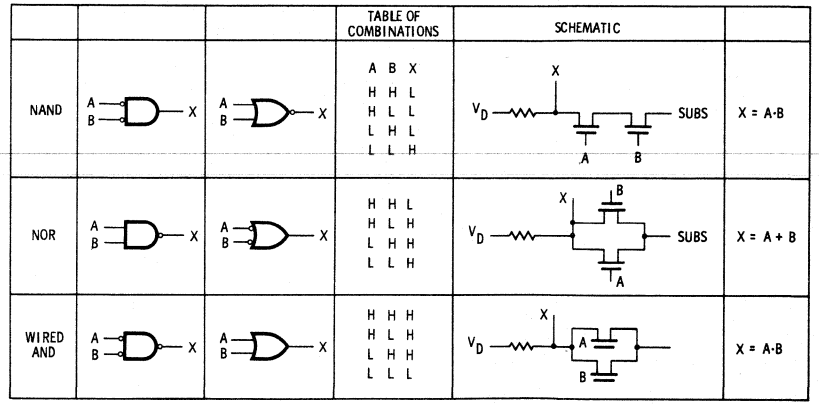

Fig. 1. Logic Symbols

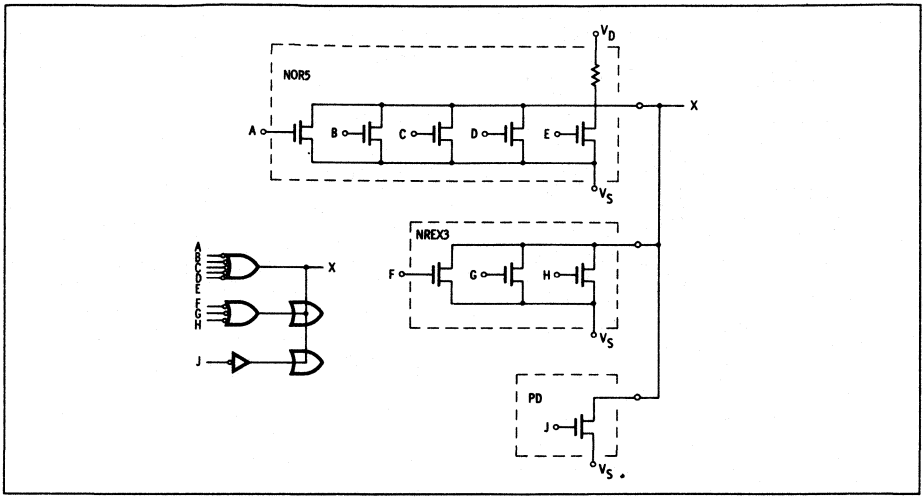

Fig. 2. Implementation of 9 input NOR gate. Note other combinations may be as efficient i.e. a NOR3 and 2 NREX3s.

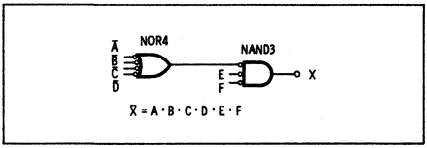

Fig. 3. Expansion of NAND gate by using NOR gate.

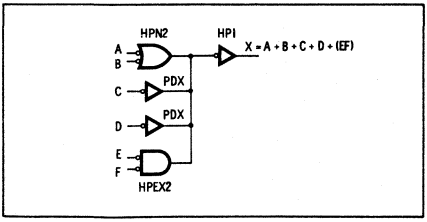

Fig. 4. High speed cell example

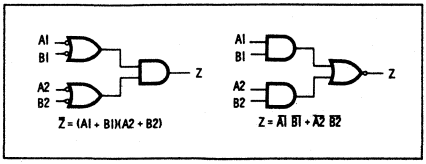

Fig. 5. GAI provides sum of products or product of sums

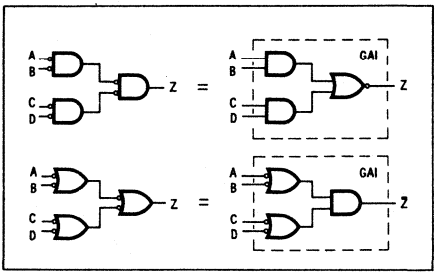

Fig. 6. Substitution of GAI for NAND's and NOR's

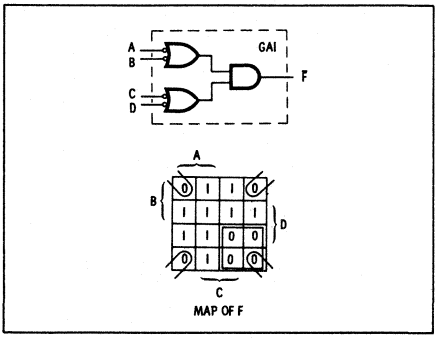

Fig. 7.

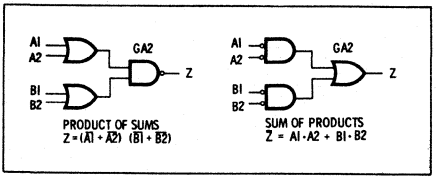

Fig. 8.

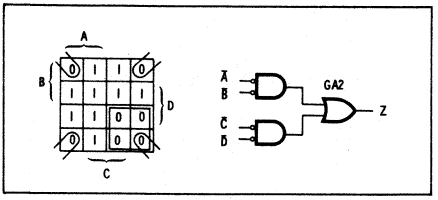

Fig. 9. To generate the non-inverted sum of products, determine a sum of products for F (0's on map, A·B + C·D) and connect as shown in the logic diagram.

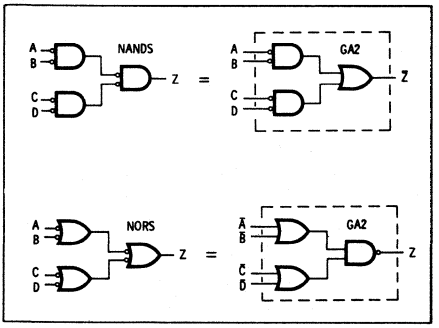

Fig. 10. Substitution of GA2 cells for combinations of NAND's or NOR's.

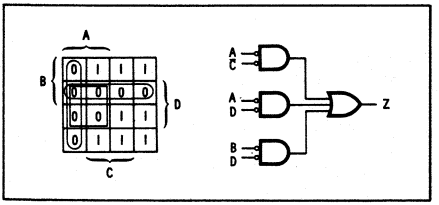

Fig. 11. Generation of non-inverted sum of products using GA3.

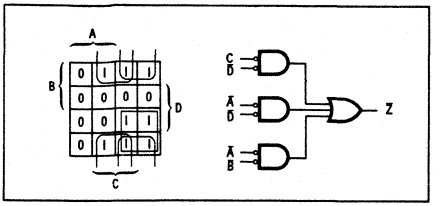

Fig. 12. Generation of inverted sum of products using GA3.

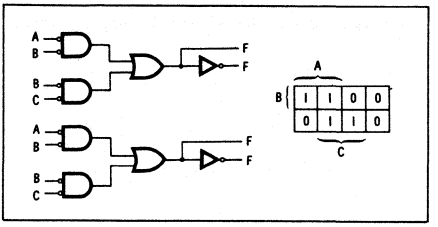

Fig. 13. Alternate implementations of functions F and F using GA4.

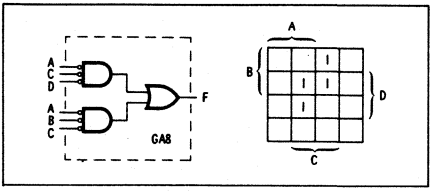

Fig. 14. Implementation of inverted function using GA8 cell.

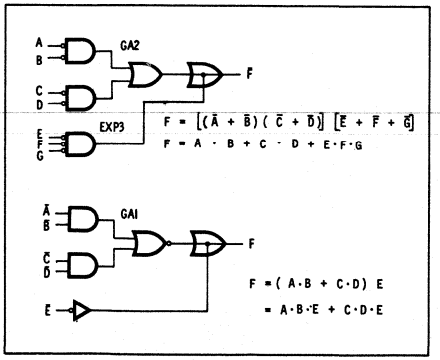

Fig. 15. Example of the use of expanders.

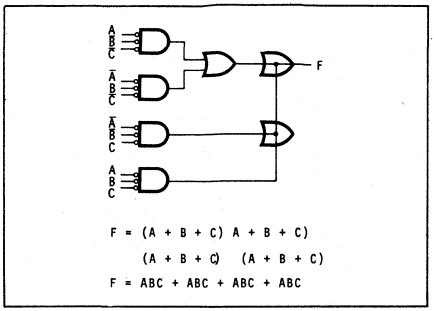

Fig. 15 (continued)

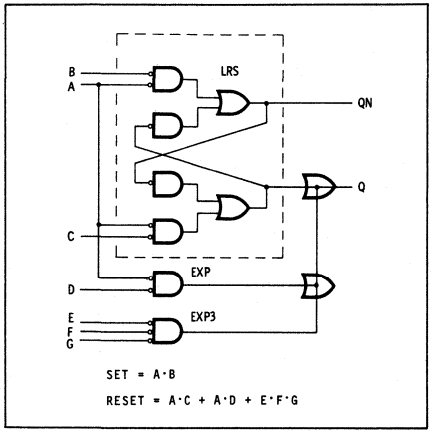

Fig. 16. Use of expander elements to control latch.

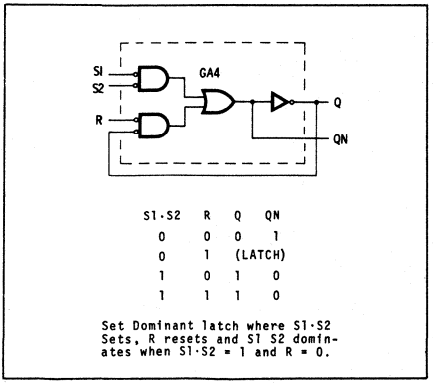

Fig. 17a. Special purpose latch.

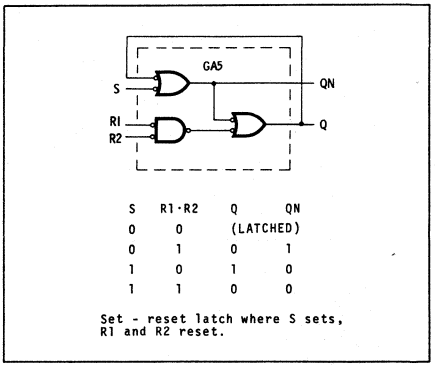

Fig. 17b. Special purpose latch.

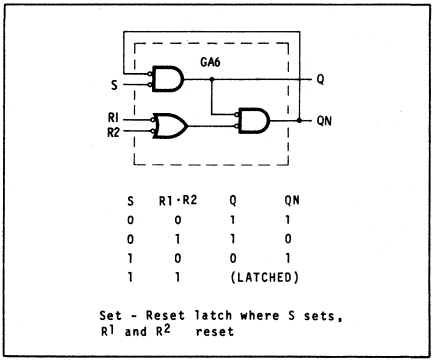

Fig. 17c. Special purpose latch.

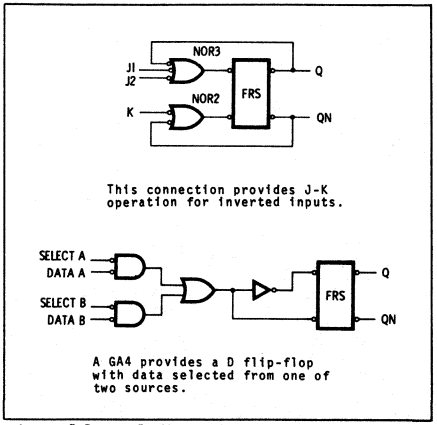

Fig. 18. J-K and D flip-flop implementations.

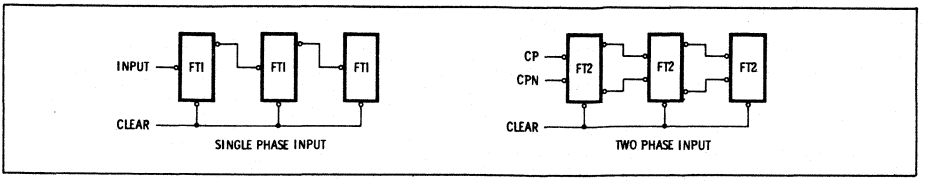

Fig. 19. Ripple counters.

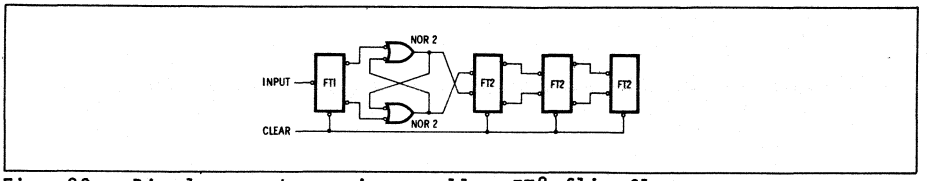

Fig. 20. Ripple counter using smaller FT2 flip-flops.

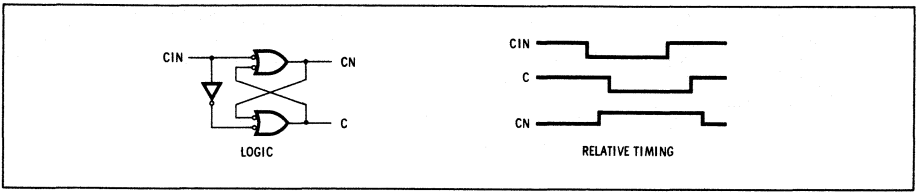

Fig. 21. 2-phase clock generator using 2 NOR 2'S and 1 inv.

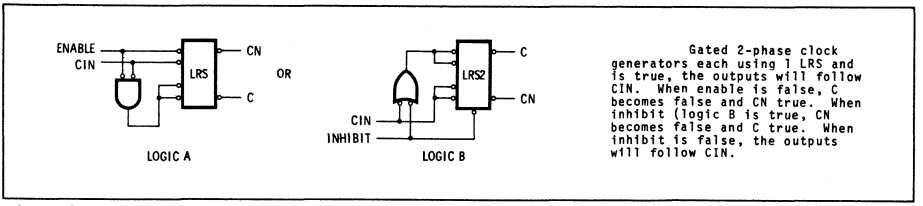

Fig. 22.

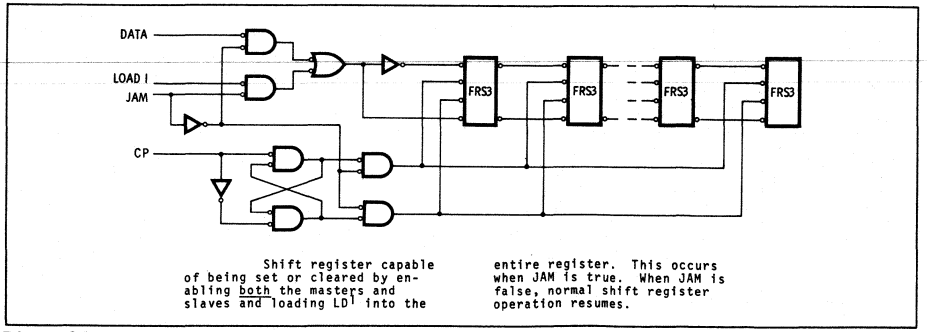

Fig. 23.

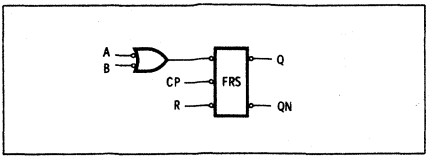

Fig. 24. Potential ones catching hazard.

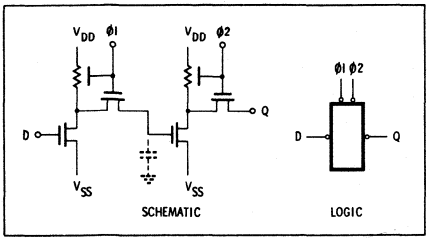

Fig. 25. SR1 dynamic shift register cell. This cell is sensitive to the D input only when Ø1 is true. The Q output changes when Ø2 is true. Its width is 4 mils.

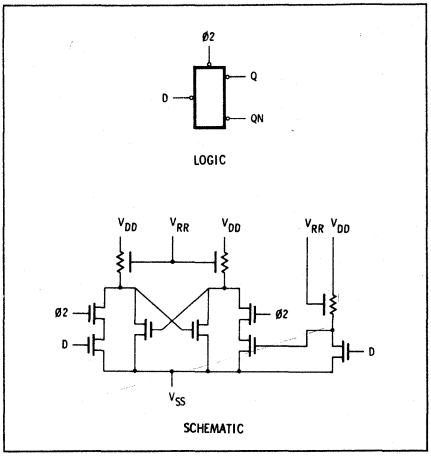

Fig. 26. SRB dynamic shift register buffer cell. This cell is sensitive to the D input only when 02 is true. When 02 is false, the outputs remain latched. Its width is 7 mils.

TABLE 1 COMPARISON OF FRS1, FRS2, FT1, FT2

	FRS1	FRS2	FRS3	FT1	FT2
CELL LENGTH	13 MILS	11 MILS	11 MILS	13 MILS	11 MILS
CLOCK SOURCE	ANY SINGLE PHASE SIGNAL	2 PHASE CLOCK MUST BE GENERATED BY: 1) CLOCK GENERATOR (16 MILS CELL LENGTH) 2) OTHER SIMPLE OR COMPLEX FUNCTION CELLS (<16 MILS CELL LENGTH) 3) OTHER FRS2, FRS3 OR FT2 4) 2 MUTUALLY EXCLUSIVE NON-OVERLAPPING SIGNALS	SAME AS FRS2	ANY	SAME AS FRS2
CLEAR DIRECT	MASTER AND/OR SLAVE	MASTER. USE PD FOR SLAVE.	USE PD FOR MASTER. USE PD FOR SLAVE.	MASTER. AND/OR SLAVE.	MASTER. USE PD FOR SLAVE.
SET DIRECT	USE PD FOR SLAVE.	USE PD FOR MASTER. USE PD FOR SLAVE.	USE PD FOR MASTER. USE PD FOR SLAVE.	USE PD FOR SLAVE	USE PD FOR SLAVE.
ACCESSABILITY FOR SET FUNCTION EXPANSION	NO, COMPLETE SET FUNCTION MUST BE ENTERED AT S INPUT	YES	YES	NO	NO
ACCESSABILITY FOR RESET FUNCTION EXPANSION	NO	NO	YES	NO	NO
MAY BE USED AS CLOCK GENERATOR FOR 2 PHASE CLOCK	NO, Q AND QN OUTPUTS OVERLAP WHEN CHANGING STATE.	YES, Q AND QN OUTPUTS DO NOT OVERLAP WHEN CHANGING STATE.	YES, Q AND QN OUTPUTS DO NOT OVERLAP WHEN CHANGING STATE	NO, Q AND QN OUTPUTS OVERLAP WHEN CHANGING STATE.	YES, Q AND QN OUTPUTS DO NOT OVERLAP WHEN CHANGING STATE

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